ninth edition

electronic devices

conventional current version

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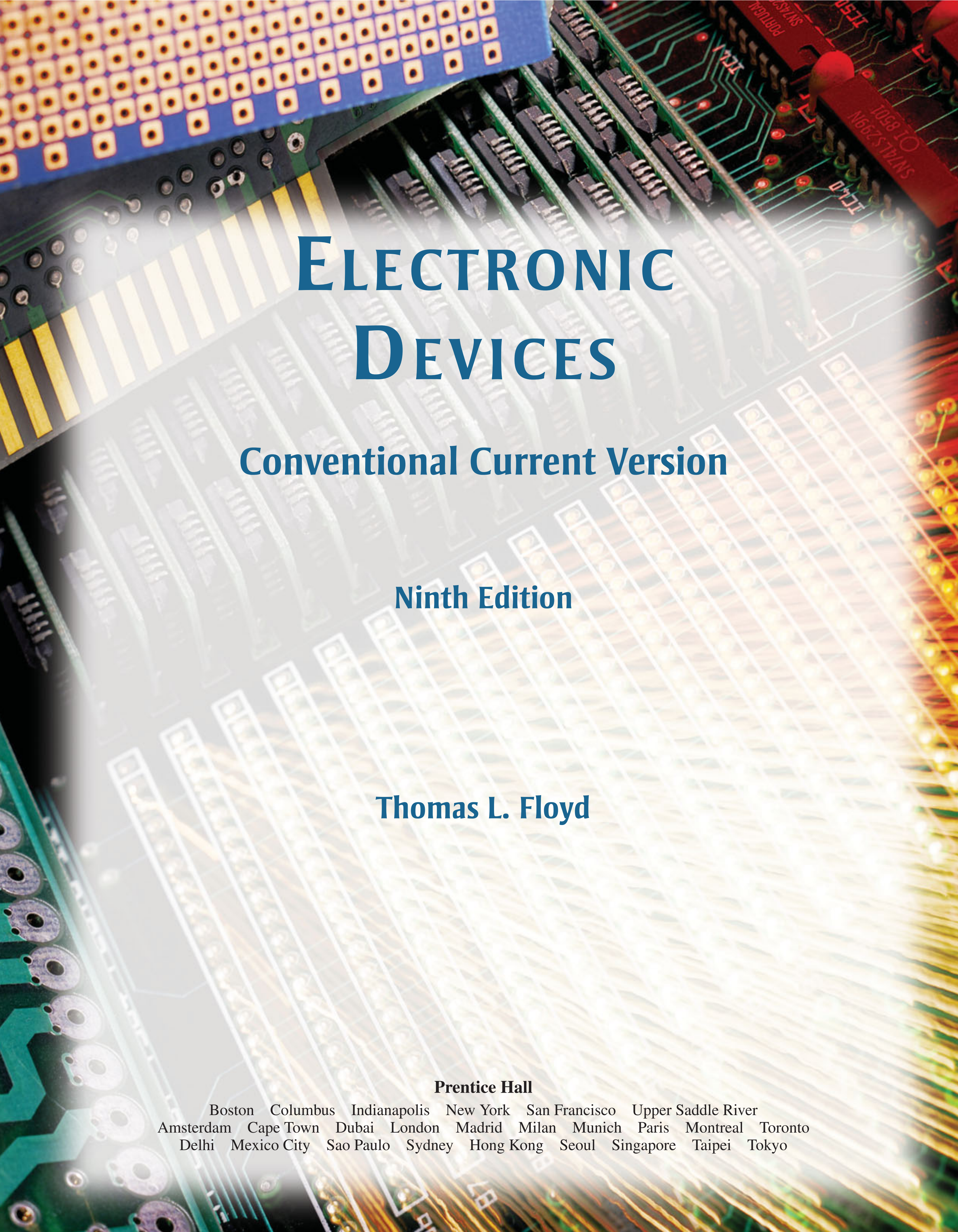

ELECTRONIC DEVICES

Conventional Current Version

Ninth Edition

Thomas L. Floyd

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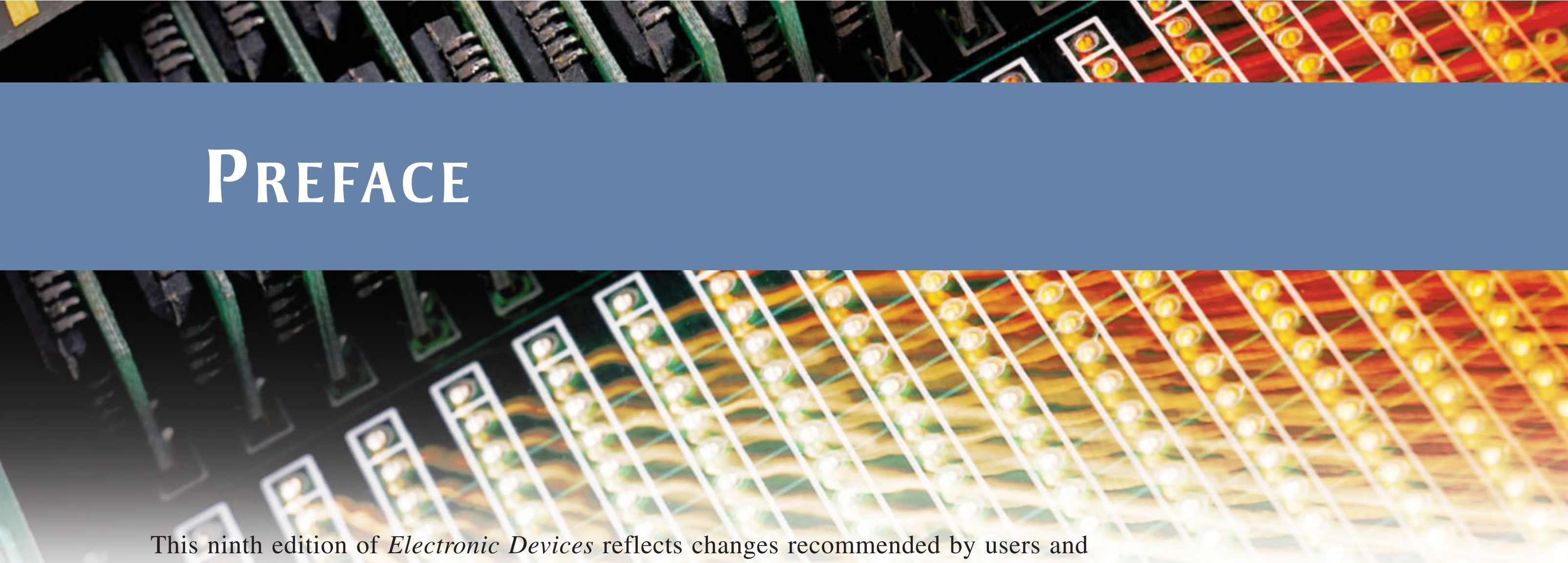


PREFACE

This ninth edition of *Electronic Devices* reflects changes recommended by users and reviewers. Applications and troubleshooting coverage have been expanded to include several new topics related to renewable energy and automated test programming. As in the previous edition, Chapters 1 through 11 are essentially devoted to discrete devices and circuits. Chapters 12 through 17 primarily cover linear integrated circuits. A completely new Chapter 18 covers an introduction to programming for device testing. It can be used as a "floating" chapter and introduced in conjunction with any of the troubleshooting sections. Chapter 19, which was Chapter 18 in the last edition, is an online chapter that covers electronic communications. Multisim® files in versions 10 and 11 are now available at the companion website, www.pearsonhighered.com/electronics.

New in This Edition

Reorganizations of Chapters 1 and 2 These chapters have been significantly reworked for a more effective coverage of the introduction to electronics and diodes. New topics such as the quantum model of the atom have been added.

GreenTech Applications This new feature appears after each of the first six chapters and introduces the application of electronics to solar energy and wind energy. A significant effort is being made to create renewable and sustainable energy sources to offset, and eventually replace, fossil fuels. Today's electronics technician should have some familiarity with these relatively new technologies. The coverage in this text provides a starting point for those who may pursue a career in the renewable energy field.

Basic Programming Concepts for Automated Testing A totally new chapter by Gary Snyder covers the basics of programming used for the automated testing of electronic devices. It has become increasingly important for electronic technicians, particularly those working in certain environments such as production testing, to have a fundamental grounding in automated testing that involves programming. This chapter is intended to be used in conjunction with the traditional troubleshooting sections and can be introduced or omitted at the instructor's discretion.

More Multisim® Circuits Updated to Newest Versions Additional Multisim® circuit files have been added to this edition. All the files have been updated to versions 10 and 11.

New Format for Section Objectives The section objectives have been rewritten to provide a better indication of the coverage in each section. The new format better reflects the topics covered and their hierarchy.

Miscellaneous Improvements An expanded and updated coverage of LEDs includes high-intensity LEDs, which are becoming widely used in many areas such as residential lighting, automotive lighting, traffic signals, and informational signs. Also, the topic of quantum dots is discussed, and more emphasis is given to MOSFETs, particularly in switching power supplies.

Standard Features

- Full-color format.
- Chapter openers include a chapter outline, chapter objectives, introduction, key terms list, Application Activity preview, and website reference.
- Introduction and objectives for each section within a chapter.
- Large selection of worked-out examples set off in a graphic box. Each example has a related problem for which the answer can be found at www.pearsonhighered.com/electronics.
- Multisim® circuit files for selected examples, troubleshooting, and selected problems are on the companion website.
- Section checkup questions are at the end of each section within a chapter. Answers can be found at www.pearsonhighered.com/electronics.
- Troubleshooting sections in many chapters.
- An Application Activity is at the end of most chapters.
- A Programmable Analog Technology feature is at the end of selected chapters.
- A sectionalized chapter summary, key term glossary, and formula list at the end of each chapter.
- True/false quiz, circuit-action quiz, self-test, and categorized problem set with basic and advanced problems at the end of each chapter.
- Appendix with answers to odd-numbered problems, glossary, and index are at the end of the book.
- PowerPoint® slides, developed by Dave Buchla, are available online. These innovative, interactive slides are coordinated with each text chapter and are an excellent tool to supplement classroom presentations.

Student Resources

Companion Website ***(www.pearsonhighered.com/floyd)*** This website offers students an online study guide that they can check for conceptual understanding of key topics. Also included on the website are the following: Chapter 19, "Electronic Communications Systems and Devices," a table of standard resistor values, derivatives of selected equations, a discussion of circuit simulation using Multisim and NI ELVIS, and an examination of National Instruments' LabVIEW™. The LabVIEW software is an example of a visual programming application and relates to new Chapter 18. Answers to Section Checkups, Related Problems for Examples, True/False Quizzes, Circuit-Action Quizzes, and Self-Tests are found on this website.

Multisim® These online files include simulation circuits in Multisim® 10 and 11 for selected examples, troubleshooting sections, and selected problems in the text. These circuits were created for use with Multisim® software. Multisim® is widely regarded as an excellent circuit simulation tool for classroom and laboratory learning. However, no part of your textbook is dependent upon the Multisim® software or provided files.

Laboratory Exercises for Electronic Devices, Ninth Edition, by Dave Buchla and Steve Wetterling. ISBN: 0-13-25419-5.

Instructor Resources

To access supplementary materials online, instructors need to request an instructor access code. Go to www.pearsonhighered.com/irc to register for an instructor access code. Within 48 hours of registering, you will receive a confirming e-mail including an instructor access code. Once you have received your code, locate your text in the online catalog and click on the Instructor Resources button on the left side of the catalog product page. Select a supplement, and a login page will appear. Once you have logged in, you can access instructor material for all Prentice Hall textbooks. If you have any difficulties accessing the site or downloading a supplement, please contact Customer Service at http://247.prenhall.com.

Online Instructor's Resource Manual Includes solutions to chapter problems, Application Activity results, summary of Multisim® circuit files, and a test item file. Solutions to the lab manual are also included.

Online Course Support If your program is offering your electronics course in a distance learning format, please contact your local Pearson sales representative for a list of product solutions.

Online PowerPoint® Slides This innovative, interactive PowerPoint slide presentation for each chapter in the book provides an effective supplement to classroom lectures.

Online TestGen This is a test bank of over 800 questions.

Chapter Features

Chapter Opener Each chapter begins with an opening page, as shown in Figure P–1. The chapter opener includes a chapter introduction, a list of chapter sections, chapter objectives, key terms, an Application Activity preview, and a website reference for associated study aids.

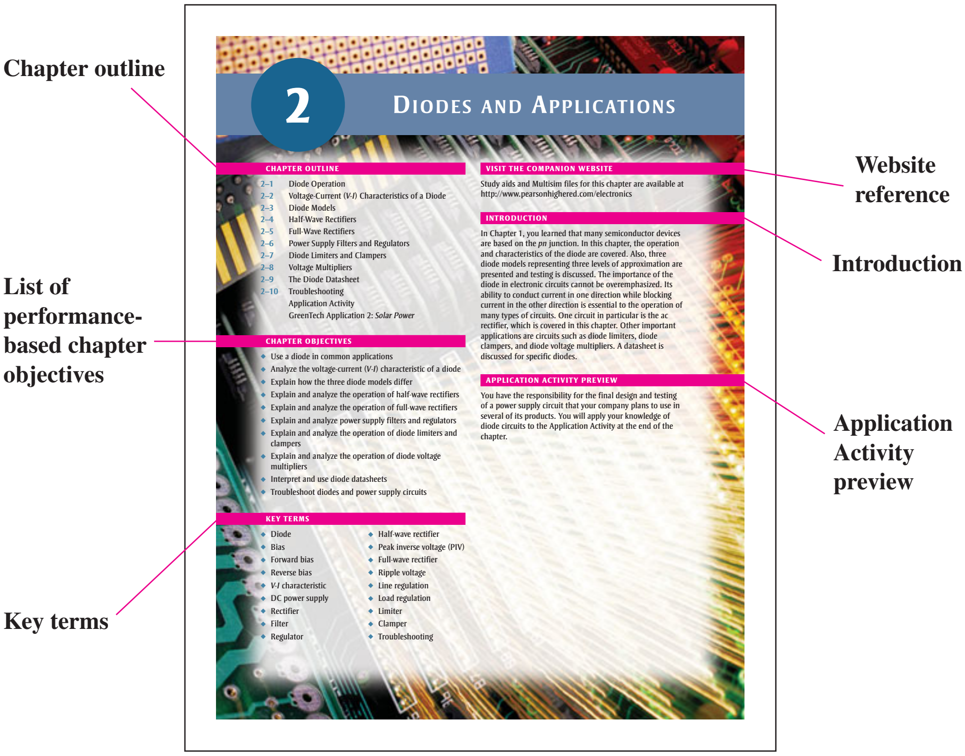


FIGURE P–1

A typical chapter opener.

Chapter outline
List of performance-based chapter objectives
Key terms
Website reference
Introduction
Application Activity preview

2

DIODES AND APPLICATIONS

CHAPTER OUTLINE

- 2–1 Diode Operation
- 2–2 Voltage-Current (*V-I*) Characteristics of a Diode
- 2–3 Diode Models
- 2–4 Half-Wave Rectifiers
- 2–5 Full-Wave Rectifiers
- 2–6 Power Supply Filters and Regulators
- 2–7 Diode Limiters and Clampers
- 2–8 Voltage Multipliers
- 2–9 The Diode Datasheet
- 2–10 Troubleshooting
- Application Activity
- GreenTech Application 2: *Solar Power*

CHAPTER OBJECTIVES

- Use a diode in common applications
- Analyze the voltage-current (*V-I*) characteristic of a diode
- Explain how the three diode models differ
- Explain and analyze the operation of half-wave rectifiers
- Explain and analyze the operation of full-wave rectifiers
- Explain and analyze power supply filters and regulators
- Explain and analyze the operation of diode limiters and clampers
- Explain and analyze the operation of diode voltage multipliers
- Interpret and use diode datasheets
- Troubleshoot diodes and power supply circuits

KEY TERMS

- Diode
- Bias
- Forward bias
- Reverse bias
- *V-I* characteristic
- DC power supply
- Rectifier
- Filter
- Regulator
- Half-wave rectifier
- Peak inverse voltage (PIV)
- Full-wave rectifier
- Ripple voltage
- Line regulation
- Load regulation
- Limiter
- Clamper
- Troubleshooting

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In Chapter 1, you learned that many semiconductor devices are based on the *pn* junction. In this chapter, the operation and characteristics of the diode are covered. Also, three diode models representing three levels of approximation are presented and testing is discussed. The importance of the diode in electronic circuits cannot be overemphasized. Its ability to conduct current in one direction while blocking current in the other direction is essential to the operation of many types of circuits. One circuit in particular is the ac rectifier, which is covered in this chapter. Other important applications are circuits such as diode limiters, diode clampers, and diode voltage multipliers. A datasheet is discussed for specific diodes.

APPLICATION ACTIVITY PREVIEW

You have the responsibility for the final design and testing of a power supply circuit that your company plans to use in several of its products. You will apply your knowledge of diode circuits to the Application Activity at the end of the chapter.

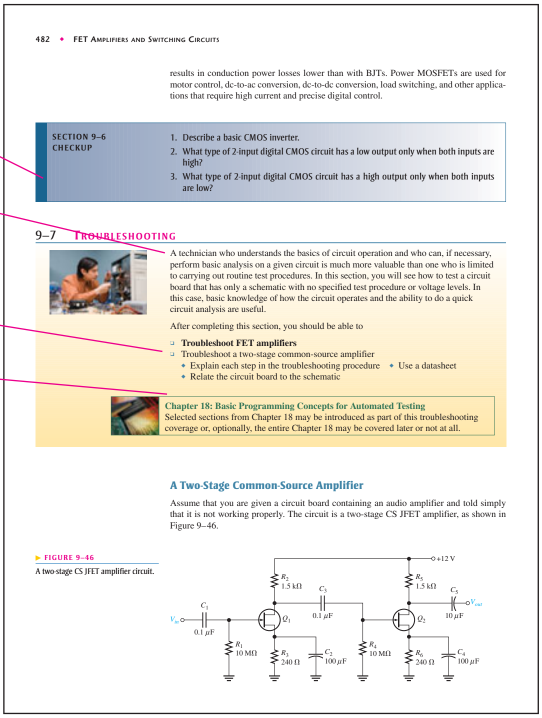
Section Opener Each section in a chapter begins with a brief introduction and section objectives. An example is shown in Figure P–2.

Section Checkup Each section in a chapter ends with a list of questions that focus on the main concepts presented in the section. This feature is also illustrated in Figure P–2. The answers to the Section Checkups can be found at www.pearsonhighered.com/electronics.

Troubleshooting Sections Many chapters include a troubleshooting section that relates to the topics covered in the chapter and that illustrates troubleshooting procedures and techniques. The Troubleshooting section also provides Multisim® Troubleshooting exercises. A reference to the optional Chapter 18 (Basic Programming Concepts for Automated Testing) is included in each Troubleshooting section.

▶ FIGURE P–2

A typical section opener and section review.



Section checkup ends each section.

Introductory paragraph begins each section.

Performance-based section objectives

Reference to Chapter 18, “Basic Programming Concepts for Automated Testing”

482 ◆ FET AMPLIFIERS AND SWITCHING CIRCUITS

results in conduction power losses lower than with BJTs. Power MOSFETs are used for motor control, dc-to-ac conversion, dc-to-dc conversion, load switching, and other applications that require high current and precise digital control.

SECTION 9–6 CHECKUP

1. Describe a basic CMOS inverter.
2. What type of 2-input digital CMOS circuit has a low output only when both inputs are high?
3. What type of 2-input digital CMOS circuit has a high output only when both inputs are low?

9–7 TROUBLESHOOTING

A technician who understands the basics of circuit operation and who can, if necessary, perform basic analysis on a given circuit is much more valuable than one who is limited to carrying out routine test procedures. In this section, you will see how to test a circuit board that has only a schematic with no specified test procedure or voltage levels. In this case, basic knowledge of how the circuit operates and the ability to do a quick circuit analysis are useful.

After completing this section, you should be able to

- ❑ **Troubleshoot FET amplifiers**
- ❑ Troubleshoot a two-stage common-source amplifier
  - ◆ Explain each step in the troubleshooting procedure
  - ◆ Use a datasheet
  - ◆ Relate the circuit board to the schematic

Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

A Two-Stage Common-Source Amplifier

Assume that you are given a circuit board containing an audio amplifier and told simply that it is not working properly. The circuit is a two-stage CS JFET amplifier, as shown in Figure 9–46.

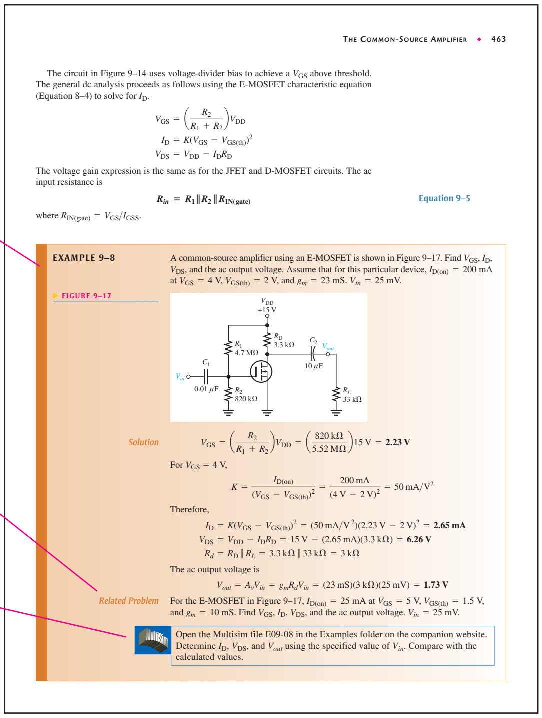
▶ FIGURE 9–46

A two-stage CS JFET amplifier circuit.

Worked Examples, Related Problems, and Multisim® Exercises Numerous worked-out examples throughout each chapter illustrate and clarify basic concepts or specific procedures. Each example ends with a Related Problem that reinforces or expands on the example by requiring the student to work through a problem similar to the example. Selected examples feature a Multisim® exercise keyed to a file on the companion website that contains the circuit illustrated in the example. A typical example with a Related Problem and a Multisim® exercise are shown in Figure P–3. Answers to Related Problems can be found at www.pearsonhighered.com/electronics.

▶ FIGURE P–3

A typical example with a related problem and Multisim® exercise.



Examples are set off from text.

Each example contains a related problem relevant to the example.

Selected examples include a Multisim® exercise coordinated with the Multisim circuit files on the companion website.

THE COMMON-SOURCE AMPLIFIER ◆ 463

The circuit in Figure 9–14 uses voltage-divider bias to achieve a V_{GS} above threshold. The general dc analysis proceeds as follows using the E-MOSFET characteristic equation (Equation 8–4) to solve for I_D.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$
$$I_D = K(V_{GS} - V_{GS(th)})^2$$
$$V_{DS} = V_{DD} - I_DR_D$$

The voltage gain expression is the same as for the JFET and D-MOSFET circuits. The ac input resistance is

$$\boldsymbol{R_{in} = R_1 \| R_2 \| R_{IN(gate)}}$$

Equation 9–5

where $R_{IN(gate)} = V_{GS}/I_{GSS}$.

EXAMPLE 9–8

A common-source amplifier using an E-MOSFET is shown in Figure 9–17. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. Assume that for this particular device, $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V, $V_{GS(th)} = 2$ V, and $g_m = 23$ mS. $V_{in} = 25$ mV.

▶ FIGURE 9–17

Solution

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{820\text{ k}\Omega}{5.52\text{ M}\Omega}\right)15\text{ V} = \mathbf{2.23\text{ V}}$$

For $V_{GS} = 4$ V,

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = 50\text{ mA/V}^2$$

Therefore,

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(2.23\text{ V} - 2\text{ V})^2 = \mathbf{2.65\text{ mA}}$$
$$V_{DS} = V_{DD} - I_DR_D = 15\text{ V} - (2.65\text{ mA})(3.3\text{ k}\Omega) = \mathbf{6.26\text{ V}}$$
$$R_d = R_D \| R_L = 3.3\text{ k}\Omega \| 33\text{ k}\Omega = 3\text{ k}\Omega$$

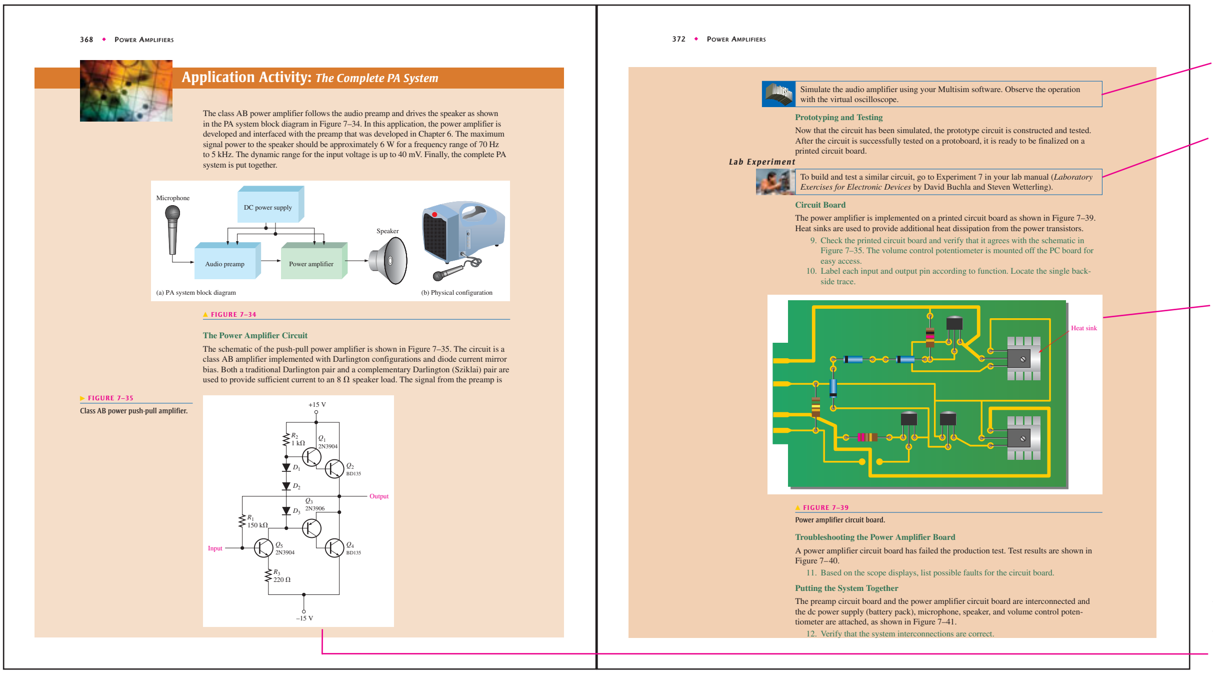
The ac output voltage is

$$V_{out} = A_vV_{in} = g_mR_dV_{in} = (23\text{ mS})(3\text{ k}\Omega)(25\text{ mV}) = \mathbf{1.73\text{ V}}$$

Related Problem For the E-MOSFET in Figure 9–17, $I_{D(on)} = 25$ mA at $V_{GS} = 5$ V, $V_{GS(th)} = 1.5$ V, and $g_m = 10$ mS. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. $V_{in} = 25$ mV.

Open the Multisim file E09-08 in the Examples folder on the companion website. Determine I_D, V_{DS}, and V_{out} using the specified value of V_{in}. Compare with the calculated values.

Application Activity This feature follows the last section in most chapters and is identified by a special graphic design. A practical application of devices or circuits covered in the chapter is presented. The student learns how the specific device or circuit is used and is taken through the steps of design specification, simulation, prototyping, circuit board implementation, and testing. A typical Application Activity is shown in Figure P–4. Application Activities are optional. Results are provided in the Online Instructor's Resource Manual.



368 ◆ POWER AMPLIFIERS

Application Activity: ***The Complete PA System***

The class AB power amplifier follows the audio preamp and drives the speaker as shown in the PA system block diagram in Figure 7–34. In this application, the power amplifier is developed and interfaced with the preamp that was developed in Chapter 6. The maximum signal power to the speaker should be approximately 6 W for a frequency range of 70 Hz to 5 kHz. The dynamic range for the input voltage is up to 40 mV. Finally, the complete PA system is put together.

(a) PA system block diagram (b) Physical configuration

▲ FIGURE 7–34

The Power Amplifier Circuit

The schematic of the push-pull power amplifier is shown in Figure 7–35. The circuit is a class AB amplifier implemented with Darlington configurations and diode current mirror bias. Both a traditional Darlington pair and a complementary Darlington (Sziklai) pair are used to provide sufficient current to an 8 Ω speaker load. The signal from the preamp is

► FIGURE 7–35

Class AB power push-pull amplifier.

372 ◆ POWER AMPLIFIERS

Simulate the audio amplifier using your Multisim software. Observe the operation with the virtual oscilloscope.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a similar circuit, go to Experiment 7 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The power amplifier is implemented on a printed circuit board as shown in Figure 7–39. Heat sinks are used to provide additional heat dissipation from the power transistors.

9. Check the printed circuit board and verify that it agrees with the schematic in Figure 7–35. The volume control potentiometer is mounted off the PC board for easy access.
10. Label each input and output pin according to function. Locate the single backside trace.

▲ FIGURE 7–39

Power amplifier circuit board.

Troubleshooting the Power Amplifier Board

A power amplifier circuit board has failed the production test. Test results are shown in Figure 7–40.

11. Based on the scope displays, list possible faults for the circuit board.

Putting the System Together

The preamp circuit board and the power amplifier circuit board are interconnected and the dc power supply (battery pack), microphone, speaker, and volume control potentiometer are attached, as shown in Figure 7–41.

12. Verify that the system interconnections are correct.

Multisim® Activity

Link to experiment in lab manual

Printed circuit board

Simulations are provided for most Application Activity circuits.

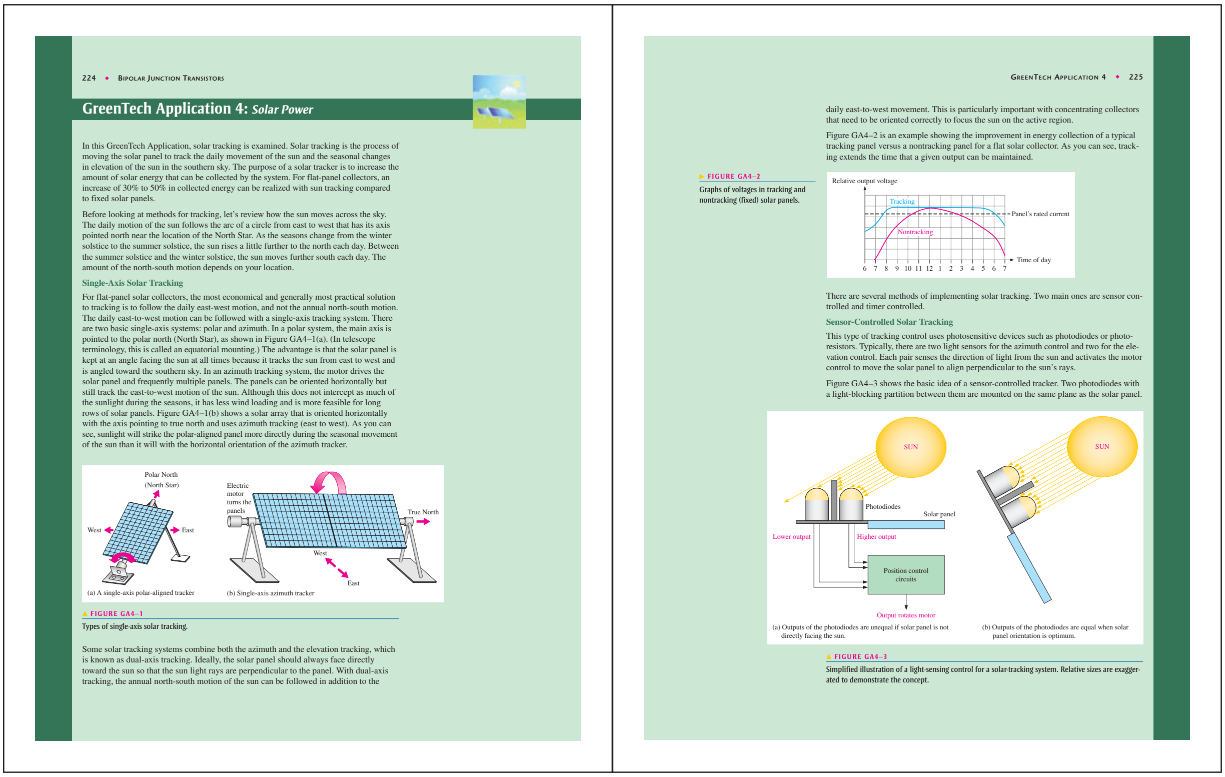
▲ FIGURE P–4

Portion of a typical Application Activity section.

GreenTech Application Inserts These inserts are placed after each of the first six chapters to introduce renewable energy concepts and the application of electronic devices to solar and wind technologies. Figure P–5 illustrates typical GreenTech Application pages.

Chapter End Matter The following pedagogical features are found at the end of most chapters:

- Summary
- Key Term Glossary
- Key Formulas
- True/False Quiz
- Circuit-Action Quiz
- Self-Test
- Basic Problems
- Advanced Problems
- Datasheet Problems (selected chapters)
- Application Activity Problems (many chapters)
- Multisim® Troubleshooting Problems (most chapters)



224 ◆ BIPOLAR JUNCTION TRANSISTORS

GreenTech Application 4: ***Solar Power***

In this GreenTech Application, solar tracking is examined. Solar tracking is the process of moving the solar panel to track the daily movement of the sun and the seasonal changes in elevation of the sun in the southern sky. The purpose of a solar tracker is to increase the amount of solar energy that can be collected by the system. For flat-panel collectors, an increase of 30% to 50% in collected energy can be realized with sun tracking compared to fixed solar panels.

Before looking at methods for tracking, let's review how the sun moves across the sky. The daily motion of the sun follows the arc of a circle from east to west that has its axis pointed north near the location of the North Star. As the seasons change from the winter solstice to the summer solstice, the sun rises a little further to the north each day. Between the summer solstice and the winter solstice, the sun moves further south each day. The amount of the north-south motion depends on your location.

Single-Axis Solar Tracking

For flat-panel solar collectors, the most economical and generally most practical solution to tracking is to follow the daily east-west motion, and not the annual north-south motion. The daily east-to-west motion can be followed with a single-axis tracking system. There are two basic single-axis systems: polar and azimuth. In a polar system, the main axis is pointed to the polar north (North Star), as shown in Figure GA4–1(a). (In telescope terminology, this is called an equatorial mounting.) The advantage is that the solar panel is kept at an angle facing the sun at all times because it tracks the sun from east to west and is angled toward the southern sky. In an azimuth tracking system, the motor drives the solar panel and frequently multiple panels. The panels can be oriented horizontally but still track the east-to-west motion of the sun. Although this does not intercept as much of the sunlight during the seasons, it has less wind loading and is more feasible for long rows of solar panels. Figure GA4–1(b) shows a solar array that is oriented horizontally with the axis pointing to true north and uses azimuth tracking (east to west). As you can see, sunlight will strike the polar-aligned panel more directly during the seasonal movement of the sun than it will with the horizontal orientation of the azimuth tracker.

(a) A single-axis polar-aligned tracker

(b) Single-axis azimuth tracker

▲ FIGURE GA4–1

Types of single-axis solar tracking.

Some solar tracking systems combine both the azimuth and the elevation tracking, which is known as dual-axis tracking. Ideally, the solar panel should always face directly toward the sun so that the sun light rays are perpendicular to the panel. With dual-axis tracking, the annual north-south motion of the sun can be followed in addition to the daily east-to-west movement. This is particularly important with concentrating collectors that need to be oriented correctly to focus the sun on the active region.

GREENTECH APPLICATION 4 ◆ 225

Figure GA4–2 is an example showing the improvement in energy collection of a typical tracking panel versus a nontracking panel for a flat solar collector. As you can see, tracking extends the time that a given output can be maintained.

▶ FIGURE GA4–2

Graphs of voltages in tracking and nontracking (fixed) solar panels.

There are several methods of implementing solar tracking. Two main ones are sensor controlled and timer controlled.

Sensor-Controlled Solar Tracking

This type of tracking control uses photosensitive devices such as photodiodes or photoresistors. Typically, there are two light sensors for the azimuth control and two for the elevation control. Each pair senses the direction of light from the sun and activates the motor control to move the solar panel to align perpendicular to the sun's rays.

Figure GA4–3 shows the basic idea of a sensor-controlled tracker. Two photodiodes with a light-blocking partition between them are mounted on the same plane as the solar panel.

(a) Outputs of the photodiodes are unequal if solar panel is not directly facing the sun.

(b) Outputs of the photodiodes are equal when solar panel orientation is optimum.

▲ FIGURE GA4–3

Simplified illustration of a light-sensing control for a solar-tracking system. Relative sizes are exaggerated to demonstrate the concept.

▲ FIGURE P–5

Portion of a typical GreenTech Application.

Suggestions for Using This Textbook

As mentioned, this book covers discrete devices and circuits in Chapters 1 through 11 and linear integrated circuits in Chapters 12 through 17. Chapter 18 introduces programming concepts for device testing and is linked to Troubleshooting sections.

Option 1 (two terms) Chapters 1 through 11 can be covered in the first term. Depending on individual preferences and program emphasis, selective coverage may be necessary. Chapters 12 through 17 can be covered in the second term. Again, selective coverage may be necessary.

Option 2 (one term) By omitting certain topics and by maintaining a rigorous schedule, this book can be used in one-term courses. For example, a course covering only discrete devices and circuits would use Chapters 1 through 11 with, perhaps, some selectivity.

Similarly, a course requiring only linear integrated circuit coverage would use Chapters 12 through 17. Another approach is a very selective coverage of discrete devices and circuits topics followed by a limited coverage of integrated circuits (only op-amps, for example). Also, elements such as the Multisim exercises, Application Activities, and GreenTech Applications can be omitted or selectively used.

To the Student

When studying a particular chapter, study one section until you understand it and only then move on to the next one. Read each section and study the related illustrations carefully; think about the material; work through each example step-by-step, work its Related Problem and check the answer; then answer each question in the Section Checkup, and check your answers. Don't expect each concept to be completely clear after a single reading; you may have to read the material two or even three times. Once you think that you understand the material, review the chapter summary, key formula list, and key term definitions at the end of the chapter. Take the true/false quiz, the circuit-action quiz, and the self-test. Finally, work the assigned problems at the end of the chapter. Working through these problems is perhaps the most important way to check and reinforce your comprehension of the chapter. By working problems, you acquire an additional level of insight and understanding, and develop logical thinking that reading or classroom lectures alone do not provide.

Generally, you cannot fully understand a concept or procedure by simply watching or listening to someone else. Only hard work and critical thinking will produce the results you expect and deserve.

Acknowledgments

Many capable people have contributed to the ninth edition of *Electronic Devices.* It has been thoroughly reviewed and checked for both content and accuracy. Those at Prentice Hall who have contributed greatly to this project throughout the many phases of development and production include Rex Davidson, Yvette Schlarman, and Wyatt Morris. Lois Porter has once more done an outstanding job editing the manuscript. Thanks to Sudip Sinha at Aptara for his management of the art and text programs. Dave Buchla contributed extensively to the content of the book, helping to make this edition the best one yet. Gary Snyder created the circuit files for the Multisim® features in this edition. Gary also wrote Chapter 18, Basic Programming Concepts for Automated Testing. I wish to express my appreciation to those already mentioned as well as the reviewers who provided many valuable suggestions and constructive criticism that greatly influenced this edition. These reviewers are William Dolan, Kennebec Valley Community College; John Duncan, Kent State University; Art Eggers, Community College of Southern Nevada; Paul Garrett, ITT Technical Institute; Mark Hughes, Cleveland Community College; Lisa Jones, Southwest Tennessee Community College; Max Rabiee, University of Cincinnati; and Jim Rhodes, Blue Ridge Community College.

Tom Floyd

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BRIEF CONTENTS

1 Introduction to Electronics 1

2 Diodes and Applications 30

3 Special-Purpose Diodes 112

4 Bipolar Junction Transistors 173

5 Transistor Bias Circuits 228

6 BJT Amplifiers 271

7 Power Amplifiers 339

8 Field-Effect Transistors (FETs) 384

9 FET Amplifiers and Switching Circuits 451

10 Amplifier Frequency Response 505

11 Thyristors 564

12 The Operational Amplifier 602

13 Basic Op-Amp Circuits 667

14 Special-Purpose Op-Amp Circuits 718

15 Active Filters 763

16 Oscillators 806

17 Voltage Regulators 851

18 Basic Programming Concepts for Automated Testing 890

Answers to Odd-Numbered Problems 931

Glossary 944

Index 951

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CONTENTS

1 Introduction to Electronics 1

1–1 The Atom 2
1–2 Materials Used in Electronics 7
1–3 Current in Semiconductors 11
1–4 *N*-Type and *P*-Type Semiconductors 14
1–5 The *PN* Junction 16
GreenTech Application 1: *Solar Power* 24

2 Diodes and Applications 30

2–1 Diode Operation 31
2–2 Voltage-Current (*V-I*) Characteristics 36
2–3 Diode Models 39
2–4 Half-Wave Rectifiers 44
2–5 Full-Wave Rectifiers 50
2–6 Power Supply Filters and Regulators 57
2–7 Diode Limiters and Clampers 64
2–8 Voltage Multipliers 71
2–9 The Diode Datasheet 73
2–10 Troubleshooting 76
Application Activity 85
GreenTech Application 2: *Solar Power* 108

3 Special-Purpose Diodes 112

3–1 The Zener Diode 113
3–2 Zener Diode Applications 120
3–3 The Varactor Diode 128
3–4 Optical Diodes 133
3–5 Other Types of Diodes 147
3–6 Troubleshooting 153
Application Activity 155
GreenTech Application 3: *Solar Power* 170

4 Bipolar Junction Transistors 173

4–1 Bipolar Junction Transistor (BJT) Structure 174
4–2 Basic BJT Operation 175
4–3 BJT Characteristics and Parameters 177
4–4 The BJT as an Amplifier 190
4–5 The BJT as a Switch 192
4–6 The Phototransistor 196
4–7 Transistor Categories and Packaging 199
4–8 Troubleshooting 201
Application Activity 208
GreenTech Application 4: *Solar Power* 224

5 Transistor Bias Circuits 228

5–1 The DC Operating Point 229
5–2 Voltage-Divider Bias 235
5–3 Other Bias Methods 241
5–4 Troubleshooting 248
Application Activity 252
GreenTech Application 5: *Wind Power* 267

6 BJT Amplifiers 271

6–1 Amplifier Operation 272
6–2 Transistor AC Models 275
6–3 The Common-Emitter Amplifier 278
6–4 The Common-Collector Amplifier 291
6–5 The Common-Base Amplifier 298
6–6 Multistage Amplifiers 301
6–7 The Differential Amplifier 304
6–8 Troubleshooting 310
Application Activity 314
GreenTech Application 6: *Wind Power* 335

7 Power Amplifiers 339

7–1 The Class A Power Amplifier 340
7–2 The Class B and Class AB Push-Pull Amplifiers 346
7–3 The Class C Amplifier 357
7–4 Troubleshooting 365
Application Activity 368

8 Field-Effect Transistors (FETs) 384

8–1 The JFET 385
8–2 JFET Characteristics and Parameters 387
8–3 JFET Biasing 397
8–4 The Ohmic Region 408
8–5 The MOSFET 412

8–6 MOSFET Characteristics and Parameters 417
8–7 MOSFET Biasing 420
8–8 The IGBT 423
8–9 Troubleshooting 425
Application Activity 427

9 FET Amplifiers and Switching Circuits 451

9–1 The Common-Source Amplifier 452
9–2 The Common-Drain Amplifier 464
9–3 The Common-Gate Amplifier 467
9–4 The Class D Amplifier 470
9–5 MOSFET Analog Switching 474
9–6 MOSFET Digital Switching 479
9–7 Troubleshooting 482
Application Activity 485

10 Amplifier Frequency Response 505

10–1 Basic Concepts 506
10–2 The Decibel 509
10–3 Low-Frequency Amplifier Response 512
10–4 High-Frequency Amplifier Response 530
10–5 Total Amplifier Frequency Response 540
10–6 Frequency Response of Multistage Amplifiers 543
10–7 Frequency Response Measurements 546
Application Activity 549

11 Thyristors 564

11–1 The Four-Layer Diode 565
11–2 The Silicon-Controlled Rectifier (SCR) 568
11–3 SCR Applications 573
11–4 The Diac and Triac 578
11–5 The Silicon-Controlled Switch (SCS) 582
11–6 The Unijunction Transistor (UJT) 583
11–7 The Programmable Unijunction Transistor (PUT) 588
Application Activity 590

12 The Operational Amplifier 602

12–1 Introduction to Operational Amplifiers 603
12–2 Op-Amp Input Modes and Parameters 605
12–3 Negative Feedback 613
12–4 Op-Amps with Negative Feedback 614
12–5 Effects of Negative Feedback on Op-Amp Impedances 619
12–6 Bias Current and Offset Voltage 624
12–7 Open-Loop Frequency and Phase Responses 627
12–8 Closed-Loop Frequency Response 633
12–9 Troubleshooting 636
Application Activity 638
Programmable Analog Technology 644

13 Basic Op-Amp Circuits 667

13–1 Comparators 668
13–2 Summing Amplifiers 679
13–3 Integrators and Differentiators 687
13–4 Troubleshooting 694
Application Activity 698
Programmable Analog Technology 704

14 Special-Purpose Op-Amp Circuits 718

14–1 Instrumentation Amplifiers 719
14–2 Isolation Amplifiers 725
14–3 Operational Transconductance Amplifiers (OTAs) 730
14–4 Log and Antilog Amplifiers 736
14–5 Converters and Other Op-Amp Circuits 742
Application Activity 744
Programmable Analog Technology 750

15 Active Filters 763

15–1 Basic Filter Responses 764
15–2 Filter Response Characteristics 768
15–3 Active Low-Pass Filters 772
15–4 Active High-Pass Filters 776
15–5 Active Band-Pass Filters 779
15–6 Active Band-Stop Filters 785
15–7 Filter Response Measurements 787
Application Activity 789
Programmable Analog Technology 794

16 Oscillators 806

16–1 The Oscillator 807
16–2 Feedback Oscillators 808
16–3 Oscillators with *RC* Feedback Circuits 810
16–4 Oscillators with *LC* Feedback Circuits 817
16–5 Relaxation Oscillators 825
16–6 The 555 Timer as an Oscillator 830
Application Activity 836
Programmable Analog Technology 840

17 Voltage Regulators 851

17–1 Voltage Regulation 852
17–2 Basic Linear Series Regulators 855
17–3 Basic Linear Shunt Regulators 860
17–4 Basic Switching Regulators 863
17–5 Integrated Circuit Voltage Regulators 869
17–6 Integrated Circuit Voltage Regulator Configurations 875
Application Activity 879

18 Basic Programming Concepts for Automated Testing 890

18–1 Programming Basics 891
18–2 Automated Testing Basics 893
18–3 The Simple Sequential Program 898
18–4 Conditional Execution 900
18–5 Program Loops 905
18–6 Branching and Subroutines 913

Answers to Odd-Numbered Problems 931

Glossary 944

Index 951

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1

INTRODUCTION TO ELECTRONICS

CHAPTER OUTLINE

1–1 The Atom
1–2 Materials Used in Electronics
1–3 Current in Semiconductors
1–4 *N*-Type and *P*-Type Semiconductors
1–5 The *PN* Junction
GreenTech Application 1: *Solar Power*

CHAPTER OBJECTIVES

- Describe the structure of an atom
- Discuss insulators, conductors, and semiconductors and how they differ
- Describe how current is produced in a semiconductor
- Describe the properties of *n*-type and *p*-type semiconductors
- Describe how a *pn* junction is formed

KEY TERMS

- Atom
- Proton
- Electron
- Shell
- Valence
- Ionization
- Free electron
- Orbital
- Insulator
- Conductor
- Semiconductor
- Silicon
- Crystal
- Hole
- Doping
- *PN* junction
- Barrier potential

VISIT THE COMPANION WEBSITE

Study aids for this chapter are available at
http://www.pearsonhighered.com/electronics

INTRODUCTION

Electronic devices such as diodes, transistors, and integrated circuits are made of a semiconductive material. To understand how these devices work, you should have a basic knowledge of the structure of atoms and the interaction of atomic particles. An important concept introduced in this chapter is that of the *pn* junction that is formed when two different types of semiconductive material are joined. The *pn* junction is fundamental to the operation of devices such as the solar cell, the diode, and certain types of transistors.

1–1 THE ATOM

All matter is composed of atoms; all atoms consist of electrons, protons, and neutrons except normal hydrogen, which does not have a neutron. Each element in the periodic table has a unique atomic structure, and all atoms within a given element have the same number of protons. At first, the atom was thought to be a tiny indivisible sphere. Later it was shown that the atom was not a single particle but was made up of a small dense nucleus around which electrons orbit at great distances from the nucleus, similar to the way planets orbit the sun. Niels Bohr proposed that the electrons in an atom circle the nucleus in different obits, similar to the way planets orbit the sun in our solar system. The Bohr model is often referred to as the planetary model. Another view of the atom called the *quantum model* is considered a more accurate representation, but it is difficult to visualize. For most practical purposes in electronics, the Bohr model suffices and is commonly used because it is easy to visualize.

After completing this section, you should be able to

- ❑ **Describe the structure of an atom**
    - ◆ Discuss the Bohr model of an atom ◆ Define *electron, proton, neutron,* and *nucleus*
- ❑ Define *atomic number*
- ❑ Discuss electron shells and orbits
    - ◆ Explain energy levels
- ❑ Define *valence electron*
- ❑ Discuss ionization
    - ◆ Define *free electron* and *ion*
- ❑ Discuss the basic concept of the quantum model of the atom

The Bohr Model

An **atom***[*] is the smallest particle of an element that retains the characteristics of that element. Each of the known 118 elements has atoms that are different from the atoms of all other elements. This gives each element a unique atomic structure. According to the classical Bohr model, atoms have a planetary type of structure that consists of a central nucleus surrounded by orbiting electrons, as illustrated in Figure 1–1. The **nucleus** consists of positively charged particles called **protons** and uncharged particles called **neutrons.** The basic particles of negative charge are called **electrons**.

Each type of atom has a certain number of electrons and protons that distinguishes it from the atoms of all other elements. For example, the simplest atom is that of hydrogen, which has one proton and one electron, as shown in Figure 1–2(a). As another example, the helium atom, shown in Figure 1–2(b), has two protons and two neutrons in the nucleus and two electrons orbiting the nucleus.

HISTORY NOTE

Niels Henrik David Bohr (October 7, 1885–November 18, 1962) was a Danish physicist, who made important contributions to understanding the structure of the atom and quantum mechanics by postulating the “planetary” model of the atom. He received the Nobel prize in physics in 1922. Bohr drew upon the work or collaborated with scientists such as Dalton, Thomson, and Rutherford, among others and has been described as one of the most influential physicists of the 20th century.

Atomic Number

All elements are arranged in the periodic table of the elements in order according to their atomic number. The **atomic number** equals the number of protons in the nucleus, which is the same as the number of electrons in an electrically balanced (neutral) atom. For example, hydrogen has an atomic number of 1 and helium has an atomic number of 2. In their normal (or neutral) state, all atoms of a given element have the same number of electrons as protons; the positive charges cancel the negative charges, and the atom has a net charge of zero.

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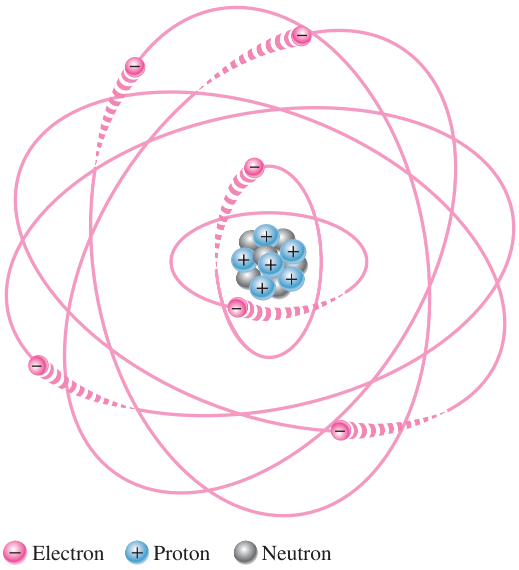
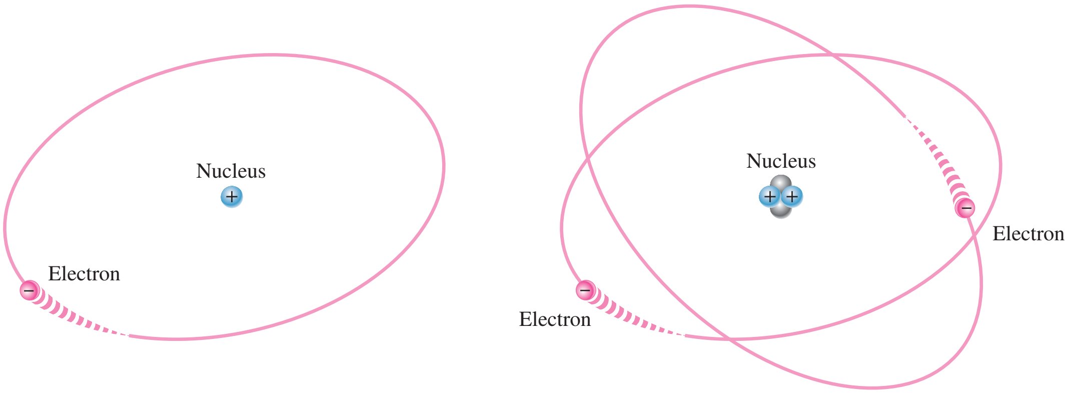
[*] **All bold terms are in the end-of-book glossary. The bold terms in color are key terms and are also defined at the end of the chapter.**



▲ **FIGURE 1–1**

The Bohr model of an atom showing electrons in orbits around the nucleus, which consists of protons and neutrons. The “tails” on the electrons indicate motion.



(a) Hydrogen atom

(b) Helium atom

▲ **FIGURE 1–2**

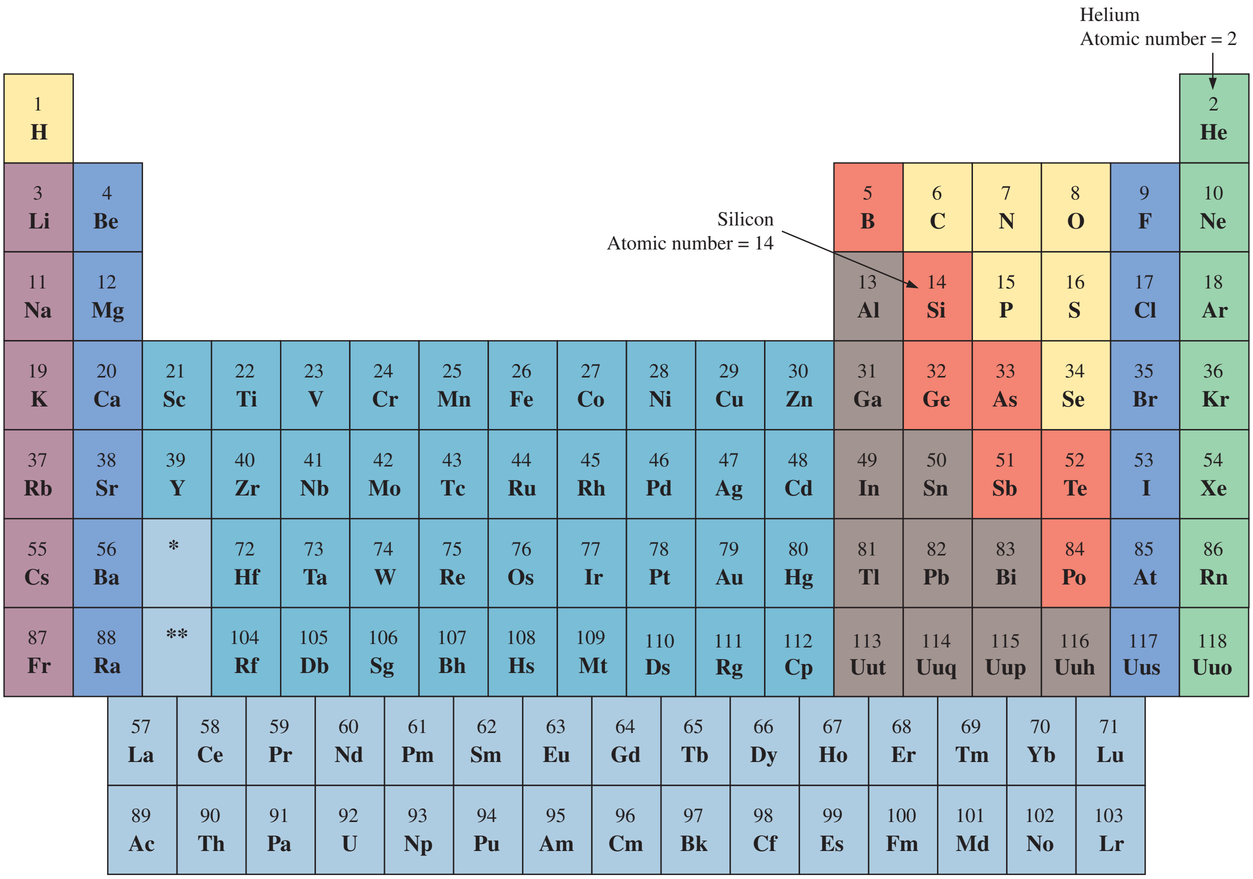
Two simple atoms, hydrogen and helium.

Atomic numbers of all the elements are shown on the periodic table of the elements in Figure 1–3.

Electrons and Shells

Energy Levels Electrons orbit the nucleus of an atom at certain distances from the nucleus. Electrons near the nucleus have less energy than those in more distant orbits. Only discrete (separate and distinct) values of electron energies exist within atomic structures. Therefore, electrons must orbit only at discrete distances from the nucleus.

Each discrete distance (**orbit**) from the nucleus corresponds to a certain energy level. In an atom, the orbits are grouped into energy levels known as **shells**. A given atom has a fixed number of shells. Each shell has a fixed maximum number of electrons. The shells (energy levels) are designated 1, 2, 3, and so on, with 1 being closest to the nucleus. The Bohr model of the silicon atom is shown in Figure 1–4. Notice that there are 14 electrons and 14 each of protons and neutrons in the nucleus.


Helium
Atomic number = 2
Silicon
Atomic number = 14

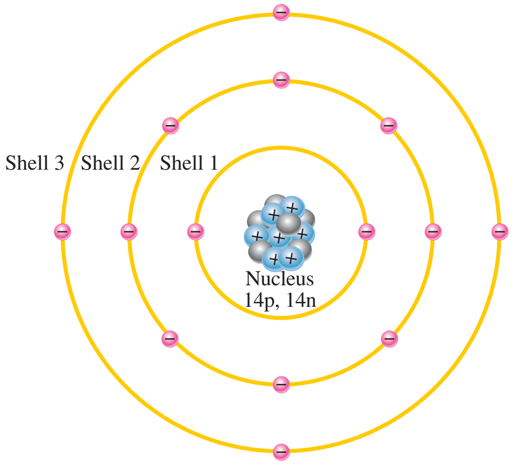
1 H																	2 He
3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba	*	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra	**	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cp	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo
		57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu	
		89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr	

▲ **FIGURE 1–3**

The periodic table of the elements. Some tables also show atomic mass.

▶ **FIGURE 1–4**

Illustration of the Bohr model of the silicon atom.



The Maximum Number of Electrons in Each Shell The maximum number of electrons (N_e) that can exist in each shell of an atom is a fact of nature and can be calculated by the formula,

Equation 1–1

$$N_e = 2n^2$$

where n is the number of the shell. The maximum number of electrons that can exist in the innermost shell (shell 1) is

$$N_e = 2n^2 = 2(1)^2 = 2$$

The maximum number of electrons that can exist in shell 2 is

$$N_e = 2n^2 = 2(2)^2 = 2(4) = 8$$

The maximum number of electrons that can exist in shell 3 is

$$N_e = 2n^2 = 2(3)^2 = 2(9) = 18$$

The maximum number of electrons that can exist in shell 4 is

$$N_e = 2n^2 = 2(4)^2 = 2(16) = 32$$

Valence Electrons

Electrons that are in orbits farther from the nucleus have higher energy and are less tightly bound to the atom than those closer to the nucleus. This is because the force of attraction between the positively charged nucleus and the negatively charged electron decreases with increasing distance from the nucleus. Electrons with the highest energy exist in the outermost shell of an atom and are relatively loosely bound to the atom. This outermost shell is known as the **valence** shell and electrons in this shell are called *valence electrons.* These valence electrons contribute to chemical reactions and bonding within the structure of a material and determine its electrical properties. When a valence electron gains sufficient energy from an external source, it can break free from its atom. This is the basis for conduction in materials.

FYI

Atoms are extremely small and cannot be seen even with the strongest optical microscopes; however, a scanning tunneling microscope can detect a single atom. The nucleus is so small and the electrons orbit at such distances that the atom is mostly empty space. To put it in perspective, if the proton in a hydrogen atom were the size of a golf ball, the electron orbit would be approximately one mile away.

Protons and neutrons are approximately the same mass. The mass of an electron is 1/1836 of a proton. Within protons and neutrons there are even smaller particles called quarks.

Ionization

When an atom absorbs energy from a heat source or from light, for example, the energies of the electrons are raised. The valence electrons possess more energy and are more loosely bound to the atom than inner electrons, so they can easily jump to higher energy shells when external energy is absorbed by the atom.

If a valence electron acquires a sufficient amount of energy, called *ionization energy,* it can actually escape from the outer shell and the atom's influence. The departure of a valence electron leaves a previously neutral atom with an excess of positive charge (more protons than electrons). The process of losing a valence electron is known as **ionization**, and the resulting positively charged atom is called a *positive ion.* For example, the chemical symbol for hydrogen is H. When a neutral hydrogen atom loses its valence electron and becomes a positive ion, it is designated H^+. The escaped valence electron is called a **free electron**.

The reverse process can occur in certain atoms when a free electron collides with the atom and is captured, releasing energy. The atom that has acquired the extra electron is called a *negative ion*. The ionization process is not restricted to single atoms. In many chemical reactions, a group of atoms that are bonded together can lose or acquire one or more electrons.

For some nonmetallic materials such as chlorine, a free electron can be captured by the neutral atom, forming a negative ion. In the case of chlorine, the ion is more stable than the neutral atom because it has a filled outer shell. The chlorine ion is designated as Cl^-.

The Quantum Model

Although the Bohr model of an atom is widely used because of its simplicity and ease of visualization, it is not a complete model. The quantum model, a more recent model, is considered to be more accurate. The quantum model is a statistical model and very difficult to understand or visualize. Like the Bohr model, the quantum model has a nucleus of protons and neutrons surrounded by electrons. Unlike the Bohr model, the electrons in the quantum model do not exist in precise circular orbits as particles. Two important theories underlie the quantum model: the wave-particle duality and the uncertainty principle.

- *Wave-particle duality.* Just as light can be both a wave and a particle **(photon),** electrons are thought to exhibit a dual characteristic. The velocity of an orbiting electron is considered to be its wavelength, which interferes with neighboring electron waves by amplifying or canceling each other.

FYI

De Broglie showed that every particle has wave characteristics. Schrodiger developed a wave equation for electrons.

- *Uncertainly principle.* As you know, a wave is characterized by peaks and valleys; therefore, electrons acting as waves cannot be precisely identified in terms of their position. According to Heisenberg, it is impossible to determine simultaneously both the position and velocity of an electron with any degree of accuracy or certainty. The result of this principle produces a concept of the atom with *probability clouds,* which are mathematical descriptions of where electrons in an atom are most likely to be located.

In the quantum model, each shell or energy level consists of up to four subshells called **orbitals**, which are designated *s*, *p*, *d*, and *f*. Orbital *s* can hold a maximum of two electrons, orbital *p* can hold six electrons, orbital *d* can hold ten electrons, and orbital *f* can hold fourteen electrons. Each atom can be described by an electron configuration table that shows the shells or energy levels, the orbitals, and the number of electrons in each orbital. For example, the electron configuration table for the nitrogen atom is given in Table 1–1. The first full-size number is the shell or energy level, the letter is the orbital, and the exponent is the number of electrons in the orbital.

TABLE 1–1

Electron configuration table for nitrogen.

NOTATION	EXPLANATION
$1s^2$	2 electrons in shell 1, orbital *s*
$2s^2$ $2p^3$	5 electrons in shell 2: 2 in orbital *s*, 3 in orbital *p*

Atomic orbitals do not resemble a discrete circular path for the electron as depicted in Bohr's planetary model. In the quantum picture, each shell in the Bohr model is a three-dimensional space surrounding the atom that represents the mean (average) energy of the electron cloud. The term **electron cloud** (probability cloud) is used to describe the area around an atom's nucleus where an electron will probably be found.

EXAMPLE 1–1

Using the atomic number from the periodic table in Figure 1–3, describe a silicon (Si) atom using an electron configuration table.

Solution The atomic number of silicon is 14. This means that there are 14 protons in the nucleus. Since there is always the same number of electrons as protons in a neutral atom, there are also 14 electrons. As you know, there can be up to two electrons in shell 1, eight in shell 2, and eighteen in shell 3. Therefore, in silicon there are two electrons in shell 1, eight electrons in shell 2, and four electrons in shell 3 for a total of 14 electrons. The electron configuration table for silicon is shown in Table 1–2.

TABLE 1–2

NOTATION	EXPLANATION
$1s^2$	2 electrons in shell 1, orbital *s*
$2s^2$ $2p^6$	8 electrons in shell 2: 2 in orbital *s*, 6 in orbital *p*
$3s^2$ $3p^2$	4 electrons in shell 3: 2 in orbital *s*, 2 in orbital *p*

*Related Problem** Develop an electron configuration table for the germanium (Ge) atom in the periodic table.

---

*Answers can be found at www.pearsonhighered.com/floyd.

In a three-dimensional representation of the quantum model of an atom, the *s*-orbitals are shaped like spheres with the nucleus in the center. For energy level 1, the sphere is "solid" but for energy levels 2 or more, each single *s*-orbital is composed of spherical surfaces that are nested shells. A *p*-orbital for shell 2 has the form of two ellipsoidal lobes with a point of tangency at the nucleus (sometimes referred to as a dumbbell shape.) The three *p*-orbitals in each energy level are oriented at right angles to each other. One is oriented on the *x*-axis, one on the *y*-axis, and one on the *z*-axis. For example, a view of the quantum model of a sodium atom (Na) that has 11 electrons is shown in Figure 1–5. The three axes are shown to give you a 3-D perspective.

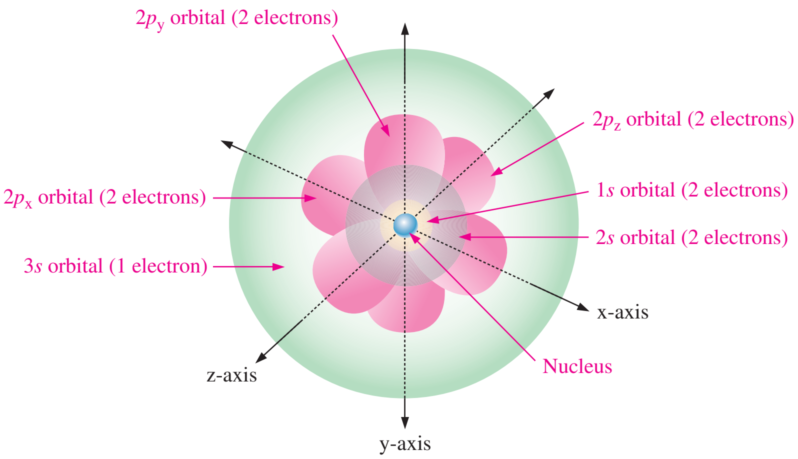

$2p_y$ orbital (2 electrons)
$2p_z$ orbital (2 electrons)
$2p_x$ orbital (2 electrons)
$1s$ orbital (2 electrons)
$2s$ orbital (2 electrons)
$3s$ orbital (1 electron)
x-axis
Nucleus
z-axis
y-axis

FIGURE 1–5

Three-dimensional quantum model of the sodium atom, showing the orbitals and number of electrons in each orbital.

SECTION 1–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

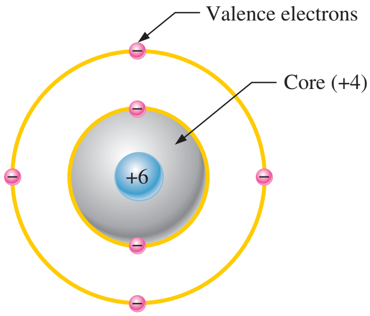
1. Describe the Bohr model of the atom.
2. Define *electron.*
3. What is the nucleus of an atom composed of? Define each component.
4. Define *atomic number.*
5. Discuss electron shells and orbits and their energy levels.
6. What is a valence electron?
7. What is a free electron?
8. Discuss the difference between positive and negative ionization.
9. Name two theories that distinguish the quantum model.

1–2 MATERIALS USED IN ELECTRONICS

In terms of their electrical properties, materials can be classified into three groups: conductors, semiconductors, and insulators. When atoms combine to form a solid, crystalline material, they arrange themselves in a symmetrical pattern. The atoms within the crystal structure are held together by covalent bonds, which are created by the interaction of the valence electrons of the atoms. Silicon is a crystalline material.

After completing this section, you should be able to

- ☐ **Discuss insulators, conductors, and semiconductors and how they differ**
  ◆ Define the *core* of an atom ◆ Describe the carbon atom ◆ Name two types each of semiconductors, conductors, and insulators
- ☐ Explain the band gap
  ◆ Define *valence band* and *conduction band* ◆ Compare a semiconductor atom to a conductor atom
- ☐ Discuss silicon and gemanium atoms
- ☐ Explain covalent bonds
  ◆ Define *crystal*



▲ FIGURE 1–6

Diagram of a carbon atom.

Insulators, Conductors, and Semiconductors

All materials are made up of atoms. These atoms contribute to the electrical properties of a material, including its ability to conduct electrical current.

For purposes of discussing electrical properties, an atom can be represented by the valence shell and a **core** that consists of all the inner shells and the nucleus. This concept is illustrated in Figure 1–6 for a carbon atom. Carbon is used in some types of electrical resistors. Notice that the carbon atom has four electrons in the valence shell and two electrons in the inner shell. The nucleus consists of six protons and six neutrons, so the +6 indicates the positive charge of the six protons. The core has a net charge of +4 (+6 for the nucleus and −2 for the two inner-shell electrons).

Insulators An **insulator** is a material that does not conduct electrical current under normal conditions. Most good insulators are compounds rather than single-element materials and have very high resistivities. Valence electrons are tightly bound to the atoms; therefore, there are very few free electrons in an insulator. Examples of insulators are rubber, plastics, glass, mica, and quartz.

Conductors A **conductor** is a material that easily conducts electrical current. Most metals are good conductors. The best conductors are single-element materials, such as copper (Cu), silver (Ag), gold (Au), and aluminum (Al), which are characterized by atoms with only one valence electron very loosely bound to the atom. These loosely bound valence electrons become free electrons. Therefore, in a conductive material the free electrons are valence electrons.

Semiconductors A **semiconductor** is a material that is between conductors and insulators in its ability to conduct electrical current. A semiconductor in its pure (intrinsic) state is neither a good conductor nor a good insulator. Single-element semiconductors are antimony (Sb), arsenic (As), astatine (At), boron (B), polonium (Po), tellurium (Te), silicon (Si), and germanium (Ge). Compound semiconductors such as gallium arsenide, indium phosphide, gallium nitride, silicon carbide, and silicon germanium are also commonly used. The single-element semiconductors are characterized by atoms with four valence electrons. Silicon is the most commonly used semiconductor.

Band Gap

Recall that the valence shell of an atom represents a band of energy levels and that the valence electrons are confined to that band. When an electron acquires enough additional energy, it can leave the valence shell, become a *free electron,* and exist in what is known as the *conduction band.*

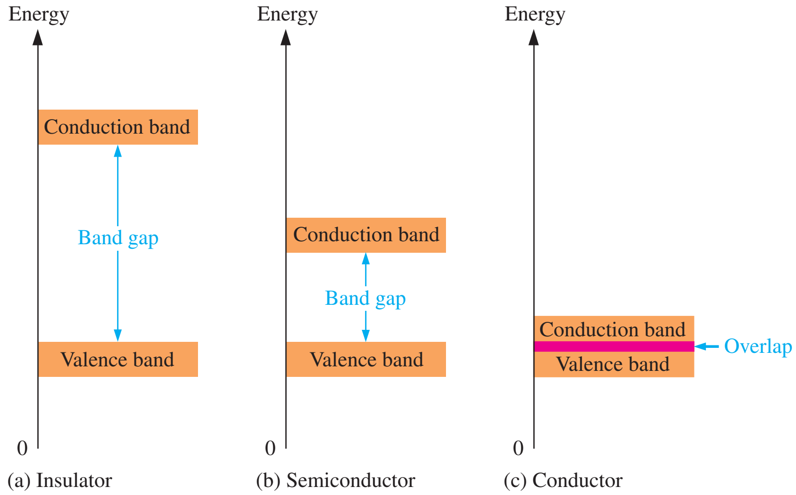
The difference in energy between the valence band and the conduction band is called an *energy gap* or **band gap**. This is the amount of energy that a valence electron must have in order to jump from the valence band to the conduction band. Once in the conduction band, the electron is free to move throughout the material and is not tied to any given atom.

Figure 1–7 shows energy diagrams for insulators, semiconductors, and conductors. The energy gap or band gap is the difference between two energy levels and is “not allowed” in quantum theory. It is a region in insulators and semiconductors where no electron states exist. Although an electron may not exist in this region, it can “jump” across it under certain conditions. For insulators, the gap can be crossed only when breakdown conditions occur—as when a very high voltage is applied across the material. The band gap is illustrated in Figure 1–7(a) for insulators. In semiconductors the band gap is smaller, allowing an electron in the valence band to jump into the conduction band if it absorbs a photon. The band gap depends on the semiconductor material. This is illustrated in Figure 1–7(b). In conductors, the conduction band and valence band overlap, so there is no gap, as shown in Figure 1–7(c). This means that electrons in the valence band move freely into the conduction band, so there are always electrons available as free electrons.

FYI

Next to silicon, the second most common semiconductor material is gallium arsenide, GaAs. This is a crystalline compound, not an element. Its properties can be controlled by varying the relative amount of gallium and arsenic.

GaAs has the advantage of making semiconductor devices that respond very quickly to electrical signals. This makes it better than silicon for applications like amplifying the high frequency (1 GHz to 10 GHz) signals from TV satellites, etc. The main disadvantage of GaAs is that it is more difficult to make and the chemicals involved are quite often toxic!



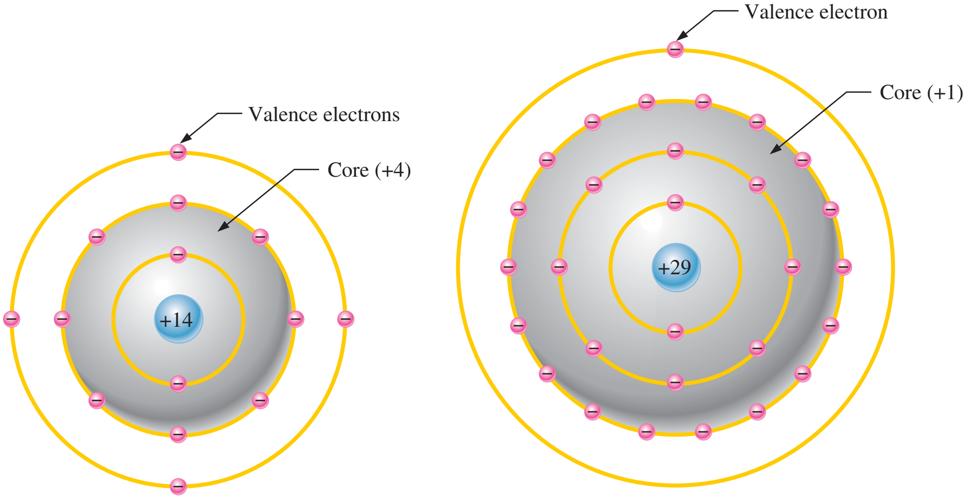
(a) Insulator (b) Semiconductor (c) Conductor

FIGURE 1–7

Energy diagrams for the three types of materials.

Comparison of a Semiconductor Atom to a Conductor Atom

Silicon is a semiconductor and copper is a conductor. Bohr diagrams of the silicon atom and the copper atom are shown in Figure 1–8. Notice that the core of the silicon atom has a net charge of +4 (14 protons − 10 electrons) and the core of the copper atom has a net charge of +1 (29 protons − 28 electrons). The core includes everything except the valence electrons.



(a) Silicon atom (b) Copper atom

FIGURE 1–8

Bohr diagrams of the silicon and copper atoms.

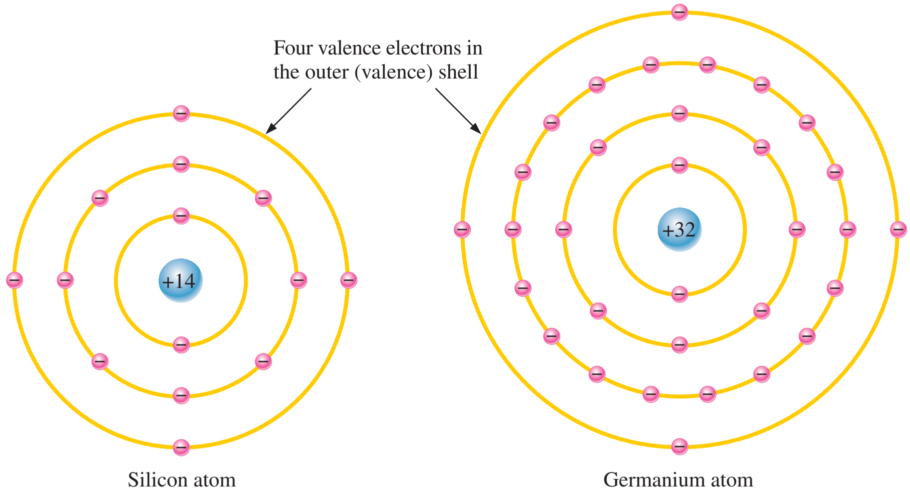
The valence electron in the copper atom "feels" an attractive force of +1 compared to a valence electron in the silicon atom which "feels" an attractive force of +4. Therefore, there is more force trying to hold a valence electron to the atom in silicon than in copper. The copper's valence electron is in the fourth shell, which is a greater distance from its nucleus than the silicon's valence electron in the third shell. Recall that electrons farthest from the nucleus have the most energy. The valence electron in copper has more energy than the valence electron in silicon. This means that it is easier for valence electrons in copper to acquire enough additional energy to escape from their atoms and become free electrons than it is in silicon. In fact, large numbers of valence electrons in copper already have sufficient energy to be free electrons at normal room temperature.

Silicon and Germanium

The atomic structures of silicon and germanium are compared in Figure 1–9. **Silicon** is used in diodes, transistors, integrated circuits, and other semiconductor devices. Notice that both silicon and **germanium** have the characteristic four valence electrons.

FIGURE 1–9

Diagrams of the silicon and germanium atoms.

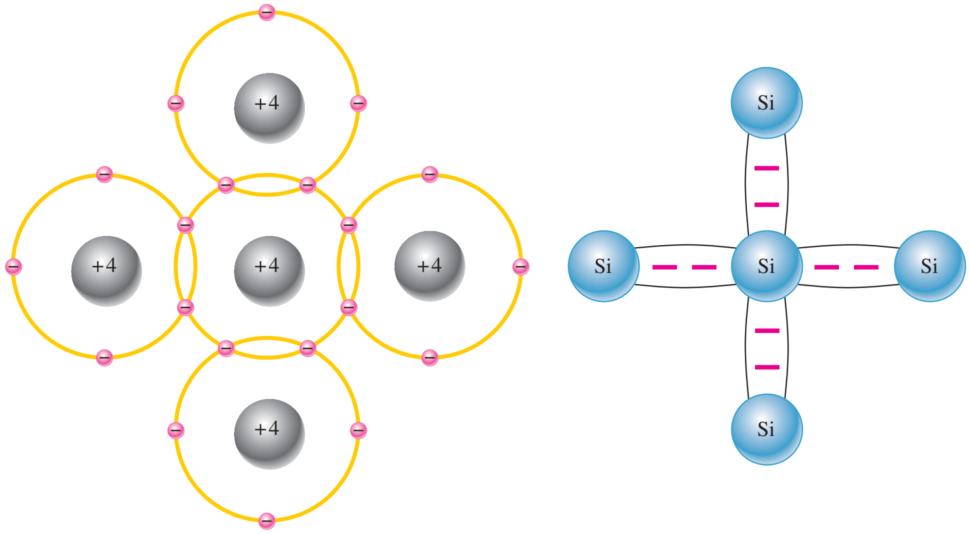


The valence electrons in germanium are in the fourth shell while those in silicon are in the third shell, closer to the nucleus. This means that the germanium valence electrons are at higher energy levels than those in silicon and, therefore, require a smaller amount of additional energy to escape from the atom. This property makes germanium more unstable at high temperatures and results in excessive reverse current. This is why silicon is a more widely used semiconductive material.

Covalent Bonds Figure 1–10 shows how each silicon atom positions itself with four adjacent silicon atoms to form a silicon **crystal**. A silicon (Si) atom with its four valence electrons shares an electron with each of its four neighbors. This effectively creates eight shared valence electrons for each atom and produces a state of chemical stability. Also, this sharing of valence electrons produces the **covalent** bonds that hold the atoms together; each valence electron is attracted equally by the two adjacent atoms which share it. Covalent bonding in an intrinsic silicon crystal is shown in Figure 1–11. An **intrinsic** crystal is one that has no impurities. Covalent bonding for germanium is similar because it also has four valence electrons.

FIGURE 1–10

Illustration of covalent bonds in silicon.



(a) The center silicon atom shares an electron with each of the four surrounding silicon atoms, creating a covalent bond with each. The surrounding atoms are in turn bonded to other atoms, and so on.

(b) Bonding diagram. The red negative signs represent the shared valence electrons.

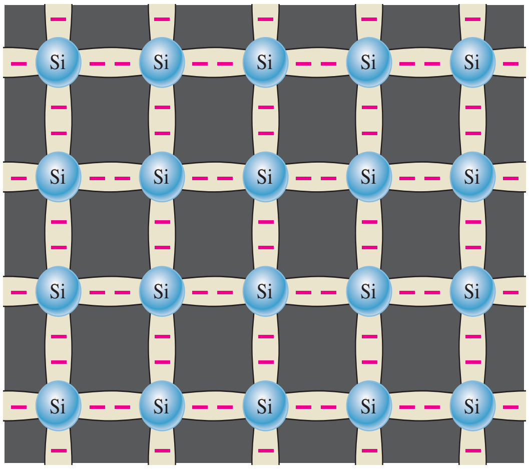


FIGURE 1–11

Covalent bonds in a silicon crystal.

SECTION 1–2 CHECKUP

1. What is the basic difference between conductors and insulators?
2. How do semiconductors differ from conductors and insulators?
3. How many valence electrons does a conductor such as copper have?
4. How many valence electrons does a semiconductor have?
5. Name three of the best conductive materials.
6. What is the most widely used semiconductive material?
7. Why does a semiconductor have fewer free electrons than a conductor?
8. How are covalent bonds formed?
9. What is meant by the term *intrinsic*?
10. What is a crystal?

1–3 CURRENT IN SEMICONDUCTORS

The way a material conducts electrical current is important in understanding how electronic devices operate. You can't really understand the operation of a device such as a diode or transistor without knowing something about current in semiconductors.

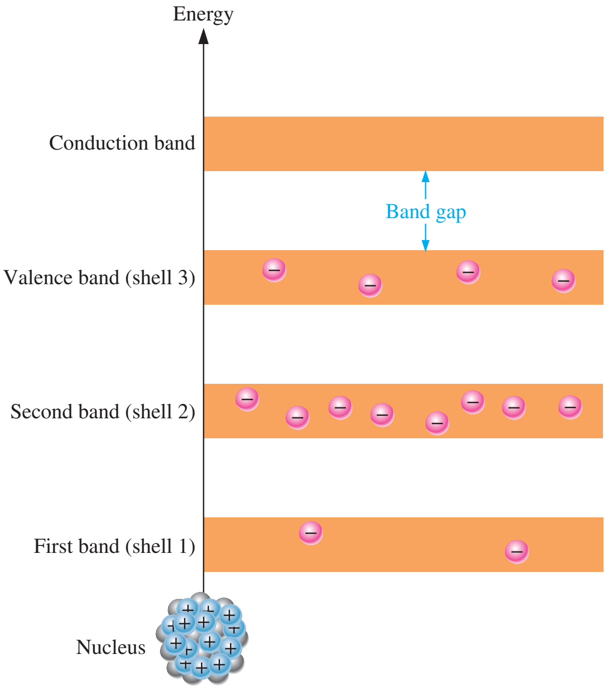
After completing this section, you should be able to

- **Describe how current is produced in a semiconductor**
- Discuss conduction electrons and holes
  - Explain an electron-hole pair
  - Discuss recombination
- Explain electron and hole current

As you have learned, the electrons of an atom can exist only within prescribed energy bands. Each shell around the nucleus corresponds to a certain energy band and is separated from adjacent shells by band gaps, in which no electrons can exist. Figure 1–12 shows the energy band diagram for an unexcited (no external energy such as heat) atom in a pure silicon crystal. This condition occurs *only* at a temperature of absolute 0 Kelvin.

FIGURE 1–12

Energy band diagram for an unexcited atom in a pure (intrinsic) silicon crystal. There are no electrons in the conduction band.



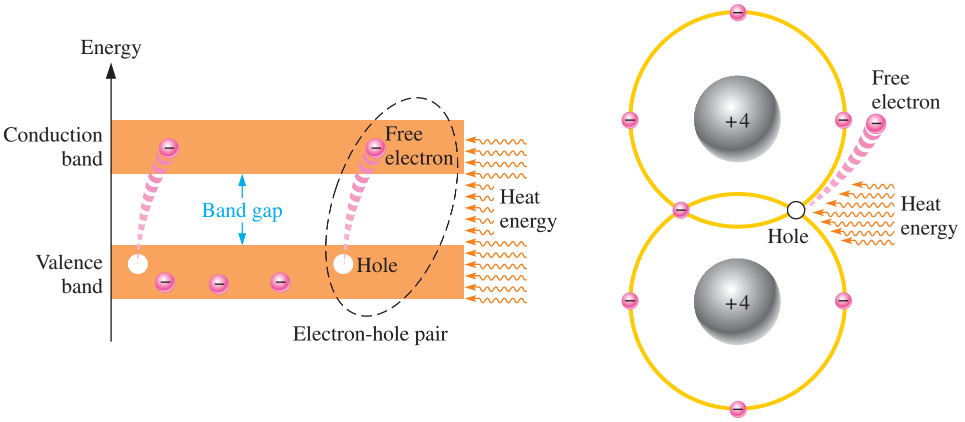
Energy
Conduction band
Band gap
Valence band (shell 3)
Second band (shell 2)
First band (shell 1)
Nucleus

Conduction Electrons and Holes

An intrinsic (pure) silicon crystal at room temperature has sufficient heat (thermal) energy for some valence electrons to jump the gap from the valence band into the conduction band, becoming free electrons. Free electrons are also called **conduction electrons.** This is illustrated in the energy diagram of Figure 1–13(a) and in the bonding diagram of Figure 1–13(b).

FIGURE 1–13

Creation of electron-hole pairs in a silicon crystal. Electrons in the conduction band are free electrons.



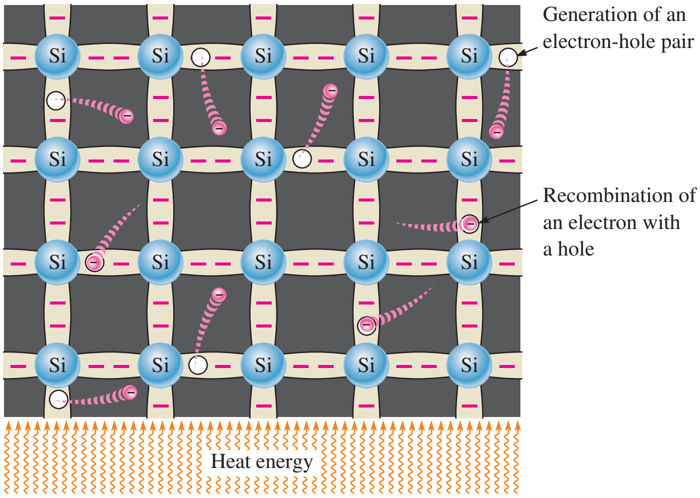
Energy
Conduction band
Band gap
Valence band
Free electron
Hole
Heat energy
Electron-hole pair
+4
+4
Free electron
Hole
Heat energy

(a) Energy diagram

(b) Bonding diagram

When an electron jumps to the conduction band, a vacancy is left in the valence band within the crystal. This vacancy is called a **hole**. For every electron raised to the conduction band by external energy, there is one hole left in the valence band, creating what is called an **electron-hole pair. Recombination** occurs when a conduction-band electron loses energy and falls back into a hole in the valence band.

To summarize, a piece of intrinsic silicon at room temperature has, at any instant, a number of conduction-band (free) electrons that are unattached to any atom and are essentially drifting randomly throughout the material. There is also an equal number of holes in the valence band created when these electrons jump into the conduction band. This is illustrated in Figure 1–14.

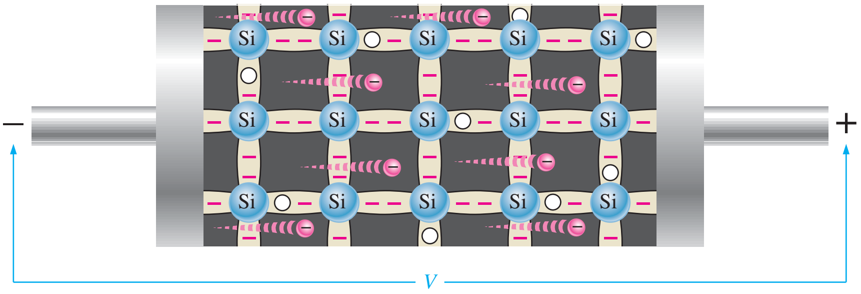

Generation of an electron-hole pair
Recombination of an electron with a hole
Heat energy
Si

◀ FIGURE 1–14

Electron-hole pairs in a silicon crystal. Free electrons are being generated continuously while some recombine with holes.

Electron and Hole Current

When a voltage is applied across a piece of intrinsic silicon, as shown in Figure 1-15, the thermally generated free electrons in the conduction band, which are free to move randomly in the crystal structure, are now easily attracted toward the positive end. This movement of free electrons is one type of **current** in a semiconductive material and is called *electron current.*



◀ FIGURE 1–15

Electron current in intrinsic silicon is produced by the movement of thermally generated free electrons.

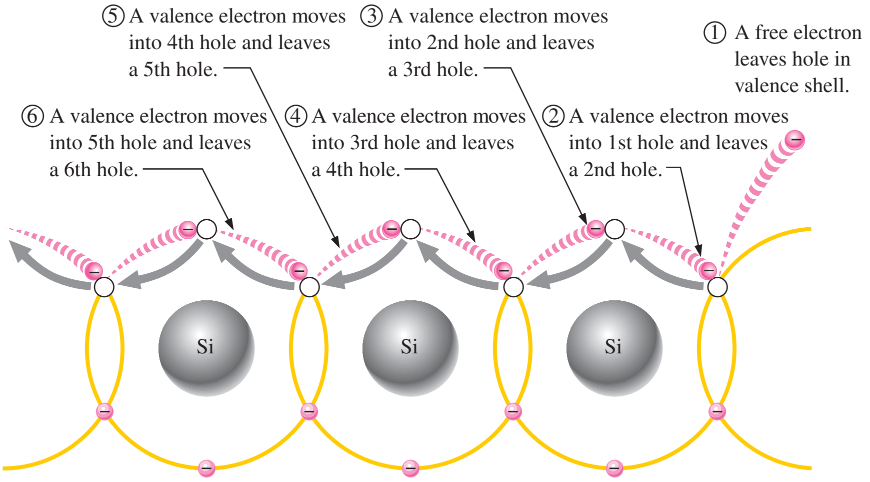
Another type of current occurs in the valence band, where the holes created by the free electrons exist. Electrons remaining in the valence band are still attached to their atoms and are not free to move randomly in the crystal structure as are the free electrons. However, a valence electron can move into a nearby hole with little change in its energy level, thus leaving another hole where it came from. Effectively the hole has moved from one place to another in the crystal structure, as illustrated in Figure 1–16. Although current in the valence band is produced by valence electrons, it is called *hole current* to distinguish it from electron current in the conduction band.

As you have seen, conduction in semiconductors is considered to be either the movement of free electrons in the conduction band or the movement of holes in the valence band, which is actually the movement of valence electrons to nearby atoms, creating hole current in the opposite direction.

It is interesting to contrast the two types of charge movement in a semiconductor with the charge movement in a metallic conductor, such as copper. Copper atoms form a different type of crystal in which the atoms are not covalently bonded to each other but consist of a “sea” of positive ion cores, which are atoms stripped of their valence electrons. The valence electrons are attracted to the positive ions, keeping the positive ions together and forming the metallic bond. The valence electrons do not belong to a given atom, but to the crystal as a whole. Since the valence electrons in copper are free to move, the application of a voltage results in current. There is only one type of current—the movement of free electrons—because there are no “holes” in the metallic crystal structure.

FIGURE 1–16

Hole current in intrinsic silicon.


⑤ A valence electron moves into 4th hole and leaves a 5th hole.
③ A valence electron moves into 2nd hole and leaves a 3rd hole.
① A free electron leaves hole in valence shell.
⑥ A valence electron moves into 5th hole and leaves a 6th hole.
④ A valence electron moves into 3rd hole and leaves a 4th hole.
② A valence electron moves into 1st hole and leaves a 2nd hole.
Si
Si
Si

When a valence electron moves left to right to fill a hole while leaving another hole behind, the hole has effectively moved from right to left. Gray arrows indicate effective movement of a hole.

SECTION 1–3 CHECKUP

1. Are free electrons in the valence band or in the conduction band?
2. Which electrons are responsible for electron current in silicon?
3. What is a hole?
4. At what energy level does hole current occur?

1–4 *N*-TYPE AND *P*-TYPE SEMICONDUCTORS

Semiconductive materials do not conduct current well and are of limited value in their intrinsic state. This is because of the limited number of free electrons in the conduction band and holes in the valence band. Intrinsic silicon (or germanium) must be modified by increasing the number of free electrons or holes to increase its conductivity and make it useful in electronic devices. This is done by adding impurities to the intrinsic material. Two types of extrinsic (impure) semiconductive materials, *n*-type and *p*-type, are the key building blocks for most types of electronic devices.

After completing this section, you should be able to

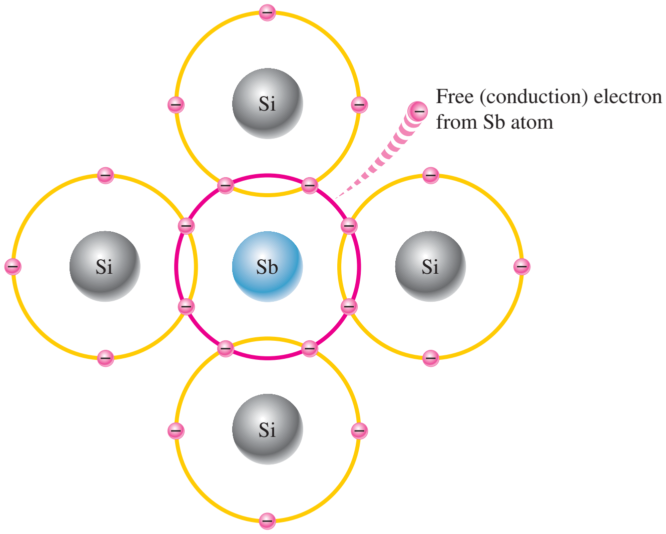
- **Describe the properties of *n*-type and *p*-type semiconductors**
  - Define *doping*
- Explain how *n*-type semiconductors are formed
  - Describe a majority carrier and minority carrier in *n*-type material
- Explain how *p*-type semiconductors are formed
  - Describe a majority carrier and minority carrier in *p*-type material

Since semiconductors are generally poor conductors, their conductivity can be drastically increased by the controlled addition of impurities to the intrinsic (pure) semiconductive material. This process, called **doping**, increases the number of current carriers (electrons or holes). The two categories of impurities are *n*-type and *p*-type.

N-Type Semiconductor

To increase the number of conduction-band electrons in intrinsic silicon, **pentavalent** impurity atoms are added. These are atoms with five valence electrons such as arsenic (As), phosphorus (P), bismuth (Bi), and antimony (Sb).

As illustrated in Figure 1–17, each pentavalent atom (antimony, in this case) forms covalent bonds with four adjacent silicon atoms. Four of the antimony atom's valence electrons are used to form the covalent bonds with silicon atoms, leaving one extra electron. This extra electron becomes a conduction electron because it is not involved in bonding. Because the pentavalent atom gives up an electron, it is often called a *donor atom.* The number of conduction electrons can be carefully controlled by the number of impurity atoms added to the silicon. A conduction electron created by this doping process does not leave a hole in the valence band because it is in excess of the number required to fill the valence band.



◀ **FIGURE 1–17**

Pentavalent impurity atom in a silicon crystal structure. An antimony (Sb) impurity atom is shown in the center. The extra electron from the Sb atom becomes a free electron.

Majority and Minority Carriers Since most of the current carriers are electrons, silicon (or germanium) doped with pentavalent atoms is an *n*-type semiconductor (the *n* stands for the negative charge on an electron). The electrons are called the **majority carriers** in *n*-type material. Although the majority of current carriers in *n*-type material are electrons, there are also a few holes that are created when electron-hole pairs are thermally generated. These holes are *not* produced by the addition of the pentavalent impurity atoms. Holes in an *n*-type material are called **minority carriers.**

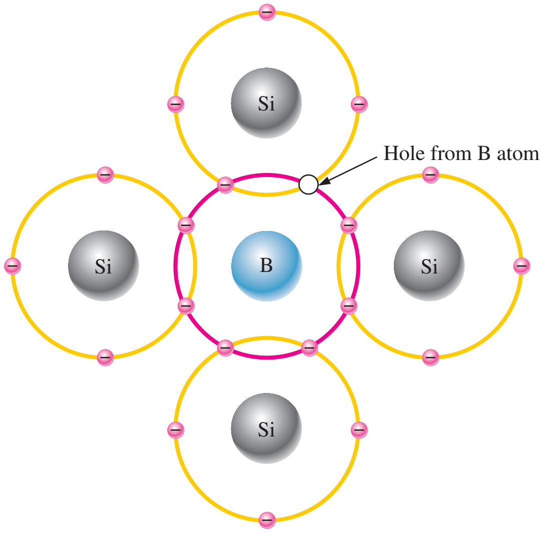
P-Type Semiconductor

To increase the number of holes in intrinsic silicon, **trivalent** impurity atoms are added. These are atoms with three valence electrons such as boron (B), indium (In), and gallium (Ga). As illustrated in Figure 1–18, each trivalent atom (boron, in this case) forms covalent bonds with four adjacent silicon atoms. All three of the boron atom's valence electrons are used in the covalent bonds; and, since four electrons are required, a hole results when each trivalent atom is added. Because the trivalent atom can take an electron, it is often referred to as an *acceptor atom.* The number of holes can be carefully controlled by the number of trivalent impurity atoms added to the silicon. A hole created by this doping process is *not* accompanied by a conduction (free) electron.

Majority and Minority Carriers Since most of the current carriers are holes, silicon (or germanium) doped with trivalent atoms is called a *p*-type semiconductor. The holes are the majority carriers in *p*-type material. Although the majority of current carriers in *p*-type material are holes, there are also a few conduction-band electrons that are created when electron-hole pairs are thermally generated. These conduction-band electrons are *not* produced by the addition of the trivalent impurity atoms. Conduction-band electrons in *p*-type material are the minority carriers.

▶ FIGURE 1–18

Trivalent impurity atom in a silicon crystal structure. A boron (B) impurity atom is shown in the center.



SECTION 1–4 CHECKUP

1. Define *doping.*
2. What is the difference between a pentavalent atom and a trivalent atom?
3. What are other names for the pentavalent and trivalent atoms?
4. How is an *n*-type semiconductor formed?
5. How is a *p*-type semiconductor formed?
6. What is the majority carrier in an *n*-type semiconductor?
7. What is the majority carrier in a *p*-type semiconductor?
8. By what process are the majority carriers produced?
9. By what process are the minority carriers produced?
10. What is the difference between intrinsic and extrinsic semiconductors?

1–5 THE *PN* JUNCTION

When you take a block of silicon and dope part of it with a trivalent impurity and the other part with a pentavalent impurity, a boundary called the *pn* junction is formed between the resulting *p*-type and *n*-type portions. The *pn* junction is the basis for diodes, certain transistors, solar cells, and other devices, as you will learn later.

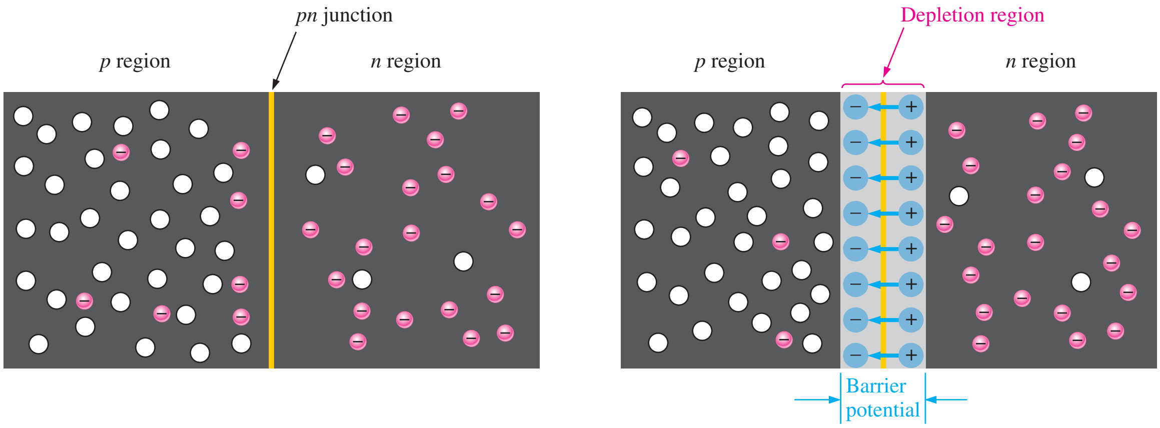
After completing this section, you should be able to

- ❑ **Describe how a *pn* junction is formed**
  - ◆ Discuss diffusion across a *pn* junction
- ❑ Explain the formation of the depletion region
  - ◆ Define *barrier potential* and discuss its significance ◆ State the values of barrier potential in silicon and germanium
- ❑ Discuss energy diagrams
  - ◆ Define *energy hill*

A *p*-type material consists of silicon atoms and trivalent impurity atoms such as boron. The boron atom adds a hole when it bonds with the silicon atoms. However, since the number of protons and the number of electrons are equal throughout the material, there is no net charge in the material and so it is neutral.

An *n*-type silicon material consists of silicon atoms and pentavalent impurity atoms such as antimony. As you have seen, an impurity atom releases an electron when it bonds with four silicon atoms. Since there is still an equal number of protons and electrons (including the free electrons) throughout the material, there is no net charge in the material and so it is neutral.

If a piece of intrinsic silicon is doped so that part is *n*-type and the other part is *p*-type, a ***pn* junction** forms at the boundary between the two regions and a diode is created, as indicated in Figure 1–19(a). The *p* region has many holes (majority carriers) from the impurity atoms and only a few thermally generated free electrons (minority carriers). The *n* region has many free electrons (majority carriers) from the impurity atoms and only a few thermally generated holes (minority carriers).



(a) The basic silicon structure at the instant of junction formation showing only the majority and minority carriers. Free electrons in the *n* region near the *pn* junction begin to diffuse across the junction and fall into holes near the junction in the *p* region.

(b) For every electron that diffuses across the junction and combines with a hole, a positive charge is left in the *n* region and a negative charge is created in the *p* region, forming a barrier potential. This action continues until the voltage of the barrier repels further diffusion. The blue arrows between the positive and negative charges in the depletion region represent the electric field.

▲ **FIGURE 1–19**

Formation of the depletion region. The width of the depletion region is exaggerated for illustration purposes.

Formation of the Depletion Region

The free electrons in the *n* region are randomly drifting in all directions. At the instant of the *pn* junction formation, the free electrons near the junction in the *n* region begin to diffuse across the junction into the *p* region where they combine with holes near the junction, as shown in Figure 1–19(b).

Before the *pn* junction is formed, recall that there are as many electrons as protons in the *n*-type material, making the material neutral in terms of net charge. The same is true for the *p*-type material.

When the *pn* junction is formed, the *n* region loses free electrons as they diffuse across the junction. This creates a layer of positive charges (pentavalent ions) near the junction. As the electrons move across the junction, the *p* region loses holes as the electrons and holes combine. This creates a layer of negative charges (trivalent ions) near the junction. These two layers of positive and negative charges form the **depletion region,** as shown in Figure 1–19(b). The term *depletion* refers to the fact that the region near the *pn* junction is depleted of charge carriers (electrons and holes) due to diffusion across the junction. Keep in mind that the depletion region is formed very quickly and is very thin compared to the *n* region and *p* region.

After the initial surge of free electrons across the *pn* junction, the depletion region has expanded to a point where equilibrium is established and there is no further diffusion of

HISTORY NOTE

After the invention of the light bulb, Edison continued to experiment and in 1883 found that he could detect electrons flowing through the vacuum from the lighted filament to a metal plate mounted inside the bulb. This discovery became known as the *Edison effect.*

An English physicist, John Fleming, took up where Edison left off and found that the Edison effect could also be used to detect radio waves and convert them to electrical signals. He went on to develop a two-element vacuum tube called the *Fleming valve,* later known as the *diode.* Modern *pn* junction devices are an outgrowth of this.

electrons across the junction. This occurs as follows. As electrons continue to diffuse across the junction, more and more positive and negative charges are created near the junction as the depletion region is formed. A point is reached where the total negative charge in the depletion region repels any further diffusion of electrons (negatively charged particles) into the *p* region (like charges repel) and the diffusion stops. In other words, the depletion region acts as a barrier to the further movement of electrons across the junction.

HISTORY NOTE

Russell Ohl, working at Bell Labs in 1940, stumbled on the semiconductor *pn* junction. Ohl was working with a silicon sample that had an accidental crack down its middle. He was using an ohmmeter to test the electrical resistance of the sample when he noted that when the sample was exposed to light, the current that flowed between the two sides of the crack made a significant jump. This discovery was fundamental to the work of the team that invented the transistor in 1947.

Barrier Potential Any time there is a positive charge and a negative charge near each other, there is a force acting on the charges as described by Coulomb's law. In the depletion region there are many positive charges and many negative charges on opposite sides of the *pn* junction. The forces between the opposite charges form an *electric field,* as illustrated in Figure 1–19(b) by the blue arrows between the positive charges and the negative charges. This electric field is a barrier to the free electrons in the *n* region, and energy must be expended to move an electron through the electric field. That is, external energy must be applied to get the electrons to move across the barrier of the electric field in the depletion region.

The potential difference of the electric field across the depletion region is the amount of voltage required to move electrons through the electric field. This potential difference is called the **barrier potential** and is expressed in volts. Stated another way, a certain amount of voltage equal to the barrier potential and with the proper polarity must be applied across a *pn* junction before electrons will begin to flow across the junction. You will learn more about this when we discuss *biasing* in Chapter 2.

The barrier potential of a *pn* junction depends on several factors, including the type of semiconductive material, the amount of doping, and the temperature. The typical barrier potential is approximately 0.7 V for silicon and 0.3 V for germanium at 25°C. Because germanium devices are not widely used, silicon will be used throughout the rest of the book.

Energy Diagrams of the *PN* Junction and Depletion Region

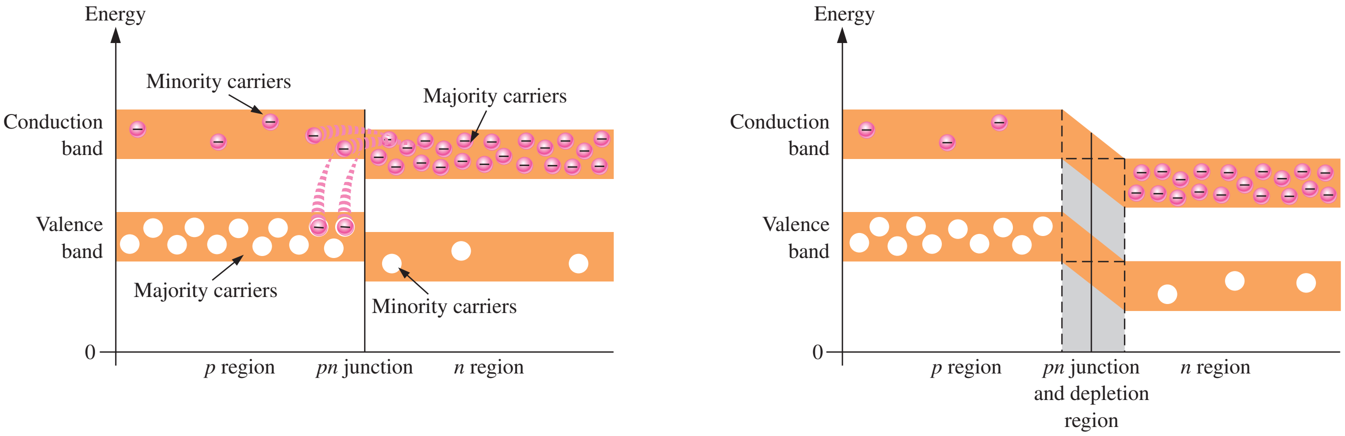
The valence and conduction bands in an *n*-type material are at slightly lower energy levels than the valence and conduction bands in a *p*-type material. Recall that *p*-type material has trivalent impurities and *n*-type material has pentavalent impurities. The trivalent impurities exert lower forces on the outer-shell electrons than the pentavalent impurities. The lower forces in *p*-type materials mean that the electron orbits are slightly larger and hence have greater energy than the electron orbits in the *n*-type materials.

An energy diagram for a *pn* junction at the instant of formation is shown in Figure 1–20(a). As you can see, the valence and conduction bands in the *n* region are at lower energy levels than those in the *p* region, but there is a significant amount of overlapping.

The free electrons in the *n* region that occupy the upper part of the conduction band in terms of their energy can easily diffuse across the junction (they do not have to gain additional energy) and temporarily become free electrons in the lower part of the *p*-region conduction band. After crossing the junction, the electrons quickly lose energy and fall into the holes in the *p*-region valence band as indicated in Figure 1-20(a).

As the diffusion continues, the depletion region begins to form and the energy level of the *n*-region conduction band decreases. The decrease in the energy level of the conduction band in the *n* region is due to the loss of the higher-energy electrons that have diffused across the junction to the *p* region. Soon, there are no electrons left in the *n*-region conduction band with enough energy to get across the junction to the *p*-region conduction band, as indicated by the alignment of the top of the *n*-region conduction band and the bottom of the *p*-region conduction band in Figure 1–20(b). At this point, the junction is at equilibrium; and the depletion region is complete because diffusion has ceased. There is an energy gradiant across the depletion region which acts as an "energy hill" that an *n*-region electron must climb to get to the *p* region.

Notice that as the energy level of the *n*-region conduction band has shifted downward, the energy level of the valence band has also shifted downward. It still takes the same amount of energy for a valence electron to become a free electron. In other words, the energy gap between the valence band and the conduction band remains the same.



(a) At the instant of junction formation

(b) At equilibrium

▲ **FIGURE 1–20**

Energy diagrams illustrating the formation of the *pn* junction and depletion region.

SECTION 1–5 CHECKUP

1. What is a *pn* junction?
2. Explain diffusion.
3. Describe the depletion region.
4. Explain what the barrier potential is and how it is created.
5. What is the typical value of the barrier potential for a silicon diode?
6. What is the typical value of the barrier potential for a germanium diode?

SUMMARY

Section 1–1

- According to the classical Bohr model, the atom is viewed as having a planetary-type structure with electrons orbiting at various distances around the central nucleus.
- According to the quantum model, electrons do not exist in precise circular orbits as particles as in the Bohr model. The electrons can be waves or particles and precise location at any time is uncertain.
- The nucleus of an atom consists of protons and neutrons. The protons have a positive charge and the neutrons are uncharged. The number of protons is the atomic number of the atom.
- Electrons have a negative charge and orbit around the nucleus at distances that depend on their energy level. An atom has discrete bands of energy called *shells* in which the electrons orbit. Atomic structure allows a certain maximum number of electrons in each shell. In their natural state, all atoms are neutral because they have an equal number of protons and electrons.
- The outermost shell or band of an atom is called the *valence band,* and electrons that orbit in this band are called *valence electrons.* These electrons have the highest energy of all those in the atom. If a valence electron acquires enough energy from an outside source such as heat, it can jump out of the valence band and break away from its atom.

Section 1–2

- Insulating materials have very few free electrons and do not conduct current at all under normal circumstances.
- Materials that are conductors have a large number of free electrons and conduct current very well.
- Semiconductive materials fall in between conductors and insulators in their ability to conduct current.
- Semiconductor atoms have four valence electrons. Silicon is the most widely used semiconductive material.

- Semiconductor atoms bond together in a symmetrical pattern to form a solid material called a *crystal.* The bonds that hold a crystal together are called *covalent bonds.*

Section 1–3

- The valence electrons that manage to escape from their parent atom are called *conduction electrons* or *free electrons.* They have more energy than the electrons in the valence band and are free to drift throughout the material.
- When an electron breaks away to become free, it leaves a hole in the valence band creating what is called an *electron-hole pair.* These electron-hole pairs are thermally produced because the electron has acquired enough energy from external heat to break away from its atom.
- A free electron will eventually lose energy and fall back into a hole. This is called *recombination.* Electron-hole pairs are continuously being thermally generated so there are always free electrons in the material.
- When a voltage is applied across the semiconductor, the thermally produced free electrons move toward the positive end and form the current. This is one type of current and is called electron current.
- Another type of current is the hole current. This occurs as valence electrons move from hole to hole creating, in effect, a movement of holes in the opposite direction.

Section 1–4

- An *n*-type semiconductive material is created by adding impurity atoms that have five valence electrons. These impurities are *pentavalent atoms.* A *p*-type semiconductor is created by adding impurity atoms with only three valence electrons. These impurities are *trivalent atoms.*
- The process of adding pentavalent or trivalent impurities to a semiconductor is called *doping.*
- The majority carriers in an *n*-type semiconductor are free electrons acquired by the doping process, and the minority carriers are holes produced by thermally generated electron-hole pairs. The majority carriers in a *p*-type semiconductor are holes acquired by the doping process, and the minority carriers are free electrons produced by thermally generated electron-hole pairs.

Section 1–5

- A *pn* junction is formed when part of a material is doped *n*-type and part of it is doped *p*-type. A depletion region forms starting at the junction that is devoid of any majority carriers. The depletion region is formed by ionization.
- The barrier potential is typically 0.7 V for a silicon diode and 0.3 V for germanium.

KEY TERMS

Key terms and other bold terms are defined in the end-of-book glossary.

Atom The smallest particle of an element that possesses the unique characteristics of that element.

Barrier potential The amount of energy required to produce full conduction across the *pn* junction in forward bias.

Conductor A material that easily conducts electrical current.

Crystal A solid material in which the atoms are arranged in a symmetrical pattern.

Doping The process of imparting impurities to an intrinsic semiconductive material in order to control its conduction characteristics.

Electron The basic particle of negative electrical charge.

Free electron An electron that has acquired enough energy to break away from the valence band of the parent atom; also called a *conduction electron.*

Hole The absence of an electron in the valence band of an atom.

Insulator A material that does not normally conduct current.

Ionization The removal or addition of an electron from or to a neutral atom so that the resulting atom (called an ion) has a net positive or negative charge.

Orbital Subshell in the quantum model of an atom.

***PN* junction** The boundary between two different types of semiconductive materials.

Proton The basic particle of positive charge.

Semiconductor A material that lies between conductors and insulators in its conductive properties. Silicon, germanium, and carbon are examples.

Shell An energy band in which electrons orbit the nucleus of an atom.

Silicon A semiconductive material.

Valence Related to the outer shell of an atom.

KEY FORMULA

1–1 $N_e = 2n^2$ Maximum number of electrons in any shell

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. An atom is the smallest particle in an element.
2. An electron is a negatively charged particle.
3. An atom is made up of electrons, protons, and neutrons.
4. Electrons are part of the nucleus of an atom.
5. Valence electrons exist in the outer shell of an atom.
6. Crystals are formed by the bonding of atoms.
7. Silicon is a conductive material.
8. Silicon doped with *p* and *n* impurities has one *pn* junction.
9. The *p* and *n* regions are formed by a process called *ionization.*

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 1–1

1. Every known element has
   (a) the same type of atoms **(b)** the same number of atoms
   (c) a unique type of atom **(d)** several different types of atoms
2. An atom consists of
   (a) one nucleus and only one electron **(b)** one nucleus and one or more electrons
   (c) protons, electrons, and neutrons **(d)** answers (b) and (c)
3. The nucleus of an atom is made up of
   (a) protons and neutrons **(b)** electrons
   (c) electrons and protons **(d)** electrons and neutrons
4. Valence electrons are
   (a) in the closest orbit to the nucleus **(b)** in the most distant orbit from the nucleus
   (c) in various orbits around the nucleus **(d)** not associated with a particular atom
5. A positive ion is formed when
   (a) a valence electron breaks away from the atom
   (b) there are more holes than electrons in the outer orbit
   (c) two atoms bond together
   (d) an atom gains an extra valence electron

Section 1–2

6. The most widely used semiconductive material in electronic devices is
   (a) germanium **(b)** carbon **(c)** copper **(d)** silicon
7. The difference between an insulator and a semiconductor is
   (a) a wider energy gap between the valence band and the conduction band
   (b) the number of free electrons
   (c) the atomic structure
   (d) answers (a), (b), and (c)
8. The energy band in which free electrons exist is the
   (a) first band **(b)** second band **(c)** conduction band **(d)** valence band

9. In a semiconductor crystal, the atoms are held together by
   (a) the interaction of valence electrons **(b)** forces of attraction
   (c) covalent bonds **(d)** answers (a), (b), and (c)
10. The atomic number of silicon is
    (a) 8 **(b)** 2 **(c)** 4 **(d)** 14
11. The atomic number of germanium is
    (a) 8 **(b)** 2 **(c)** 4 **(d)** 32
12. The valence shell in a silicon atom has the number designation of
    (a) 0 **(b)** 1 **(c)** 2 **(d)** 3
13. Each atom in a silicon crystal has
    (a) four valence electrons
    (b) four conduction electrons
    (c) eight valence electrons, four of its own and four shared
    (d) no valence electrons because all are shared with other atoms

Section 1–3

14. Electron-hole pairs are produced by
    (a) recombination **(b)** thermal energy **(c)** ionization **(d)** doping
15. Recombination is when
    (a) an electron falls into a hole
    (b) a positive and a negative ion bond together
    (c) a valence electron becomes a conduction electron
    (d) a crystal is formed
16. The current in a semiconductor is produced by
    (a) electrons only **(b)** holes only **(c)** negative ions **(d)** both electrons and holes

Section 1–4

17. In an intrinsic semiconductor,
    (a) there are no free electrons
    (b) the free electrons are thermally produced
    (c) there are only holes
    (d) there are as many electrons as there are holes
    (e) answers (b) and (d)
18. The process of adding an impurity to an intrinsic semiconductor is called
    (a) doping **(b)** recombination **(c)** atomic modification **(d)** ionization
19. A trivalent impurity is added to silicon to create
    (a) germanium **(b)** a *p*-type semiconductor
    (c) an *n*-type semiconductor **(d)** a depletion region
20. The purpose of a pentavalent impurity is to
    (a) reduce the conductivity of silicon **(b)** increase the number of holes
    (c) increase the number of free electrons **(d)** create minority carriers
21. The majority carriers in an *n*-type semiconductor are
    (a) holes **(b)** valence electrons **(c)** conduction electrons **(d)** protons
22. Holes in an *n*-type semiconductor are
    (a) minority carriers that are thermally produced
    (b) minority carriers that are produced by doping
    (c) majority carriers that are thermally produced
    (d) majority carriers that are produced by doping

Section 1–5

23. A *pn* junction is formed by
    (a) the recombination of electrons and holes
    (b) ionization

(c) the boundary of a *p*-type and an *n*-type material
(d) the collision of a proton and a neutron

24. The depletion region is created by

(a) ionization **(b)** diffusion **(c)** recombination **(d)** answers (a), (b), and (c)

25. The depletion region consists of

(a) nothing but minority carriers **(b)** positive and negative ions
(c) no majority carriers **(d)** answers (b) and (c)

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 1–1 The Atom

1. If the atomic number of a neutral atom is 6, how many electrons does the atom have? How many protons?

2. What is the maximum number of electrons that can exist in the 3rd shell of an atom?

Section 1–2 Materials Used in Electronics

3. For each of the energy diagrams in Figure 1–21, determine the class of material based on relative comparisons.

4. A certain atom has four valence electrons. What type of atom is it?

5. In a silicon crystal, how many covalent bonds does a single atom form?

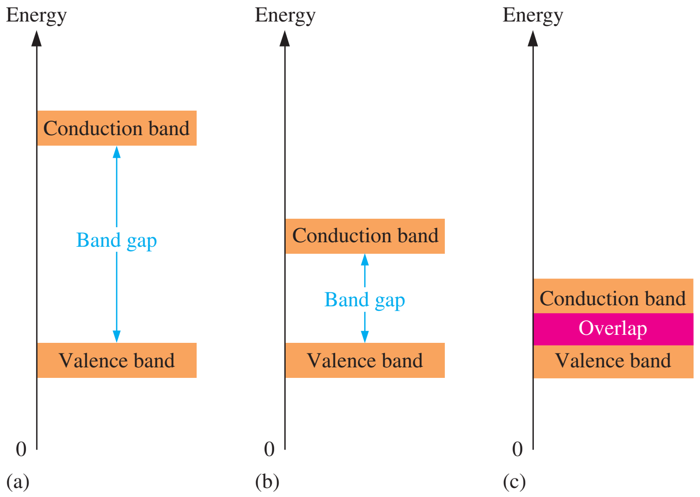


FIGURE 1–21

Section 1–3 Current in Semiconductors

6. What happens when heat is added to silicon?

7. Name the two energy bands at which current is produced in silicon.

Section 1–4 *N*-Type and *P*-Type Semiconductors

8. Describe the process of doping and explain how it alters the atomic structure of silicon.

9. What is antimony? What is boron?

Section 1–5 The *PN* Junction

10. How is the electric field across the *pn* junction created?

11. Because of its barrier potential, can a diode be used as a voltage source? Explain.

GreenTech Application 1: *Solar Power*

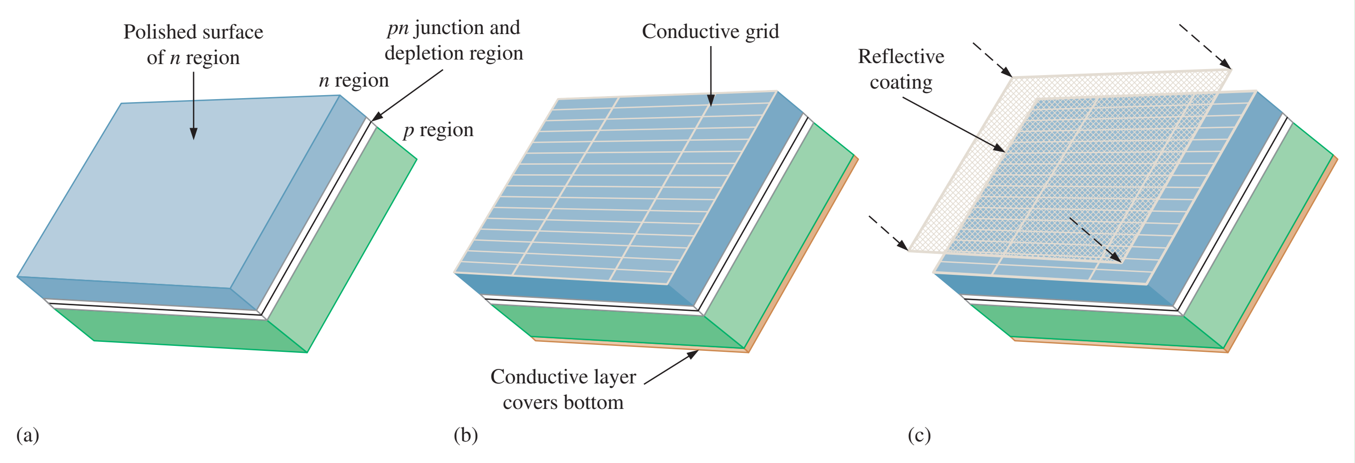
Photovoltaic (PV) Cell Structure and Operation

The key feature of a PV (solar) cell is the *pn* junction that was covered in Chapter 1. The **photovoltaic effect** is the basic physical process by which a solar cell converts sunlight into electricity. Sunlight contains photons or "packets" of energy sufficient to create electron-hole pairs in the *n* and *p* regions. Electrons accumulate in the *n*-region and holes accumulate in the *p* region, producing a potential difference (voltage) across the cell. When an external load is connected, the electrons flow through the semiconductor material and provide current to the external load.

The Solar Cell Structure Although there are other types of solar cells and continuing research promises new developments in the future, the crystalline silicon solar cell is by far the most widely used. A silicon solar cell consists of a thin layer or wafer of silicon that has been doped to create a *pn* junction. The depth and distribution of impurity atoms can be controlled very precisely during the doping process. The most commonly used process for creating a silicon ingot, from which a silicon wafer is cut, is called the *Czochralski method.* In this process, a seed crystal of silicon is dipped into melted polycrystalline silicon. As the seed crystal is withdrawn and rotated, a cylindrical ingot of silicon is formed.

Thin circular shaped-wafers are sliced from an ingot of ultra-pure silicon and then are polished and trimmed to an octagonal, hexagonal, or rectangular shape for maximum coverage when fitted into an array. The silicon wafer is doped so that the *n* region is much thinner than the *p* region to permit light penetration, as shown in Figure GA1–1(a).

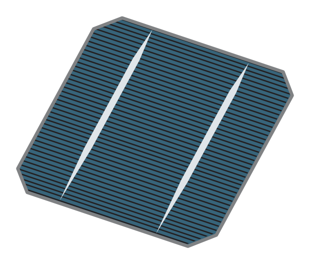
A grid-work of very thin conductive contact strips are deposited on top of the wafer by methods such as photoresist or silk-screen, as shown in part (b). The contact grid must maximize the surface area of the silicon wafer that be exposed to the sunlight in order to collect as much light energy as possible.


Polished surface of *n* region
pn junction and depletion region
n region
p region
Conductive grid
Reflective coating
Conductive layer covers bottom
(a)
(b)
(c)

▲ FIGURE GA1–1

Basic construction of a PV solar cell.

The conductive grid across the top of the cell is necessary so that the electrons have a shorter distance to travel through the silicon when an external load is connected. The farther electrons travel through the silicon material, the greater the energy loss due to resistance. A solid contact covering all of the bottom of the wafer is then added, as indicated in the figure. Thickness of the solar cell compared to the surface area is greatly exaggerated for purposes of illustration.



▲ **FIGURE GA1–2**

A complete PV solar cell.

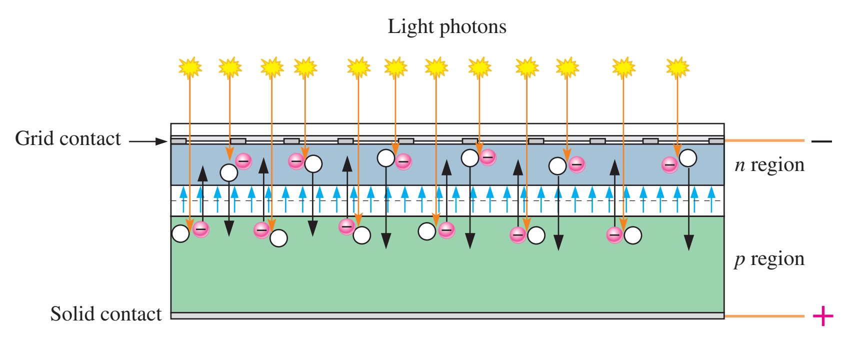
After the contacts are incorporated, an antireflective coating is placed on top the contact grid and *n* region, as shown in Figure GA1–1(c). This allows the solar cell to absorb as much of the sun's energy as possible by reducing the amount of light energy reflected away from the surface of the cell. Finally, a glass or transparent plastic layer is attached to the top of the cell with transparent adhesive to protect it from the weather. Figure GA1–2 shows a completed solar cell.

Operation of a Solar Cell As indicated before, sunlight is composed of photons, or "packets" of energy. The sun produces an astounding amount of energy. The small fraction of the sun's total energy that reaches the earth is enough to meet all of our power needs many times over. There is sufficient solar energy striking the earth each hour to meet worldwide demands for an entire year.

The *n*-type layer is very thin compared to the *p* region to allow light penetration into the *p* region. The thickness of the entire cell is actually about the thickness of an eggshell. When a photon penetrates either the *n* region or the *p*-type region and strikes a silicon atom near the *pn* junction with sufficient energy to knock an electron out of the valence band, the electron becomes a free electron and leaves a hole in the valence band, creating an *electron-hole pair.* The amount of energy required to free an electron from the valence band of a silicon atom is called the band-gap energy and is 1.12 eV (electron volts). In the *p* region, the free electron is swept across the depletion region by the electric field into the *n* region. In the *n* region, the hole is swept across the depletion region by the electric field into the *p* region. Electrons accumulate in the *n* region, creating a negative charge; and holes accumulate in the *p* region, creating a positive charge. A voltage is developed between the *n* region and *p* region contacts, as shown in Figure GA1–3.

▶ **FIGURE GA1–3**

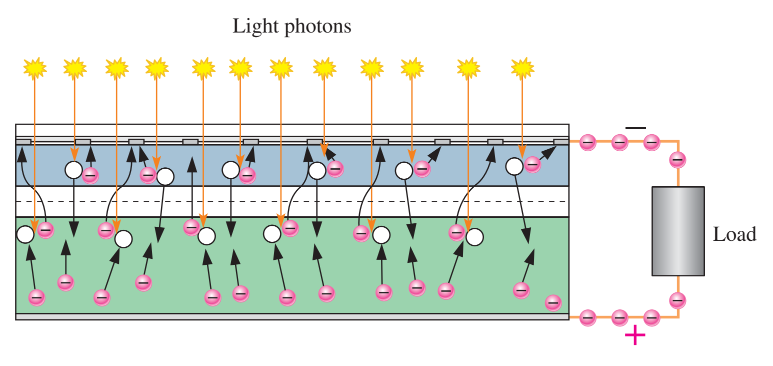
Basic operation of a solar cell with incident sunlight.



When a load is connected to a solar cell via the top and bottom contacts, the free electrons flow out of the *n* region to the grid contacts on the top surface, through the negative contact, through the load and back into the positive contact on the bottom surface, and into the *p* region where they can recombine with holes. The sunlight energy continues to create new electron-hole pairs and the process goes on, as illustrated in Figure GA1–4.

▶ **FIGURE GA1–4**

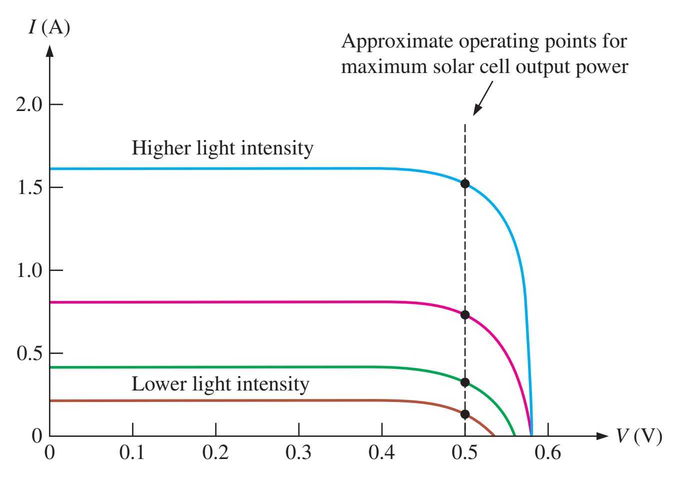
A solar cell producing voltage and current through a load under incident sunlight.



Solar Cell Characteristics

Solar cells are typically 100 cm^2 to 225 cm^2 in size. The usable voltage from silicon solar cells is approximately 0.5 V to 0.6 V. Terminal voltage is only slightly dependent on the intensity of light radiation, but the current increases with light intensity. For example, a 100 cm^2 silicon cell reaches a maximum current of approximately 2 A when radiated by 1000 W/m^2 of light.

Figure GA1–5 shows the *V-I* characteristic curves for a typical solar cell for various light intensities. Higher light intensity produces more current. The operating point for maximum power output for a given light intensity should be in the "knee" area of the curve, as indicated by the dashed line. The load on the solar cell controls this operating point ($R_L = V/I$).



◄ **FIGURE GA1–5**

V-I **characteristic for a typical single solar cell from increasing light intensities.**

In a solar power system, the cell is generally loaded by a charge controller or an inverter. A special method called *maximum power point tracking* will sense the operating point and adjust the load resistance to keep it in the knee region. For example, assume the solar cell is operating on the highest intensity curve (blue) shown in Figure GA1–5. For maximum power (dashed line), the voltage is 0.5 V and the current is 1.5 A. For this condition, the load is

$$R_L = \frac{V}{I} = \frac{0.5\text{ V}}{1.5\text{ A}} = 0.33\ \Omega$$

Now, if the light intensity falls to where the cell is operating on the red curve, the current is less and the load resistance will have to change to maintain maximum power output as follows:

$$R_L = \frac{V}{I} = \frac{0.5\text{ V}}{0.8\text{ A}} = 0.625\ \Omega$$

If the resistance did not change, the voltage output would drop to

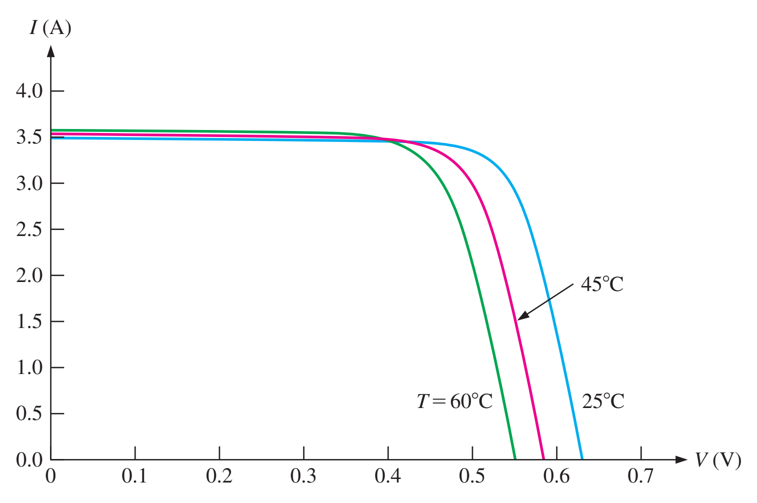
$$V = IR = (0.8\text{ A})(0.33\text{ W}) = 0.264\text{ V}$$

resulting in less than maximum power output for the red curve. Of course, the power will still be less on the red curve than on the blue curve because the current is less.

The output voltage and current of a solar cell is also temperature dependent. Notice in Figure GA1–6 that for a constant light intensity the output voltage decreases as the temperature increases but the current is affected only by a small amount.

FIGURE GA1–6

Effect of temperature on output voltage and current for a fixed light intensity in a solar cell.



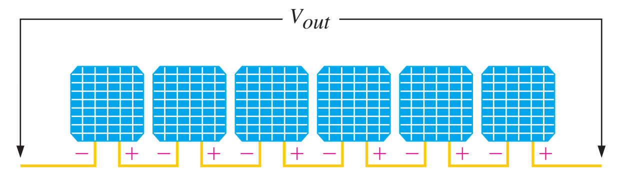
Solar Cell Panels

Currently, the problem is in harnessing solar energy in sufficient amounts and at a reasonable cost to meet our requirements. It takes approximately a square meter solar panel to produce 100 W in a sunny climate. Some energy can be harvested even if cloud cover exists, but no energy can be obtained during the night.

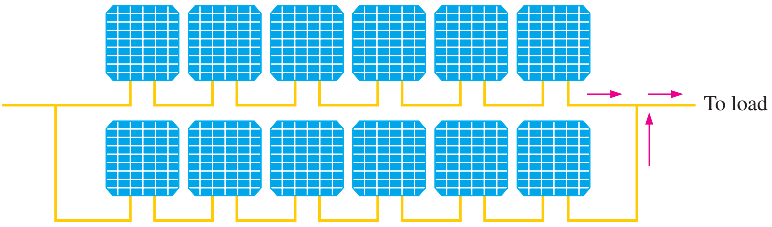
A single solar cell is impractical for most applications because it can produce only about 0.5 V to 0.6 V. To produce higher voltages, multiple solar cells are connected in series as shown in Figure GA1–7(a). For example, the six series cells will ideally produce 6(0.5 V) = 3 V. Since they are connected in series, the six cells will produce the same current as a single cell. For increased current capacity, series cells are connected in parallel, as shown in part (b). Assuming a cell can produce 2 A, the series-parallel arrangement of twelve cells will produce 4 A at 3 V. Multiple cells connected to produce a specified power output are called *solar panels* or *solar modules.*

FIGURE GA1–7

Solar cells connected together to create an array called a solar panel.



(a) Series connection increases



(b) Series-parallel connection increases current

Solar panels are generally available in 12 V, 24 V, 36 V, and 48 V versions. Higher output solar panels are also available for special applications. In actuality, a 12 V solar panel produces more than 12 V (15 V to 20 V) in order to charge a 12 V battery and compensate for voltage drops in the series connection and other losses. Ideally, a panel with 24 individual solar cells is required to produce an output of 12 V, assuming each cell produces 0.5 V. In practice, more than thirty cells are typically used in a 12 V panel. Manufacturers usually specify the output of a solar panel in terms of power at a certain solar radiation called the *peak sun irradiance* which is 1000 W/m^2. For example, a 12 V solar panel that has a rated voltage of 17 V and produces a current of 3.5 A to a load at peak sun condition has a specified output power of

$$P = VI = (17\text{ V})(3.5\text{ A}) = 59.5\text{ W}$$

Many solar panels can be interconnected to form large arrays for high power outputs, as illustrated in Figure GA1–8.

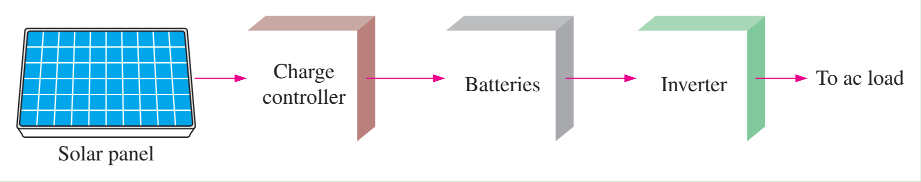
▲ FIGURE GA1–8

Large array of solar panels.

The Solar Power System

A basic solar power system that can supply power to ac loads generally consists of four components, as shown in the block diagram in Figure GA1-9. These components are the solar panel, the charge controller, the batteries, and the inverter. For supplying only dc loads, such as solar-powered instruments and dc lamps, the inverter is not needed. Some solar power systems do not include battery backup or the charge controller and are used to provide supplemental power only when the sun is shining.

Efficiency is an important characteristic of a solar power system. Energy loss due to voltage drops, the photovoltaic process, and other factors are inevitable, so minimizing losses is a critical consideration in solar power systems.



◀ FIGURE GA1–9

Basic solar power system with battery backup.

Solar Panel The solar panel collects energy from the sun and converts it to electrical energy through the photovoltaic process. Of course, the solar panel will not produce the specified power output all of the time. For example, if there is 4 hours of peak sun during a given day, a 60 W panel will produce $4 \times 60\text{ W} = 240\text{ Wh}$ of energy. For the hours that the sun is not peak, the output will depend on the percentage of peak sun and is less than the specified output. A system is typically designed taking into account the annual of average peak sun per day for a given geographical area.

Charge Controller A charge controller, also called a charge regulator, takes the output of the solar panel and ensures that the battery is charged efficiently and is not overcharged. Generally, the charge controller is rated based on the amount of current it can regulate. The operation of many solar charge controllers is based on the principle of *pulse-width modulation.* Also, some controllers include a charging method that maximizes charging, called maximum power point tracking. The charge controller and batteries in a solar power system will be examined in more detail in GreenTech Application 2.

Battery Deep-cycle batteries, such as lead-acid, are used in solar power systems because they can be charged and discharged hundreds or thousands of times. Recall that batteries are rated in ampere-hours (Ah), which specifies the current that can be supplied for certain number of hours. For example, a 400 Ah battery can supply 400 A for one hour, 4 A for 100 hours, or 10 A for 40 hours. Batteries can be connected in series to increase voltage or in parallel to increase amp-hrs.

Inverter The inverter changes DC voltage stored in the battery to the standard 120/240 Vac used in most common applications such as lighting, appliances, and motors. Basically, in an inverter the dc from the battery is electronically switched on and off and filtered to produce a sinusoidal ac output. The ac output is then applied to a step-up transformer to get 120 Vac. The inverter in a solar system will be covered in more detail in GreenTech Application 3.

QUESTIONS

Some questions may require research beyond the content of this coverage. Answers can be found at www.pearsonhighered.com/floyd.

1. What are the four elements of a solar power system?
2. How must solar cells be connected to increase output voltage?
3. What is the function of the charge controller?
4. What is the function of the inverter?
5. What range of solar panels in terms of output voltage and power are available?

The following websites are recommended for viewing solar cells in action. Many other websites are also available. Note that websites can occasionally be removed and are not guaranteed to be available.

http://www.youtube.com/watch?v=hdUdu5C8Tis&feature=related

http://www.youtube.com/watch?v=Caf1Jlz4X2l

http://www.youtube.com/watch?v=K76r41jaGJg&feature=related

http://www.youtube.com/watch?v=2mCTSV2f36A&feature=related

http://www.youtube.com/watch?v=PbPcmo3x1Ug&feature=related

2

DIODES AND APPLICATIONS

CHAPTER OUTLINE

2–1 Diode Operation
2–2 Voltage-Current (*V-I*) Characteristics of a Diode
2–3 Diode Models
2–4 Half-Wave Rectifiers
2–5 Full-Wave Rectifiers
2–6 Power Supply Filters and Regulators
2–7 Diode Limiters and Clampers
2–8 Voltage Multipliers
2–9 The Diode Datasheet
2–10 Troubleshooting
Application Activity
GreenTech Application 2: *Solar Power*

CHAPTER OBJECTIVES

- Use a diode in common applications
- Analyze the voltage-current (*V-I*) characteristic of a diode
- Explain how the three diode models differ
- Explain and analyze the operation of half-wave rectifiers
- Explain and analyze the operation of full-wave rectifiers
- Explain and analyze power supply filters and regulators
- Explain and analyze the operation of diode limiters and clampers
- Explain and analyze the operation of diode voltage multipliers
- Interpret and use diode datasheets
- Troubleshoot diodes and power supply circuits

KEY TERMS

- Diode
- Bias
- Forward bias
- Reverse bias
- *V-I* characteristic
- DC power supply
- Rectifier
- Filter
- Regulator
- Half-wave rectifier
- Peak inverse voltage (PIV)
- Full-wave rectifier
- Ripple voltage
- Line regulation
- Load regulation
- Limiter
- Clamper
- Troubleshooting

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In Chapter 1, you learned that many semiconductor devices are based on the *pn* junction. In this chapter, the operation and characteristics of the diode are covered. Also, three diode models representing three levels of approximation are presented and testing is discussed. The importance of the diode in electronic circuits cannot be overemphasized. Its ability to conduct current in one direction while blocking current in the other direction is essential to the operation of many types of circuits. One circuit in particular is the ac rectifier, which is covered in this chapter. Other important applications are circuits such as diode limiters, diode clampers, and diode voltage multipliers. A datasheet is discussed for specific diodes.

APPLICATION ACTIVITY PREVIEW

You have the responsibility for the final design and testing of a power supply circuit that your company plans to use in several of its products. You will apply your knowledge of diode circuits to the Application Activity at the end of the chapter.

2–1 DIODE OPERATION

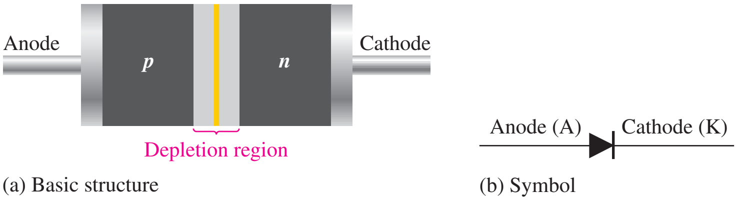
Similar to the solar cell in Chapter 1, a diode is a two-terminal semiconductor device formed by two doped regions of silicon separated by a *pn* junction. In this chapter, the most common category of diode, known as the general-purpose diode, is covered. Other names, such as rectifier diode or signal diode, depend on the particular type of application for which the diode was designed. You will learn how to use a voltage to cause the diode to conduct current in one direction and block it in the other direction. This process is called *biasing*.

After completing this section, you should be able to

- ❑ **Use a diode in common applications**
- ❑ Recognize the electrical symbol for a diode and several diode package configurations
- ❑ Apply forward bias to a diode
  ◆ Define *forward bias* and state the required conditions ◆ Discuss the effect of forward bias on the depletion region ◆ Define *barrier potential* and its effects during forward bias
- ❑ Reverse-bias a diode
  ◆ Define *reverse bias* and state the required conditions ◆ Discuss reverse current and reverse breakdown

The Diode

As mentioned, a **diode** is made from a small piece of semiconductor material, usually silicon, in which half is doped as a *p* region and half is doped as an *n* region with a *pn* junction and depletion region in between. The *p* region is called the **anode** and is connected to a conductive terminal. The *n* region is called the **cathode** and is connected to a second conductive terminal. The basic diode structure and schematic symbol are shown in Figure 2–1.



(a) Basic structure (b) Symbol

◀ FIGURE 2–1

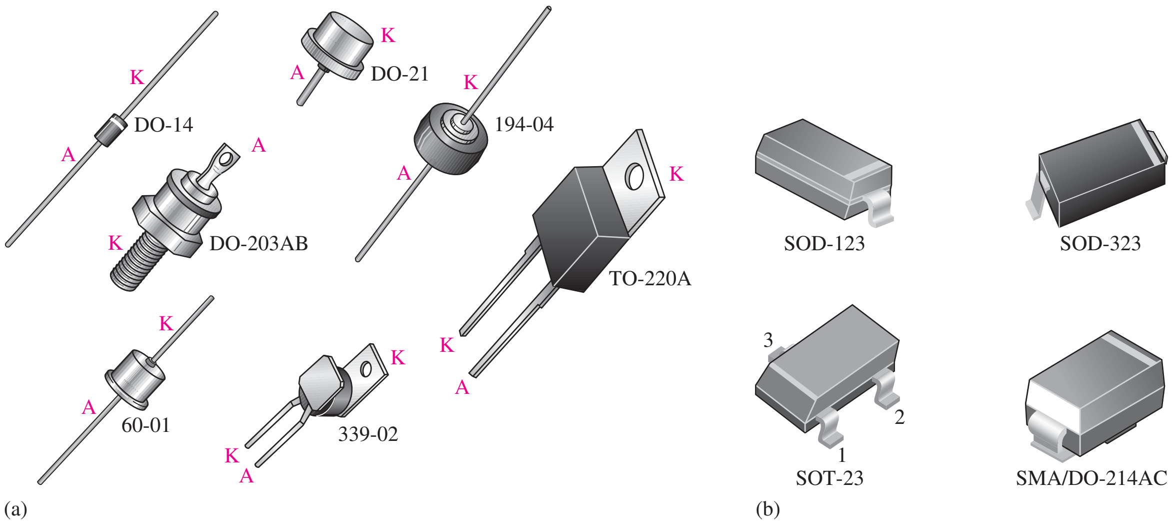
The diode.

GREENTECH NOTE

The diodes covered in this chapter are based on the *pn* junction just like the solar cell, also known as the photovoltaic cell or PV cell, that was introduced in Chapter 1. A solar cell is basically a diode with a different geometric construction than rectifier and signal diodes. The *p* and *n* regions in the solar cell are much thinner to allow light energy to activate the photovoltaic effect, and a solar cell's exposed surface is transparent.

Typical Diode Packages Several common physical configurations of through-hole mounted diodes are illustrated in Figure 2–2(a). The anode (A) and cathode (K) are indicated on a diode in several ways, depending on the type of package. The cathode is usually marked by a band, a tab, or some other feature. On those packages where one lead is connected to the case, the case is the cathode.

Surface-Mount Diode Packages Figure 2–2(b) shows typical diode packages for surface mounting on a printed circuit board. The SOD and SOT packages have gull-wing shaped leads. The SMA package has L-shaped leads that bend under the package. The SOD and SMA types have a band on one end to indicate the cathode. The SOT type is a three-terminal package in which there are either one or two diodes. In a single-diode SOT package, pin 1 is usually the anode and pin 3 is the cathode. In a dual-diode SOT package, pin 3 is the common terminal and can be either the anode or the cathode. Always check the datasheet for the particular diode to verify the pin configurations.



▲ FIGURE 2–2

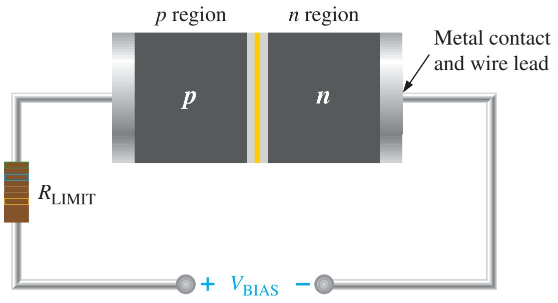
Typical diode packages with terminal identification. The letter K is used for cathode to avoid confusion with certain electrical quantities that are represented by *C*. Case type numbers are indicated for each diode.

Forward Bias

To **bias** a diode, you apply a dc voltage across it. **Forward bias** is the condition that allows current through the *pn* junction. Figure 2–3 shows a dc voltage source connected by conductive material (contacts and wire) across a diode in the direction to produce forward bias. This external bias voltage is designated as V_{BIAS}. The resistor limits the forward current to a value that will not damage the diode. Notice that the negative side of V_{BIAS} is connected to the *n* region of the diode and the positive side is connected to the *p* region. This is one requirement for forward bias. A second requirement is that the bias voltage, V_{BIAS}, must be greater than the **barrier potential**.

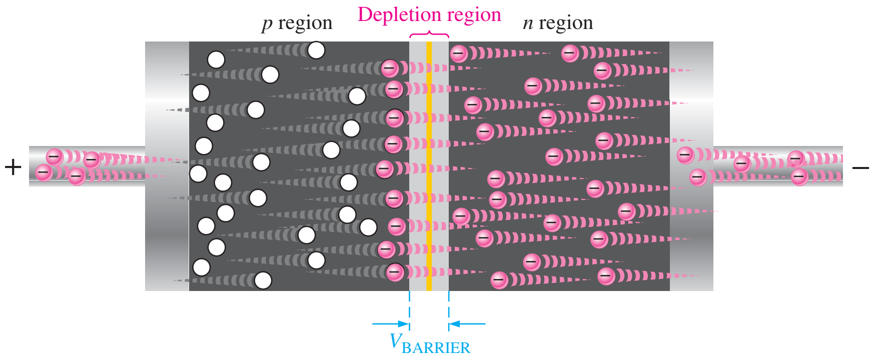
► FIGURE 2–3

A diode connected for forward bias.



A fundamental picture of what happens when a diode is forward-biased is shown in Figure 2–4. Because like charges repel, the negative side of the bias-voltage source “pushes” the free electrons, which are the majority carriers in the *n* region, toward the *pn* junction. This flow of free electrons is called *electron current.* The negative side of the source also provides a continuous flow of electrons through the external connection (conductor) and into the *n* region as shown.

The bias-voltage source imparts sufficient energy to the free electrons for them to overcome the barrier potential of the depletion region and move on through into the *p* region. Once in the *p* region, these conduction electrons have lost enough energy to immediately combine with holes in the valence band.



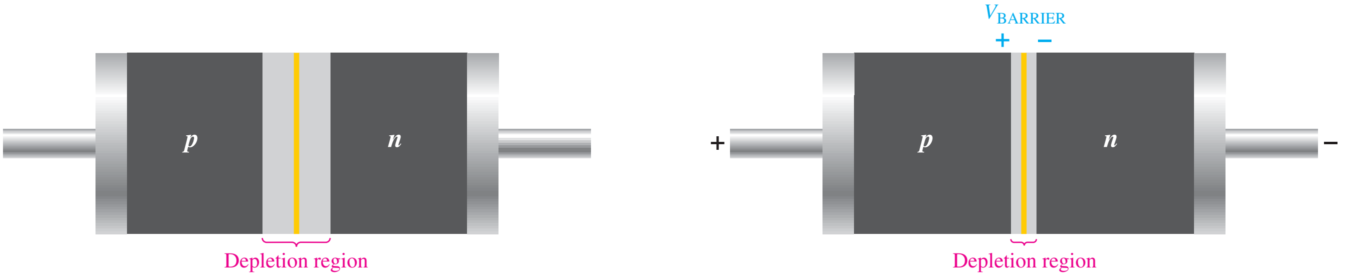
◀ FIGURE 2–4

A forward-biased diode showing the flow of majority carriers and the voltage due to the barrier potential across the depletion region.

Now, the electrons are in the valence band in the *p* region, simply because they have lost too much energy overcoming the barrier potential to remain in the conduction band. Since unlike charges attract, the positive side of the bias-voltage source attracts the valence electrons toward the left end of the *p* region. The holes in the *p* region provide the medium or "pathway" for these valence electrons to move through the *p* region. The valence electrons move from one hole to the next toward the left. The holes, which are the majority carriers in the *p* region, effectively (not actually) move to the right toward the junction, as you can see in Figure 2–4. This *effective* flow of holes is the hole current. You can also view the hole current as being created by the flow of valence electrons through the *p* region, with the holes providing the only means for these electrons to flow.

As the electrons flow out of the *p* region through the external connection (conductor) and to the positive side of the bias-voltage source, they leave holes behind in the *p* region; at the same time, these electrons become conduction electrons in the metal conductor. Recall that the conduction band in a conductor overlaps the valence band so that it takes much less energy for an electron to be a free electron in a conductor than in a semiconductor and that metallic conductors do not have holes in their structure. There is a continuous availability of holes effectively moving toward the *pn* junction to combine with the continuous stream of electrons as they come across the junction into the *p* region.

The Effect of Forward Bias on the Depletion Region As more electrons flow into the depletion region, the number of positive ions is reduced. As more holes effectively flow into the depletion region on the other side of the *pn* junction, the number of negative ions is reduced. This reduction in positive and negative ions during forward bias causes the depletion region to narrow, as indicated in Figure 2–5.



(a) At equilibrium (no bias)

(b) Forward bias narrows the depletion region and produces a voltage drop across the *pn* junction equal to the barrier potential.

▲ FIGURE 2–5

The depletion region narrows and a voltage drop is produced across the *pn* junction when the diode is forward-biased.

The Effect of the Barrier Potential During Forward Bias Recall that the electric field between the positive and negative ions in the depletion region on either side of the junction creates an "energy hill" that prevents free electrons from diffusing across the junction at equilibrium. This is known as the *barrier potential.*

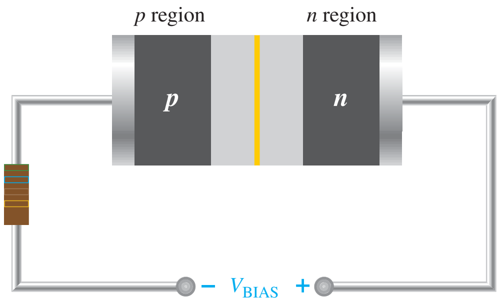
When forward bias is applied, the free electrons are provided with enough energy from the bias-voltage source to overcome the barrier potential and effectively "climb the energy hill" and cross the depletion region. The energy that the electrons require in order to pass through the depletion region is equal to the barrier potential. In other words, the electrons give up an amount of energy equivalent to the barrier potential when they cross the depletion region. This energy loss results in a voltage drop across the *pn* junction equal to the barrier potential (0.7 V), as indicated in Figure 2–5(b). An additional small voltage drop occurs across the *p* and *n* regions due to the internal resistance of the material. For doped semiconductive material, this resistance, called the **dynamic resistance,** is very small and can usually be neglected. This is discussed in more detail in Section 2–2.

Reverse Bias

Reverse bias is the condition that essentially prevents current through the diode. Figure 2–6 shows a dc voltage source connected across a diode in the direction to produce reverse bias. This external bias voltage is designated as V_{BIAS} just as it was for forward bias. Notice that the positive side of V_{BIAS} is connected to the *n* region of the diode and the negative side is connected to the *p* region. Also note that the depletion region is shown much wider than in forward bias or equilibrium.

▶ FIGURE 2–6

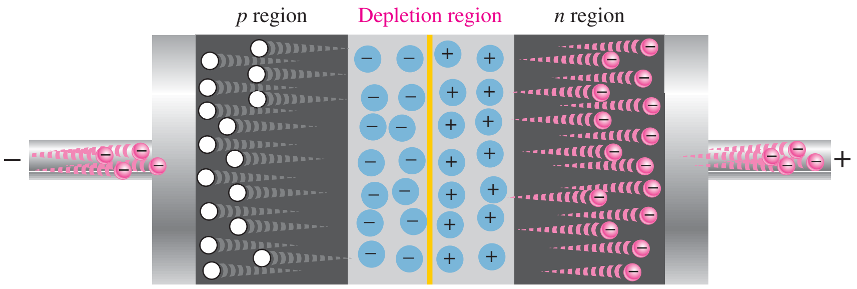
A diode connected for reverse bias. A limiting resistor is shown although it is not important in reverse bias because there is essentially no current.



An illustration of what happens when a diode is reverse-biased is shown in Figure 2–7. Because unlike charges attract, the positive side of the bias-voltage source "pulls" the free electrons, which are the majority carriers in the *n* region, away from the *pn* junction. As the electrons flow toward the positive side of the voltage source, additional positive ions are created. This results in a widening of the depletion region and a depletion of majority carriers.

▶ FIGURE 2–7

The diode during the short transition time immediately after reverse-bias voltage is applied.

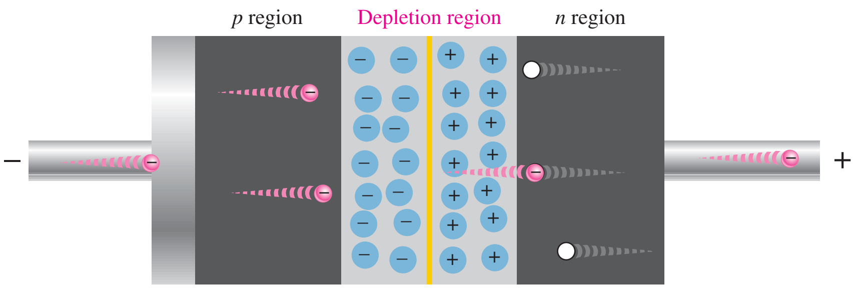


In the *p* region, electrons from the negative side of the voltage source enter as valence electrons and move from hole to hole toward the depletion region where they create additional negative ions. This results in a widening of the depletion region and a depletion of majority carriers. The flow of valence electrons can be viewed as holes being "pulled" toward the positive side.

The initial flow of charge carriers is transitional and lasts for only a very short time after the reverse-bias voltage is applied. As the depletion region widens, the availability of majority carriers decreases. As more of the *n* and *p* regions become depleted of majority carriers, the electric field between the positive and negative ions increases in strength until the potential across the depletion region equals the bias voltage, V_{BIAS}. At this point, the transition current essentially ceases except for a very small reverse current that can usually be neglected.

Reverse Current The extremely small current that exists in reverse bias after the transition current dies out is caused by the minority carriers in the *n* and *p* regions that are produced by thermally generated electron-hole pairs. The small number of free minority electrons in the *p* region are "pushed" toward the *pn* junction by the negative bias voltage. When these electrons reach the wide depletion region, they "fall down the energy hill" and combine with the minority holes in the *n* region as valence electrons and flow toward the positive bias voltage, creating a small hole current.

The conduction band in the *p* region is at a higher energy level than the conduction band in the *n* region. Therefore, the minority electrons easily pass through the depletion region because they require no additional energy. Reverse current is illustrated in Figure 2–8.



◀ **FIGURE 2–8**

The extremely small reverse current in a reverse-biased diode is due to the minority carriers from thermally generated electron-hole pairs.

Reverse Breakdown Normally, the reverse current is so small that it can be neglected. However, if the external reverse-bias voltage is increased to a value called the *breakdown voltage,* the reverse current will drastically increase.

This is what happens. The high reverse-bias voltage imparts energy to the free minority electrons so that as they speed through the *p* region, they collide with atoms with enough energy to knock valence electrons out of orbit and into the conduction band. The newly created conduction electrons are also high in energy and repeat the process. If one electron knocks only two others out of their valence orbit during its travel through the *p* region, the numbers quickly multiply. As these high-energy electrons go through the depletion region, they have enough energy to go through the *n* region as conduction electrons, rather than combining with holes.

The multiplication of conduction electrons just discussed is known as the **avalanche effect,** and reverse current can increase dramatically if steps are not taken to limit the current. When the reverse current is not limited, the resulting heating will permanently damage the diode. Most diodes are not operated in reverse breakdown, but if the current is limited (by adding a series-limiting resistor for example), there is no permanent damage to the diode.

SECTION 2–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. Describe forward bias of a diode.
2. Explain how to forward-bias a diode.
3. Describe reverse bias of a diode.
4. Explain how to reverse-bias a diode.
5. Compare the depletion regions in forward bias and reverse bias.
6. Which bias condition produces majority carrier current?
7. How is reverse current in a diode produced?
8. When does reverse breakdown occur in a diode?
9. Define *avalanche effect* as applied to diodes.

2–2 VOLTAGE-CURRENT CHARACTERISTIC OF A DIODE

As you have learned, forward bias produces current through a diode and reverse bias essentially prevents current, except for a negligible reverse current. Reverse bias prevents current as long as the reverse-bias voltage does not equal or exceed the breakdown voltage of the junction. In this section, we will examine the relationship between the voltage and the current in a diode on a graphical basis.

After completing this section, you should be able to

- ❑ **Analyze the voltage-current (*V-I*) characteristic of a diode**
- ❑ Explain the *V-I* characteristic for forward bias
  - ◆ Graph the *V-I* curve for forward bias ◆ Describe how the barrier potential affects the *V-I* curve ◆ Define *dynamic resistance*
- ❑ Explain the *V-I* characteristic for reverse bias
  - ◆ Graph the *V-I* curve for reverse bias
- ❑ Discuss the complete *V-I* characteristic curve
  - ◆ Describe the effects of temperature on the diode characteristic

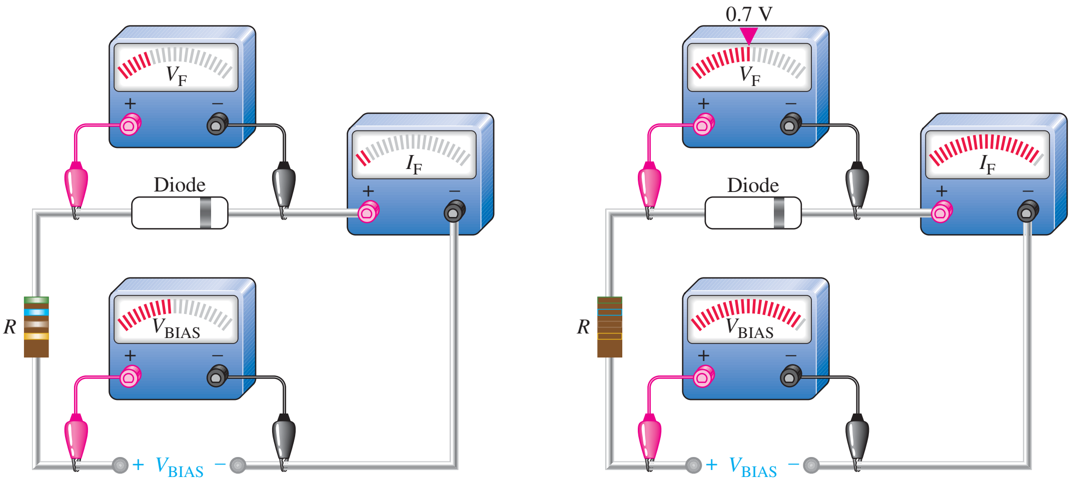
V-I Characteristic for Forward Bias

When a forward-bias voltage is applied across a diode, there is current. This current is called the *forward current* and is designated I_F. Figure 2–9 illustrates what happens as the forward-bias voltage is increased positively from 0 V. The resistor is used to limit the forward current to a value that will not overheat the diode and cause damage.

With 0 V across the diode, there is no forward current. As you gradually increase the forward-bias voltage, the forward current *and* the voltage across the diode gradually increase, as shown in Figure 2–9(a). A portion of the forward-bias voltage is dropped across the limiting resistor. When the forward-bias voltage is increased to a value where the voltage across the diode reaches approximately 0.7 V (barrier potential), the forward current begins to increase rapidly, as illustrated in Figure 2–9(b).

As you continue to increase the forward-bias voltage, the current continues to increase very rapidly, but the voltage across the diode increases only gradually above 0.7 V. This small increase in the diode voltage above the barrier potential is due to the voltage drop across the internal dynamic resistance of the semiconductive material.

Graphing the V-I Curve If you plot the results of the type of measurements shown in Figure 2–9 on a graph, you get the ***V-I* characteristic** curve for a forward-biased diode, as shown in Figure 2–10(a). The diode forward voltage (V_F) increases to the right along the horizontal axis, and the forward current (I_F) increases upward along the vertical axis.

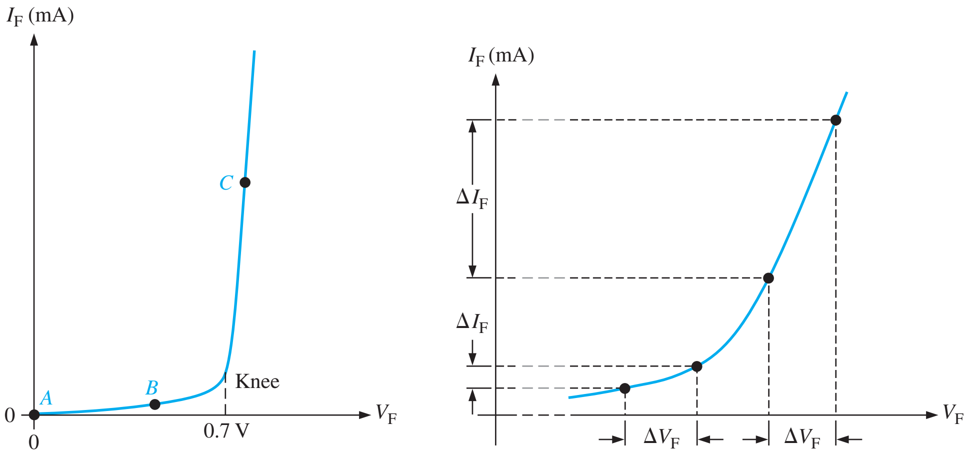


(a) Small forward-bias voltage ($V_F < 0.7$ V), very small forward current.

(b) Forward voltage reaches and remains nearly constant at approximately 0.7 V. Forward current continues to increase as the bias voltage is increased.

▲ **FIGURE 2–9**

Forward-bias measurements show general changes in V_F and I_F as V_{BIAS} is increased.



(a) V-I characteristic curve for forward bias.

(b) Expanded view of a portion of the curve in part (a). The dynamic resistance r'_d decreases as you move up the curve, as indicated by the decrease in the value of $\Delta V_F/\Delta I_F$.

◀ **FIGURE 2–10**

Relationship of voltage and current in a forward-biased diode.

As you can see in Figure 2–10(a), the forward current increases very little until the forward voltage across the *pn* junction reaches approximately 0.7 V at the knee of the curve. After this point, the forward voltage remains nearly constant at approximately 0.7 V, but I_F increases rapidly. As previously mentioned, there is a slight increase in V_F above 0.7 V as the current increases due mainly to the voltage drop across the dynamic resistance. The I_F scale is typically in mA, as indicated.

Three points *A*, *B*, and *C* are shown on the curve in Figure 2–10(a). Point *A* corresponds to a zero-bias condition. Point *B* corresponds to Figure 2–10(a) where the forward voltage is less than the barrier potential of 0.7 V. Point *C* corresponds to Figure 2–10(a) where the forward voltage *approximately* equals the barrier potential. As the external bias voltage and forward current continue to increase above the knee, the forward voltage will increase slightly above 0.7 V. In reality, the forward voltage can be as much as approximately 1 V, depending on the forward current.

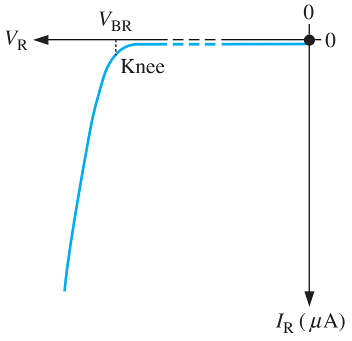
Dynamic Resistance Figure 2–10(b) is an expanded view of the *V-I* characteristic curve in part (a) and illustrates dynamic resistance. Unlike a linear resistance, the resistance of the forward-biased diode is not constant over the entire curve. Because the resistance changes as you move along the *V-I* curve, it is called *dynamic* or *ac resistance.* Internal resistances of electronic devices are usually designated by lowercase italic *r* with a prime, instead of the standard *R*. The dynamic resistance of a diode is designated r'_d.

Below the knee of the curve the resistance is greatest because the current increases very little for a given change in voltage ($r'_d = \Delta V_F/\Delta I_F$). The resistance begins to decrease in the region of the knee of the curve and becomes smallest above the knee where there is a large change in current for a given change in voltage.

V-I Characteristic for Reverse Bias

When a reverse-bias voltage is applied across a diode, there is only an extremely small reverse current (I_R) through the *pn* junction. With 0 V across the diode, there is no reverse current. As you gradually increase the reverse-bias voltage, there is a very small reverse current and the voltage across the diode increases. When the applied bias voltage is increased to a value where the reverse voltage across the diode (V_R) reaches the breakdown value (V_{BR}), the reverse current begins to increase rapidly.

As you continue to increase the bias voltage, the current continues to increase very rapidly, but the voltage across the diode increases very little above V_{BR}. Breakdown, with exceptions, is not a normal mode of operation for most *pn* junction devices.



▲ FIGURE 2–11

V-I characteristic curve for a reverse-biased diode.

Graphing the V-I Curve If you plot the results of reverse-bias measurements on a graph, you get the *V-I* characteristic curve for a reverse-biased diode. A typical curve is shown in Figure 2–11. The diode reverse voltage (V_R) increases to the left along the horizontal axis, and the reverse current (I_R) increases downward along the vertical axis.

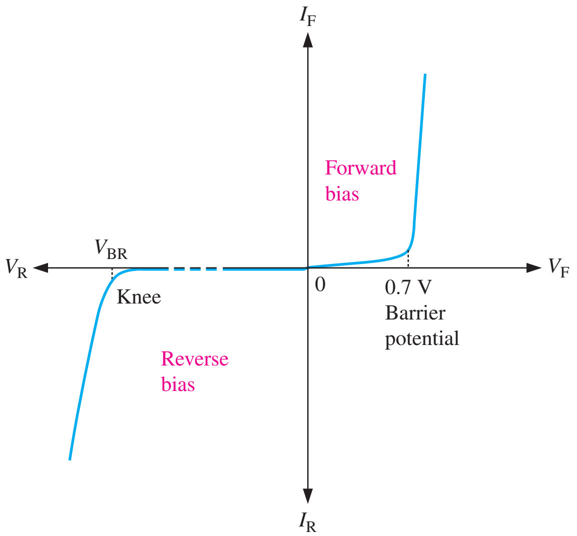
There is very little reverse current (usually μA or nA) until the reverse voltage across the diode reaches approximately the breakdown value (V_{BR}) at the knee of the curve. After this point, the reverse voltage remains at approximately V_{BR}, but I_R increases very rapidly, resulting in overheating and possible damage if current is not limited to a safe level. The breakdown voltage for a diode depends on the doping level, which the manufacturer sets, depending on the type of diode. A typical rectifier diode (the most widely used type) has a breakdown voltage of greater than 50 V. Some specialized diodes have a breakdown voltage that is only 5 V.

The Complete *V-I* Characteristic Curve

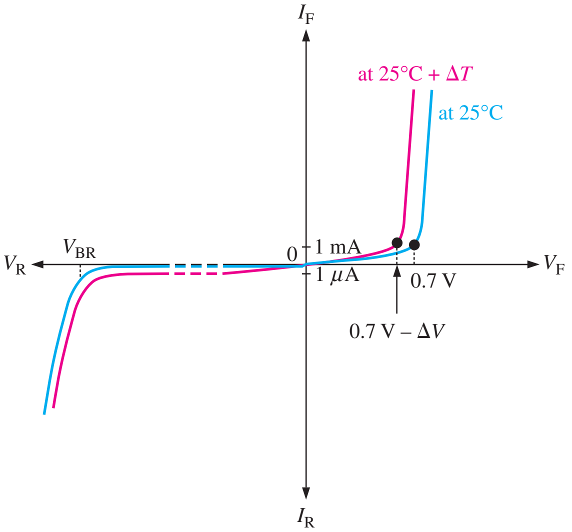
Combine the curves for both forward bias and reverse bias, and you have the complete *V-I* characteristic curve for a diode, as shown in Figure 2–12.

► FIGURE 2–12

The complete *V-I* characteristic curve for a diode.



Temperature Effects For a forward-biased diode, as temperature is increased, the forward current increases for a given value of forward voltage. Also, for a given value of forward current, the forward voltage decreases. This is shown with the *V-I* characteristic curves in Figure 2–13. The blue curve is at room temperature (25°C) and the red curve is at an elevated temperature (25°C + ΔT). The barrier potential decreases by 2 mV for each degree increase in temperature.



◀ **FIGURE 2–13**

Temperature effect on the diode *V-I* characteristic. The 1 mA and 1 μA marks on the vertical axis are given as a basis for a relative comparison of the current scales.

For a reverse-biased diode, as temperature is increased, the reverse current increases. The difference in the two curves is exaggerated on the graph in Figure 2–13 for illustration. Keep in mind that the reverse current below breakdown remains extremely small and can usually be neglected.

SECTION 2–2 CHECKUP

1. Discuss the significance of the knee of the characteristic curve in forward bias.
2. On what part of the curve is a forward-biased diode normally operated?
3. Which is greater, the breakdown voltage or the barrier potential?
4. On what part of the curve is a reverse-biased diode normally operated?
5. What happens to the barrier potential when the temperature increases?

2–3 DIODE MODELS

You have learned that a diode is a *pn* junction device. In this section, you will learn the electrical symbol for a diode and how a diode can be modeled for circuit analysis using any one of three levels of complexity. Also, diode packaging and terminal identification are introduced.

After completing this section, you should be able to

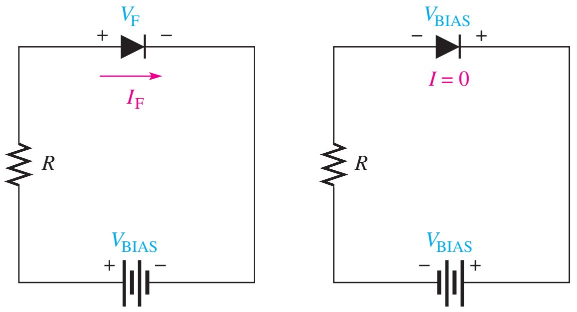
- **Explain how the three diode models differ**
- Discuss bias connections
- Describe the diode approximations
  - Describe the ideal diode model
  - Describe the practical diode model
  - Describe the complete diode model

Bias Connections

Forward-Bias Recall that a diode is forward-biased when a voltage source is connected as shown in Figure 2–14(a). The positive terminal of the source is connected to the anode through a current-limiting resistor. The negative terminal of the source is connected to the cathode. The forward current (I_F) is from anode to cathode as indicated. The forward voltage drop (V_F) due to the barrier potential is from positive at the anode to negative at the cathode.

▶ FIGURE 2–14

Forward-bias and reverse-bias connections showing the diode symbol.

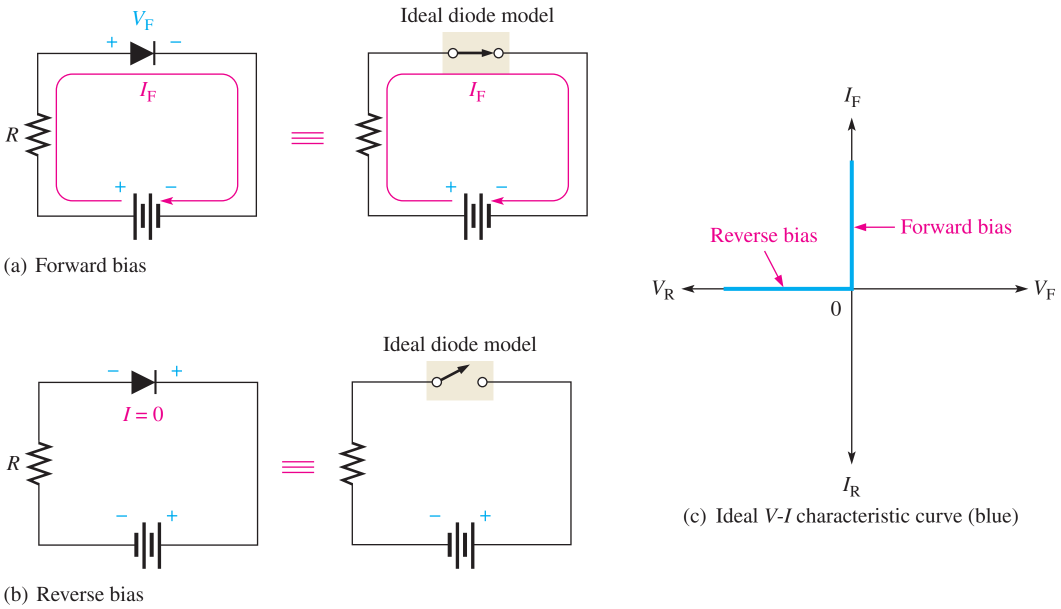

V_F
+
−
I_F
R
V_{BIAS}
+
−
V_{BIAS}
−
+
I = 0
R
V_{BIAS}
−
+

(a) Forward bias (b) Reverse bias

Reverse-Bias Connection A diode is reverse-biased when a voltage source is connected as shown in Figure 2–14(b). The negative terminal of the source is connected to the anode side of the circuit, and the positive terminal is connected to the cathode side. A resistor is not necessary in reverse bias but it is shown for circuit consistency. The reverse current is extremely small and can be considered to be zero. Notice that the entire bias voltage (V_{BIAS}) appears across the diode.

Diode Approximations

The Ideal Diode Model The ideal model of a diode is the least accurate approximation and can be represented by a simple switch. When the diode is forward-biased, it ideally acts like a closed (on) switch, as shown in Figure 2–15(a). When the diode is reverse-biased, it


V_F
+
−
I_F
R
+
−
Ideal diode model
I_F
+
−
(a) Forward bias
−
+
I = 0
R
−
+
Ideal diode model
−
+
(b) Reverse bias
I_F
Reverse bias
Forward bias
V_R
V_F
0
I_R
(c) Ideal V-I characteristic curve (blue)

▲ FIGURE 2–15

The ideal model of a diode.

ideally acts like an open (off) switch, as shown in part (b). Although the barrier potential, the forward dynamic resistance, and the reverse current are all neglected, this model is adequate for most troubleshooting when you are trying to determine if the diode is working properly.

In Figure 2–15(c), the ideal *V-I* characteristic curve graphically depicts the ideal diode operation. Since the barrier potential and the forward dynamic resistance are neglected, the diode is assumed to have a zero voltage across it when forward-biased, as indicated by the portion of the curve on the positive vertical axis.

$$V_F = 0\text{ V}$$

The forward current is determined by the bias voltage and the limiting resistor using Ohm's law.

$$\boldsymbol{I_F = \frac{V_{BIAS}}{R_{LIMIT}}}$$

Equation 2–1

Since the reverse current is neglected, its value is assumed to be zero, as indicated in Figure 2–15(c) by the portion of the curve on the negative horizontal axis.

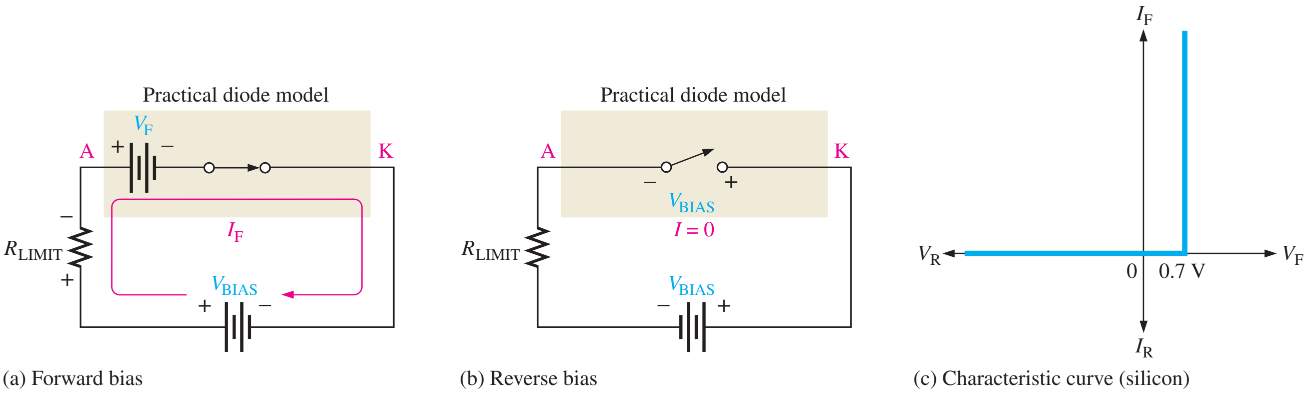
$$I_R = 0\text{ A}$$

The reverse voltage equals the bias voltage.

$$V_R = V_{BIAS}$$

You may want to use the ideal model when you are troubleshooting or trying to figure out the operation of a circuit and are not concerned with more exact values of voltage or current.

The Practical Diode Model The practical model includes the barrier potential. When the diode is forward-biased, it is equivalent to a closed switch in series with a small equivalent voltage source (V_F) equal to the barrier potential (0.7 V) with the positive side toward the anode, as indicated in Figure 2–16(a). This equivalent voltage source represents the barrier potential that must be exceeded by the bias voltage before the diode will conduct and is not an active source of voltage. When conducting, a voltage drop of 0.7 V appears across the diode.



(a) Forward bias (b) Reverse bias (c) Characteristic curve (silicon)

▲ FIGURE 2–16

The practical model of a diode.

When the diode is reverse-biased, it is equivalent to an open switch just as in the ideal model, as shown in Figure 2–16(b). The barrier potential does not affect reverse bias, so it is not a factor.

The characteristic curve for the practical diode model is shown in Figure 2–16(c). Since the barrier potential is included and the dynamic resistance is neglected, the diode is assumed to have a voltage across it when forward-biased, as indicated by the portion of the curve to the right of the origin.

$$V_F = 0.7\text{ V}$$

The forward current is determined as follows by first applying Kirchhoff's voltage law to Figure 2–16(a):

$$V_{\text{BIAS}} - V_{\text{F}} - V_{R_{\text{LIMIT}}} = 0$$
$$V_{R_{\text{LIMIT}}} = I_{\text{F}} R_{\text{LIMIT}}$$

Substituting and solving for I_{F},

Equation 2–2

$$\boldsymbol{I_{\text{F}} = \frac{V_{\text{BIAS}} - V_{\text{F}}}{R_{\text{LIMIT}}}}$$

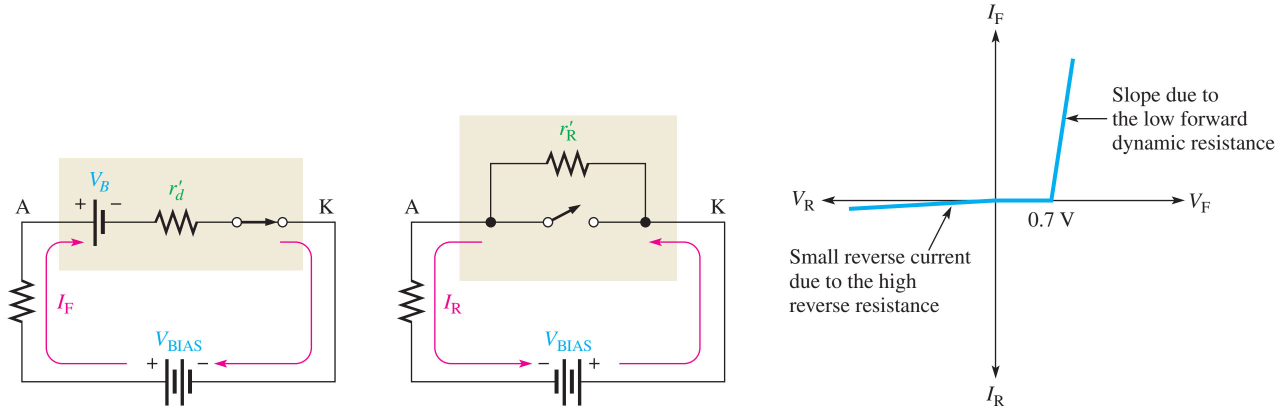
The diode is assumed to have zero reverse current, as indicated by the portion of the curve on the negative horizontal axis.

$$I_{\text{R}} = 0\text{ A}$$
$$V_{\text{R}} = V_{\text{BIAS}}$$

The practical model is useful when you are troubleshooting in lower-voltage circuits. In these cases, the 0.7 V drop across the diode may be significant and should be taken into account. The practical model is also useful when you are designing basic diode circuits.

The Complete Diode Model The complete model of a diode is the most accurate approximation and includes the barrier potential, the small forward dynamic resistance (r'_d), and the large internal reverse resistance (r'_{R}). The reverse resistance is taken into account because it provides a path for the reverse current, which is included in this diode model.

When the diode is forward-biased, it acts as a closed switch in series with the equivalent barrier potential voltage (V_B) and the small forward dynamic resistance (r'_d), as indicated in Figure 2–17(a). When the diode is reverse-biased, it acts as an open switch in parallel with the large internal reverse resistance (r'_{R}), as shown in Figure 2–17(b). The barrier potential does not affect reverse bias, so it is not a factor.



(a) Forward bias

(b) Reverse bias

(c) *V-I* characteristic curve

▲ FIGURE 2–17

The complete model of a diode.

The characteristic curve for the complete diode model is shown in Figure 2–17(c). Since the barrier potential and the forward dynamic resistance are included, the diode is assumed to have a voltage across it when forward-biased. This voltage (V_{F}) consists of the barrier potential voltage plus the small voltage drop across the dynamic resistance, as indicated by the portion of the curve to the right of the origin. The curve slopes because the voltage drop due to dynamic resistance increases as the current increases. For the complete model of a silicon diode, the following formulas apply:

$$V_F = 0.7\text{ V} + I_F r'_d$$

$$I_F = \frac{V_{BIAS} - 0.7\text{ V}}{R_{LIMIT} + r'_d}$$

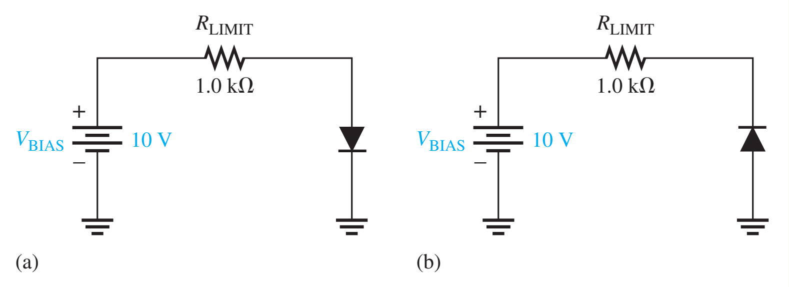
The reverse current is taken into account with the parallel resistance and is indicated by the portion of the curve to the left of the origin. The breakdown portion of the curve is not shown because breakdown is not a normal mode of operation for most diodes.

For troubleshooting work, it is unnecessary to use the complete model, as it involves complicated calculations. This model is generally suited to design problems using a computer for simulation. The ideal and practical models are used for circuits in this text, except in the following example, which illustrates the differences in the three models.

EXAMPLE 2–1

(a) Determine the forward voltage and forward current for the diode in Figure 2–18(a) for each of the diode models. Also find the voltage across the limiting resistor in each case. Assume $r'_d = 10\ \Omega$ at the determined value of forward current.

(b) Determine the reverse voltage and reverse current for the diode in Figure 2–18(b) for each of the diode models. Also find the voltage across the limiting resistor in each case. Assume $I_R = 1\ \mu\text{A}$.



▲ FIGURE 2–18

Solution **(a)** Ideal model:

$$V_F = \mathbf{0\ V}$$

$$I_F = \frac{V_{BIAS}}{R_{LIMIT}} = \frac{10\text{ V}}{1.0\text{ k}\Omega} = \mathbf{10\ mA}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (10\text{ mA})(1.0\text{ k}\Omega) = \mathbf{10\ V}$$

Practical model:

$$V_F = \mathbf{0.7\ V}$$

$$I_F = \frac{V_{BIAS} - V_F}{R_{LIMIT}} = \frac{10\text{ V} - 0.7\text{ V}}{1.0\text{ k}\Omega} = \frac{9.3\text{ V}}{1.0\text{ k}\Omega} = \mathbf{9.3\ mA}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (9.3\text{ mA})(1.0\text{ k}\Omega) = \mathbf{9.3\ V}$$

Complete model:

$$I_F = \frac{V_{BIAS} - 0.7\text{ V}}{R_{LIMIT} + r'_d} = \frac{10\text{ V} - 0.7\text{ V}}{1.0\text{ k}\Omega + 10\ \Omega} = \frac{9.3\text{ V}}{1010\ \Omega} = \mathbf{9.21\ mA}$$

$$V_F = 0.7\ V + I_F r'_d = 0.7\text{ V} + (9.21\text{ mA})(10\ \Omega) = \mathbf{792\ mV}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (9.21\text{ mA})(1.0\text{ k}\Omega) = \mathbf{9.21\ V}$$

(b) Ideal model:

$$I_R = \mathbf{0\ A}$$
$$V_R = V_{BIAS} = \mathbf{10\ V}$$
$$V_{R_{LIMIT}} = \mathbf{0\ V}$$

Practical model:

$$I_R = \mathbf{0\ A}$$
$$V_R = V_{BIAS} = \mathbf{10\ V}$$
$$V_{R_{LIMIT}} = \mathbf{0\ V}$$

Complete model:

$$I_R = \mathbf{1\ \mu A}$$
$$V_{R_{LIMIT}} = I_R R_{LIMIT} = (1\ \mu\text{A})(1.0\ \text{k}\Omega) = \mathbf{1\ mV}$$
$$V_R = V_{BIAS} - V_{R_{LIMIT}} = 10\ \text{V} - 1\ \text{mV} = \mathbf{9.999\ V}$$

*Related Problem** Assume that the diode in Figure 2–18(a) fails open. What is the voltage across the diode and the voltage across the limiting resistor?

***Answers can be found at www.pearsonhighered.com/floyd.**

Open the Multisim file E02-01 in the Examples folder on the companion website. Measure the voltages across the diode and the resistor in both circuits and compare with the calculated results in this example.

SECTION 2–3 CHECKUP

1. What are the two conditions under which a diode is operated?
2. Under what condition is a diode never intentionally operated?
3. What is the simplest way to visualize a diode?
4. To more accurately represent a diode, what factors must be included?
5. Which diode model represents the most accurate approximation?

2–4 HALF-WAVE RECTIFIERS

Because of their ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert ac voltage into dc voltage. Rectifiers are found in all dc power supplies that operate from an ac voltage source. A power supply is an essential part of each electronic system from the simplest to the most complex.

After completing this section, you should be able to

- **Explain and analyze the operation of half-wave rectifiers**
- Describe a basic dc power supply
- Discuss half-wave rectification
    - Determine the average value of a half-wave voltage
- Explain how the barrier potential affects a half-wave rectifier output
    - Calculate the output voltage
- Define *peak inverse voltage*
- Explain the operation of a transformer-coupled rectifier

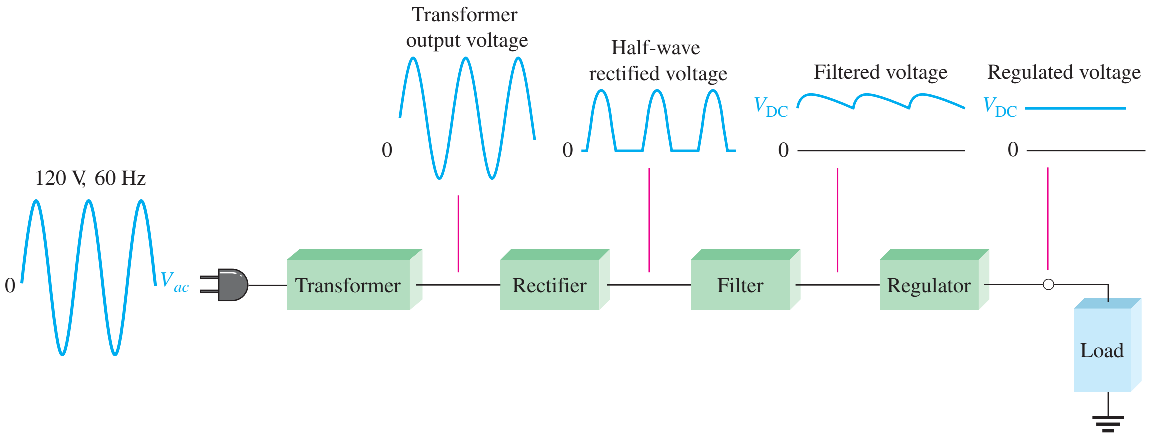
The Basic DC Power Supply

All active electronic devices require a source of constant dc that can be supplied by a battery or a dc power supply. The **dc power supply** converts the standard 120 V, 60 Hz ac voltage available at wall outlets into a constant dc voltage. The dc power supply is one of the most common circuits you will find, so it is important to understand how it works. The voltage produced is used to power all types of electronic circuits including consumer electronics (televisions, DVDs, etc.), computers, industrial controllers, and most laboratory instrumentation systems and equipment. The dc voltage level required depends on the application, but most applications require relatively low voltages.

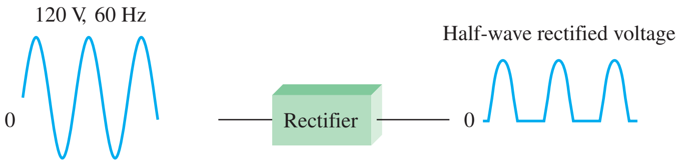
A basic block diagram of the complete power supply is shown in Figure 2–19(a). Generally the ac input line voltage is stepped down to a lower ac voltage with a transformer (although it may be stepped up when higher voltages are needed or there may be no transformer at all in rare instances). As you learned in your dc/ac course, a **transformer** changes ac voltages based on the turns ratio between the primary and secondary. If the secondary has more turns than the primary, the output voltage across the secondary will be higher and the current will be smaller. If the secondary has fewer turns than the primary, the output voltage across the secondary will be lower and the current will be higher. The rectifier can be either a half-wave rectifier or a full-wave rectifier (covered in Section 2–5). The **rectifier** converts the ac input voltage to a pulsating dc voltage, called a half-wave rectified voltage, as shown in Figure 2–19(b). The **filter** eliminates the fluctuations in the rectified voltage and produces a relatively smooth dc voltage. The power supply filter is covered in Section 2–6. The **regulator** is a circuit that maintains a constant dc voltage for variations in the input line voltage or in the load. Regulators vary from a single semiconductor device to more complex integrated circuits. The load is a circuit or device connected to the output of the power supply and operates from the power supply voltage and current.

FYI

The standard line voltage in North America is 120 V/240 V at 60 Hz. Most small appliances operate on 120 V and larger appliances such as dryers, ranges, and heaters operate on 240 V. Occasionally, you will see references to 110 V or 115 V, but the standard is 120 V. Some foreign countries do use 110 V or 115 V at either 60 Hz or 50 Hz.



(a) Complete power supply with transformer, rectifier, filter, and regulator



(b) Half-wave rectifier

▲ **FIGURE 2–19**

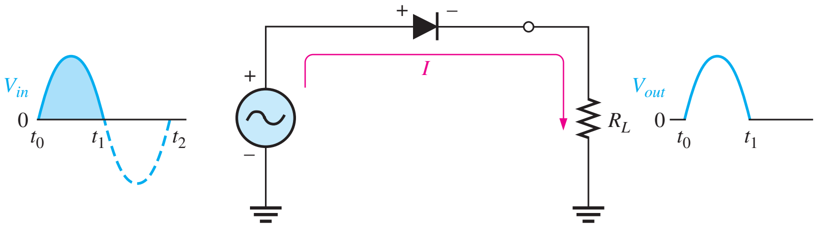
Block diagram of a dc power supply with a load and a rectifier.

GREENTECH NOTE

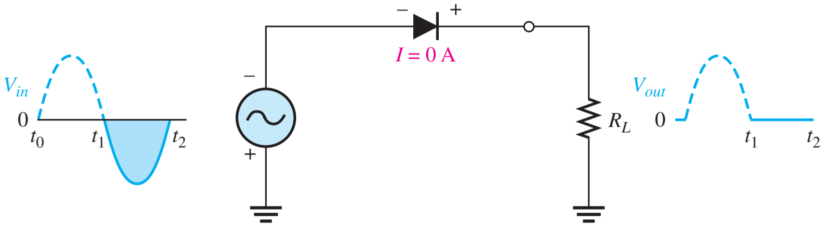
The *Energy Star* program was originally established by the EPA as a voluntary labeling program designed to indicate energy-efficient products. In order for power supplies to comply with the Energy Star requirements, they must have a minimum 80% efficiency rating for all rated power output. Try to choose a power supply that carries as 80 PLUS logo on it. This means that the power supply efficiency has been tested and approved to meet the Energy Star guidelines. Not all power supplies that claim to be high efficiency meet the Energy Star requirements.

Half-Wave Rectifier Operation

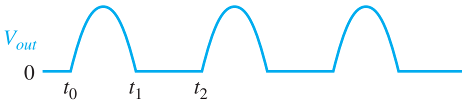
Figure 2–20 illustrates the process called *half-wave rectification.* A diode is connected to an ac source and to a load resistor, R_L, forming a **half-wave rectifier**. Keep in mind that all ground symbols represent the same point electrically. Let's examine what happens during one cycle of the input voltage using the ideal model for the diode. When the sinusoidal input voltage (V_{in}) goes positive, the diode is forward-biased and conducts current through the load resistor, as shown in part (a). The current produces an output voltage across the load R_L, which has the same shape as the positive half-cycle of the input voltage.



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source.



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 60 Hz half-wave output voltage for three input cycles

▲ **FIGURE 2–20**

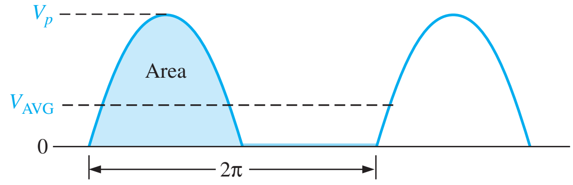
Half-wave rectifier operation. The diode is considered to be ideal.

When the input voltage goes negative during the second half of its cycle, the diode is reverse-biased. There is no current, so the voltage across the load resistor is 0 V, as shown in Figure 2–20(b). The net result is that only the positive half-cycles of the ac input voltage appear across the load. Since the output does not change polarity, it is a pulsating dc voltage with a frequency of 60 Hz, as shown in part (c).

Average Value of the Half-Wave Output Voltage The average value of the half-wave rectified output voltage is the value you would measure on a dc voltmeter. Mathematically, it is determined by finding the area under the curve over a full cycle, as illustrated in Figure 2–21, and then dividing by 2π, the number of radians in a full cycle. The result of this is expressed in Equation 2–3, where V_p is the peak value of the voltage. This equation shows that V_{AVG} is approximately 31.8% of V_p for a half-wave rectified voltage. The derivation for this equation can be found in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

Equation 2–3

$$V_{\mathrm{AVG}} = \frac{V_p}{\pi}$$



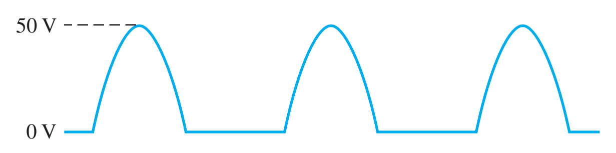
◀ FIGURE 2–21

Average value of the half-wave rectified signal.

EXAMPLE 2–2

What is the average value of the half-wave rectified voltage in Figure 2–22?

▶ FIGURE 2–22



Solution

$$V_{AVG} = \frac{V_p}{\pi} = \frac{50\text{ V}}{\pi} = \mathbf{15.9\text{ V}}$$

Notice that V_{AVG} is 31.8% of V_p.

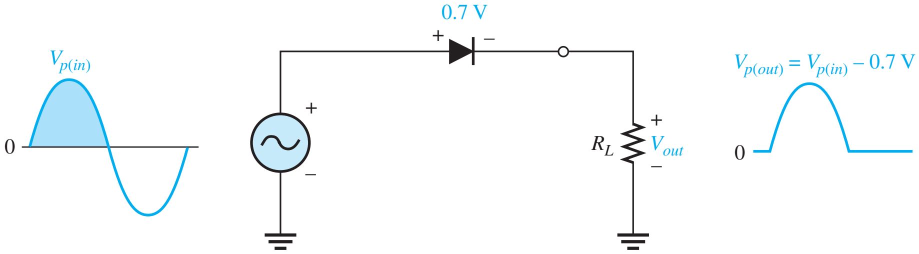
Related Problem Determine the average value of the half-wave voltage if its peak amplitude is 12 V.

Effect of the Barrier Potential on the Half-Wave Rectifier Output

In the previous discussion, the diode was considered ideal. When the practical diode model is used with the barrier potential of 0.7 V taken into account, this is what happens. During the positive half-cycle, the input voltage must overcome the barrier potential before the diode becomes forward-biased. This results in a half-wave output with a peak value that is 0.7 V less than the peak value of the input, as shown in Figure 2–23. The expression for the peak output voltage is

$$\mathbf{V_{p(out)} = V_{p(in)} - 0.7\text{ V}}$$

Equation 2–4



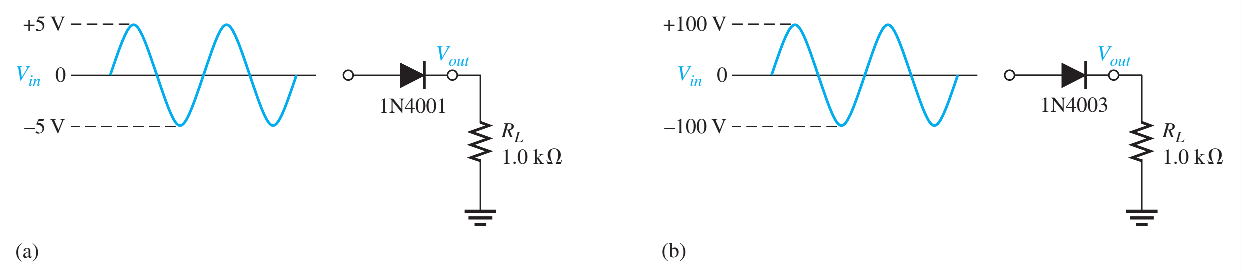
▲ FIGURE 2–23

The effect of the barrier potential on the half-wave rectified output voltage is to reduce the peak value of the input by about 0.7 V.

It is usually acceptable to use the ideal diode model, which neglects the effect of the barrier potential, when the peak value of the applied voltage is much greater than the barrier potential (at least 10 V, as a rule of thumb). However, we will use the practical model of a diode, taking the 0.7 V barrier potential into account unless stated otherwise.

EXAMPLE 2–3

Draw the output voltages of each rectifier for the indicated input voltages, as shown in Figure 2–24. The 1N4001 and 1N4003 are specific rectifier diodes.



▲ FIGURE 2–24

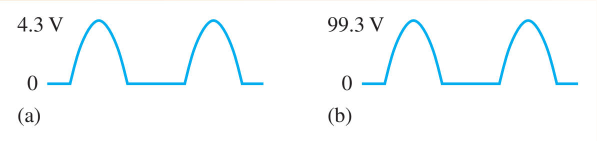
Solution The peak output voltage for circuit (a) is

$$V_{p(out)} = V_{p(in)} - 0.7\text{ V} = 5\text{ V} - 0.7\text{ V} = \mathbf{4.30\ V}$$

The peak output voltage for circuit (b) is

$$V_{p(out)} = V_{p(in)} - 0.7\text{ V} = 100\text{ V} - 0.7\text{ V} = \mathbf{99.3\ V}$$

The output voltage waveforms are shown in Figure 2–25. Note that the barrier potential could have been neglected in circuit (b) with very little error (0.7 percent); but, if it is neglected in circuit (a), a significant error results (14 percent).



▲ FIGURE 2–25

Output voltages for the circuits in Figure 2–24. They are not shown on the same scale.

Related Problem Determine the peak output voltages for the rectifiers in Figure 2–24 if the peak input in part (a) is 3 V and the peak input in part (b) is 50 V.

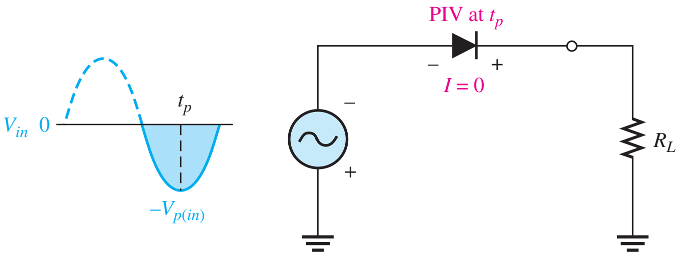
Open the Multisim file E02-03 in the Examples folder on the companion website. For the inputs specified in the example, measure the resulting output voltage waveforms. Compare your measured results with those shown in the example.

Peak Inverse Voltage (PIV)

The **peak inverse voltage (PIV)** equals the peak value of the input voltage, and the diode must be capable of withstanding this amount of repetitive reverse voltage. For the diode in Figure 2–26, the maximum value of reverse voltage, designated as PIV, occurs at the peak of each negative alternation of the input voltage when the diode is reverse-biased. A diode should be rated at least 20% higher than the PIV.

Equation 2–5

$$\mathbf{PIV} = V_{p(in)}$$

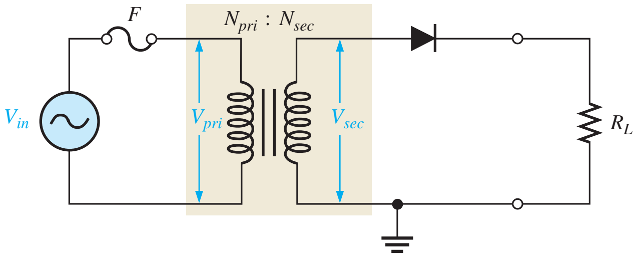


▲ FIGURE 2–26

The PIV occurs at the peak of each half-cycle of the input voltage when the diode is reverse-biased. In this circuit, the PIV occurs at the peak of each negative half-cycle.

Transformer Coupling

As you have seen, a transformer is often used to couple the ac input voltage from the source to the rectifier, as shown in Figure 2–27. Transformer coupling provides two advantages. First, it allows the source voltage to be stepped down as needed. Second, the ac source is electrically isolated from the rectifier, thus preventing a shock hazard in the secondary circuit.



◀ FIGURE 2–27

Half-wave rectifier with transformer-coupled input voltage.

The amount that the voltage is stepped down is determined by the **turns ratio** of the transformer. Unfortunately, the definition of turns ratio for transformers is not consistent between various sources and disciplines. In this text, we use the definition given by the IEEE for electronic power transformers, which is “the number of turns in the secondary (N_{sec}) divided by the number of turns in the primary (N_{pri}).” Thus, a transformer with a turns ratio less than 1 is a step-down type and one with a turns ratio greater than 1 is a step-up type. To show the turns ratio on a schematic, it is common practice to show the numerical ratio directly above the windings.

The secondary voltage of a transformer equals the turns ratio, n, times the primary voltage.

$$V_{sec} = nV_{pri}$$

If $n > 1$, the secondary voltage is greater than the primary voltage. If $n < 1$, the secondary voltage is less than the primary voltage. If $n = 1$, then $V_{sec} = V_{pri}$.

The peak secondary voltage, $V_{p(sec)}$, in a transformer-coupled half-wave rectifier is the same as $V_{p(in)}$ in Equation 2–4. Therefore, Equation 2–4 written in terms of $V_{p(sec)}$ is

$$V_{p(out)} = V_{p(sec)} - 0.7\text{ V}$$

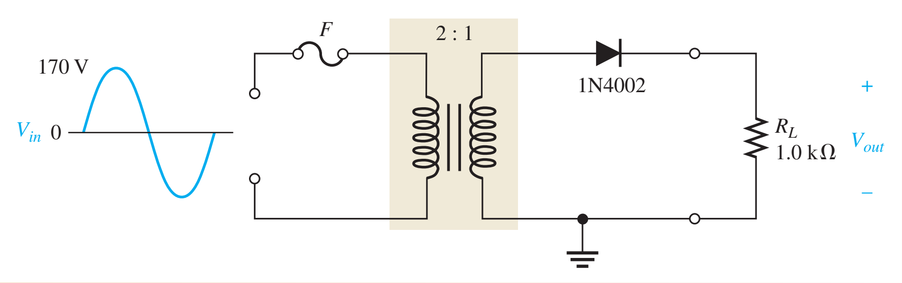
and Equation 2–5 in terms of $V_{p(sec)}$ is

$$\text{PIV} = V_{p(sec)}$$

Turns ratio is useful for understanding the voltage transfer from primary to secondary. However, transformer datasheets rarely show the turns ratio. A transformer is generally specified based on the secondary voltage rather than the turns ratio.

EXAMPLE 2–4 Determine the peak value of the output voltage for Figure 2–28 if the turns ratio is 0.5.

▶ FIGURE 2–28



Solution

$$V_{p(pri)} = V_{p(in)} = 170\text{ V}$$

The peak secondary voltage is

$$V_{p(sec)} = nV_{p(pri)} = 0.5(170\text{ V}) = 85\text{ V}$$

The rectified peak output voltage is

$$V_{p(out)} = V_{p(sec)} - 0.7\text{ V} = 85\text{ V} - 0.7\text{ V} = \mathbf{84.3\text{ V}}$$

where $V_{p(sec)}$ is the input to the rectifier.

Related Problem

(a) Determine the peak value of the output voltage for Figure 2–28 if $n = 2$ and $V_{p(in)} = 312$ V.

(b) What is the PIV across the diode?

(c) Describe the output voltage if the diode is turned around.

Open the Multisim file E02-04 in the Examples folder on the companion website. For the specified input, measure the peak output voltage. Compare your measured result with the calculated value.

SECTION 2–4 CHECKUP

1. At what point on the input cycle does the PIV occur?
2. For a half-wave rectifier, there is current through the load for approximately what percentage of the input cycle?
3. What is the average of a half-wave rectified voltage with a peak value of 10 V?
4. What is the peak value of the output voltage of a half-wave rectifier with a peak sine wave input of 25 V?
5. What PIV rating must a diode have to be used in a rectifier with a peak output voltage of 50 V?

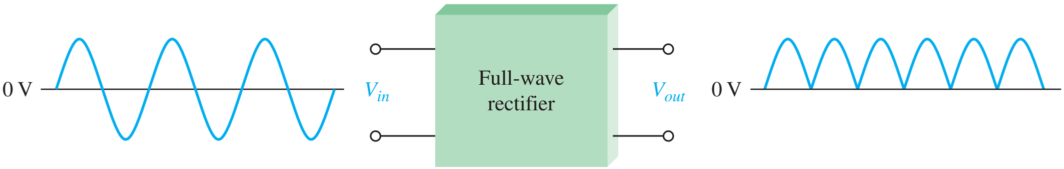
2–5 FULL-WAVE RECTIFIERS

Although half-wave rectifiers have some applications, the full-wave rectifier is the most commonly used type in dc power supplies. In this section, you will use what you learned about half-wave rectification and expand it to full-wave rectifiers. You will learn about two types of full-wave rectifiers: center-tapped and bridge.

After completing this section, you should be able to

- **Explain and analyze the operation of full-wave rectifiers**
- Describe how a center-tapped full-wave rectifier works
  - Discuss the effect of the turns ratio on the rectifier output
  - Calculate the peak inverse voltage
- Describe how a bridge full-wave rectifier works
  - Determine the bridge output voltage
  - Calculate the peak inverse voltage

A **full-wave rectifier** allows unidirectional (one-way) current through the load during the entire 360° of the input cycle, whereas a half-wave rectifier allows current through the load only during one-half of the cycle. The result of full-wave rectification is an output voltage with a frequency twice the input frequency and that pulsates every half-cycle of the input, as shown in Figure 2–29.



▲ FIGURE 2–29

Full-wave rectification.

The number of positive alternations that make up the full-wave rectified voltage is twice that of the half-wave voltage for the same time interval. The average value, which is the value measured on a dc voltmeter, for a full-wave rectified sinusoidal voltage is twice that of the half-wave, as shown in the following formula:

Equation 2–6

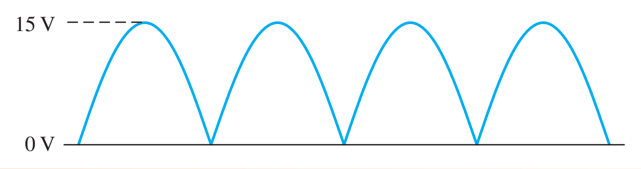
$$V_{\text{AVG}} = \frac{2V_p}{\pi}$$

V_{AVG} is approximately 63.7% of V_p for a full-wave rectified voltage.

EXAMPLE 2–5

Find the average value of the full-wave rectified voltage in Figure 2–30.

▶ FIGURE 2–30



Solution

$$V_{\text{AVG}} = \frac{2V_p}{\pi} = \frac{2(15\text{ V})}{\pi} = \mathbf{9.55\text{ V}}$$

V_{AVG} is 63.7% of V_p.

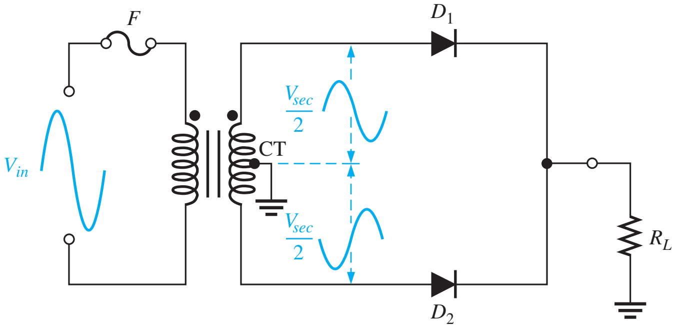
Related Problem Find the average value of the full-wave rectified voltage if its peak is 155 V.

Center-Tapped Full-Wave Rectifier Operation

A **center-tapped rectifier** is a type of full-wave rectifier that uses two diodes connected to the secondary of a center-tapped transformer, as shown in Figure 2–31. The input voltage is coupled through the transformer to the center-tapped secondary. Half of the total secondary voltage appears between the center tap and each end of the secondary winding as shown.

FIGURE 2–31

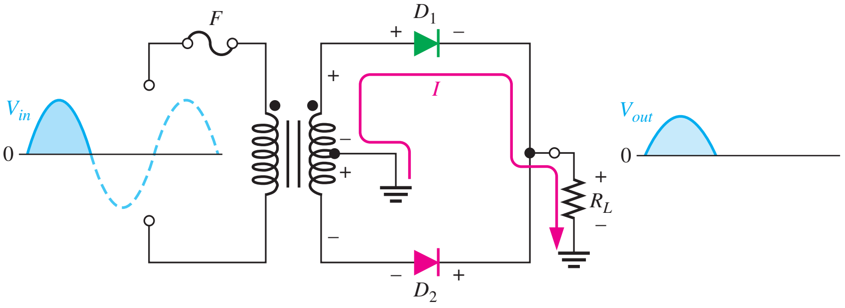
A center-tapped full-wave rectifier.



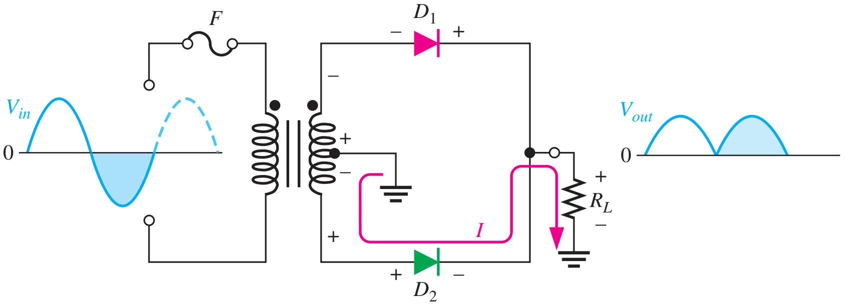
For a positive half-cycle of the input voltage, the polarities of the secondary voltages are as shown in Figure 2–32(a). This condition forward-biases diode D_1 and reverse-biases diode D_2. The current path is through D_1 and the load resistor R_L, as indicated. For a negative half-cycle of the input voltage, the voltage polarities on the secondary are as shown in Figure 2–32(b). This condition reverse-biases D_1 and forward-biases D_2. The current path is through D_2 and R_L, as indicated. Because the output current during both the positive and negative portions of the input cycle is in the same direction through the load, the output voltage developed across the load resistor is a full-wave rectified dc voltage, as shown.

FIGURE 2–32

Basic operation of a center-tapped full-wave rectifier. Note that the current through the load resistor is in the same direction during the entire input cycle, so the output voltage always has the same polarity.

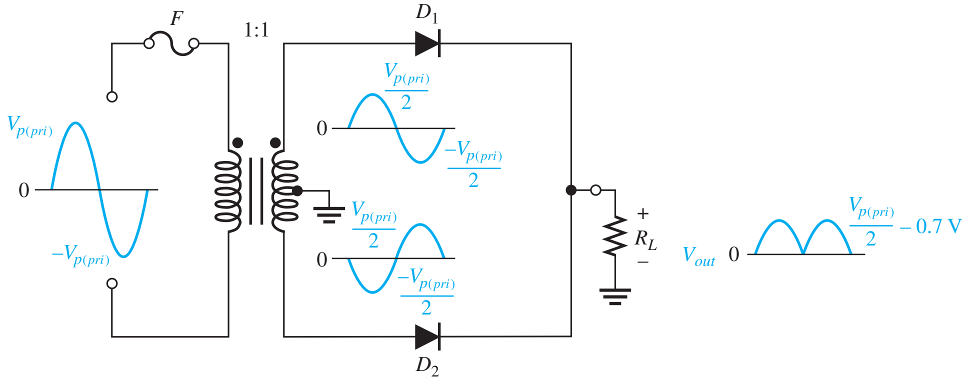


(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

Effect of the Turns Ratio on the Output Voltage If the transformer's turns ratio is 1, the peak value of the rectified output voltage equals half the peak value of the primary input voltage less the barrier potential, as illustrated in Figure 2–33. Half of the primary



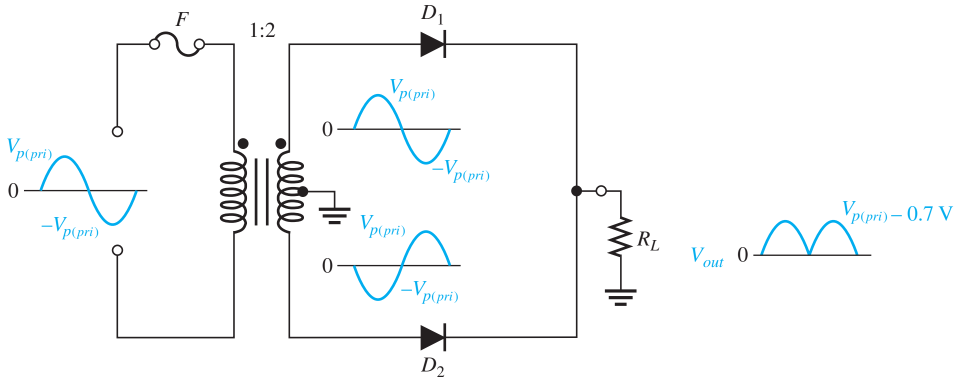
F
1:1
D_1
$V_{p(pri)}$
0
$-V_{p(pri)}$
$\frac{V_{p(pri)}}{2}$
0
$-\frac{V_{p(pri)}}{2}$
$\frac{V_{p(pri)}}{2}$
0
$-\frac{V_{p(pri)}}{2}$
+
R_L
–
V_{out}
0
$\frac{V_{p(pri)}}{2} - 0.7\text{ V}$
D_2

FIGURE 2–33

Center-tapped full-wave rectifier with a transformer turns ratio of 1. $V_{p(pri)}$ is the peak value of the primary voltage.

voltage appears across each half of the secondary winding ($V_{p(sec)} = V_{p(pri)}$). We will begin referring to the forward voltage due to the barrier potential as the **diode drop.**

In order to obtain an output voltage with a peak equal to the input peak (less the diode drop), a step-up transformer with a turns ratio of $n = 2$ must be used, as shown in Figure 2–34. In this case, the total secondary voltage (V_{sec}) is twice the primary voltage ($2V_{pri}$), so the voltage across each half of the secondary is equal to V_{pri}.



F
1:2
D_1
$V_{p(pri)}$
0
$-V_{p(pri)}$
$V_{p(pri)}$
0
$-V_{p(pri)}$
$V_{p(pri)}$
0
$-V_{p(pri)}$
R_L
V_{out}
0
$V_{p(pri)} - 0.7\text{ V}$
D_2

FIGURE 2–34

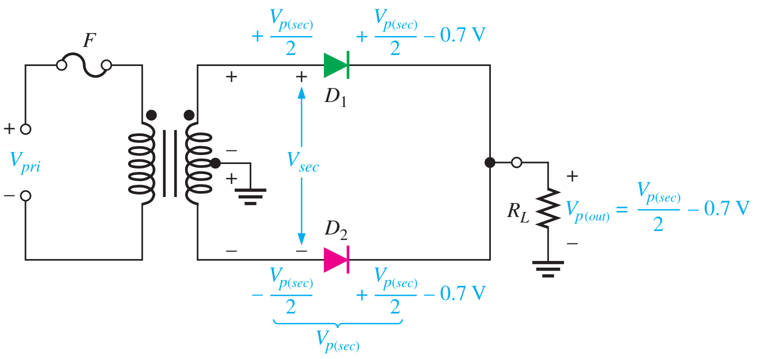
Center-tapped full-wave rectifier with a transformer turns ratio of 2.

In any case, the output voltage of a center-tapped full-wave rectifier is always one-half of the total secondary voltage less the diode drop, no matter what the turns ratio.

$$V_{out} = \frac{V_{sec}}{2} - 0.7\text{ V}$$

Equation 2–7

Peak Inverse Voltage Each diode in the full-wave rectifier is alternately forward-biased and then reverse-biased. The maximum reverse voltage that each diode must withstand is the peak secondary voltage $V_{p(sec)}$. This is shown in Figure 2–35 where D_2 is assumed to be reverse-biased (red) and D_1 is assumed to be forward-biased (green) to illustrate the concept.



$+\frac{V_{p(sec)}}{2}$
$+\frac{V_{p(sec)}}{2} - 0.7\text{ V}$
F
+
+
D_1
+
V_{pri}
–
–
+
V_{sec}
D_2
–
–
+
R_L
$V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7\text{ V}$
–
$-\frac{V_{p(sec)}}{2}$
$+\frac{V_{p(sec)}}{2} - 0.7\text{ V}$
$V_{p(sec)}$

FIGURE 2–35

Diode reverse voltage (D_2 shown reverse-biased and D_1 shown forward-biased).

When the total secondary voltage V_{sec} has the polarity shown, the maximum anode voltage of D_1 is $+V_{p(sec)}/2$ and the maximum anode voltage of D_2 is $-V_{p(sec)}/2$. Since D_1 is assumed to be forward-biased, its cathode is at the same voltage as its anode minus the diode drop; this is also the voltage on the cathode of D_2.

The peak inverse voltage across D_2 is

$$\text{PIV} = \left(\frac{V_{p(sec)}}{2} - 0.7\text{ V}\right) - \left(-\frac{V_{p(sec)}}{2}\right) = \frac{V_{p(sec)}}{2} + \frac{V_{p(sec)}}{2} - 0.7\text{ V}$$

$$= V_{p(sec)} - 0.7\text{ V}$$

Since $V_{p(out)} = V_{p(sec)}/2 - 0.7$ V, then by multiplying each term by 2 and transposing,

$$V_{p(sec)} = 2V_{p(out)} + 1.4\text{ V}$$

Therefore, by substitution, the peak inverse voltage across either diode in a full-wave center-tapped rectifier is

Equation 2–8

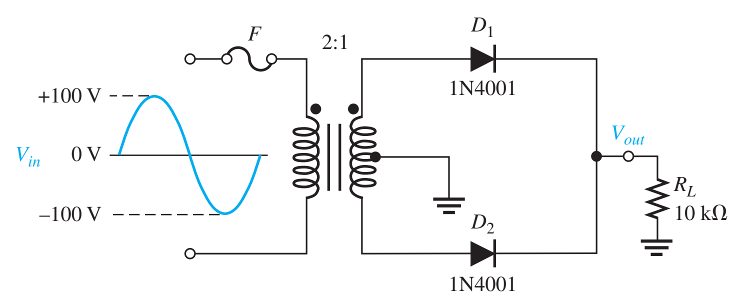
$$\mathbf{PIV = 2V_{p(out)} + 0.7\ V}$$

EXAMPLE 2–6

(a) Show the voltage waveforms across each half of the secondary winding and across R_L when a 100 V peak sine wave is applied to the primary winding in Figure 2–36.

(b) What minimum PIV rating must the diodes have?

▶ FIGURE 2–36



Solution

(a) The transformer turns ratio $n = 0.5$. The total peak secondary voltage is

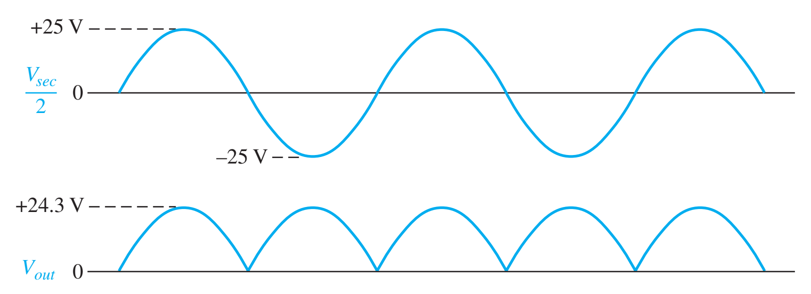
$$V_{p(sec)} = nV_{p(pri)} = 0.5(100\text{ V}) = 50\text{ V}$$

There is a 25 V peak across each half of the secondary with respect to ground. The output load voltage has a peak value of 25 V, less the 0.7 V drop across the diode. The waveforms are shown in Figure 2–37.

(b) Each diode must have a minimum PIV rating of

$$\text{PIV} = 2V_{p(out)} + 0.7\text{ V} = 2(24.3\text{ V}) + 0.7\text{ V} = \mathbf{49.3\ V}$$

▶ FIGURE 2–37



Related Problem What diode PIV rating is required to handle a peak input of 160 V in Figure 2–36?

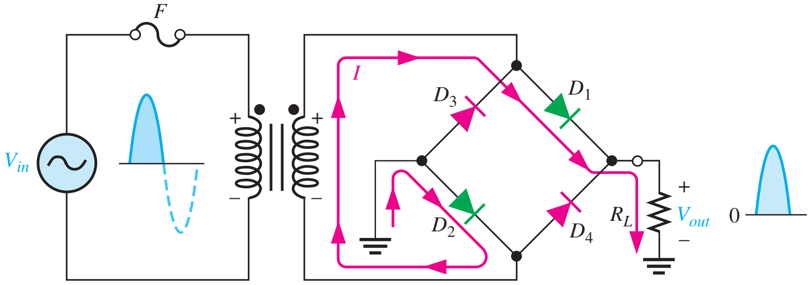
Open the Multisim file E02-06 in the Examples folder on the companion website. For the specified input voltage, measure the voltage waveforms across each half of the secondary and across the load resistor. Compare with the results shown in the example.

Bridge Full-Wave Rectifier Operation

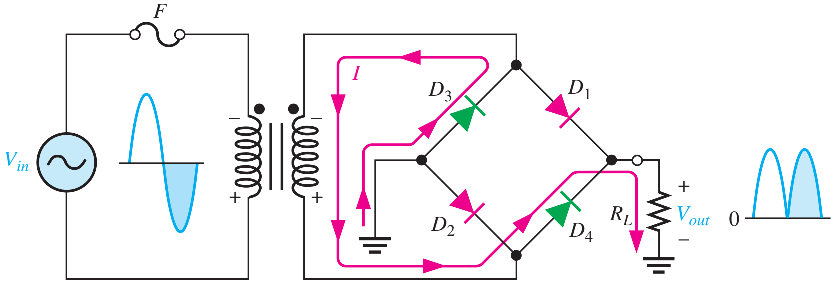
The **bridge rectifier** uses four diodes connected as shown in Figure 2–38. When the input cycle is positive as in part (a), diodes D_1 and D_2 are forward-biased and conduct current in the direction shown. A voltage is developed across R_L that looks like the positive half of the input cycle. During this time, diodes D_3 and D_4 are reverse-biased.

FIGURE 2–38

Operation of a bridge rectifier.



(a) During the positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.



(b) During the negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

When the input cycle is negative as in Figure 2–38(b), diodes D_3 and D_4 are forward-biased and conduct current in the same direction through R_L as during the positive half-cycle. During the negative half-cycle, D_1 and D_2 are reverse-biased. A full-wave rectified output voltage appears across R_L as a result of this action.

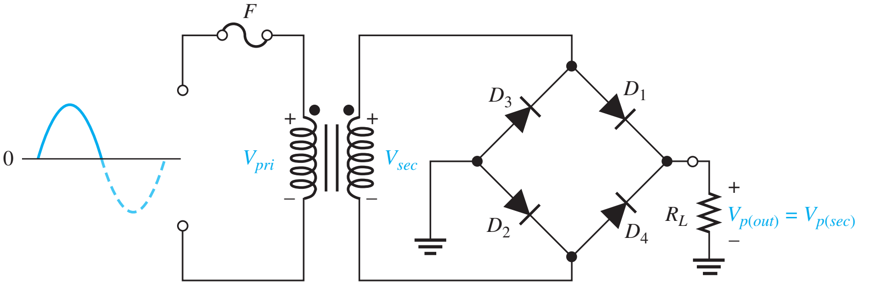
Bridge Output Voltage A bridge rectifier with a transformer-coupled input is shown in Figure 2–39(a). During the positive half-cycle of the total secondary voltage, diodes D_1 and D_2 are forward-biased. Neglecting the diode drops, the secondary voltage appears across the load resistor. The same is true when D_3 and D_4 are forward-biased during the negative half-cycle.

$$V_{p(out)} = V_{p(sec)}$$

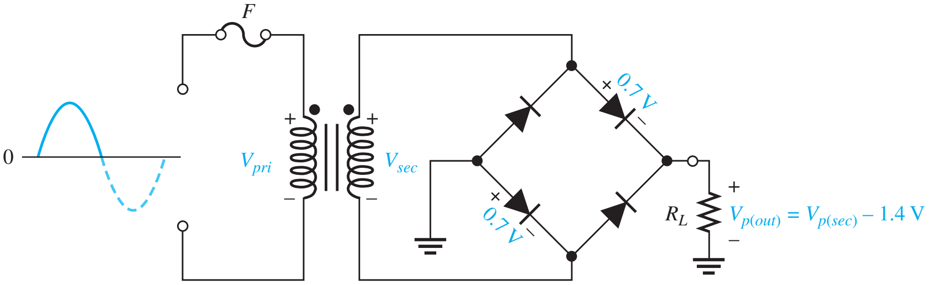
As you can see in Figure 2–39(b), two diodes are always in series with the load resistor during both the positive and negative half-cycles. If these diode drops are taken into account, the output voltage is

$$\boldsymbol{V_{p(out)} = V_{p(sec)} - 1.4\,\text{V}}$$

Equation 2–9


F
0
V_{pri}
V_{sec}
D_3
D_1
D_2
D_4
R_L
$V_{p(out)} = V_{p(sec)}$

(a) Ideal diodes


F
0
V_{pri}
V_{sec}
0.7 V
0.7 V
R_L
$V_{p(out)} = V_{p(sec)} - 1.4$ V

(b) Practical diodes (Diode drops included)

▲ FIGURE 2–39

Bridge operation during a positive half-cycle of the primary and secondary voltages.

Peak Inverse Voltage Let's assume that D_1 and D_2 are forward-biased and examine the reverse voltage across D_3 and D_4. Visualizing D_1 and D_2 as shorts (ideal model), as in Figure 2–40(a), you can see that D_3 and D_4 have a peak inverse voltage equal to the peak secondary voltage. Since the output voltage is *ideally* equal to the secondary voltage,

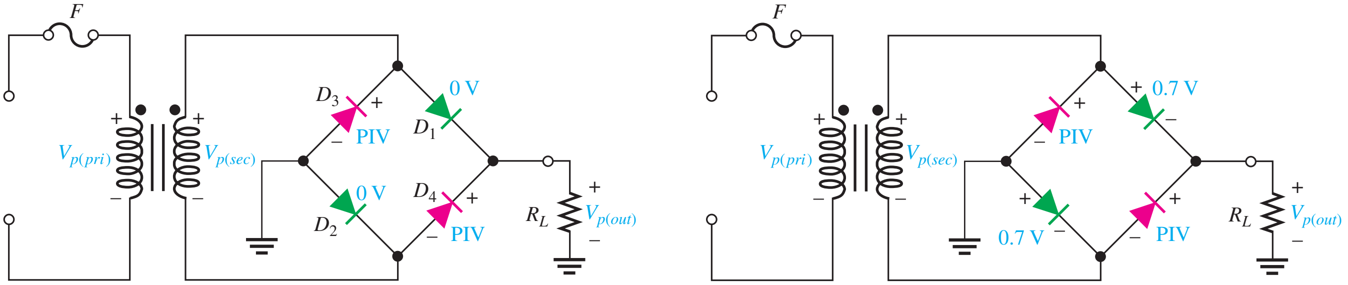
$$\text{PIV} = V_{p(out)}$$

If the diode drops of the forward-biased diodes are included as shown in Figure 2–40(b), the peak inverse voltage across each reverse-biased diode in terms of $V_{p(out)}$ is

Equation 2–10

$$\textbf{PIV} = \boldsymbol{V_{p(out)}} + \textbf{0.7 V}$$

The PIV rating of the bridge diodes is less than that required for the center-tapped configuration. If the diode drop is neglected, the bridge rectifier requires diodes with half the PIV rating of those in a center-tapped rectifier for the same output voltage.


F
$V_{p(pri)}$
$V_{p(sec)}$
D_3
PIV
0 V
D_1
0 V
D_4
D_2
PIV
R_L
$V_{p(out)}$
F
$V_{p(pri)}$
$V_{p(sec)}$
PIV
0.7 V
0.7 V
PIV
R_L
$V_{p(out)}$

(a) For the ideal diode model (forward-biased diodes D_1 and D_2 are shown in green), PIV = $V_{p(out)}$.

(b) For the practical diode model (forward-biased diodes D_1 and D_2 are shown in green), PIV = $V_{p(out)}$ + 0.7 V.

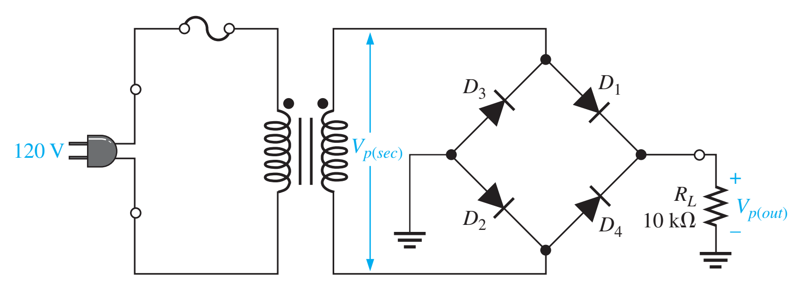
▲ FIGURE 2–40

Peak inverse voltages across diodes D_3 and D_4 in a bridge rectifier during the positive half-cycle of the secondary voltage.

EXAMPLE 2–7

Determine the peak output voltage for the bridge rectifier in Figure 2–41. Assuming the practical model, what PIV rating is required for the diodes? The transformer is specified to have a 12 V rms secondary voltage for the standard 120 V across the primary.

▶ FIGURE 2–41



Solution The peak output voltage (taking into account the two diode drops) is

$$V_{p(sec)} = 1.414V_{rms} = 1.414(12\text{ V}) \cong 17\text{ V}$$

$$V_{p(out)} = V_{p(sec)} - 1.4\text{ V} = 17\text{ V} - 1.4\text{ V} = \mathbf{15.6\text{ V}}$$

The PIV rating for each diode is

$$\text{PIV} = V_{p(out)} + 0.7\text{ V} = 15.6\text{ V} + 0.7\text{ V} = \mathbf{16.3\text{ V}}$$

Related Problem Determine the peak output voltage for the bridge rectifier in Figure 2–41 if the transformer produces an rms secondary voltage of 30 V. What is the PIV rating for the diodes?

Open the Multisim file E02-07 in the Examples folder on the companion website. Measure the output voltage and compare to the calculated value.

SECTION 2–5 CHECKUP

1. How does a full-wave voltage differ from a half-wave voltage?
2. What is the average value of a full-wave rectified voltage with a peak value of 60 V?
3. Which type of full-wave rectifier has the greater output voltage for the same input voltage and transformer turns ratio?
4. For a peak output voltage of 45 V, in which type of rectifier would you use diodes with a PIV rating of 50 V?
5. What PIV rating is required for diodes used in the type of rectifier that was not selected in Question 4?

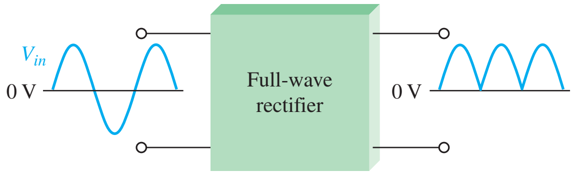
2–6 POWER SUPPLY FILTERS AND REGULATORS

A power supply filter ideally eliminates the fluctuations in the output voltage of a half-wave or full-wave rectifier and produces a constant-level dc voltage. Filtering is necessary because electronic circuits require a constant source of dc voltage and current to provide power and biasing for proper operation. Filters are implemented with capacitors, as you will see in this section. Voltage regulation in power supplies is usually done with integrated circuit voltage regulators. A voltage regulator prevents changes in the filtered dc voltage due to variations in input voltage or load.

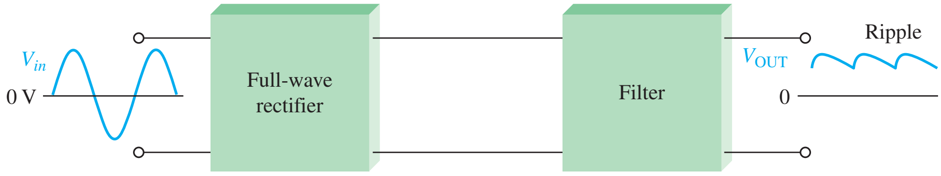
After completing this section, you should be able to

- **Explain and analyze power supply filters and regulators**
- Describe the operation of a capacitor-input filter
  - ◆ Define *ripple voltage* ◆ Calculate the ripple factor ◆ Calculate the output voltage of a filtered full-wave rectifier ◆ Discuss surge current
- Discuss voltage regulators
  - ◆ Calculate the line regulation ◆ Calculate the load regulation

In most power supply applications, the standard 60 Hz ac power line voltage must be converted to an approximately constant dc voltage. The 60 Hz pulsating dc output of a half-wave rectifier or the 120 Hz pulsating output of a full-wave rectifier must be filtered to reduce the large voltage variations. Figure 2–42 illustrates the filtering concept showing a nearly smooth dc output voltage from the filter. The small amount of fluctuation in the filter output voltage is called *ripple*.



(a) Rectifier without a filter



(b) Rectifier with a filter (output ripple is exaggerated)

▲ FIGURE 2–42

Power supply filtering.

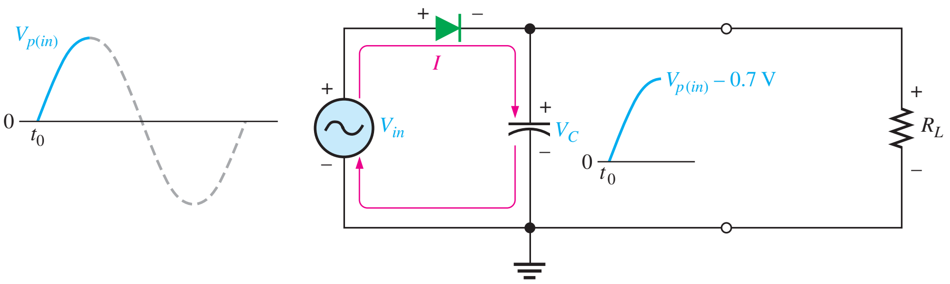
Capacitor-Input Filter

A half-wave rectifier with a capacitor-input filter is shown in Figure 2–43. The filter is simply a capacitor connected from the rectifier output to ground. R_L represents the equivalent resistance of a load. We will use the half-wave rectifier to illustrate the basic principle and then expand the concept to full-wave rectification.

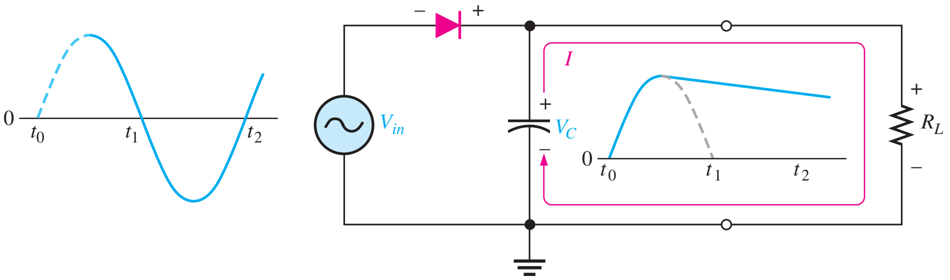
During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7 V of the input peak, as illustrated in Figure 2–43(a). When the input begins to decrease below its peak, as shown in part (b), the capacitor retains its charge and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only through the load resistance at a rate determined by the R_LC time constant, which is normally long compared to the period of the input. The larger the time constant, the less the capacitor will discharge. During the first quarter of the next cycle, as illustrated in part (c), the diode will again become forward-biased when the input voltage exceeds the capacitor voltage by approximately 0.7 V.

SAFETY NOTE

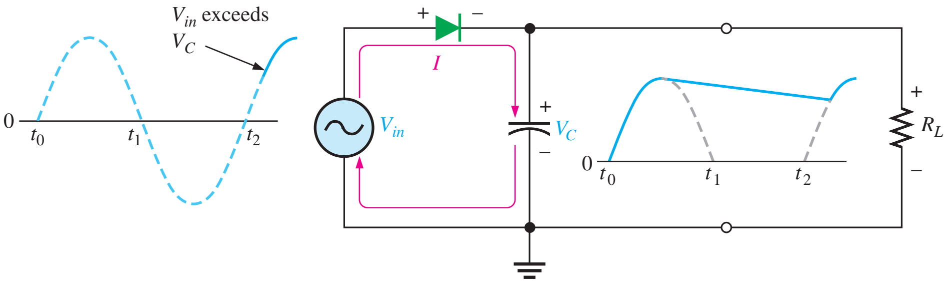
When installing polarized capacitors in a circuit, be sure to observe the proper polarity. The positive lead always connects to the more positive side of the circuit. An incorrectly connected polarized capacitor can explode.



(a) Initial charging of the capacitor (diode is forward-biased) happens only once when power is turned on.



(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid dark blue curve.

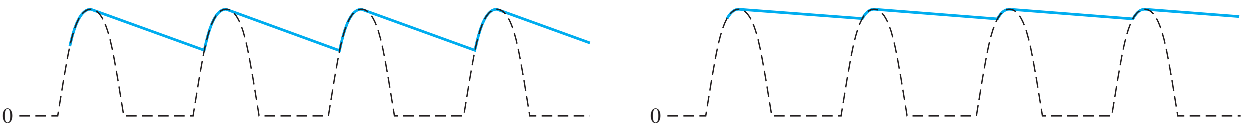


(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid dark blue curve.

▲ **FIGURE 2–43**

Operation of a half-wave rectifier with a capacitor-input filter. The current indicates charging or discharging of the capacitor.

Ripple Voltage As you have seen, the capacitor quickly charges at the beginning of a cycle and slowly discharges through R_L after the positive peak of the input voltage (when the diode is reverse-biased). The variation in the capacitor voltage due to the charging and discharging is called the **ripple voltage**. Generally, ripple is undesirable; thus, the smaller the ripple, the better the filtering action, as illustrated in Figure 2–44.



(a) Larger ripple (blue) means less effective filtering.

(b) Smaller ripple means more effective filtering. Generally, the larger the capacitor value, the smaller the ripple for the same input and load.

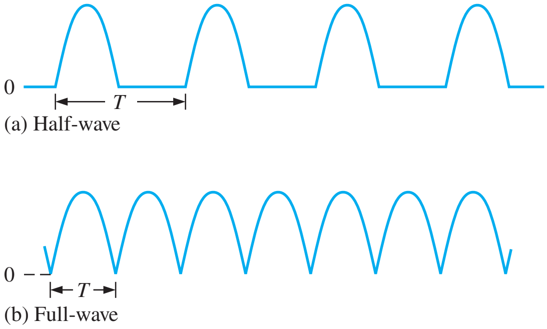
▲ **FIGURE 2–44**

Half-wave ripple voltage (blue line).

For a given input frequency, the output frequency of a full-wave rectifier is twice that of a half-wave rectifier, as illustrated in Figure 2–45. This makes a full-wave rectifier easier to filter because of the shorter time between peaks. When filtered, the full-wave rectified voltage has a smaller ripple than does a half-wave voltage for the same load resistance and capacitor values. The capacitor discharges less during the shorter interval between full-wave pulses, as shown in Figure 2–46.

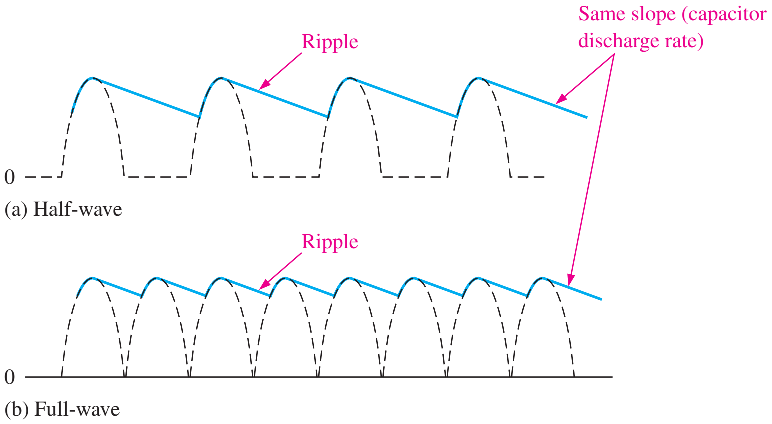
▶ FIGURE 2–45

The period of a full-wave rectified voltage is half that of a half-wave rectified voltage. The output frequency of a full-wave rectifier is twice that of a half-wave rectifier.



▶ FIGURE 2–46

Comparison of ripple voltages for half-wave and full-wave rectified voltages with the same filter capacitor and load and derived from the same sinusoidal input voltage.



Ripple Factor The **ripple factor (*r*)** is an indication of the effectiveness of the filter and is defined as

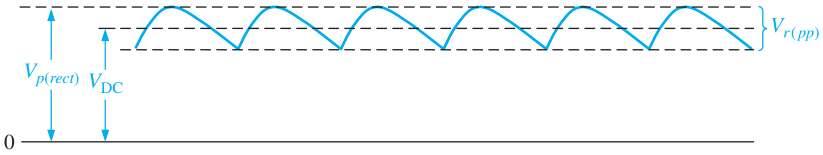
Equation 2–11

$$r = \frac{V_{r(pp)}}{V_{\mathrm{DC}}}$$

where $V_{r(pp)}$ is the peak-to-peak ripple voltage and V_{DC} is the dc (average) value of the filter's output voltage, as illustrated in Figure 2–47. The lower the ripple factor, the better the filter. The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load resistance.

▶ FIGURE 2–47

V_r and V_{DC} determine the ripple factor.



For a full-wave rectifier with a capacitor-input filter, approximations for the peak-to-peak ripple voltage, $V_{r(pp)}$, and the dc value of the filter output voltage, V_{DC}, are given in the following equations. The variable $V_{p(rect)}$ is the unfiltered peak rectified voltage. Notice that if R_L or C increases, the ripple voltage decreases and the dc voltage increases.

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)}$$ **Equation 2–12**

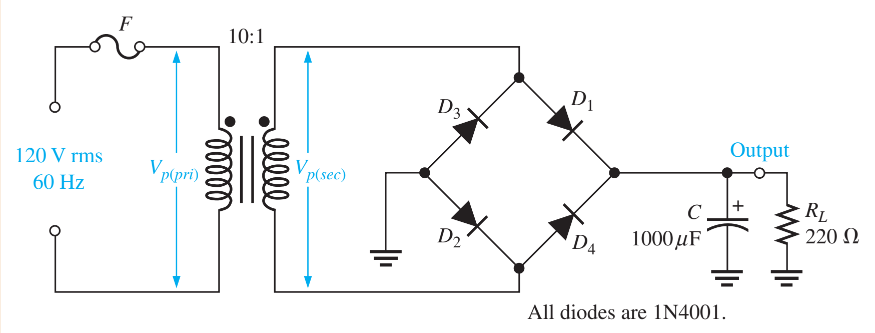
$$V_{\mathrm{DC}} \cong \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)}$$ **Equation 2–13**

The derivations for these equations can be found in “Derivations of Selected Equations” at www.pearsonhighered.com/floyd.

EXAMPLE 2–8

Determine the ripple factor for the filtered bridge rectifier with a load as indicated in Figure 2–48.

▶ **FIGURE 2–48**



All diodes are 1N4001.

Solution The transformer turns ratio is $n = 0.1$. The peak primary voltage is

$$V_{p(pri)} = 1.414V_{rms} = 1.414(120\text{ V}) = 170\text{ V}$$

The peak secondary voltage is

$$V_{p(sec)} = nV_{p(pri)} = 0.1(170\text{ V}) = 17.0\text{ V}$$

The unfiltered peak full-wave rectified voltage is

$$V_{p(rect)} = V_{p(sec)} - 1.4\text{ V} = 17.0\text{ V} - 1.4\text{ V} = 15.6\text{ V}$$

The frequency of a full-wave rectified voltage is 120 Hz. The approximate peak-to-peak ripple voltage at the output is

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)} = \left(\frac{1}{(120\text{ Hz})(220\ \Omega)(1000\ \mu\text{F})}\right)15.6\text{ V} = 0.591\text{ V}$$

The approximate dc value of the output voltage is determined as follows:

$$V_{\mathrm{DC}} = \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)} = \left(1 - \frac{1}{(240\text{ Hz})(220\ \Omega)(1000\ \mu\text{F})}\right)15.6\text{ V} = 15.3\text{ V}$$

The resulting ripple factor is

$$r = \frac{V_{r(pp)}}{V_{\mathrm{DC}}} = \frac{0.591\text{ V}}{15.3\text{ V}} = \mathbf{0.039}$$

The percent ripple is 3.9%.

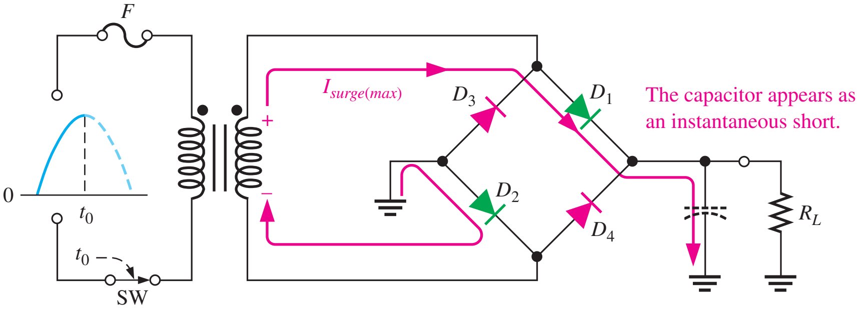
Related Problem Determine the peak-to-peak ripple voltage if the filter capacitor in Figure 2–48 is increased to 2200 μF and the load resistance changes to 2.2 kΩ.

Open the Multisim file E02-08 in the Examples folder on the companion website. For the specified input voltage, measure the peak-to-peak ripple voltage and the dc value at the output. Do the results agree closely with the calculated values? If not, can you explain why?

Surge Current in the Capacitor-Input Filter Before the switch in Figure 2–49 is closed, the filter capacitor is uncharged. At the instant the switch is closed, voltage is connected to the bridge and the uncharged capacitor appears as a short, as shown. This produces an initial surge of current, I_{surge}, through the two forward-biased diodes D_1 and D_2. The worst-case situation occurs when the switch is closed at a peak of the secondary voltage and a maximum surge current, $I_{surge(max)}$, is produced, as illustrated in the figure.

▶ FIGURE 2–49

Surge current in a capacitor-input filter.



The capacitor appears as an instantaneous short.

In dc power supplies, a **fuse** is always placed in the primary circuit of the transformer, as shown in Figure 2–49. A slow-blow type fuse is generally used because of the surge current that initially occurs when power is first turned on. The fuse rating is determined by calculating the power in the power supply load, which is the output power. Since $P_{in} = P_{out}$ in an ideal transformer, the primary current can be calculated as

$$I_{pri} = \frac{P_{in}}{120\text{ V}}$$

The fuse rating should be at least 20% larger than the calculated value of I_{pri}.

Voltage Regulators

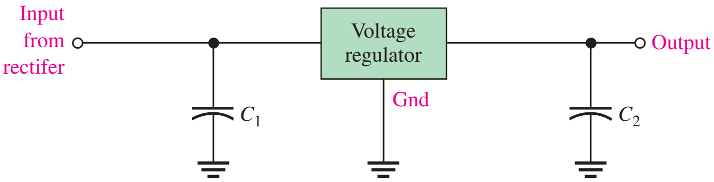
While filters can reduce the ripple from power supplies to a low value, the most effective approach is a combination of a capacitor-input filter used with a voltage regulator. A voltage regulator is connected to the output of a filtered rectifier and maintains a constant output voltage (or current) despite changes in the input, the load current, or the temperature. The capacitor-input filter reduces the input ripple to the regulator to an acceptable level. The combination of a large capacitor and a voltage regulator helps produce an excellent power supply.

Most regulators are integrated circuits and have three terminals—an input terminal, an output terminal, and a reference (or adjust) terminal. The input to the regulator is first filtered with a capacitor to reduce the ripple to <10%. The regulator reduces the ripple to a negligible amount. In addition, most regulators have an internal voltage reference, short-circuit protection, and thermal shutdown circuitry. They are available in a variety of voltages, including positive and negative outputs, and can be designed for variable outputs with a minimum of external components. Typically, voltage regulators can furnish a constant output of one or more amps of current with high ripple rejection.

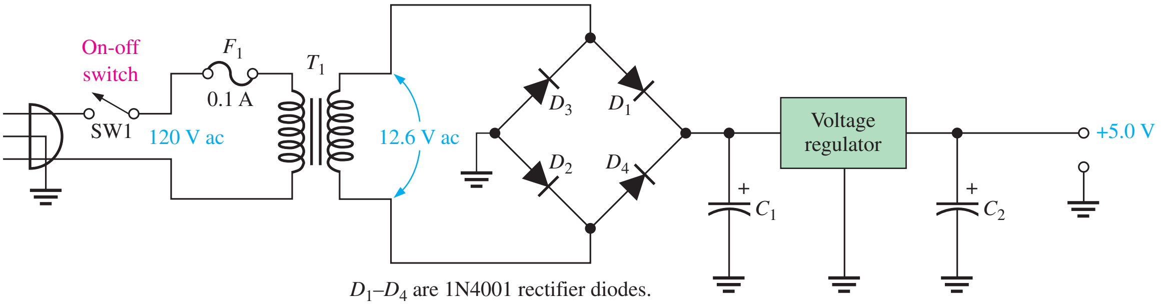
Three-terminal regulators designed for fixed output voltages require only external capacitors to complete the regulation portion of the power supply, as shown in Figure 2–50. Filtering is accomplished by a large-value capacitor between the input voltage and ground. An output capacitor (typically 0.1 μF to 1.0 μF) is connected from the output to ground to improve the transient response.

▶ FIGURE 2–50

A voltage regulator with input and output capacitors.



A basic fixed power supply with a +5 V voltage regulator is shown in Figure 2–51. Specific integrated circuit three-terminal regulators with fixed output voltages are covered in Chapter 17.



D_1–D_4 are 1N4001 rectifier diodes.

▲ **FIGURE 2–51**

A basic +5.0 V regulated power supply.

Percent Regulation

The regulation expressed as a percentage is a figure of merit used to specify the performance of a voltage regulator. It can be in terms of input (line) regulation or load regulation.

Line Regulation The **line regulation** specifies how much change occurs in the output voltage for a given change in the input voltage. It is typically defined as a ratio of a change in output voltage for a corresponding change in the input voltage expressed as a percentage.

$$\textbf{Line regulation} = \left(\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}\right)100\%$$

Equation 2–14

Load Regulation The **load regulation** specifies how much change occurs in the output voltage over a certain range of load current values, usually from minimum current (no load, NL) to maximum current (full load, FL). It is normally expressed as a percentage and can be calculated with the following formula:

$$\textbf{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}}\right)100\%$$

Equation 2–15

where V_{NL} is the output voltage with no load and V_{FL} is the output voltage with full (maximum) load.

EXAMPLE 2–9

A certain 7805 regulator has a measured no-load output voltage of 5.18 V and a full-load output of 5.15 V. What is the load regulation expressed as a percentage?

Solution

$$\text{Load regulation} = \left(\frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}}\right)100\% = \left(\frac{5.18\text{ V} - 5.15\text{ V}}{5.15\text{ V}}\right)100\% = \mathbf{0.58\%}$$

Related Problem

If the no-load output voltage of a regulator is 24.8 V and the full-load output is 23.9 V, what is the load regulation expressed as a percentage?

SECTION 2–6 CHECKUP

1. When a 60 Hz sinusoidal voltage is applied to the input of a half-wave rectifier, what is the output frequency?
2. When a 60 Hz sinusoidal voltage is applied to the input of a full-wave rectifier, what is the output frequency?

3. What causes the ripple voltage on the output of a capacitor-input filter?
4. If the load resistance connected to a filtered power supply is decreased, what happens to the ripple voltage?
5. Define *ripple factor.*
6. What is the difference between input (line) regulation and load regulation?

2–7 DIODE LIMITERS AND CLAMPERS

Diode circuits, called limiters or clippers, are sometimes used to clip off portions of signal voltages above or below certain levels. Another type of diode circuit, called a clamper, is used to add or restore a dc level to an electrical signal. Both limiter and clamper diode circuits will be examined in this section.

After completing this section, you should be able to

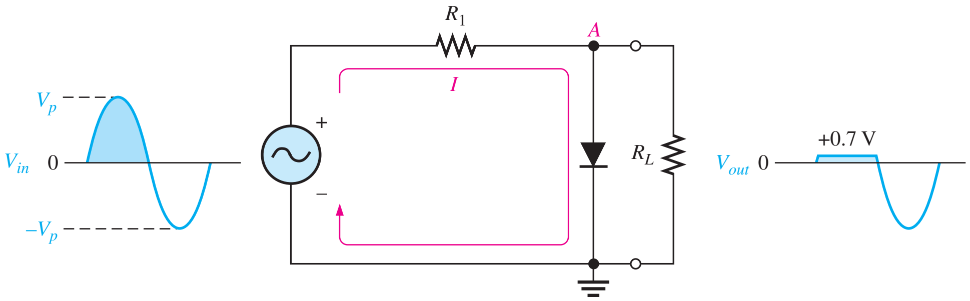
- ❑ **Explain and analyze the operation of diode limiters and clampers**
- ❑ Describe the operation of a diode limiter
  - ◆ Discuss biased limiters ◆ Discuss voltage-divider bias ◆ Describe an application
- ❑ Describe the operation of a diode clamper

Diode Limiters

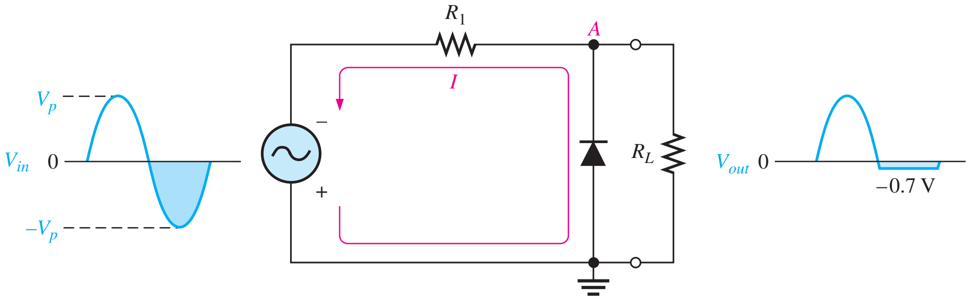
Figure 2–52(a) shows a diode positive **limiter** (also called **clipper**) that limits or clips the positive part of the input voltage. As the input voltage goes positive, the diode becomes forward-biased and conducts current. Point *A* is limited to +0.7 V when the input voltage exceeds this

▶ FIGURE 2–52

Examples of diode limiters (clippers).



(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V) and reverse-biased during the negative alternation.



(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below −0.7 V) and reverse-biased during the positive alternation.

value. When the input voltage goes back below 0.7 V, the diode is reverse-biased and appears as an open. The output voltage looks like the negative part of the input voltage, but with a magnitude determined by the voltage divider formed by R_1 and the load resistor, R_L, as follows:

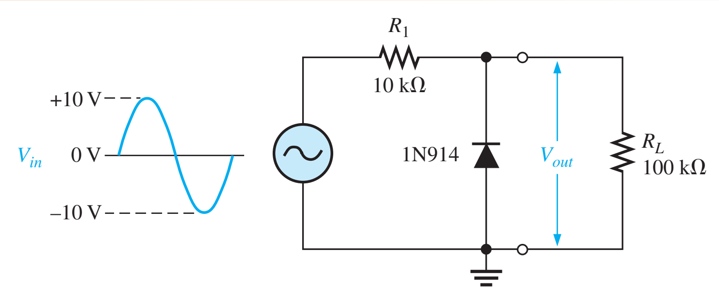
$$V_{out} = \left(\frac{R_L}{R_1 + R_L}\right)V_{in}$$

If R_1 is small compared to R_L, then $V_{out} \cong V_{in}$.

If the diode is turned around, as in Figure 2–52(b), the negative part of the input voltage is clipped off. When the diode is forward-biased during the negative part of the input voltage, point A is held at -0.7 V by the diode drop. When the input voltage goes above -0.7 V, the diode is no longer forward-biased; and a voltage appears across R_L proportional to the input voltage.

EXAMPLE 2–10

What would you expect to see displayed on an oscilloscope connected across R_L in the limiter shown in Figure 2–53?

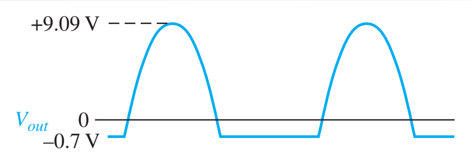


▶ FIGURE 2–53

Solution The diode is forward-biased and conducts when the input voltage goes below -0.7 V. So, for the negative limiter, determine the peak output voltage across R_L by the following equation:

$$V_{p(out)} = \left(\frac{R_L}{R_1 + R_L}\right)V_{p(in)} = \left(\frac{100\text{ k}\Omega}{110\text{ k}\Omega}\right)10\text{ V} = 9.09\text{ V}$$

The scope will display an output waveform as shown in Figure 2–54.



▶ FIGURE 2–54

Output voltage waveform for Figure 2–53.

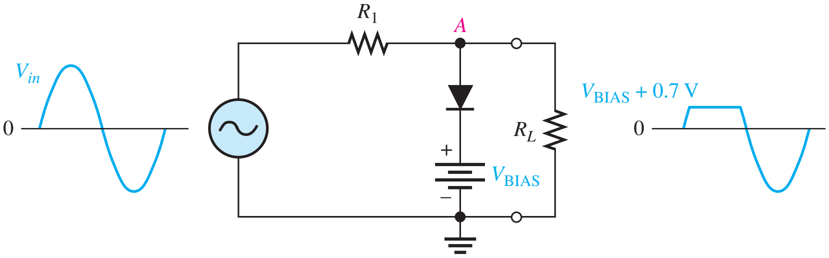
Related Problem Describe the output waveform for Figure 2–53 if R_1 is changed to 1 kΩ.

Open the Multisim file E02-10 in the Examples folder on the companion website. For the specified input, measure the resulting output waveform. Compare with the waveform shown in the example.

Biased Limiters The level to which an ac voltage is limited can be adjusted by adding a bias voltage, V_{BIAS}, in series with the diode, as shown in Figure 2–55. The voltage at point A must equal $V_{BIAS} + 0.7$ V before the diode will become forward-biased and conduct. Once the diode begins to conduct, the voltage at point A is limited to $V_{BIAS} + 0.7$ V so that all input voltage above this level is clipped off.

FIGURE 2–55

A positive limiter.

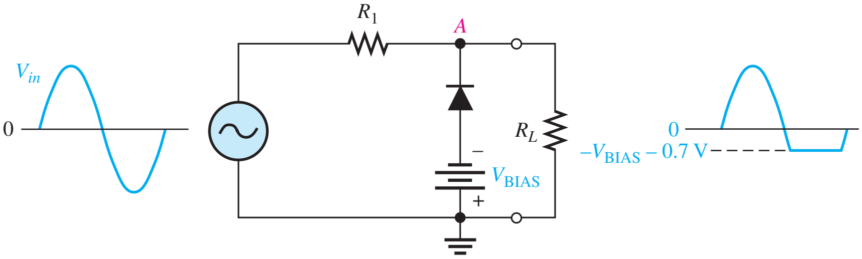


V_{in}
0
R_1
A
R_L
+
V_{BIAS}
−
$V_{BIAS} + 0.7$ V
0

To limit a voltage to a specified negative level, the diode and bias voltage must be connected as in Figure 2–56. In this case, the voltage at point A must go below $-V_{BIAS} - 0.7$ V to forward-bias the diode and initiate limiting action as shown.

FIGURE 2–56

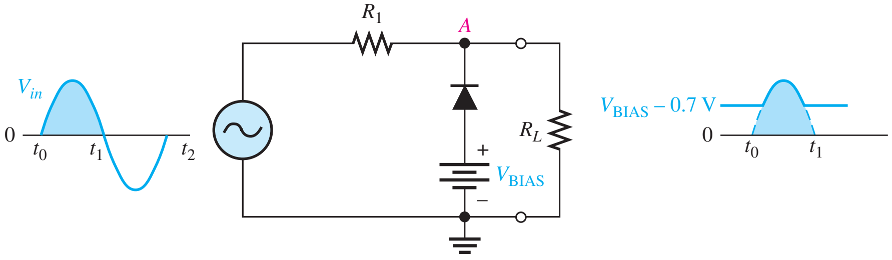
A negative limiter.



V_{in}
0
R_1
A
R_L
−
V_{BIAS}
+
0
$-V_{BIAS} - 0.7$ V

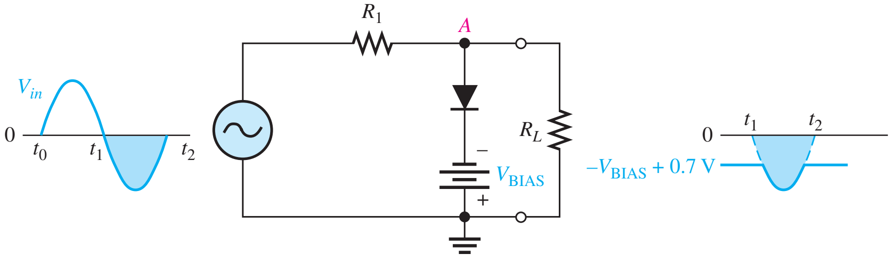
By turning the diode around, the positive limiter can be modified to limit the output voltage to the portion of the input voltage waveform above $V_{BIAS} - 0.7$ V, as shown by the output waveform in Figure 2–57(a). Similarly, the negative limiter can be modified to limit the output voltage to the portion of the input voltage waveform below $-V_{BIAS} + 0.7$ V, as shown by the output waveform in part (b).

FIGURE 2–57



V_{in}
0
t_0
t_1
t_2
R_1
A
R_L
+
V_{BIAS}
−
$V_{BIAS} - 0.7$ V
0
t_0
t_1

(a)



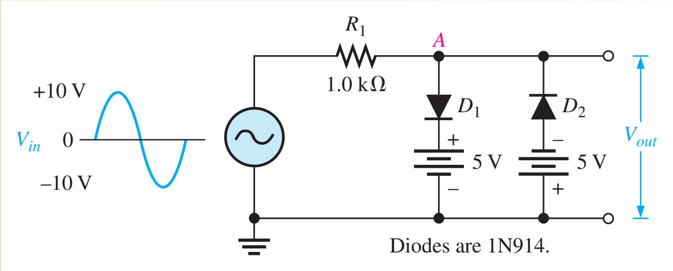
V_{in}
0
t_0
t_1
t_2
R_1
A
R_L
−
V_{BIAS}
+
0
t_1
t_2
$-V_{BIAS} + 0.7$ V

(b)

EXAMPLE 2–11

Figure 2–58 shows a circuit combining a positive limiter with a negative limiter. Determine the output voltage waveform.

▶ FIGURE 2–58

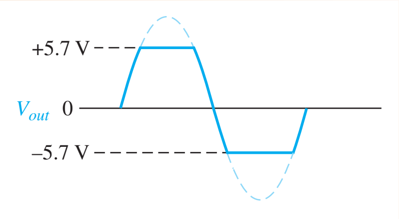


Diodes are 1N914.

Solution When the voltage at point A reaches +5.7 V, diode D_1 conducts and limits the waveform to +5.7 V. Diode D_2 does not conduct until the voltage reaches −5.7 V. Therefore, positive voltages above +5.7 V and negative voltages below −5.7 V are clipped off. The resulting output voltage waveform is shown in Figure 2–59.

▶ FIGURE 2–59

Output voltage waveform for Figure 2–58.



Related Problem Determine the output voltage waveform in Figure 2–58 if both dc sources are 10 V and the input voltage has a peak value of 20 V.

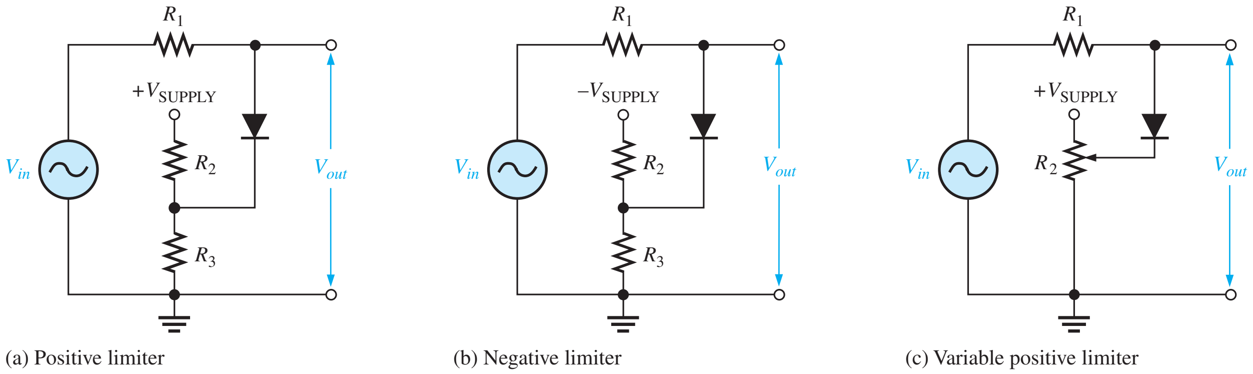
Open the Multisim file E02-11 in the Examples folder on the companion website. For the specified input, measure the resulting output waveform. Compare with the waveform shown in the example.

Voltage-Divider Bias The bias voltage sources that have been used to illustrate the basic operation of diode limiters can be replaced by a resistive voltage divider that derives the desired bias voltage from the dc supply voltage, as shown in Figure 2–60. The bias voltage is set by the resistor values according to the voltage-divider formula.

$$V_{\text{BIAS}} = \left(\frac{R_3}{R_2 + R_3}\right)V_{\text{SUPPLY}}$$

A positively biased limiter is shown in Figure 2–60(a), a negatively biased limiter is shown in part (b), and a variable positive bias circuit using a potentiometer voltage divider is shown in part (c). The bias resistors must be small compared to R_1 so that the forward current through the diode will not affect the bias voltage.

A Limiter Application Many circuits have certain restrictions on the input level to avoid damaging the circuit. For example, almost all digital circuits should not have an input level that exceeds the power supply voltage. An input of a few volts more than this could damage the circuit. To prevent the input from exceeding a specific level, you may see a diode limiter across the input signal path in many digital circuits.


R_1
$+V_{SUPPLY}$
R_2
R_3
V_{in}
V_{out}
(a) Positive limiter
$-V_{SUPPLY}$
(b) Negative limiter
(c) Variable positive limiter

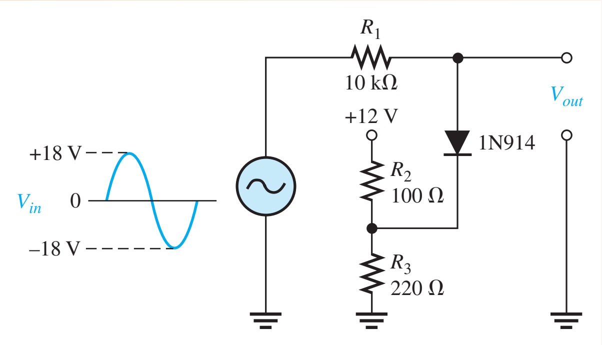
▲ FIGURE 2–60

Diode limiters implemented with voltage-divider bias.

EXAMPLE 2–12

Describe the output voltage waveform for the diode limiter in Figure 2–61.

▶ FIGURE 2–61

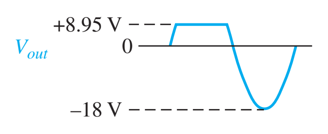

R_1
10 kΩ
+12 V
R_2
100 Ω
R_3
220 Ω
1N914
V_{out}
V_{in}
+18 V
0
−18 V

Solution The circuit is a positive limiter. Use the voltage-divider formula to determine the bias voltage.

$$V_{\text{BIAS}} = \left(\frac{R_3}{R_2 + R_3}\right)V_{\text{SUPPLY}} = \left(\frac{220\ \Omega}{100\ \Omega + 220\ \Omega}\right)12\text{ V} = 8.25\text{ V}$$

The output voltage waveform is shown in Figure 2–62. The positive part of the output voltage waveform is limited to $V_{\text{BIAS}} + 0.7$ V.

▶ FIGURE 2–62

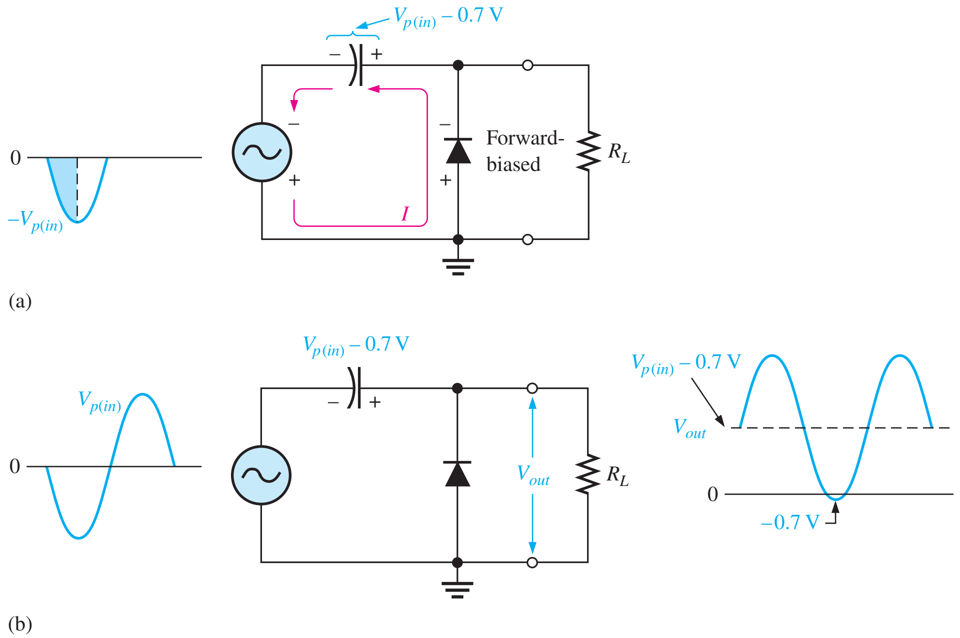


Related Problem How would you change the voltage divider in Figure 2–61 to limit the output voltage to +6.7 V?

Open the Multisim file E02-12 in the Examples folder on the companion website. Observe the output voltage on the oscilloscope and compare to the calculated result.

Diode Clampers

A clamper adds a dc level to an ac voltage. **Clampers** are sometimes known as *dc restorers*. Figure 2–63 shows a diode clamper that inserts a positive dc level in the output waveform. The operation of this circuit can be seen by considering the first negative half-cycle of the input voltage. When the input voltage initially goes negative, the diode is forward-biased, allowing the capacitor to charge to near the peak of the input ($V_{p(in)} - 0.7$ V), as shown in Figure 2–63(a). Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near $V_{p(in)} - 0.7$ V by the charge on the capacitor. The capacitor can only discharge through the high resistance of R_L. So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of R_L.



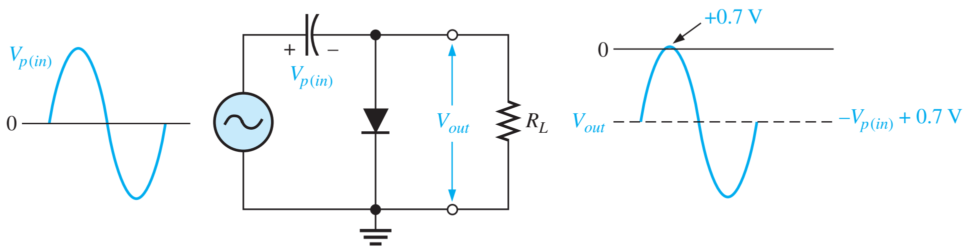
◀ FIGURE 2–63

Positive clamper operation.

If the capacitor discharges during the period of the input wave, clamping action is affected. If the *RC* time constant is 100 times the period, the clamping action is excellent. An *RC* time constant of ten times the period will have a small amount of distortion at the ground level due to the charging current.

The net effect of the clamping action is that the capacitor retains a charge approximately equal to the peak value of the input less the diode drop. The capacitor voltage acts essentially as a battery in series with the input voltage. The dc voltage of the capacitor adds to the input voltage by superposition, as in Figure 2–63(b).

If the diode is turned around, a negative dc voltage is added to the input voltage to produce the output voltage as shown in Figure 2–64.



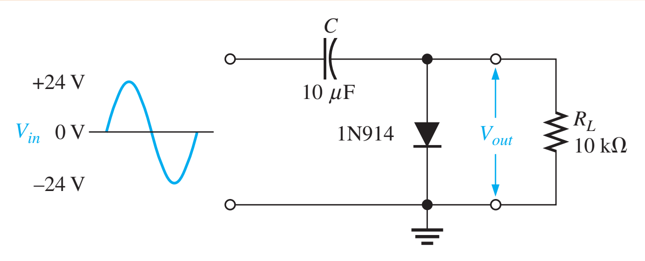
◀ FIGURE 2–64

Negative clamper.

EXAMPLE 2–13

What is the output voltage that you would expect to observe across R_L in the clamping circuit of Figure 2–65? Assume that RC is large enough to prevent significant capacitor discharge.

▶ FIGURE 2–65



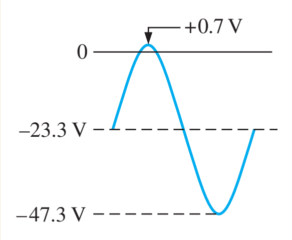
Solution Ideally, a negative dc value equal to the input peak less the diode drop is inserted by the clamping circuit.

$$V_{DC} \cong -(V_{p(in)} - 0.7\text{ V}) = -(24\text{ V} - 0.7\text{ V}) = \mathbf{-23.3\text{ V}}$$

Actually, the capacitor will discharge slightly between peaks, and, as a result, the output voltage will have an average value of slightly less than that calculated above. The output waveform goes to approximately +0.7 V, as shown in Figure 2–66.

▶ FIGURE 2–66

Output waveform across R_L for Figure 2–65.



Related Problem What is the output voltage that you would observe across R_L in Figure 2–65 for $C = 22\ \mu\text{F}$ and $R_L = 18\text{ k}\Omega$?

Open the Multisim file E02-13 in the Examples folder on the companion website. For the specified input, measure the output waveform. Compare with the waveform shown in the example.

SECTION 2–7 CHECKUP

1. Discuss how diode limiters and diode clampers differ in terms of their function.
2. What is the difference between a positive limiter and a negative limiter?
3. What is the maximum voltage across an unbiased positive silicon diode limiter during the positive alternation of the input voltage?
4. To limit the output voltage of a positive limiter to 5 V when a 10 V peak input is applied, what value must the bias voltage be?
5. What component in a clamping circuit effectively acts as a battery?

2–8 VOLTAGE MULTIPLIERS

Voltage multipliers use clamping action to increase peak rectified voltages without the necessity of increasing the transformer's voltage rating. Multiplication factors of two, three, and four are common. Voltage multipliers are used in high-voltage, low-current applications such as cathode-ray tubes (CRTs) and particle accelerators.

After completing this section, you should be able to

- **Explain and analyze the operation of diode voltage multipliers**
- Discuss voltage doublers
  - Explain the half-wave voltage doubler
  - Explain the full-wave voltage doubler
- Discuss voltage triplers
- Discuss voltage quadruplers

Voltage Doubler

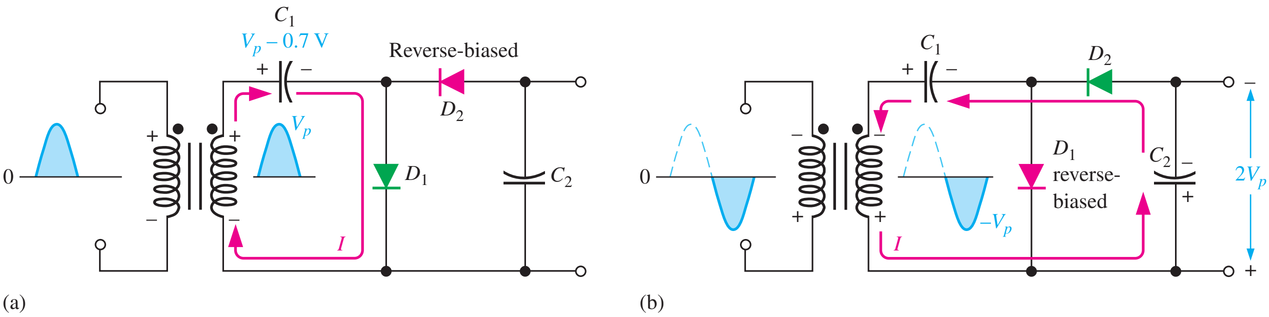
Half-Wave Voltage Doubler A voltage doubler is a **voltage multiplier** with a multiplication factor of two. A half-wave voltage doubler is shown in Figure 2–67. During the positive half-cycle of the secondary voltage, diode D_1 is forward-biased and D_2 is reverse-biased. Capacitor C_1 is charged to the peak of the secondary voltage (V_p) less the diode drop with the polarity shown in part (a). During the negative half-cycle, diode D_2 is forward-biased and D_1 is reverse-biased, as shown in part (b). Since C_1 can't discharge, the peak voltage on C_1 adds to the secondary voltage to charge C_2 to approximately $2V_p$. Applying Kirchhoff's law around the loop as shown in part (b), the voltage across C_2 is

$$V_{C1} - V_{C2} + V_p = 0$$

$$V_{C2} = V_p + V_{C1}$$

Neglecting the diode drop of D_2, $V_{C1} = V_p$. Therefore,

$$V_{C2} = V_p + V_p = 2V_p$$



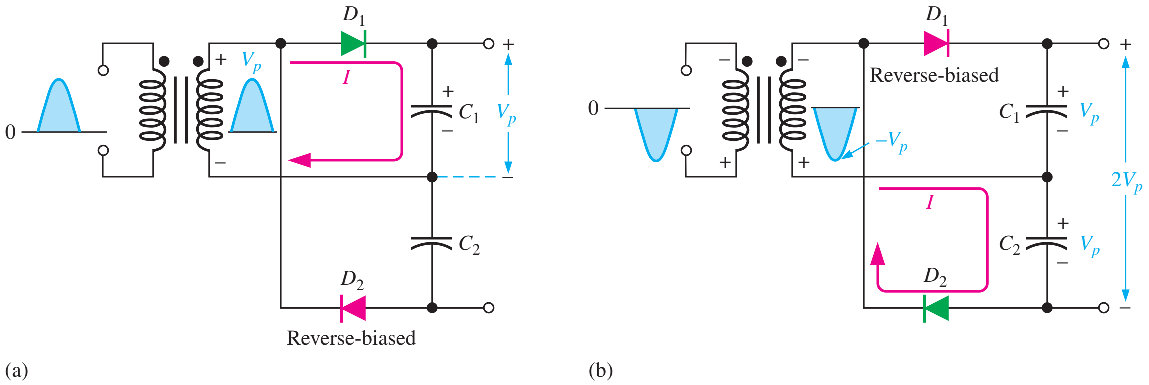
(a) (b)

▲ FIGURE 2–67

Half-wave voltage doubler operation. V_p is the peak secondary voltage.

Under a no-load condition, C_2 remains charged to approximately $2V_p$. If a load resistance is connected across the output, C_2 discharges slightly through the load on the next positive half-cycle and is again recharged to $2V_p$ on the following negative half-cycle. The resulting output is a half-wave, capacitor-filtered voltage. The peak inverse voltage across each diode is $2V_p$. If the diode were reversed, the output voltage across C_2 would have the opposite polarity.

Full-Wave Voltage Doubler A full-wave doubler is shown in Figure 2–68. When the secondary voltage is positive, D_1 is forward-biased and C_1 charges to approximately V_p, as shown in part (a). During the negative half-cycle, D_2 is forward-biased and C_2 charges to approximately V_p, as shown in part (b). The output voltage, $2V_p$, is taken across the two capacitors in series.



(a) (b)

▲ FIGURE 2–68

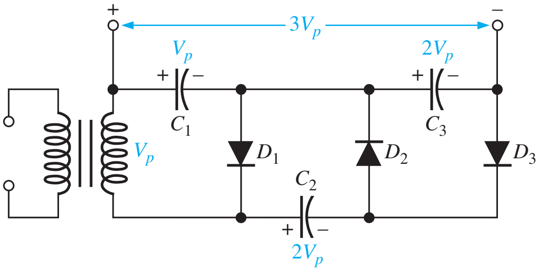
Full-wave voltage doubler operation.

Voltage Tripler

The addition of another diode-capacitor section to the half-wave voltage doubler creates a voltage tripler, as shown in Figure 2–69. The operation is as follows: On the positive half-cycle of the secondary voltage, C_1 charges to V_p through D_1. During the negative half-cycle, C_2 charges to $2V_p$ through D_2, as described for the doubler. During the next positive half-cycle, C_3 charges to $2V_p$ through D_3. The tripler output is taken across C_1 and C_3, as shown in the figure.

▶ FIGURE 2–69

Voltage tripler.

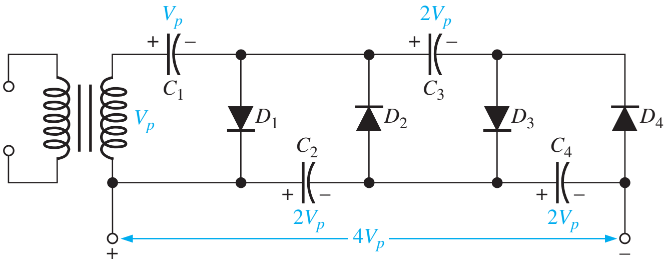


Voltage Quadrupler

The addition of still another diode-capacitor section, as shown in Figure 2–70, produces an output four times the peak secondary voltage. C_4 charges to $2V_p$ through D_4 on a negative half-cycle. The $4V_p$ output is taken across C_2 and C_4, as shown. In both the tripler and quadrupler circuits, the PIV of each diode is $2V_p$.

▶ FIGURE 2–70

Voltage quadrupler.



SECTION 2–8 CHECKUP

1. What must be the peak voltage rating of the transformer secondary for a voltage doubler that produces an output of 200 V?
2. The output voltage of a quadrupler is 620 V. What minimum PIV rating must each diode have?

2–9 THE DIODE DATASHEET

A manufacturer's datasheet gives detailed information on a device so that it can be used properly in a given application. A typical datasheet provides maximum ratings, electrical characteristics, mechanical data, and graphs of various parameters.

After completing this section, you should be able to

- **Interpret and use diode datasheets**
  - Define several absolute maximum ratings
  - Define diode thermal characteristics
  - Define several electrical characteristics
  - Interpret the forward current derating curve
  - Interpret the forward characteristic curve
  - Discuss nonrepetitive surge current
  - Discuss the reverse characteristics

Figure 2–71 shows a typical rectifier diode datasheet. The presentation of information on datasheets may vary from one manufacturer to another, but they basically all convey the same information. The mechanical information, such as package dimensions, are not shown on this particular datasheet but are generally available from the manufacturer. Notice on this datasheet that there are three categories of data given in table form and four types of characteristics shown in graphical form.

Data Categories

Absolute Maximum Ratings The absolute maximum ratings indicate the maximum values of the several parameters under which the diode can be operated without damage or degradation. For greatest reliability and longer life, the diode should be operated well under these maximums. Generally, the maximum ratings are specified for an operating ambient temperature (T_A) of 25°C unless otherwise stated. Ambient temperature is the temperature of the air surrounding the device. The parameters given in Figure 2–71 are as follows:

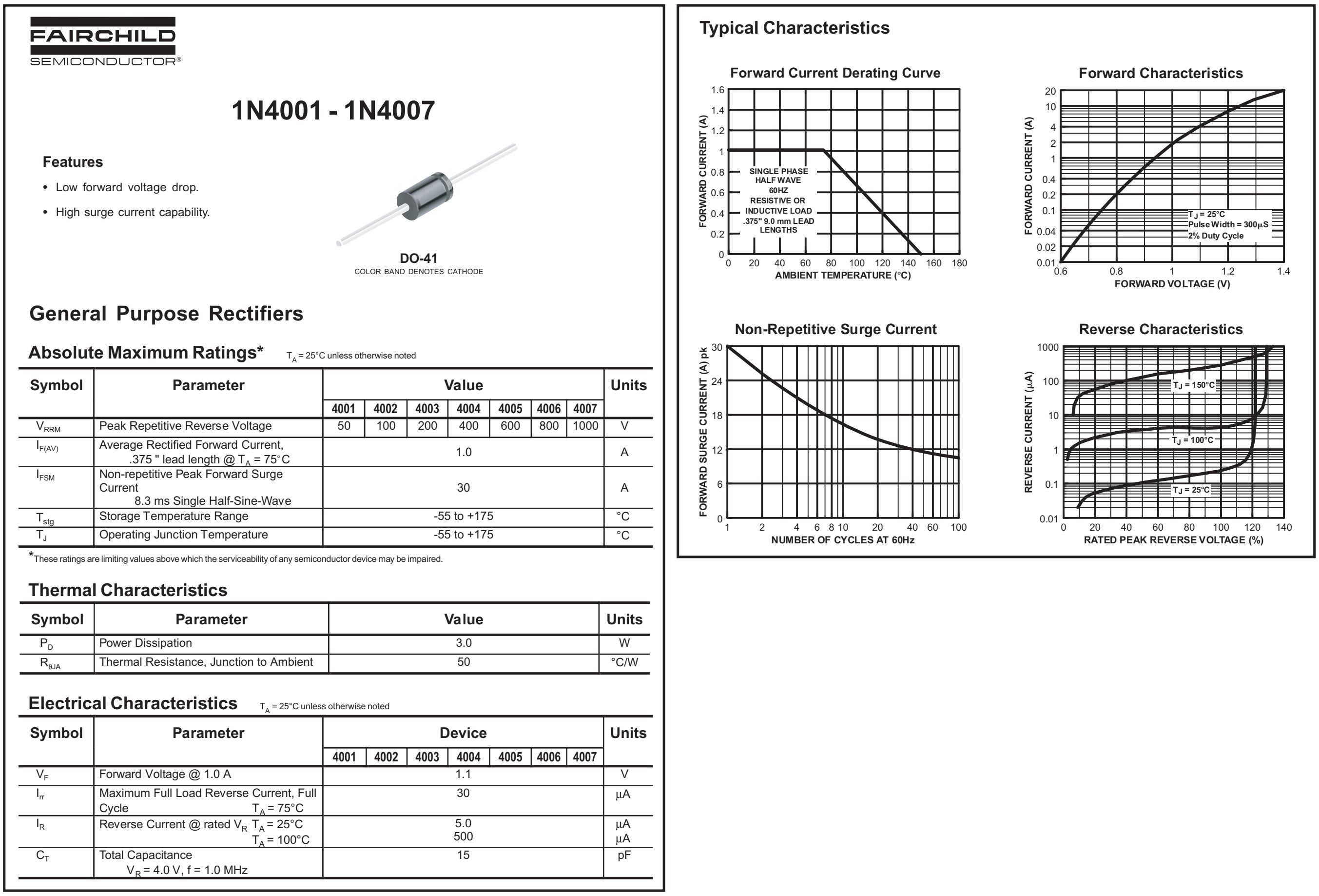
V_{RRM} The peak reverse voltage that can be applied repetitively across the diode. Notice that it is 50 V for the 1N4001 and 1000 V for the 1N4007. This rating is the same as the PIV.

$I_{F(AV)}$ The maximum average value of a 60 Hz half-wave rectified forward current. This current parameter is 1.0 A for all of the diode types and is specified for an ambient temperature of 75°C.

I_{FSM} The maximum peak value of nonrepetitive single half-sine-wave forward surge current with a duration of 8.3 ms. This current parameter is 30 A for all of the diode types.

T_{stg} The allowable range of temperatures at which the device can be kept when not operating or connected to a circuit.

T_J The allowable range of temperatures for the *pn* junction when the diode is operated in a circuit.



FAIRCHILD
SEMICONDUCTOR®

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers

Absolute Maximum Ratings* $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ $T_A = 75°C$	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle $T_A = 75°C$	30							µA
I_R	Reverse Current @ rated V_R $T_A = 25°C$ $T_A = 100°C$	5.0 500							µA µA
C_T	Total Capacitance $V_R = 4.0$ V, f = 1.0 MHz	15							pF

Typical Characteristics

Forward Current Derating Curve
FORWARD CURRENT (A)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
SINGLE PHASE
HALF WAVE
60HZ
RESISTIVE OR
INDUCTIVE LOAD
.375" 9.0 mm LEAD
LENGTHS
0 20 40 60 80 100 120 140 160 180
AMBIENT TEMPERATURE (°C)
Forward Characteristics
FORWARD CURRENT (A)
20
10
4
2
1
0.4
0.2
0.1
0.04
0.02
0.01
T J = 25°C
Pulse Width = 300µS
2% Duty Cycle
0.6 0.8 1 1.2 1.4
FORWARD VOLTAGE (V)
Non-Repetitive Surge Current
FORWARD SURGE CURRENT (A) pk
30
24
18
12
6
0
1 2 4 6 8 10 20 40 60 100
NUMBER OF CYCLES AT 60Hz
Reverse Characteristics
REVERSE CURRENT (µA)
1000
100
10
1
0.1
0.01
T J = 150°C
T J = 100°C
T J = 25°C
0 20 40 60 80 100 120 140
RATED PEAK REVERSE VOLTAGE (%)

▲ FIGURE 2–71

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Thermal Characteristics All devices have a limit on the amount of heat that they can tolerate without failing in some way.

P_D Average power dissipation is the amount of power that the diode can dissipate under any condition. A diode should never be operated at maximum power, except for brief periods, to assure reliability and longer life.

$R_{\theta JA}$ Thermal resistance from the diode junction to the surrounding air. This indicates the ability of the device material to resist the flow of heat and specifies the number of degrees difference between the junction and the surrounding air for each watt transferred from the junction to the air.

Electrical Characteristics The electrical characteristics are specified under certain conditions and are the same for each type of diode. These values are typical and can be more or less for a given diode. Some datasheets provide a minimum and a maximum value in addition to a typical value for a parameter.

V_F The forward voltage drop across the diode when there is 1 A of forward current. To determine the forward voltage for other values of forward current, you must examine the forward characteristics graph.

I_{rr} Maximum full load reverse current averaged over a full ac cycle at 75°C.

I_R The reverse current at the rated reverse voltage (V_{RRM}). Values are specified at two different ambient temperatures.

C_T This is the total diode capacitance including the junction capacitance in reverse bias at a frequency of 1 MHz. Most of the time this parameter is not important in low-frequency applications, such as power supply rectifiers.

Graphical Characteristics

The Forward Current Derating Curve This curve on the datasheet in Figure 2–71 shows maximum forward diode current $I_{F(AV)}$ in amps versus the ambient temperature. Up to about 75°C, the diode can handle a maximum of 1 A. Above 75°C, the diode cannot handle 1 A, so the maximum current must be derated as shown by the curve. For example, if a diode is operating in an ambient temperature of 120°C, it can handle only a maximum of 0.4 A, as shown in Figure 2–72.

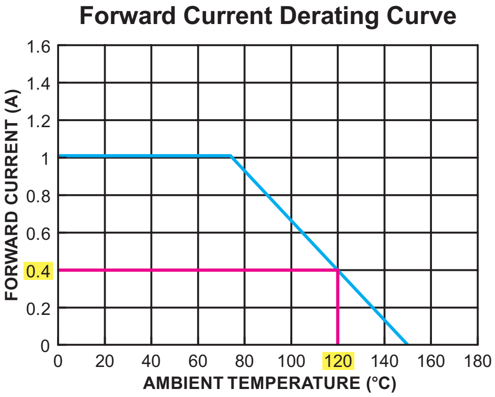


FIGURE 2–72

Forward Characteristics Curve Another graph from the datasheet shows instantaneous forward current as a function of instantaneous forward voltage. As indicated, data for this curve is derived by applying 300 μs pulses with a duty cycle of 2%. Notice that this graph is for $T_J = 25$°C. For example, a forward current of 1 A corresponds to a forward voltage of about 0.93 V, as shown in Figure 2–73.

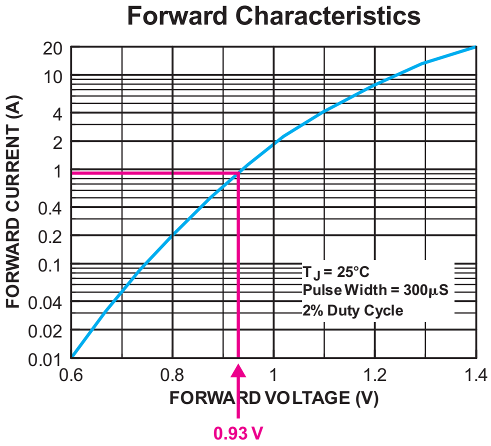
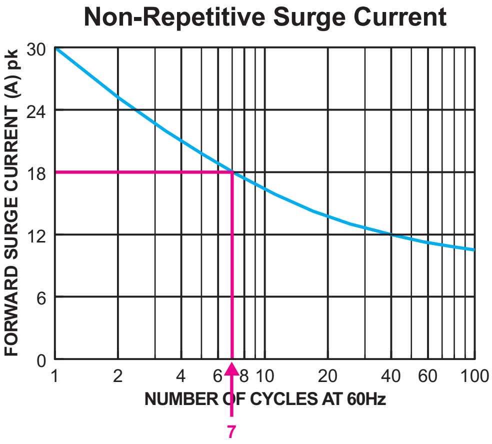


FIGURE 2–73

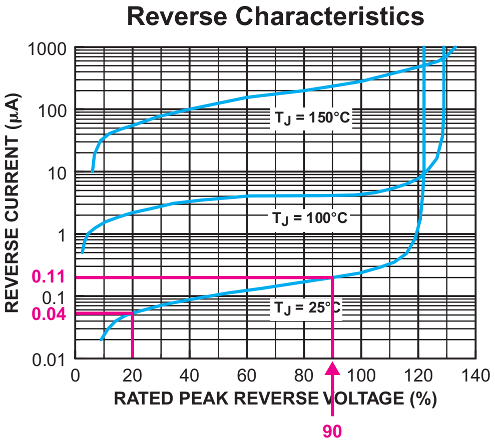
Nonrepetitive Surge Current This graph from the datasheet shows I_{FSM} as a function of the number of cycles at 60 Hz. For a one-time surge, the diode can withstand 30 A. However, if the surges are repeated at a frequency of 60 Hz, the maximum surge current decreases. For example, if the surge is repeated 7 times, the maximum current is 18 A, as shown in Figure 2–74.

FIGURE 2–74



Reverse Characteristics This graph from the datasheet shows how the reverse current varies with the reverse voltage for three different junction temperatures. The horizontal axis is the percentage of maximum reverse voltage, V_{RRM}. For example, at 25°C, a 1N4001 has a reverse current of approximately 0.04 μA at 20% of its maximum V_{RRM} or 10 V. If the V_{RRM} is increased to 90%, the reverse current increases to approximately 0.11 μA, as shown in Figure 2–75.

FIGURE 2–75



SECTION 2–9 CHECKUP

1. Determine the peak repetitive reverse voltage for each of the following diodes: 1N4002, 1N4003, 1N4004, 1N4005, 1N4006.
2. If the forward current is 800 mA and the forward voltage is 0.75 V in a 1N4005, is the power rating exceeded?
3. What is $I_{F(AV)}$ for a 1N4001 at an ambient temperature of 100°C?
4. What is I_{FSM} for a 1N4003 if the surge is repeated 40 times at 60 Hz?

2–10 TROUBLESHOOTING

This section provides a general overview and application of an approach to troubleshooting. Specific troubleshooting examples of the power supply and diode circuits are covered.

After completing this section, you should be able to

- **Troubleshoot diodes and power supply circuits**
- Test a diode with a DMM
  - Use the diode test position
  - Determine if the diode is good or bad
  - Use the Ohms function to check a diode
- Troubleshoot a dc power supply by analysis, planning, and measurement
  - Use the half-splitting method
- Perform fault analysis
  - Isolate fault to a single component

Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

Testing a Diode

A multimeter can be used as a fast and simple way to check a diode out of the circuit. A good diode will show an extremely high resistance (ideally an open) with reverse bias and a very low resistance with forward bias. A defective open diode will show an extremely high resistance (or open) for both forward and reverse bias. A defective shorted or resistive diode will show zero or a low resistance for both forward and reverse bias. An open diode is the most common type of failure.

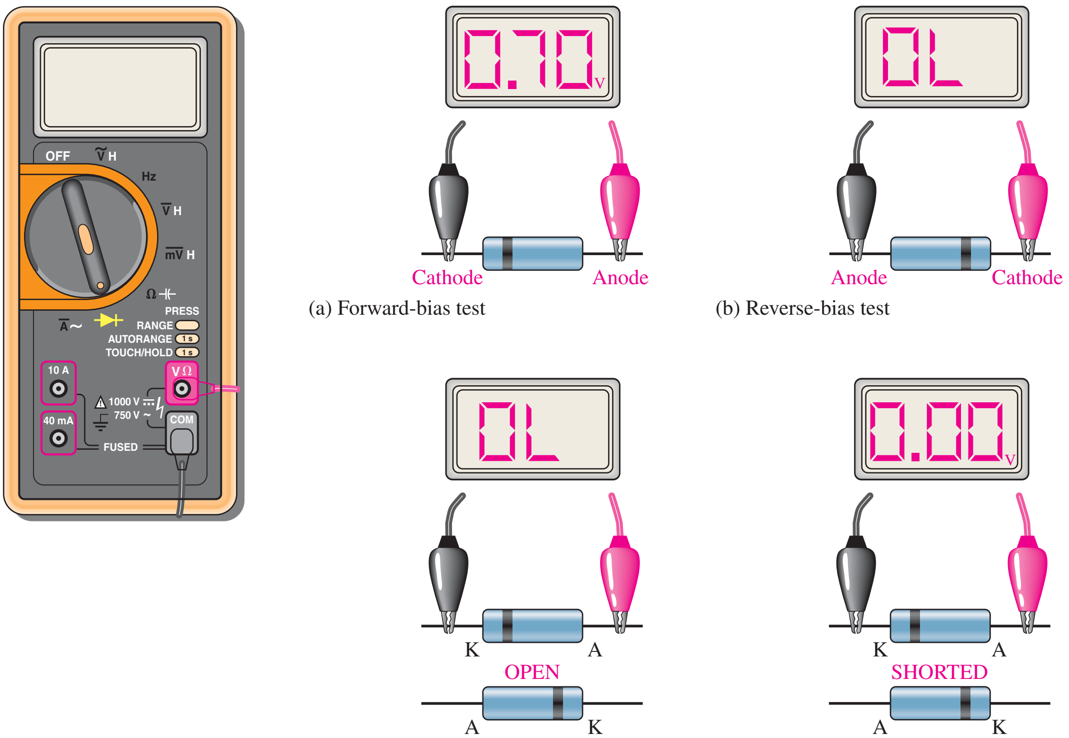
The DMM Diode Test Position Many digital multimeters (DMMs) have a diode test function that provides a convenient way to test a diode. A typical DMM, as shown in Figure 2–76, has a small diode symbol to mark the position of the function switch. When set to *diode test*, the meter provides an internal voltage sufficient to forward-bias and reverse-bias a diode. This internal voltage may vary among different makes of DMM, but 2.5 V to 3.5 V is a typical range of values. The meter provides a voltage reading or other indication to show the condition of the diode under test.

When the Diode Is Working In Figure 2–76(a), the red (positive) lead of the meter is connected to the anode and the black (negative) lead is connected to the cathode to forward-bias the diode. If the diode is good, you will get a reading of between approximately 0.5 V and 0.9 V, with 0.7 V being typical for forward bias.

In Figure 2–76(b), the diode is turned around for reverse bias as shown. If the diode is working properly, you will typically get a reading of "OL". Some DMMs may display the internal voltage for a reverse-bias condition.

When the Diode Is Defective When a diode has failed open, you get an out-of-range "OL" indication for both the forward-bias and the reverse-bias conditions, as illustrated in Figure 2–76(c). If a diode is shorted, the meter reads 0 V in both forward- and reverse-bias tests, as indicated in part (d).

Checking a Diode with the OHMs Function DMMs that do not have a diode test position can be used to check a diode by setting the function switch on an OHMs range. For a forward-bias check of a good diode, you will get a resistance reading that can vary depending on the meter's internal battery. Many meters do not have sufficient voltage on the OHMs setting to fully forward-bias a diode and you may get a reading of from several hundred to several thousand ohms. For the reverse-bias check of a good diode, you will get an



(a) Forward-bias test

(b) Reverse-bias test

(c) Forward- and reverse-bias tests for an open diode give the same indication.

(d) Forward- and reverse-bias tests for a shorted diode give the same 0 V reading.

▲ **FIGURE 2–76**

Testing a diode out-of-circuit with a DMM.

out-of-range indication such as “OL” on most DMMs because the reverse resistance is too high for the meter to measure.

Even though you may not get accurate forward- and reverse-resistance readings on a DMM, the relative readings indicate that a diode is functioning properly, and that is usually all you need to know. The out-of-range indication shows that the reverse resistance is extremely high, as you expect. The reading of a few hundred to a few thousand ohms for forward bias is relatively small compared to the reverse resistance, indicating that the diode is working properly. The actual resistance of a forward-biased diode is typically much less than 100 Ω.

Troubleshooting a Power Supply

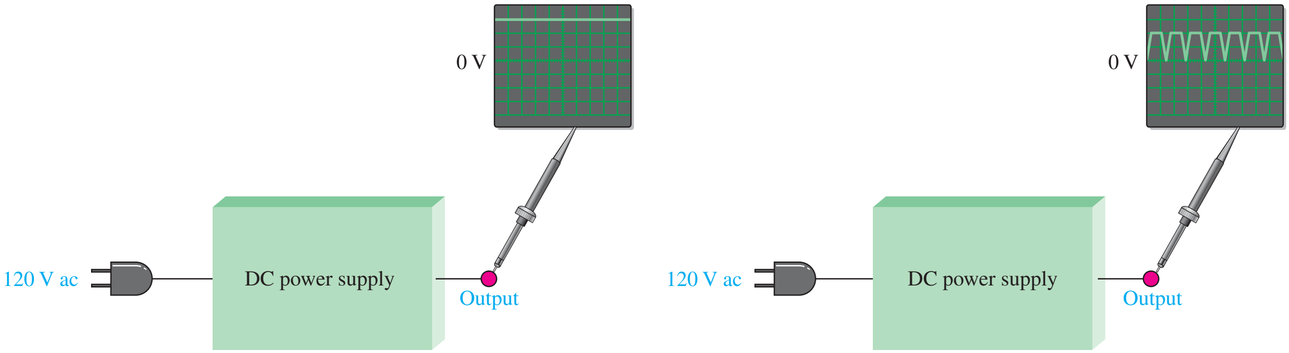
Troubleshooting is the application of logical thinking combined with a thorough knowledge of circuit or system operation to identify and correct a malfunction. A systematic approach to troubleshooting consists of three steps: *analysis, planning,* and *measuring.*

A defective circuit or system is one with a known good input but with no output or an incorrect output. For example, in Figure 2–77(a), a properly functioning dc power supply is represented by a single block with a known input voltage and a correct output voltage. A defective dc power supply is represented in part (b) as a block with an input voltage and an incorrect output voltage.

Analysis The first step in troubleshooting a defective circuit or system is to analyze the problem, which includes identifying the symptom and eliminating as many causes as possible. In the case of the power supply example illustrated in Figure 2–77(b), the symptom is that the output voltage is not a constant regulated dc voltage. This symptom does not tell you much about what the specific cause may be. In other situations, however, a particular symptom may point to a given area where a fault is most likely.

SAFETY NOTE

When working with low-voltage power supplies, be careful not to come in contact with the 120 V ac line. Severe shock or worse could result. To verify input voltage to a rectifier, it is always better to check at the transformer secondary instead of trying to measure the line voltage directly. If it becomes necessary to measure the line voltage, use a multimeter and be careful.



(a) The correct dc output voltage is measured with oscilloscope.

(b) An incorrect voltage is measured at the output with oscilloscope.

▲ FIGURE 2–77

Block representations of functioning and nonfunctioning power supplies.

The first thing you should do in analyzing the problem is to try to eliminate any obvious causes. In general, you should start by making sure the power cord is plugged into an active outlet and that the fuse is not blown. In the case of a battery-powered system, make sure the battery is good. Something as simple as this is sometimes the cause of a problem. However, in this case, there must be power because there is an output voltage.

Beyond the power check, use your senses to detect obvious defects, such as a burned resistor, broken wire, loose connection, or an open fuse. Since some failures are temperature dependent, you can sometimes find an overheated component by touch. However, be very cautious in a live circuit to avoid possible burn or shock. For intermittent failures, the circuit may work properly for awhile and then fail due to heat buildup. As a rule, you should always do a sensory check as part of the analysis phase before proceeding.

Planning In this phase, you must consider how you will attack the problem. There are three possible approaches to troubleshooting most circuits or systems.

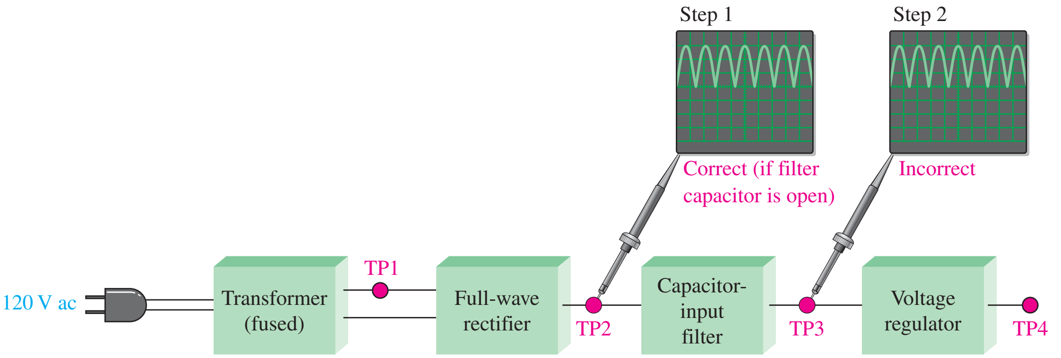
1. Start at the input (the transformer secondary in the case of a dc power supply) where there is a known input voltage and work toward the output until you get an incorrect measurement. When you find no voltage or an incorrect voltage, you have narrowed the problem to the part of the circuit between the last test point where the voltage was good and the present test point. In all troubleshooting approaches, you must know what the voltage is supposed to be at each point in order to recognize an incorrect measurement when you see it.

2. Start at the output of a circuit and work toward the input. Check for voltage at each test point until you get a correct measurement. At this point, you have isolated the problem to the part of the circuit between the last test point and the current test point where the voltage is correct.

3. Use the half-splitting method and start in the middle of the circuit. If this measurement shows a correct voltage, you know that the circuit is working properly from the input to that test point. This means that the fault is between the current test point and the output point, so begin tracing the voltage from that point toward the output. If the measurement in the middle of the circuit shows no voltage or an incorrect voltage, you know that the fault is between the input and that test point. Therefore, begin tracing the voltage from the test point toward the input.

For illustration, let's say that you decide to apply the half-splitting method using an oscilloscope.

Measurement The half-splitting method is illustrated in Figure 2–78 with the measurements indicating a particular fault (open filter capacitor in this case). At test point 2 (TP2) you observe a full-wave rectified voltage that indicates that the transformer and rectifier

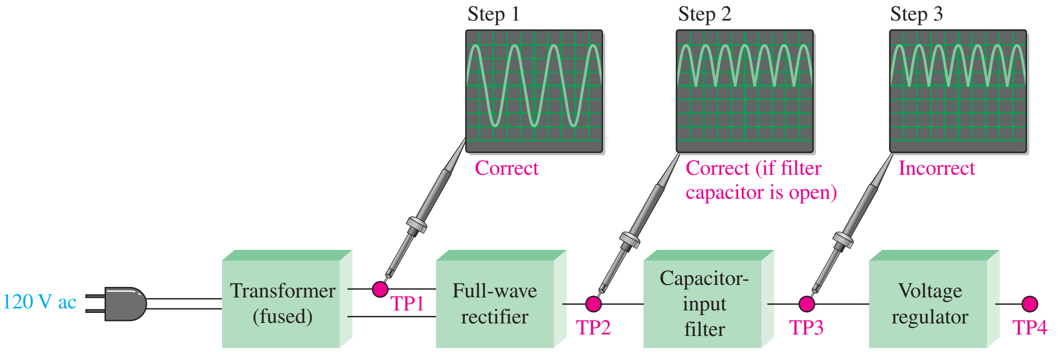

Step 1
Step 2
Correct (if filter capacitor is open)
Incorrect
120 V ac
Transformer (fused)
TP1
Full-wave rectifier
TP2
Capacitor-input filter
TP3
Voltage regulator
TP4

▲ FIGURE 2–78

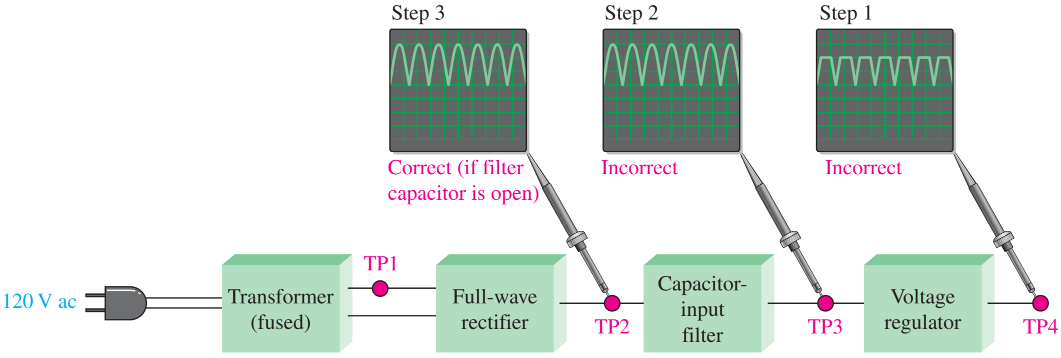
Example of the half-splitting approach. An open filter capacitor is indicated.

are working properly. This measurement also indicates that the filter capacitor is open, which is verified by the full-wave voltage at TP3. If the filter were working properly, you would measure a dc voltage at both TP2 and TP3. If the filter capacitor were shorted, you would observe no voltage at all of the test points because the fuse would most likely be blown. A short anywhere in the system is very difficult to isolate because, if the system is properly fused, the fuse will blow immediately when a short to ground develops.

For the case illustrated in Figure 2–78, the half-splitting method took two measurements to isolate the fault to the open filter capacitor. If you had started from the transformer output, it would have taken three measurements; and if you had started at the final output, it would have also taken three measurements, as illustrated in Figure 2–79.


Step 1
Step 2
Step 3
Correct
Correct (if filter capacitor is open)
Incorrect
120 V ac
Transformer (fused)
TP1
Full-wave rectifier
TP2
Capacitor-input filter
TP3
Voltage regulator
TP4

(a) Measurements starting at the transformer output


Step 3
Step 2
Step 1
Correct (if filter capacitor is open)
Incorrect
Incorrect
120 V ac
TP1
Transformer (fused)
Full-wave rectifier
TP2
Capacitor-input filter
TP3
Voltage regulator
TP4

(b) Measurements starting at the regulator output

▲ FIGURE 2–79

In this particular case, the two other approaches require more oscilloscope measurements than the half-splitting approach in Figure 2–78.

Fault Analysis

In some cases, after isolating a fault to a particular circuit, it may be necessary to isolate the problem to a single component in the circuit. In this event, you have to apply logical thinking and your knowledge of the symptoms caused by certain component failures. Some typical component failures and the symptoms they produce are now discussed.

Effect of an Open Diode in a Half-Wave Rectifier A half-wave filtered rectifier with an open diode is shown in Figure 2–80. The resulting symptom is zero output voltage as indicated. This is obvious because the open diode breaks the current path from the transformer secondary winding to the filter and load resistor and there is no load current.

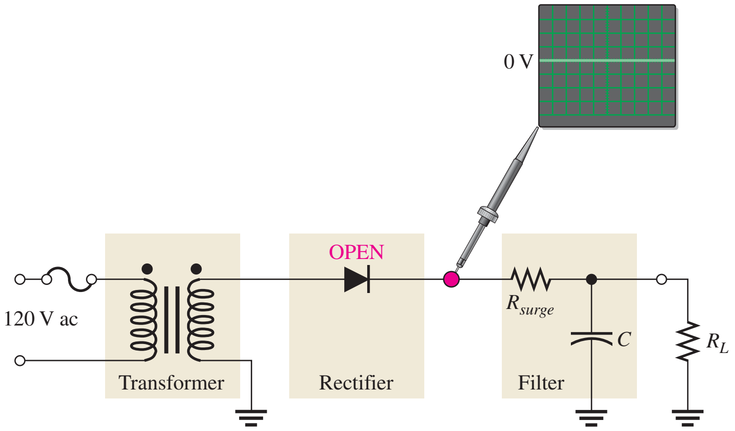

0 V
OPEN
120 V ac
Transformer
Rectifier
R_{surge}
C
R_L
Filter

FIGURE 2–80

The effect of an open diode in a half-wave rectifier is an output of 0 V.

Other faults that will cause the same symptom in this circuit are an open transformer winding, an open fuse, or no input voltage.

Effect of an Open Diode in a Full-Wave Rectifier A full-wave center-tapped filtered rectifier is shown in Figure 2–81. If either of the two diodes is open, the output voltage will have twice the normal ripple voltage at 60 Hz rather than at 120 Hz, as indicated.

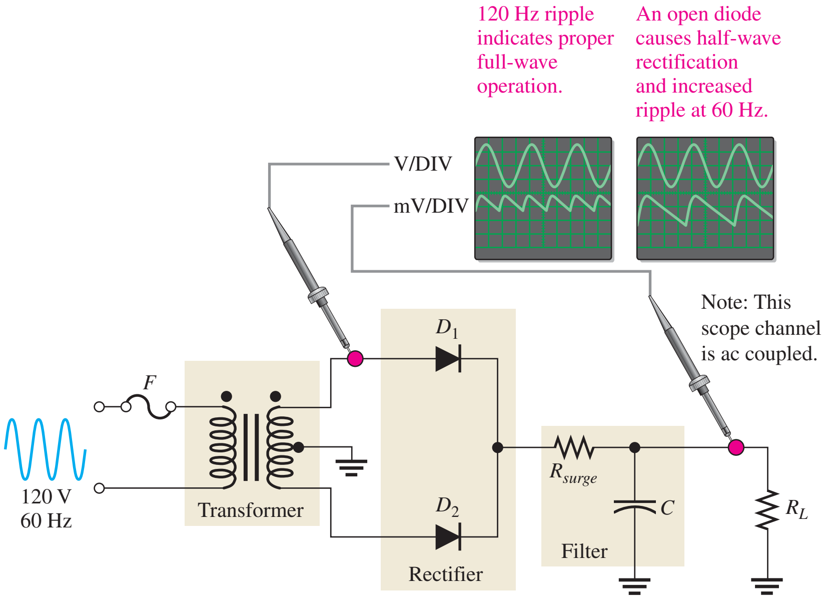

120 Hz ripple indicates proper full-wave operation.
An open diode causes half-wave rectification and increased ripple at 60 Hz.
V/DIV
mV/DIV
Note: This scope channel is ac coupled.
D_1
D_2
F
120 V
60 Hz
Transformer
Rectifier
R_{surge}
C
R_L
Filter

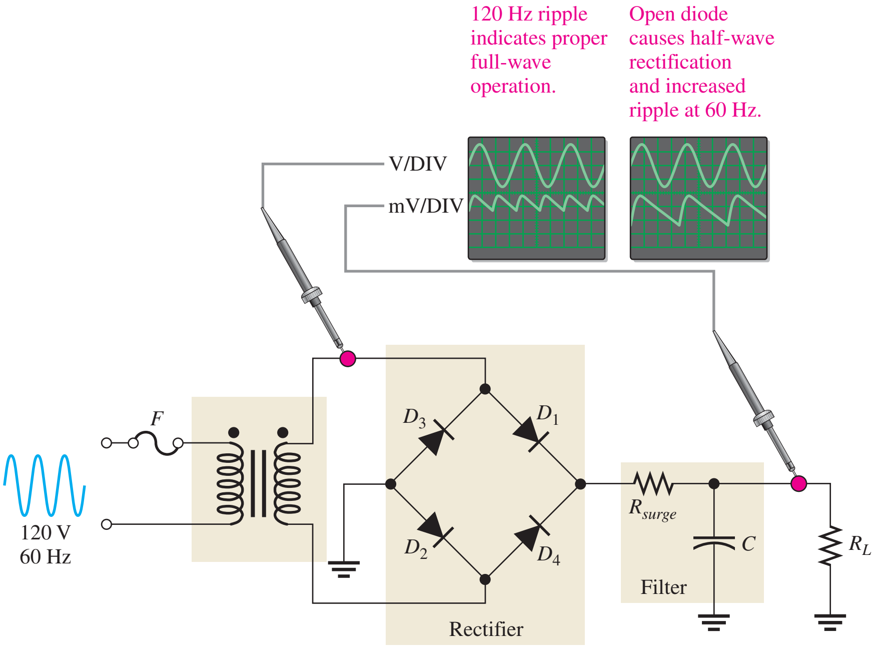
FIGURE 2–81

The effect of an open diode in a center-tapped rectifier is half-wave rectification and twice the ripple voltage at 60 Hz.

Another fault that will cause the same symptom is an open in the transformer secondary winding.

The reason for the increased ripple at 60 Hz rather than at 120 Hz is as follows. If one of the diodes in Figure 2–81 is open, there is current through R_L only during one half-cycle of the input voltage. During the other half-cycle of the input, the open path caused by the open diode prevents current through R_L. The result is half-wave rectification, as shown in Figure 2–81, which produces the larger ripple voltage with a frequency of 60 Hz.

An open diode in a full-wave bridge rectifier will produce the same symptom as in the center-tapped circuit, as shown in Figure 2–82. The open diode prevents current through R_L during half of the input voltage cycle. The result is half-wave rectification, which produces double the ripple voltage at 60 Hz.


120 Hz ripple indicates proper full-wave operation.
Open diode causes half-wave rectification and increased ripple at 60 Hz.
V/DIV
mV/DIV
F
120 V
60 Hz
D3
D1
D2
D4
Rectifier
Rsurge
C
Filter
RL

▲ FIGURE 2–82

Effect of an open diode in a bridge rectifier.

Effects of a Faulty Filter Capacitor Three types of defects of a filter capacitor are illustrated in Figure 2–83.

- *Open* If the filter capacitor for a full-wave rectifier opens, the output is a full-wave rectified voltage.
- *Shorted* If the filter capacitor shorts, the output is 0 V. A shorted capacitor should cause the fuse to blow open. If not properly fused, a shorted capacitor may cause some or all of the diodes in the rectifier to burn open due to excessive current. In any event, the output is 0 V.
- *Leaky* A leaky filter capacitor is equivalent to a capacitor with a parallel leakage resistance. The effect of the leakage resistance is to reduce the time constant and allow the capacitor to discharge more rapidly than normal. This results in an increase in the ripple voltage on the output. This fault is rare.

Effects of a Faulty Transformer An open primary or secondary winding of a power supply transformer results in an output of 0 V, as mentioned before.

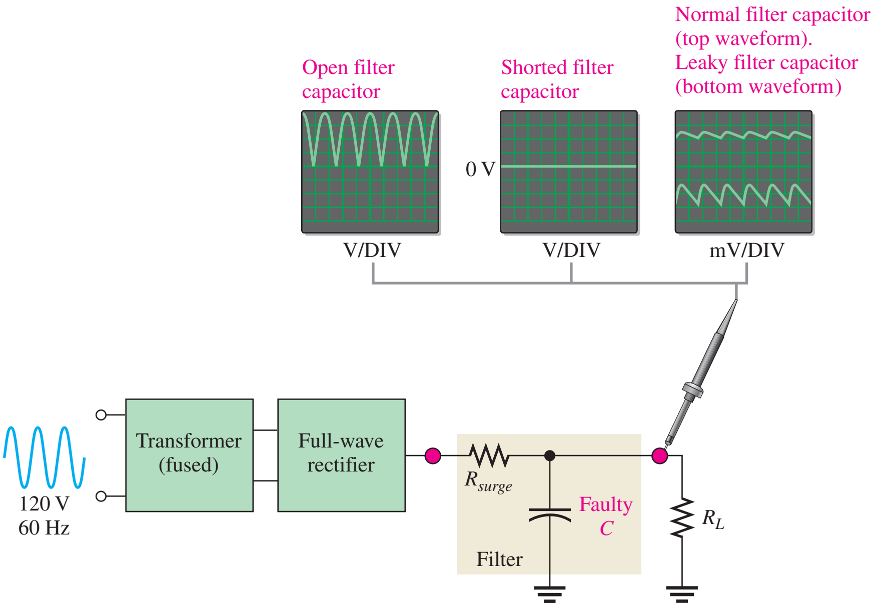

Open filter
capacitor
Shorted filter
capacitor
Normal filter capacitor
(top waveform).
Leaky filter capacitor
(bottom waveform)
0 V
V/DIV
V/DIV
mV/DIV
Transformer
(fused)
Full-wave
rectifier
120 V
60 Hz
R_{surge}
Faulty
C
Filter
R_L

FIGURE 2–83

Effects of a faulty filter capacitor.

EXAMPLE 2–14

You are troubleshooting the power supply shown in the block diagram of Figure 2–84. You have found in the analysis phase that there is no output voltage from the regulator, as indicated. Also, you have found that the unit is plugged into the outlet and have verified the input to the transformer with a DMM. You decide to use the half-splitting method using the scope. What is the problem?

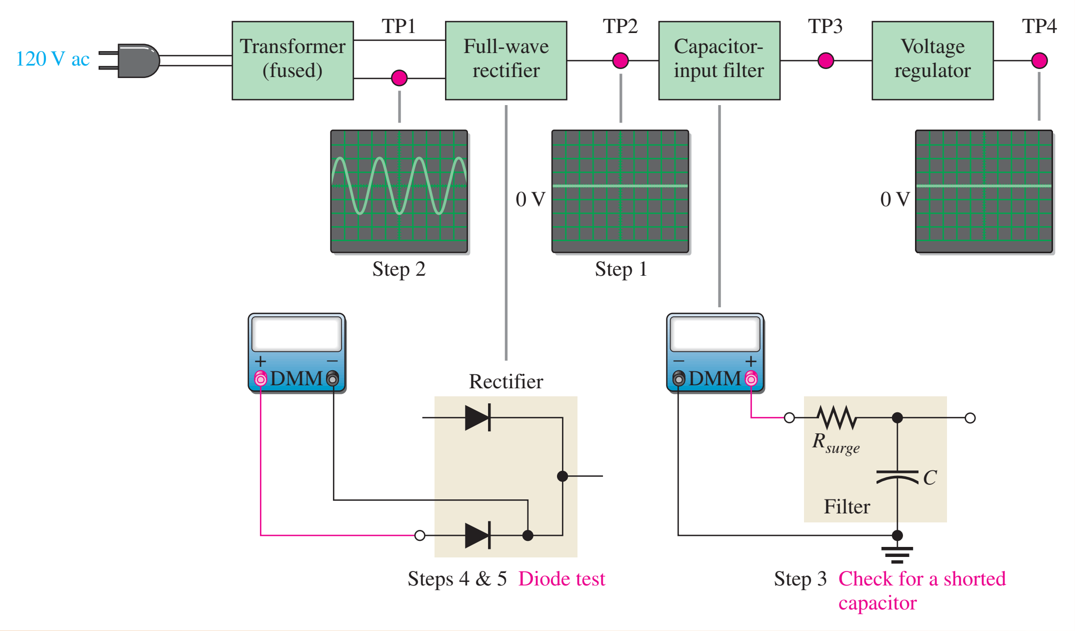

120 V ac
Transformer
(fused)
TP1
Full-wave
rectifier
TP2
Capacitor-
input filter
TP3
Voltage
regulator
TP4
0 V
0 V
Step 2
Step 1
DMM
DMM
Rectifier
R_{surge}
C
Filter
Steps 4 & 5 Diode test
Step 3 Check for a shorted
capacitor

FIGURE 2–84

Solution The step-by-step measurement procedure is illustrated in the figure and described as follows.

Step 1: There is no voltage at test point 2 (TP2). This indicates that the fault is between the input to the transformer and the output of the rectifier. Most likely, the problem is in the transformer or in the rectifier, but there may be a short from the filter input to ground.

Step 2: The voltage at test point 1 (TP1) is correct, indicating that the transformer is working. So, the problem must be in the rectifier or a shorted filter input.

Step 3: With the power turned off, use a DMM to check for a short from the filter input to ground. Assume that the DMM indicates no short. The fault is now isolated to the rectifier.

Step 4: Apply fault analysis to the rectifier circuit. Determine the component failure in the rectifier that will produce a 0 V input. If only one of the diodes in the rectifier is open, there should be a half-wave rectified output voltage, so this is not the problem. In order to have a 0 V output, there must be an open in the rectifier circuit.

Step 5: With the power off, use the DMM in the diode test mode to check each diode. Replace the defective diodes, turn the power on, and check for proper operation. Assume this corrects the problem.

Related Problem Suppose you had found a short in Step 3, what would have been the logical next step?

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE02-01
2. Multisim file TSE02-02
3. Multisim file TSE02-03
4. Multisim file TSE02-04

SECTION 2–10 CHECKUP

1. A properly functioning diode will produce a reading in what range when forward-biased?
2. What reading might a DMM produce when a diode is reverse-biased?
3. What effect does an open diode have on the output voltage of a half-wave rectifier?
4. What effect does an open diode have on the output voltage of a full-wave rectifier?
5. If one of the diodes in a bridge rectifier shorts, what are some possible consequences?
6. What happens to the output voltage of a rectifier if the filter capacitor becomes very leaky?
7. The primary winding of the transformer in a power supply opens. What will you observe on the rectifier output?
8. The dc output voltage of a filtered rectifier is less than it should be. What may be the problem?

Application Activity: *DC Power Supply*

Assume that you are working for a company that designs, tests, manufactures, and markets various electronic instruments including dc power supplies. Your first assignment is to develop and test a basic unregulated power supply using the knowledge that you have acquired so far. Later modifications will include the addition of a regulator. The power supply must meet or exceed the following specifications:

- Input voltage: 120 V rms @60 Hz
- Output voltage: 16 V dc ±10%
- Ripple factor (max): 3.00%
- Load current (max): 250 mA

Design of the Power Supply

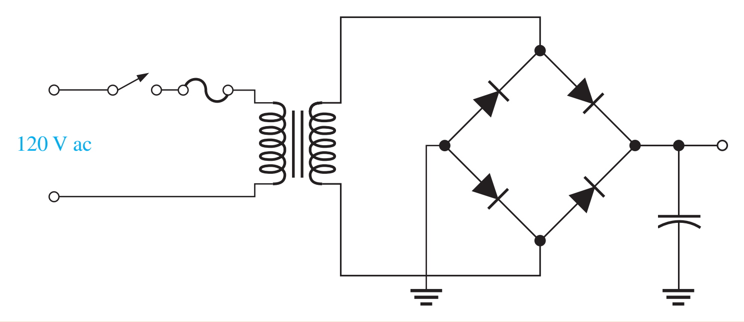
The Rectifier Circuit A full-wave rectifier has less ripple for a given filter capacitor than a half-wave rectifier. A full-wave bridge rectifier is probably the best choice because it provides the most output voltage for a given input voltage and the PIV is less than for a center-tapped rectifier. Also, the full-wave bridge does not require a center-tapped transformer.

1. Compare Equations 2–7 and 2–9 for output voltages.
2. Compare Equations 2–8 and 2–10 for PIV.

The full-wave bridge rectifier circuit is shown in Figure 2–85.

FIGURE 2–85

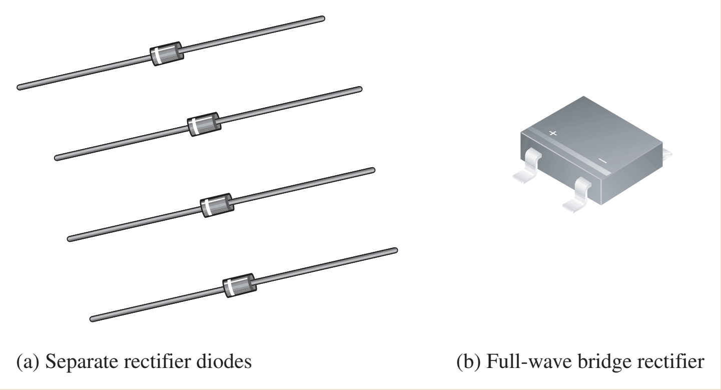
Power supply with full-wave bridge rectifier and capacitor filter.



The Rectifier Diodes There are two approaches for implementing the full-wave bridge: Four individual diodes, as shown in Figure 2–86(a) or a single IC package containing four diodes connected as a bridge rectifier, as shown in part (b).

FIGURE 2–86

Rectifier components.


(a) Separate rectifier diodes

(b) Full-wave bridge rectifier

Because the rectifier in the single IC package exceeds the specifications and requires less wiring on a board, takes up less space, and requires stocking and handling of only one component versus four, it is the best choice. Another factor to consider is the cost. Requirements for the diodes in the bridge are

- Forward current rating must be equal or greater than 250 mA (maximum load current).
- PIV must be greater than the minimum calculated value of 16.7 V (PIV $= V_{p(out)} + 0.7$ V).

By reviewing manufacturer's datasheets on-line, a specific device can be chosen. Figure 2–87 shows a partial datasheet for the rectifier to be used for this power supply. Notice that it exceeds the specified requirements. Four possible websites for rectifiers and diodes are *fairchildsemiconductor.com; onsemi.com*; *semiconductor.phillips.com*; and *rectron.com*.

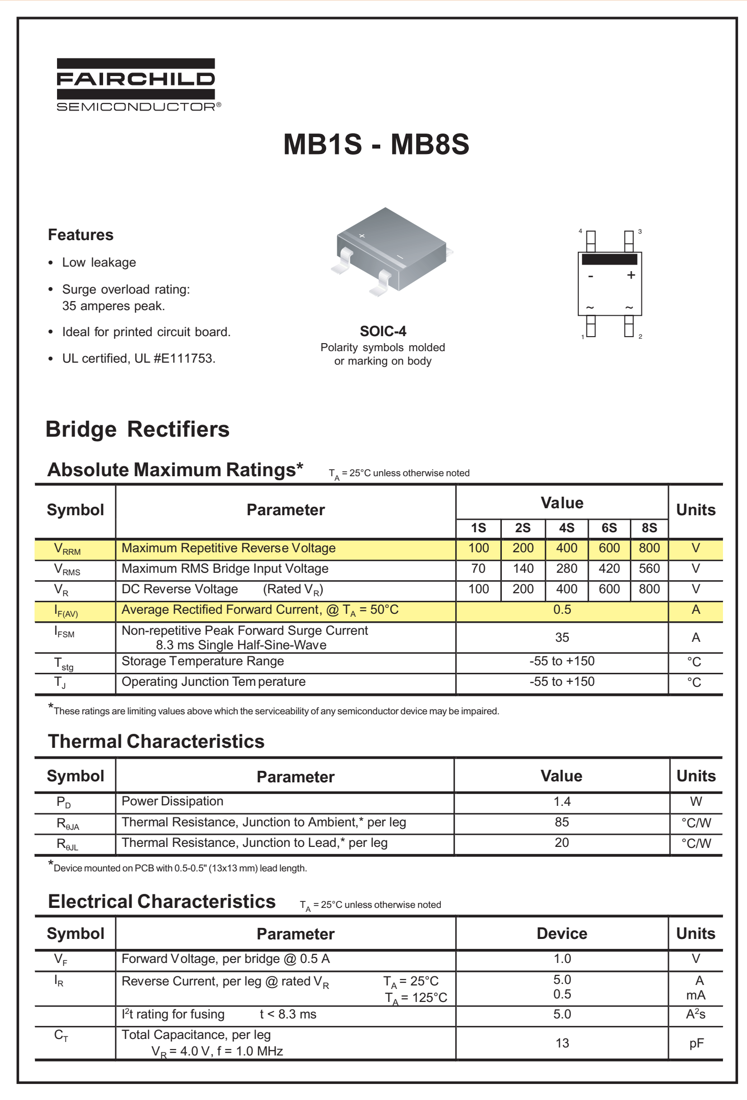


FIGURE 2–87

Rectifier datasheet. You can view the entire datasheet at www.fairchildsemiconductor.com. Copyright Fairchild Semiconductor Corporation. Used by permission.

FAIRCHILD
SEMICONDUCTOR®

MB1S - MB8S

Features

- Low leakage
- Surge overload rating: 35 amperes peak.
- Ideal for printed circuit board.
- UL certified, UL #E111753.

SOIC-4
Polarity symbols molded
or marking on body

Bridge Rectifiers

Absolute Maximum Ratings* $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Value					Units
		1S	2S	4S	6S	8S	
V_{RRM}	Maximum Repetitive Reverse Voltage	100	200	400	600	800	V
V_{RMS}	Maximum RMS Bridge Input Voltage	70	140	280	420	560	V
V_R	DC Reverse Voltage (Rated V_R)	100	200	400	600	800	V
$I_{F(AV)}$	Average Rectified Forward Current, @ $T_A = 50°C$	0.5					A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	35					A
T_{stg}	Storage Temperature Range	-55 to +150					°C
T_J	Operating Junction Temperature	-55 to +150					°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	1.4	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient,* per leg	85	°C/W
$R_{\theta JL}$	Thermal Resistance, Junction to Lead,* per leg	20	°C/W

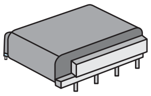
*Device mounted on PCB with 0.5-0.5" (13x13 mm) lead length.

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Device	Units
V_F	Forward Voltage, per bridge @ 0.5 A	1.0	V
I_R	Reverse Current, per leg @ rated V_R $T_A = 25°C$ $T_A = 125°C$	5.0 0.5	A mA
	I^2t rating for fusing $t < 8.3$ ms	5.0	A^2s
C_T	Total Capacitance, per leg $V_R = 4.0$ V, f = 1.0 MHz	13	pF

The Transformer The transformer must convert the 120 V line voltage to an ac voltage that will result in a rectified voltage that will produce 16 V±10% when filtered. A typical power transformer for mounting on a printed circuit board and a portion of a datasheet for the series are shown in Figure 2–88. Notice that transformer power is measured in VA (volt-amps), not watts.

3. Use Equation 2–9 to calculate the required transformer secondary rms voltage.
4. From the partial datasheet in Figure 2–88, select an appropriate transformer based on its secondary voltage (series) and a VA specification that meets the requirement.
5. Determine the required fuse rating.



	Secondary		Dimensions					Wt. Oz.
VA	Series	Parallel	H	W	L	A	B	
2.5	10.0V CT @ 0.25A	5.0V @ 0.5A	0.650	1.562	1.875	1.600	0.375	5
2.5	12.6V CT @ 0.2A	6.3V @ 0.4A	0.650	1.562	1.875	1.600	0.375	5
2.5	16.0V CT @ 0.15A	8.0V @ 0.3A	0.650	1.562	1.875	1.600	0.375	5
2.5	20.0V CT @ 0.125A	10.0V @ 0.25A	0.650	1.562	1.875	1.600	0.375	5
2.5	24.0V CT @ 0.1A	12.0V @ 0.2A	0.650	1.562	1.875	1.600	0.375	5
2.5	30.0V CT @ 0.08A	15.0V @ 0.16A	0.650	1.562	1.875	1.600	0.375	5
2.5	34.0V CT @ 0.076A	17.0V @ 0.15A	0.650	1.562	1.875	1.600	0.375	5
2.5	40.0V CT @ 0.06A	20.0V @ 0.12A	0.650	1.562	1.875	1.600	0.375	5
2.5	56.0V CT @ 0.045A	28.0V @ 0.09A	0.650	1.562	1.875	1.600	0.375	5
2.5	88.0V CT @ 0.028A	44.0V @ 0.056A	0.650	1.562	1.875	1.600	0.375	5
2.5	120.0V CT @ 0.02A	60.0V @ 0.04A	0.650	1.562	1.875	1.600	0.375	5
2.5	230.0V CT @ 0.01A	115.0V @ 0.02A	0.650	1.562	1.875	1.600	0.375	5
6.0	10.0V CT @ 0.6A	5.0V @ 1.2A	0.875	1.562	1.875	1.600	0.375	7
6.0	12.0V CT @ 0.475A	6.3V @ 0.95A	0.875	1.562	1.875	1.600	0.375	7
6.0	16.0V CT @ 0.375A	8.0V @ 0.75A	0.875	1.562	1.875	1.600	0.375	7
6.0	20.0V CT @ 0.3A	10.0V @ 0.6A	0.875	1.562	1.875	1.600	0.375	7
6.0	24.0V CT @ 0.25A	12.0V @ 0.5A	0.875	1.562	1.875	1.600	0.375	7

▲ FIGURE 2–88

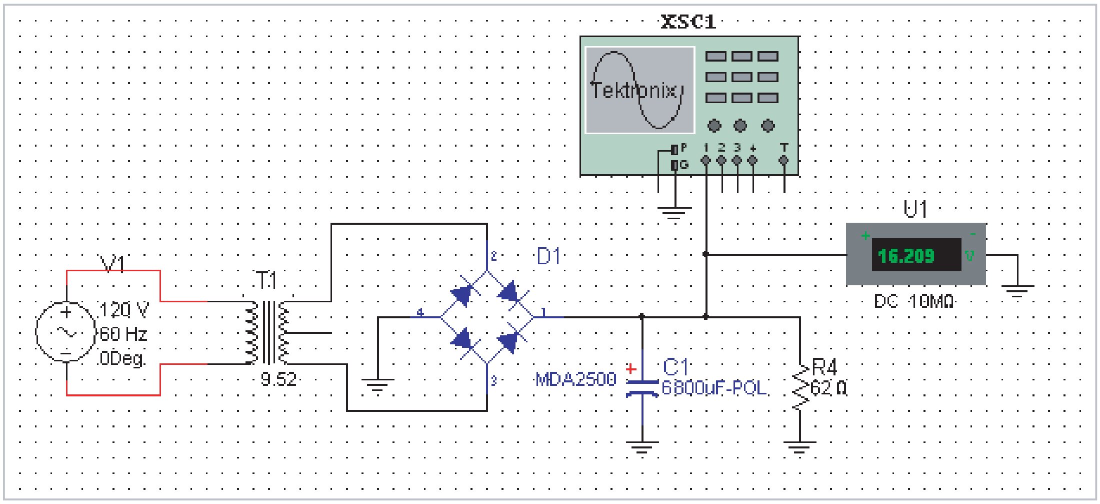
Typical pc-mounted power transformer and data. Volts are rms.

The Filter Capacitor The capacitance of the filter capacitor must be sufficiently large to provide the specified ripple.

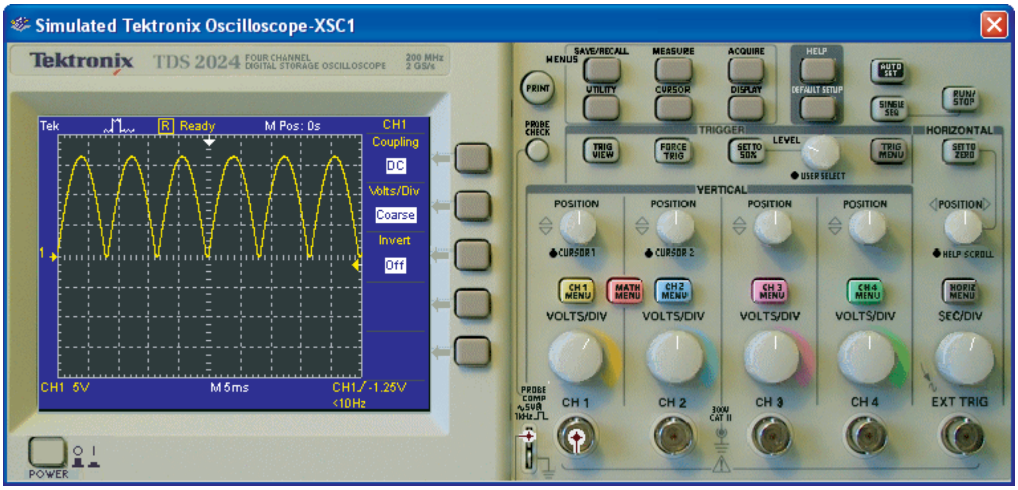
6. Use Equation 2–11 to calculate the peak-to-peak ripple voltage, assuming $V_{DC} = 16$ V.
7. Use Equation 2–12 to calculate the minimum capacitance value. Use $R_L = 64\ \Omega$, calculated on page 89.

Simulation

In the development of a new circuit, it is sometimes helpful to simulate the circuit using a software program before actually building it and committing it to hardware. We will use Multisim to simulate this power supply circuit. Figure 2–89 shows the simulated power


XSC1
Tektronix
P
G
1 2 3 4 T
U1
16.209
V
DC 10MΩ
V1
120 V
60 Hz
0Deg
T1
9.52
D1
2
4
1
3
MDA2500
C1
6800uF-POL
R4
62 Ω

(a) Multisim circuit screen


Simulated Tektronix Oscilloscope-XSC1
Tektronix TDS 2024 FOUR CHANNEL DIGITAL STORAGE OSCILLOSCOPE 200 MHz 2 GS/s
MENUS
SAVE/RECALL
MEASURE
ACQUIRE
HELP
UTILITY
CURSOR
DISPLAY
DEFAULT SETUP
AUTO SET
SINGLE SEQ
RUN/STOP
PRINT
PROBE CHECK
TRIGGER
TRIG VIEW
FORCE TRIG
SET TO 50%
LEVEL
USER SELECT
TRIG MENU
HORIZONTAL
SET TO ZERO
VERTICAL
POSITION
CURSOR 1
CURSOR 2
HELP SCROLL
CH 1 MENU
MATH MENU
CH 2 MENU
CH 3 MENU
CH 4 MENU
HORIZ MENU
VOLTS/DIV
SEC/DIV
CH 1
CH 2
CH 3
CH 4
EXT TRIG
POWER

Tek Ready M Pos: 0s

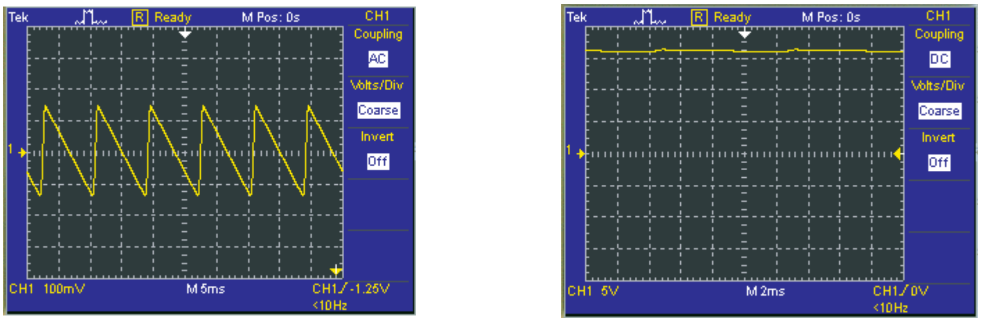
CH1 Coupling DC

Volts/Div Coarse

Invert Off

CH1 5V M 5ms CH1 ∕ -1.25V <10Hz

(b) Output voltage without the filter capacitor



Tek Ready M Pos: 0s

CH1 Coupling AC

Volts/Div Coarse

Invert Off

CH1 100mV M 5ms CH1 ∕ -1.25V <10Hz

Tek Ready M Pos: 0s

CH1 Coupling DC

Volts/Div Coarse

Invert Off

CH1 5V M 2ms CH1 ∕ 0V <10Hz

(c) Ripple voltage is less than 300 mV pp

(d) DC output voltage with filter capacitor (near top of screen)

▲ FIGURE 2–89

Power supply simulation.

supply circuit with a load connected and scope displays of the output voltage with and without the filter capacitor connected. The filter capacitor value of 6800 μF is the next highest standard value closest to the minimum calculated value required. A load resistor value was chosen to draw a current equal to or greater than the specified maximum load current.

$$R_L = \frac{16\text{ V}}{250\text{ mA}} = 64\ \Omega$$

The closest standard value is 62 Ω, which draws 258 mA at 16 V and which meets and exceeds the load current specification.

8. Determine the power rating for the load resistor.

To produce a dc output of 16 V, a peak secondary voltage of 16 V + 1.4 V = 17.4 V is required. The rms secondary voltage must be

$$V_{rms(sec)} = 0.707V_{p(sec)} = 0.707(16\text{ V} + 1.4\text{ V}) = 12.3\text{ V}$$

SAFETY NOTE

Be very careful to not touch the line voltage connections to the transformer primary. In normal practice, the board is housed in a protective box to prevent the possibility of contact with the 120 V ac line.

A standard transformer rms output voltage is 12.6 V. The transformer specification required by Multisim is

$$120\text{ V}:12.6\text{ V} = 9.52:1$$

The dc voltmeter in Figure 2–89(a) indicates an output voltage of 16.209 V, which is well within the 16 V±10% requirement. In part (c), the scope is AC coupled and set at 100 mV/division. You can see that the peak-to-peak ripple voltage is less than 300 mV, which is less than 480 mV, corresponding to the specified maximum ripple factor of 3%.

Build and simulate the circuit using your Multisim software. Observe the operation with the virtual oscilloscope and voltmeter.

Prototyping and Testing

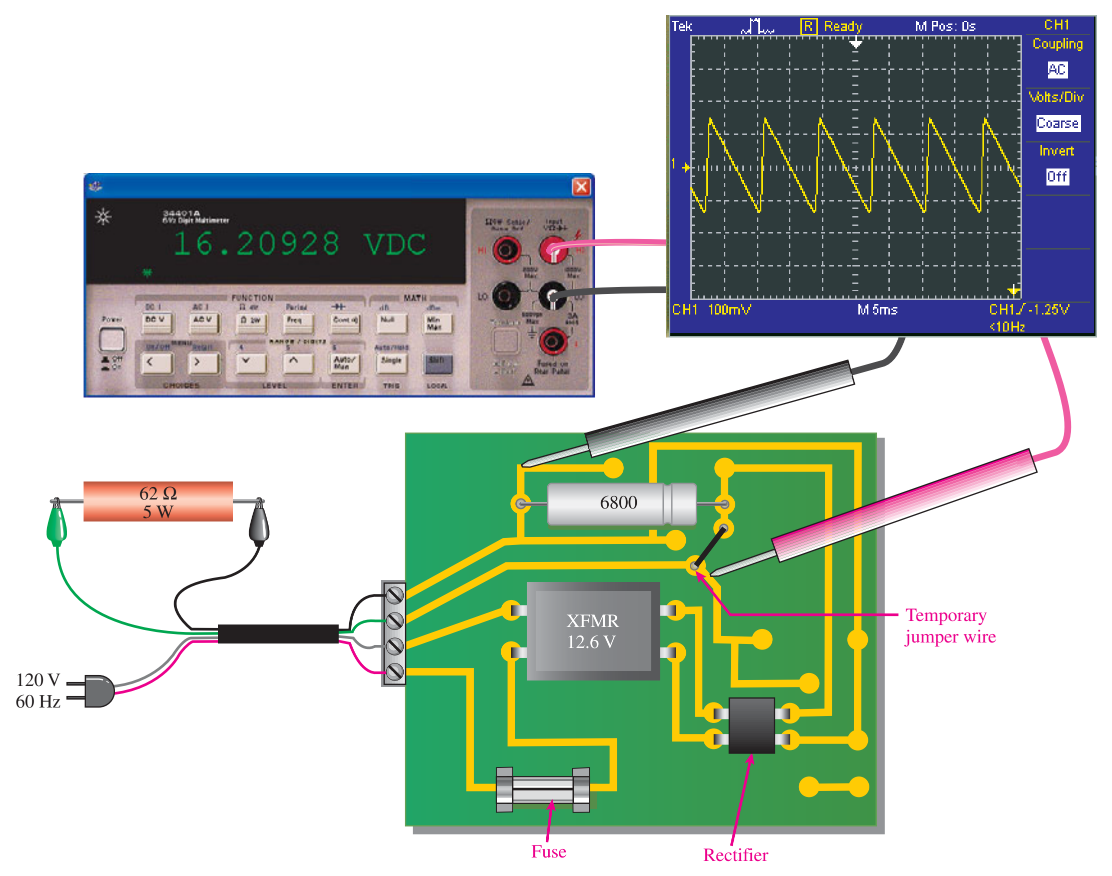
Now that all the components have been selected, the prototype circuit is constructed and tested. After the circuit is successfully tested, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a similar circuit, go to Experiment 2 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

The Printed Circuit Board

The circuit board is shown in Figure 2–90. There are additional traces and connection points on the board for expansion to a regulated power supply, which will be done in Chapter 3. The circuit board is connected to the ac voltage and to a power load resistor via a cable. The power switch shown in the original schematic will be on the PC board housing and is not shown for the test setup. A DMM measurement of the output voltage indicates a correct value. Oscilloscope measurement of the ripple shows that it is within specifications.

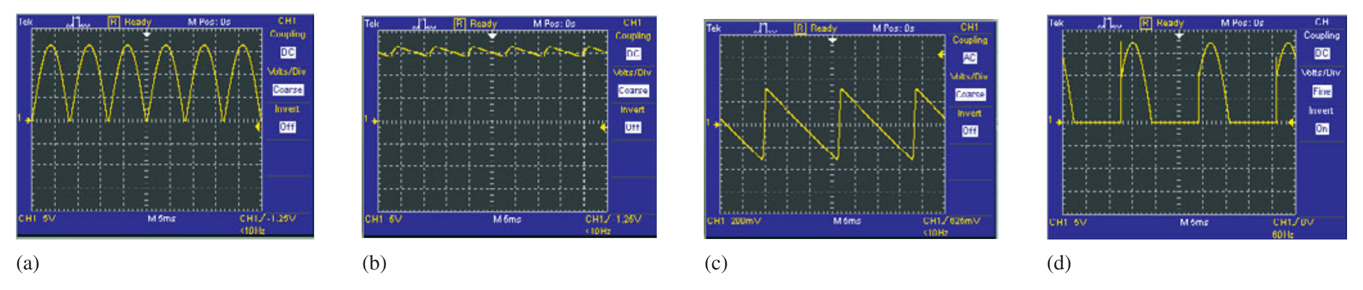

16.20928 VDC
Tek
Ready
M Pos: 0s
CH1
Coupling
AC
Volts/Div
Coarse
Invert
Off
CH1 100mV
M 5ms
CH1 ∕ -1.25V
<10Hz
62 Ω
5 W
120 V
60 Hz
6800
XFMR
12.6 V
Temporary
jumper wire
Fuse
Rectifier

▲ **FIGURE 2–90**

Testing the power supply printed circuit board. The 62 Ω load is a temporary test load to check ripple when the power supply is used at its maximum rated current.

Troubleshooting

For each of the scope output voltage measurements in Figure 2–91, determine the likely fault or faults, if any.

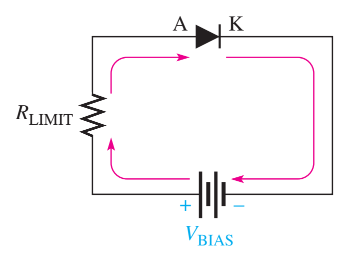


▲ **FIGURE 2–91**

Output voltage measurements on the power supply circuit.

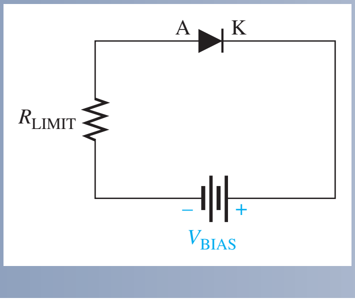
SUMMARY OF DIODE BIAS

FORWARD BIAS: PERMITS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to anode (A); negative to cathode (K).
- The bias voltage must be greater than the barrier potential.
- Barrier potential: 0.7 V for silicon.
- Majority carriers provide the forward current.
- The depletion region narrows.

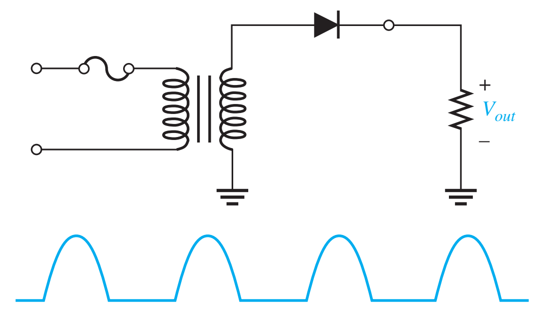
REVERSE BIAS: PREVENTS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to cathode (K); negative to anode (A).
- The bias voltage must be less than the breakdown voltage.
- There is no majority carrier current after transition time.
- Minority carriers provide a negligibly small reverse current.
- The depletion region widens.

SUMMARY OF POWER SUPPLY RECTIFIERS

HALF-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = V_{p(sec)} - 0.7\text{ V}$$

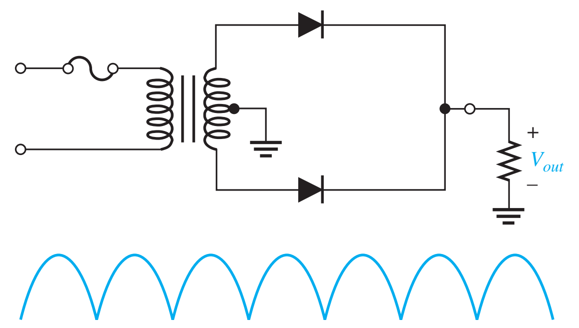
- Average value of output:

$$V_{AVG} = \frac{V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = V_{p(sec)}$$

CENTER-TAPPED FULL-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7\text{ V}$$

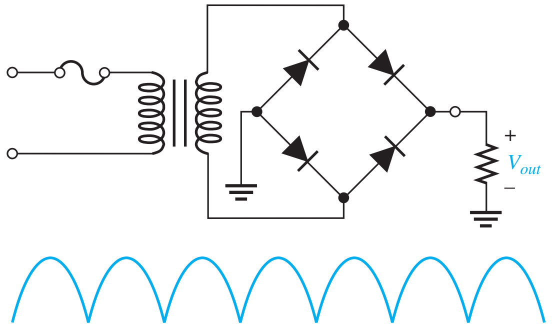
- Average value of output:

$$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = 2V_{p(out)} + 0.7\text{ V}$$

BRIDGE FULL-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = V_{p(sec)} - 1.4\text{ V}$$

- Average value of output:

$$V_{\text{AVG}} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = V_{p(out)} + 0.7\text{ V}$$

SUMMARY

Section 2–1

- There is current through a diode only when it is forward-biased. Ideally, there is no current when there is no bias nor when there is reverse bias. Actually, there is a very small current in reverse bias due to the thermally generated minority carriers, but this can usually be neglected.
- Avalanche occurs in a reverse-biased diode if the bias voltage equals or exceeds the breakdown voltage.
- A diode conducts current when forward-biased and blocks current when reversed-biased.
- Reverse breakdown voltage for a diode is typically greater than 50 V.

Section 2–2

- The *V-I* characteristic curve shows the diode current as a function of voltage across the diode.
- The resistance of a forward-biased diode is called the *dynamic* or *ac resistance.*
- Reverse current increases rapidly at the reverse breakdown voltage.
- Reverse breakdown should be avoided in most diodes.

Section 2–3

- The ideal model represents the diode as a closed switch in forward bias and as an open switch in reverse bias.
- The practical model represents the diode as a switch in series with the barrier potential.
- The complete model includes the dynamic forward resistance in series with the practical model in forward bias and the reverse resistance in parallel with the open switch in reverse bias.

Section 2–4

- A dc power supply typically consists of a transformer, a diode rectifier, a filter, and a regulator.
- The single diode in a half-wave rectifier is forward-biased and conducts for 180° of the input cycle.
- The output frequency of a half-wave rectifier equals the input frequency.
- PIV (peak inverse voltage) is the maximum voltage appearing across the diode in reverse bias.

Section 2–5

- Each diode in a full-wave rectifier is forward-biased and conducts for 180° of the input cycle.
- The output frequency of a full-wave rectifier is twice the input frequency.
- The two basic types of full-wave rectifier are center-tapped and bridge.
- The peak output voltage of a center-tapped full-wave rectifier is approximately one-half of the total peak secondary voltage less one diode drop.
- The PIV for each diode in a center-tapped full-wave rectifier is twice the peak output voltage plus one diode drop.
- The peak output voltage of a bridge rectifier equals the total peak secondary voltage less two diode drops.
- The PIV for each diode in a bridge rectifier is approximately half that required for an equivalent center-tapped configuration and is equal to the peak output voltage plus one diode drop.

Section 2–6

- A capacitor-input filter provides a dc output approximately equal to the peak of its rectified input voltage.
- Ripple voltage is caused by the charging and discharging of the filter capacitor.
- The smaller the ripple voltage, the better the filter.
- Regulation of output voltage over a range of input voltages is called *input* or *line regulation.*
- Regulation of output voltage over a range of load currents is called *load regulation.*

Section 2–7

- Diode limiters cut off voltage above or below specified levels. Limiters are also called *clippers.*
- Diode clampers add a dc level to an ac voltage.

Section 2–8

- Voltage multipliers are used in high-voltage, low-current applications such as for electron beam acceleration in CRTs and for particle accelerators.
- A voltage multiplier uses a series of diode-capacitor stages.
- Input voltage can be doubled, tripled, or quadrupled.

Section 2–9

- A datasheet provides key information about the parameters and characteristics of an electronic device.
- A diode should always be operated below the absolute maximum ratings specified on the datasheet.

Section 2–10

- Many DMMs provide a diode test function.
- DMMs display the diode drop when the diode is operating properly in forward bias.
- Most DMMs indicate “OL” when the diode is open.
- Troubleshooting is the application of logical thought combined with a thorough knowledge of the circuit or system to identify and correct a malfunction.
- Troubleshooting is a three-step process of analysis, planning, and measurement.
- Fault analysis is the isolation of a fault to a particular circuit or portion of a circuit.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Bias The application of a dc voltage to a diode to make it either conduct or block current.

Clamper A circuit that adds a dc level to an ac voltage using a diode and a capacitor.

DC power supply A circuit that converts ac line voltage to dc voltage and supplies constant power to operate a circuit or system.

Diode A semiconductor device with a single *pn* junction that conducts current in only one direction.

Filter In a power supply, the capacitor used to reduce the variation of the output voltage from a rectifier.

Forward bias The condition in which a diode conducts current.

Full-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with two output pulses occurring for each input cycle.

Half-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with one output pulse occurring for each input cycle.

Limiter A diode circuit that clips off or removes part of a waveform above and/or below a specified level.

Line regulation The change in output voltage of a regulator for a given change in input voltage, normally expressed as a percentage.

Load regulation The change in output voltage of a regulator for a given range of load currents, normally expressed as a percentage.

Peak inverse voltage (PIV) The maximum value of reverse voltage across a diode that occurs at the peak of the input cycle when the diode is reverse-biased.

Rectifier An electronic circuit that converts ac into pulsating dc; one part of a power supply.

Regulator An electronic device or circuit that maintains an essentially constant output voltage for a range of input voltage or load values; one part of a power supply.

Reverse bias The condition in which a diode prevents current.

Ripple voltage The small variation in the dc output voltage of a filtered rectifier caused by the charging and discharging of the filter capacitor.

Troubleshooting A systematic process of isolating, identifying, and correcting a fault in a circuit or system.

***V-I* characteristic** A curve showing the relationship of diode voltage and current.

KEY FORMULAS

2–1	$I_F = \dfrac{V_{BIAS}}{R_{LIMIT}}$	Forward current, ideal diode model
2–2	$I_F = \dfrac{V_{BIAS} - V_F}{R_{LIMIT}}$	Forward current, practical diode model
2–3	$V_{AVG} = \dfrac{V_p}{\pi}$	Half-wave average value
2–4	$V_{p(out)} = V_{p(in)} - 0.7\text{ V}$	Peak half-wave rectifier output (silicon)
2–5	$\text{PIV} = V_{p(in)}$	Peak inverse voltage, half-wave rectifier
2–6	$V_{AVG} = \dfrac{2V_p}{\pi}$	Full-wave average value
2–7	$V_{out} = \dfrac{V_{sec}}{2} - 0.7\text{ V}$	Center-tapped full-wave output
2–8	$\text{PIV} = 2V_{p(out)} + 0.7\text{ V}$	Peak inverse voltage, center-tapped rectifier
2–9	$V_{p(out)} = V_{p(sec)} - 1.4\text{ V}$	Bridge full-wave output
2–10	$\text{PIV} = V_{p(out)} + 0.7\text{ V}$	Peak inverse voltage, bridge rectifier
2–11	$r = \dfrac{V_{r(pp)}}{V_{DC}}$	Ripple factor
2–12	$V_{r(pp)} \cong \left(\dfrac{1}{fR_LC}\right)V_{p(rect)}$	Peak-to-peak ripple voltage, capacitor-input filter
2–13	$V_{DC} = \left(1 - \dfrac{1}{2fR_LC}\right)V_{p(rect)}$	DC output voltage, capacitor-input filter
2–14	$\text{Line regulation} = \left(\dfrac{\Delta V_{OUT}}{\Delta V_{IN}}\right)100\%$	
2–15	$\text{Load regulation} = \left(\dfrac{V_{NL} - V_{FL}}{V_{FL}}\right)100\%$	

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. The two regions of a diode are the anode and the collector.
2. A diode can conduct current in two directions with equal ease.
3. A diode conducts current when forward-biased.
4. When reverse-biased, a diode ideally appears as a short.
5. Two types of current in a diode are electron and hole.
6. A basic half-wave rectifier consists of one diode.
7. The output frequency of a half-wave rectifier is twice the input frequency.
8. The diode in a half-wave rectifier conducts for half the input cycle.
9. PIV stands for positive inverse voltage.
10. Each diode in a full-wave rectifier conducts for the entire input cycle.
11. The output frequency of a full-wave rectifier is twice the input frequency.
12. A bridge rectifier uses four diodes.
13. In a bridge rectifier, two diodes conduct during each half cycle of the input.
14. The purpose of the capacitor filter in a rectifier is to convert ac to dc.
15. The output voltage of a filtered rectifier always has some ripple voltage.

16. A smaller filter capacitor reduces the ripple.
17. Line and load regulation are the same.
18. A diode limiter is also known as a clipper.
19. The purpose of a clamper is to remove a dc level from a waveform.
20. Voltage multipliers use diodes and capacitors.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. When a diode is forward-biased and the bias voltage is increased, the forward current will

   (a) increase **(b)** decrease **(c)** not change

2. When a diode is forward-biased and the bias voltage is increased, the voltage across the diode (assuming the practical model) will

   (a) increase **(b)** decrease **(c)** not change

3. When a diode is reverse-biased and the bias voltage is increased, the reverse current (assuming the practical model) will

   (a) increase **(b)** decrease **(c)** not change

4. When a diode is reverse-biased and the bias voltage is increased, the reverse current (assuming the complete model) will

   (a) increase **(b)** decrease **(c)** not change

5. When a diode is forward-biased and the bias voltage is increased, the voltage across the diode (assuming the complete model) will

   (a) increase **(b)** decrease **(c)** not change

6. If the forward current in a diode is increased, the diode voltage (assuming the practical model) will

   (a) increase **(b)** decrease **(c)** not change

7. If the forward current in a diode is decreased, the diode voltage (assuming the complete model) will

   (a) increase **(b)** decrease **(c)** not change

8. If the barrier potential of a diode is exceeded, the forward current will

   (a) increase **(b)** decrease **(c)** not change

9. If the input voltage in Figure 2–28 is increased, the peak inverse voltage across the diode will

   (a) increase **(b)** decrease **(c)** not change

10. If the turns ratio of the transformer in Figure 2–28 is decreased, the forward current through the diode will

    (a) increase **(b)** decrease **(c)** not change

11. If the frequency of the input voltage in Figure 2–36 is increased, the output voltage will

    (a) increase **(b)** decrease **(c)** not change

12. If the PIV rating of the diodes in Figure 2–36 is increased, the current through R_L will

    (a) increase **(b)** decrease **(c)** not change

13. If one of the diodes in Figure 2–41 opens, the average voltage to the load will

    (a) increase **(b)** decrease **(c)** not change

14. If the value of R_L in Figure 2–41 is decreased, the current through each diode will

    (a) increase **(b)** decrease **(c)** not change

15. If the capacitor value in Figure 2–48 is decreased, the output ripple voltage will

    (a) increase **(b)** decrease **(c)** not change

16. If the line voltage in Figure 2–51 is increased, ideally the +5 V output will

    (a) increase **(b)** decrease **(c)** not change

17. If the bias voltage in Figure 2–55 is decreased, the positive portion of the output voltage will

    (a) increase **(b)** decrease **(c)** not change

18. If the bias voltage in Figure 2–55 is increased, the negative portion of the output voltage will

    (a) increase **(b)** decrease **(c)** not change

19. If the value of R_3 in Figure 2–61 is decreased, the positive output voltage will
(a) increase **(b)** decrease **(c)** not change

20. If the input voltage in Figure 2–65 is increased, the peak negative value of the output voltage will
(a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 2–1

1. The term *bias* means
- **(a)** the ratio of majority carriers to minority carriers
- **(b)** the amount of current across a diode
- **(c)** a dc voltage is applied to control the operation of a device
- **(d)** neither (a), (b), nor (c)

2. To forward-bias a diode,
- **(a)** an external voltage is applied that is positive at the anode and negative at the cathode
- **(b)** an external voltage is applied that is negative at the anode and positive at the cathode
- **(c)** an external voltage is applied that is positive at the *p* region and negative at the *n* region
- **(d)** answers (a) and (c)

3. When a diode is forward-biased,
- **(a)** the only current is hole current
- **(b)** the only current is electron current
- **(c)** the only current is produced by majority carriers
- **(d)** the current is produced by both holes and electrons

4. Although current is blocked in reverse bias,
- **(a)** there is some current due to majority carriers
- **(b)** there is a very small current due to minority carriers
- **(c)** there is an avalanche current

5. For a silicon diode, the value of the forward-bias voltage typically
- **(a)** must be greater than 0.3 V
- **(b)** must be greater than 0.7 V
- **(c)** depends on the width of the depletion region
- **(d)** depends on the concentration of majority carriers

6. When forward-biased, a diode
(a) blocks current **(b)** conducts current
(c) has a high resistance **(d)** drops a large voltage

Section 2–2

7. A diode is normally operated in
(a) reverse breakdown **(b)** the forward-bias region
(c) the reverse-bias region **(d)** either (b) or (c)

8. The dynamic resistance can be important when a diode is
(a) reverse-biased **(b)** forward-biased
(c) in reverse breakdown **(d)** unbiased

9. The *V-I* curve for a diode shows
- **(a)** the voltage across the diode for a given current
- **(b)** the amount of current for a given bias voltage
- **(c)** the power dissipation
- **(d)** none of these

Section 2–3

10. Ideally, a diode can be represented by a
(a) voltage source **(b)** resistance **(c)** switch **(d)** all of these

11. In the practical diode model,

(a) the barrier potential is taken into account

(b) the forward dynamic resistance is taken into account

(c) none of these

(d) both (a) and (b)

12. In the complete diode model,

(a) the barrier potential is taken into account

(b) the forward dynamic resistance is taken into account

(c) the reverse resistance is taken into account

(d) all of these

Section 2–4

13. The average value of a half-wave rectified voltage with a peak value of 200 V is

(a) 63.7 V **(b)** 127.2 V **(c)** 141 V **(d)** 0 V

14. When a 60 Hz sinusoidal voltage is applied to the input of a half-wave rectifier, the output frequency is

(a) 120 Hz **(b)** 30 Hz **(c)** 60 Hz **(d)** 0 Hz

15. The peak value of the input to a half-wave rectifier is 10 V. The approximate peak value of the output is

(a) 10 V **(b)** 3.18 V **(c)** 10.7 V **(d)** 9.3 V

16. For the circuit in Question 15, the diode must be able to withstand a reverse voltage of

(a) 10 V **(b)** 5 V **(c)** 20 V **(d)** 3.18 V

Section 2–5

17. The average value of a full-wave rectified voltage with a peak value of 75 V is

(a) 53 V **(b)** 47.8 V **(c)** 37.5 V **(d)** 23.9 V

18. When a 60 Hz sinusoidal voltage is applied to the input of a full-wave rectifier, the output frequency is

(a) 120 Hz **(b)** 60 Hz **(c)** 240 Hz **(d)** 0 Hz

19. The total secondary voltage in a center-tapped full-wave rectifier is 125 V rms. Neglecting the diode drop, the rms output voltage is

(a) 125 V **(b)** 177 V **(c)** 100 V **(d)** 62.5 V

20. When the peak output voltage is 100 V, the PIV for each diode in a center-tapped full-wave rectifier is (neglecting the diode drop)

(a) 100 V **(b)** 200 V **(c)** 141 V **(d)** 50 V

21. When the rms output voltage of a bridge full-wave rectifier is 20 V, the peak inverse voltage across the diodes is (neglecting the diode drop)

(a) 20 V **(b)** 40 V **(c)** 28.3 V **(d)** 56.6 V

Section 2–6

22. The ideal dc output voltage of a capacitor-input filter is equal to

(a) the peak value of the rectified voltage

(b) the average value of the rectified voltage

(c) the rms value of the rectified voltage

23. A certain power-supply filter produces an output with a ripple of 100 mV peak-to-peak and a dc value of 20 V. The ripple factor is

(a) 0.05 **(b)** 0.005 **(c)** 0.00005 **(d)** 0.02

24. A 60 V peak full-wave rectified voltage is applied to a capacitor-input filter. If $f = 120$ Hz, $R_L = 10\ \text{k}\Omega$, and $C = 10\ \mu\text{F}$, the ripple voltage is

(a) 0.6 V **(b)** 6 mV **(c)** 5.0 V **(d)** 2.88 V

25. If the load resistance of a capacitor-filtered full-wave rectifier is reduced, the ripple voltage

(a) increases **(b)** decreases **(c)** is not affected **(d)** has a different frequency

26. Line regulation is determined by

(a) load current

(b) zener current and load current

(c) changes in load resistance and output voltage

(d) changes in output voltage and input voltage

27. Load regulation is determined by

(a) changes in load current and input voltage

(b) changes in load current and output voltage

(c) changes in load resistance and input voltage

(d) changes in zener current and load current

Section 2–7

28. A 10 V peak-to-peak sinusoidal voltage is applied across a silicon diode and series resistor. The maximum voltage across the diode is

(a) 9.3 V **(b)** 5 V **(c)** 0.7 V **(d)** 10 V **(e)** 4.3 V

29. In a certain biased limiter, the bias voltage is 5 V and the input is a 10 V peak sine wave. If the positive terminal of the bias voltage is connected to the cathode of the diode, the maximum voltage at the anode is

(a) 10 V **(b)** 5 V **(c)** 5.7 V **(d)** 0.7 V

30. In a certain positive clamper circuit, a 120 V rms sine wave is applied to the input. The dc value of the output is

(a) 119.3 V **(b)** 169 V **(c)** 60 V **(d)** 75.6 V

Section 2–8

31. The input of a voltage doubler is 120 V rms. The peak-to-peak output is approximately

(a) 240 V **(b)** 60 V **(c)** 167 V **(d)** 339 V

32. If the input voltage to a voltage tripler has an rms value of 12 V, the dc output voltage is approximately

(a) 36 V **(b)** 50.9 V **(c)** 33.9 V **(d)** 32.4 V

Section 2–10

33. When a silicon diode is working properly in forward bias, a DMM in the diode test position will indicate

(a) 0 V **(b)** OL **(c)** approximately 0.7 V **(d)** approximately 0.3 V

34. When a silicon diode is open, a DMM will generally indicate

(a) 0 V **(b)** OL **(c)** approximately 0.7 V **(d)** approximately 0.3 V

35. In a rectifier circuit, if the secondary winding in the transformer opens, the output is

(a) 0 V **(b)** 120 V **(c)** less than it should be **(d)** unaffected

36. If one of the diodes in a bridge full-wave rectifier opens, the output is

(a) 0 V **(b)** one-fourth the amplitude of the input voltage

(c) a half-wave rectified voltage **(d)** a 120 Hz voltage

37. If you are checking a 60 Hz full-wave bridge rectifier and observe that the output has a 60 Hz ripple,

(a) the circuit is working properly **(b)** there is an open diode

(c) the transformer secondary is shorted **(d)** the filter capacitor is leaky

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 2–1

Diode Operation

1. To forward-bias a diode, to which region must the positive terminal of a voltage source be connected?

2. Explain why a series resistor is necessary when a diode is forward-biased.

Section 2–2

Voltage-Current Characteristic of a Diode

3. Explain how to generate the forward-bias portion of the characteristic curve.

4. What would cause the barrier potential of a silicon diode to decrease from 0.7 V to 0.6 V?

Section 2–3 Diode Models

5. Determine whether each silicon diode in Figure 2–92 is forward-biased or reverse-biased.

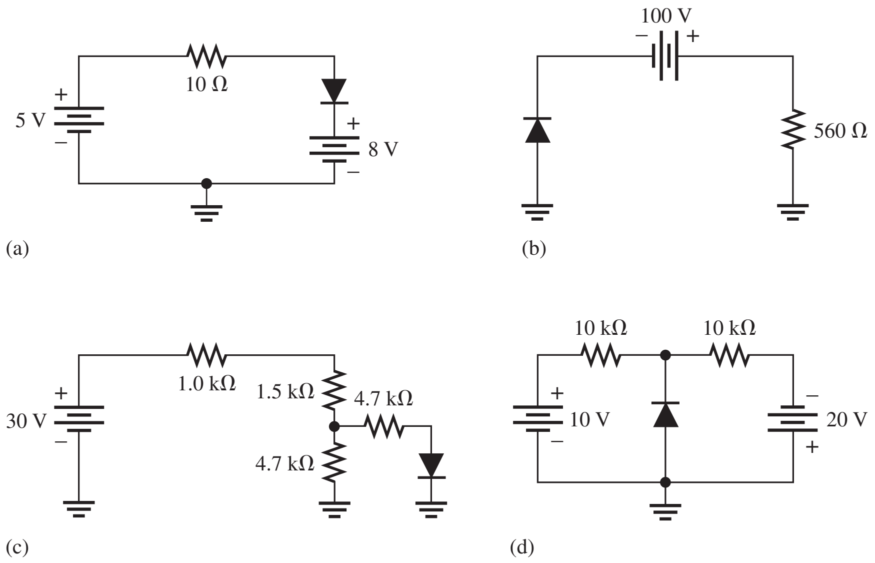
6. Determine the voltage across each diode in Figure 2–92, assuming the practical model.

7. Determine the voltage across each diode in Figure 2–92, assuming an ideal diode.

8. Determine the voltage across each diode in Figure 2–92, using the complete diode model with $r'_d = 10\ \Omega$ and $r'_R = 100\ \text{M}\Omega$.

▶ **FIGURE 2–92**

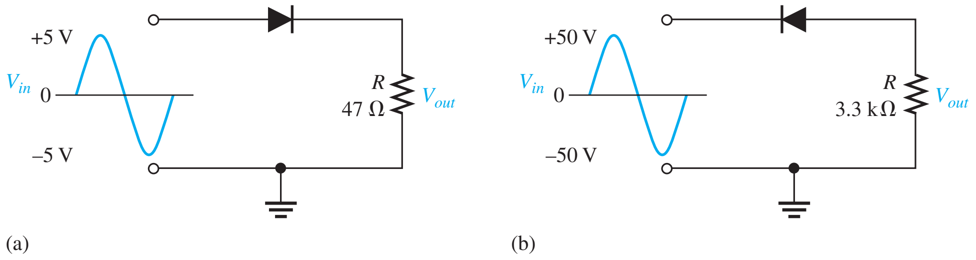
Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F02-92).



Section 2–4 Half-Wave Rectifiers

9. Draw the output voltage waveform for each circuit in Figure 2–93 and include the voltage values.

▶ **FIGURE 2–93**



10. What is the peak inverse voltage across each diode in Figure 2–93?

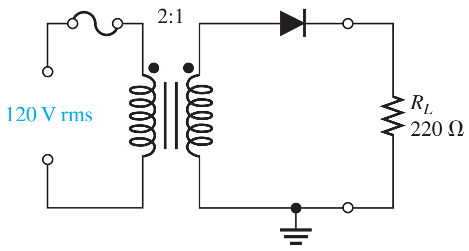
11. Calculate the average value of a half-wave rectified voltage with a peak value of 200 V.

12. What is the peak forward current through each diode in Figure 2–93?

13. A power-supply transformer has a turns ratio of 5:1. What is the secondary voltage if the primary is connected to a 120 V rms source?

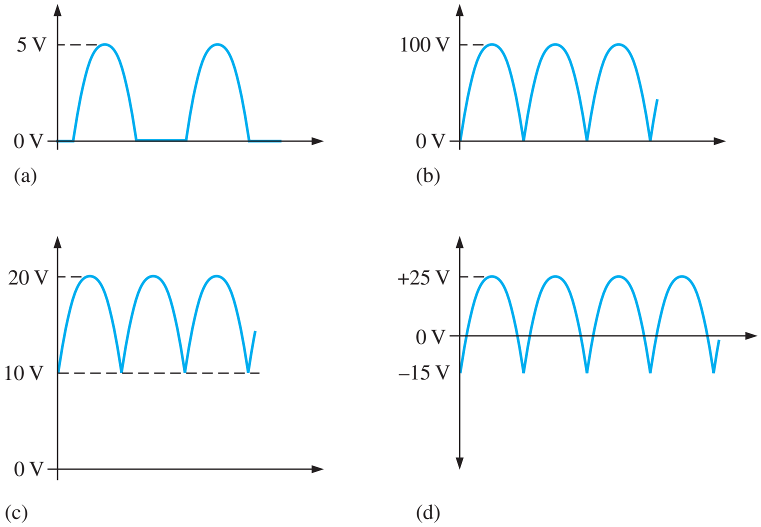
14. Determine the peak and average power delivered to R_L in Figure 2–94.

▶ **FIGURE 2–94**



Section 2–5 Full-Wave Rectifiers

15. Find the average value of each voltage in Figure 2–95.

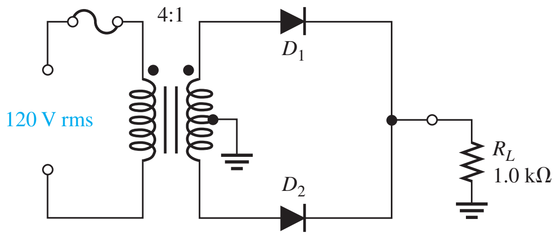


▲ FIGURE 2–95

16. Consider the circuit in Figure 2–96.

- **(a)** What type of circuit is this?
- **(b)** What is the total peak secondary voltage?
- **(c)** Find the peak voltage across each half of the secondary.
- **(d)** Sketch the voltage waveform across R_L.
- **(e)** What is the peak current through each diode?
- **(f)** What is the PIV for each diode?

▶ FIGURE 2–96



17. Calculate the peak voltage across each half of a center-tapped transformer used in a full-wave rectifier that has an average output voltage of 120 V.

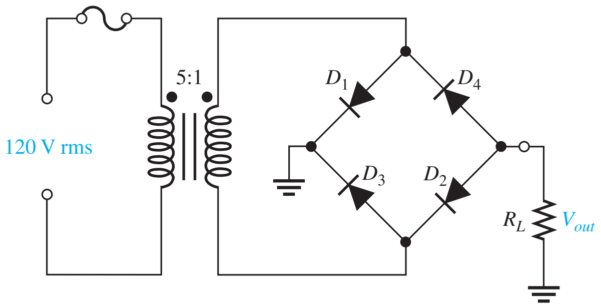
18. Show how to connect the diodes in a center-tapped rectifier in order to produce a negative-going full-wave voltage across the load resistor.

19. What PIV rating is required for the diodes in a bridge rectifier that produces an average output voltage of 50 V?

20. The rms output voltage of a bridge rectifier is 20 V. What is the peak inverse voltage across the diodes?

21. Draw the output voltage waveform for the bridge rectifier in Figure 2–97. Notice that all the diodes are reversed from circuits shown earlier in the chapter.

FIGURE 2–97



Section 2–6 Power Supply Filters and Regulators

22. A certain rectifier filter produces a dc output voltage of 75 V with a peak-to-peak ripple voltage of 0.5 V. Calculate the ripple factor.

23. A certain full-wave rectifier has a peak output voltage of 30 V. A 50 μF capacitor-input filter is connected to the rectifier. Calculate the peak-to-peak ripple and the dc output voltage developed across a 600 Ω load resistance.

24. What is the percentage of ripple for the rectifier filter in Problem 23?

25. What value of filter capacitor is required to produce a 1% ripple factor for a full-wave rectifier having a load resistance of 1.5 kΩ? Assume the rectifier produces a peak output of 18 V.

26. A full-wave rectifier produces an 80 V peak rectified voltage from a 60 Hz ac source. If a 10 μF filter capacitor is used, determine the ripple factor for a load resistance of 10 kΩ.

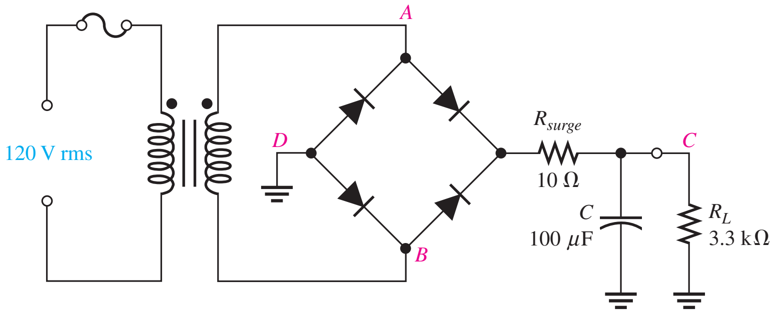
27. Determine the peak-to-peak ripple and dc output voltages in Figure 2–98. The transformer has a 36 V rms secondary voltage rating, and the line voltage has a frequency of 60 Hz.

28. Refer to Figure 2–98 and draw the following voltage waveforms in relationship to the input waveforms: V_{AB}, V_{AD}, and V_{CD}. A double letter subscript indicates a voltage from one point to another.

29. If the no-load output voltage of a regulator is 15.5 V and the full-load output is 14.9 V, what is the percent load regulation?

30. Assume a regulator has a percent load regulation of 0.5%. What is the output voltage at full-load if the unloaded output is 12.0 V?

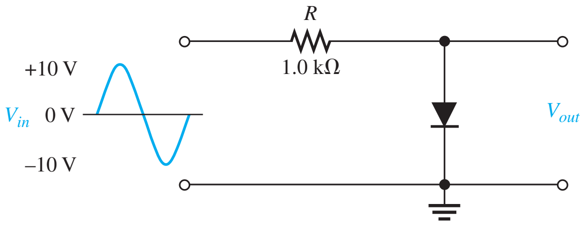
FIGURE 2–98



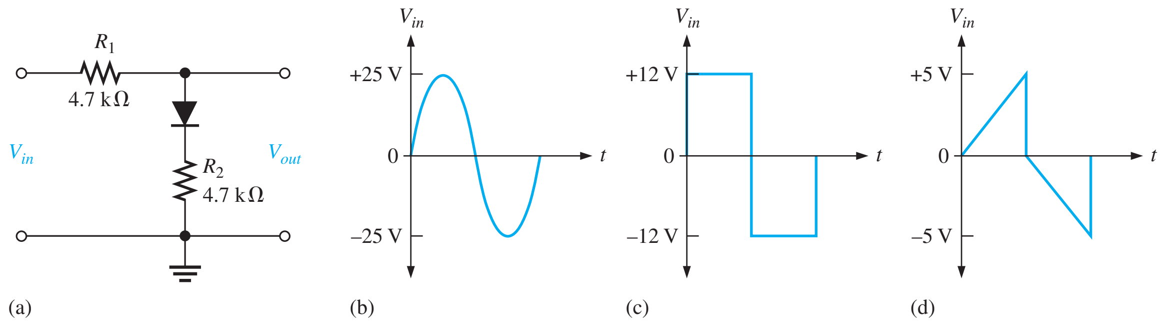
Section 2–7 Diode Limiters and Clampers

31. Determine the output waveform for the circuit of Figure 2–99.

FIGURE 2–99



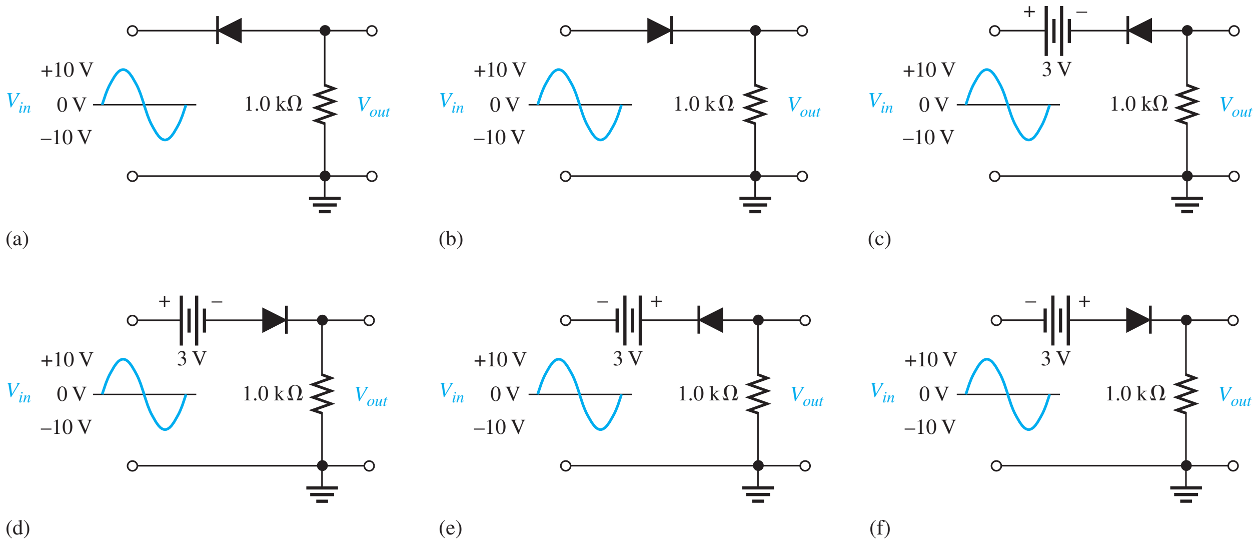
32. Determine the output voltage for the circuit in Figure 2–100(a) for each input voltage in (b), (c), and (d).



R_1
4.7 kΩ
V_{in}
R_2
4.7 kΩ
V_{out}
V_{in}
+25 V
0
–25 V
t
+12 V
–12 V
+5 V
–5 V
(a)
(b)
(c)
(d)

▲ FIGURE 2–100

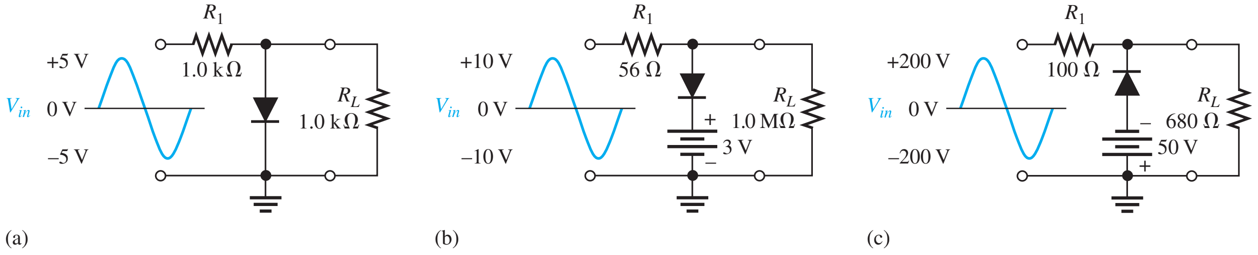
33. Determine the output voltage waveform for each circuit in Figure 2–101.



+10 V
V_{in}
0 V
–10 V
1.0 kΩ
V_{out}
3 V
+
–
(a)
(b)
(c)
(d)
(e)
(f)

▲ FIGURE 2–101

34. Determine the R_L voltage waveform for each circuit in Figure 2–102.



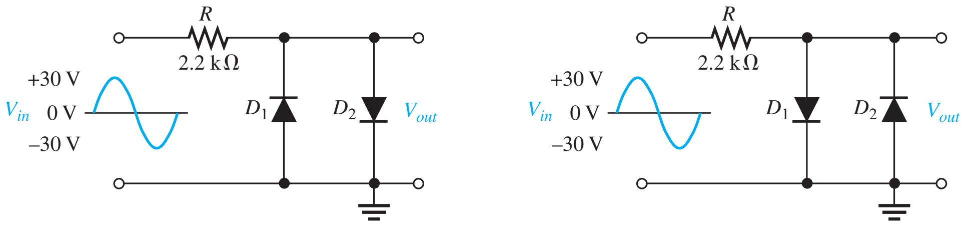
R_1
+5 V
1.0 kΩ
V_{in}
0 V
–5 V
R_L
1.0 kΩ
(a)
+10 V
56 Ω
1.0 MΩ
3 V
–10 V
(b)
+200 V
100 Ω
680 Ω
50 V
–200 V
(c)

▲ FIGURE 2–102

35. Draw the output voltage waveform for each circuit in Figure 2–103.

36. Determine the peak forward current through each diode in Figure 2–103.

▶ **FIGURE 2–103**

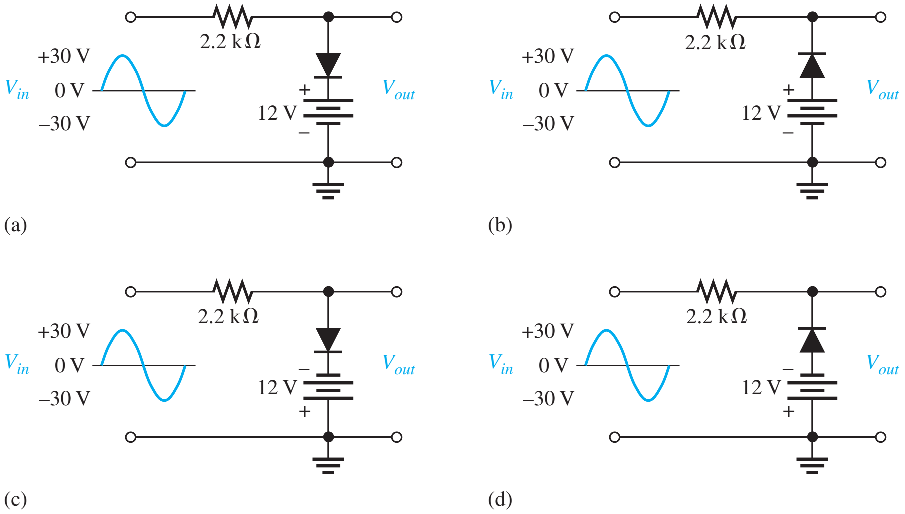

R
2.2 kΩ
+30 V
V_{in}
0 V
–30 V
D_1
D_2
V_{out}
R
2.2 kΩ
+30 V
V_{in}
0 V
–30 V
D_1
D_2
V_{out}

(a) (b)

37. Determine the peak forward current through each diode in Figure 2–104.

38. Determine the output voltage waveform for each circuit in Figure 2–104.

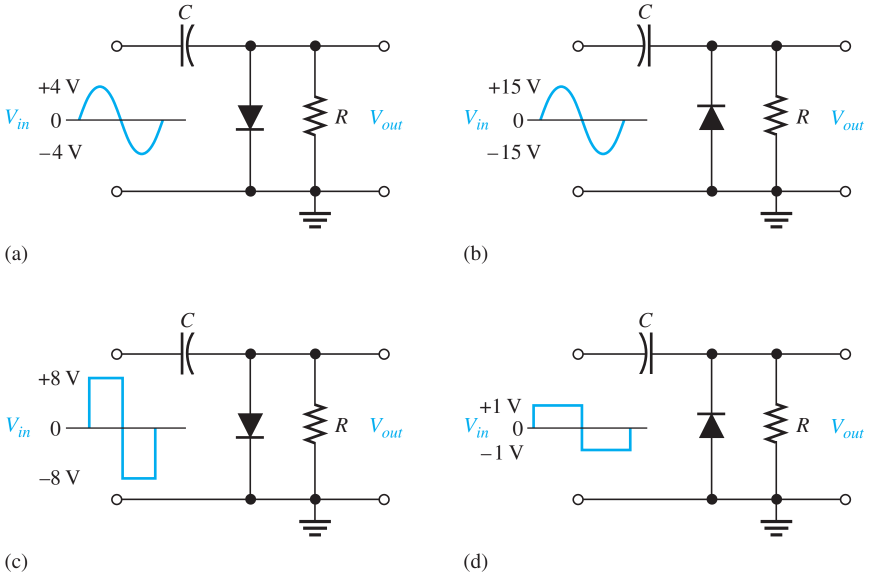
▶ **FIGURE 2–104**


2.2 kΩ
+30 V
V_{in}
0 V
–30 V
+
12 V
–
V_{out}
(a)
2.2 kΩ
+30 V
V_{in}
0 V
–30 V
+
12 V
–
V_{out}
(b)
2.2 kΩ
+30 V
V_{in}
0 V
–30 V
–
12 V
+
V_{out}
(c)
2.2 kΩ
+30 V
V_{in}
0 V
–30 V
–
12 V
+
V_{out}
(d)

39. Describe the output waveform of each circuit in Figure 2–105. Assume the *RC* time constant is much greater than the period of the input.

40. Repeat Problem 39 with the diodes turned around.

▶ **FIGURE 2–105**


C
+4 V
V_{in}
0
–4 V
R
V_{out}
(a)
C
+15 V
V_{in}
0
–15 V
R
V_{out}
(b)
C
+8 V
V_{in}
0
–8 V
R
V_{out}
(c)
C
+1 V
V_{in}
0
–1 V
R
V_{out}
(d)

Section 2–8 Voltage Multipliers

41. A certain voltage doubler has 20 V rms on its input. What is the output voltage? Draw the circuit, indicating the output terminals and PIV rating for the diode.

42. Repeat Problem 41 for a voltage tripler and quadrupler.

Section 2–9 The Diode Datasheet

43. From the datasheet in Figure 2–71, determine how much peak inverse voltage that a 1N4002 diode can withstand.

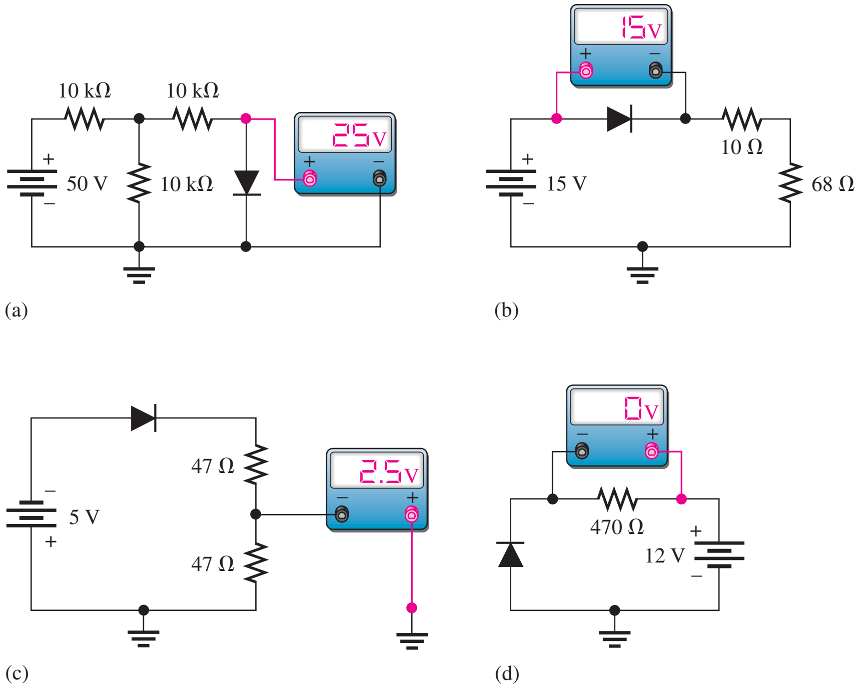
44. Repeat Problem 43 for a 1N4007.

45. If the peak output voltage of a bridge full-wave rectifier is 50 V, determine the minimum value of the load resistance that can be used when 1N4002 diodes are used.

Section 2–10 Troubleshooting

46. Consider the meter indications in each circuit of Figure 2–106, and determine whether the diode is functioning properly, or whether it is open or shorted. Assume the ideal model.

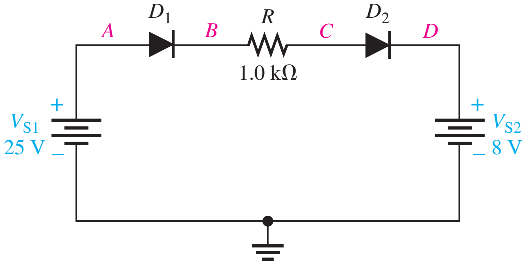
▶ FIGURE 2–106



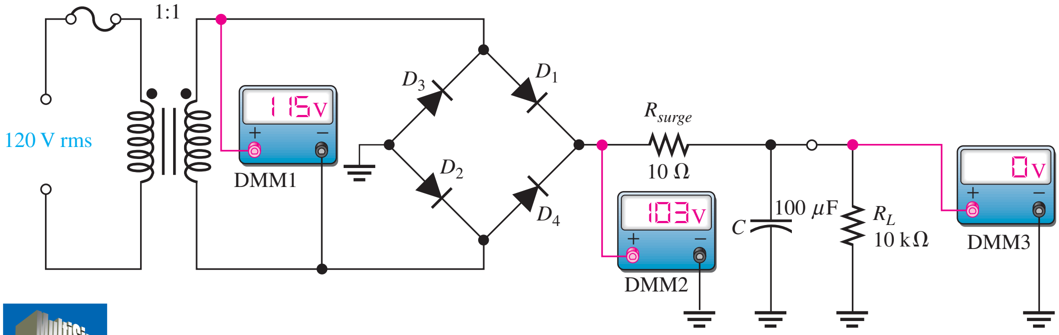
47. Determine the voltage with respect to ground at each point in Figure 2–107. Assume the practical model.

48. If one of the diodes in a bridge rectifier opens, what happens to the output?

▶ FIGURE 2–107

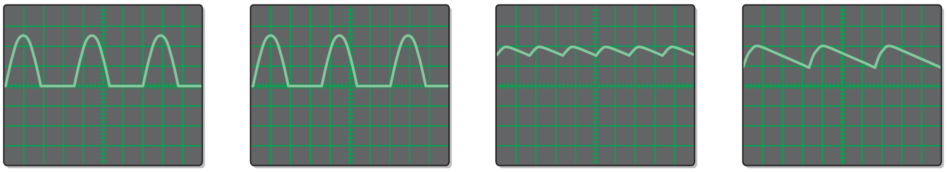


49. From the meter readings in Figure 2–108, determine if the rectifier is functioning properly. If it is not, determine the most likely failure(s).



▲ FIGURE 2–108

50. Each part of Figure 2–109 shows oscilloscope displays of various rectifier output voltages. In each case, determine whether or not the rectifier is functioning properly and if it is not, determine the most likely failure(s).



(a) Output of a half-wave unfiltered rectifier

(b) Output of a full-wave unfiltered rectifier

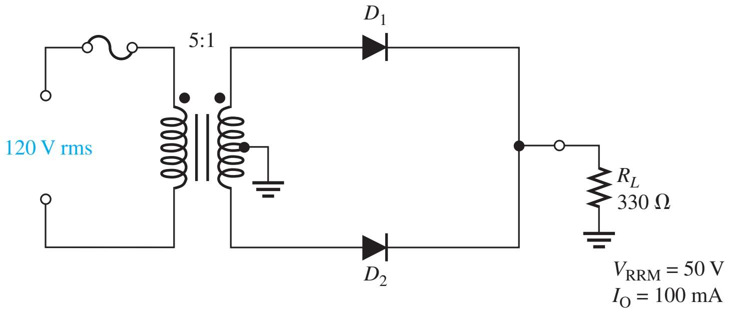
(c) Output of a full-wave filter

(d) Output of same full-wave filter as part (c)

▲ FIGURE 2–109

51. Based on the values given, would you expect the circuit in Figure 2–110 to fail? If so, why?

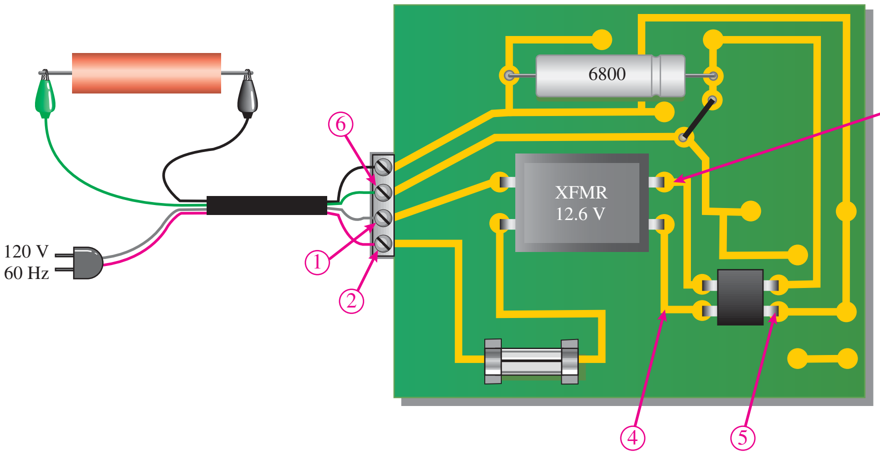
▶ FIGURE 2–110



APPLICATION ACTIVITY PROBLEMS

52. Determine the most likely failure(s) in the circuit of Figure 2–111 for each of the following symptoms. State the corrective action you would take in each case. The transformer has a rated output of 10 V rms.

- **(a)** No voltage from test point 1 to test point 2
- **(b)** No voltage from test point 3 to test point 4
- **(c)** 8 V rms from test point 3 to test point 4
- **(d)** Excessive 120 Hz ripple voltage at test point 6
- **(e)** There is a 60 Hz ripple voltage at test point 6
- **(f)** No voltage at test point 6



▲ FIGURE 2–111

53. In testing the power supply circuit in Figure 2–111 with a 10 kΩ load resistor connected, you find the voltage at the positive side of the filter capacitor to have a 60 Hz ripple voltage. You replace the bridge rectifier and check the point again but it still has the 60 Hz ripple. What now?

54. Suppose the bridge rectifier in Figure 2–111 is connected backwards such that the transformer secondary is now connected to the output pins instead of the input pins. What will be observed at test point 6?

ADVANCED PROBLEMS

55. A full-wave rectifier with a capacitor-input filter provides a dc output voltage of 35 V to a 3.3 kΩ load. Determine the minimum value of filter capacitor if the maximum peak-to-peak ripple voltage is to be 0.5 V.

56. A certain unfiltered full-wave rectifier with 120 V, 60 Hz input produces an output with a peak of 15 V. When a capacitor-input filter and a 1.0 kΩ load are connected, the dc output voltage is 14 V. What is the peak-to-peak ripple voltage?

57. For a certain full-wave rectifier, the measured surge current in the capacitor filter is 50 A. The transformer is rated for a secondary voltage of 24 V with a 120 V, 60 Hz input. Determine the value of the surge resistor in this circuit.

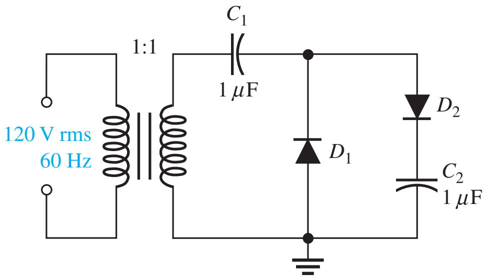
58. Design a full-wave rectifier using an 18 V center-tapped transformer. The output ripple is not to exceed 5% of the output voltage with a load resistance of 680 Ω. Specify the $I_{F(AV)}$ and PIV ratings of the diodes and select an appropriate diode from the datasheet in Figure 2–71.

59. Design a filtered power supply that can produce dc output voltages of +9 V ± 10% and −9 V ± 10% with a maximum load current of 100 mA. The voltages are to be switch selectable across one set of output terminals. The ripple voltage must not exceed 0.25 V rms.

60. Design a circuit to limit a 20 V rms sinusoidal voltage to a maximum positive amplitude of 10 V and a maximum negative amplitude of −5 V using a single 14 V dc voltage source.

61. Determine the voltage across each capacitor in the circuit of Figure 2–112.

▶ FIGURE 2–112



MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

62. Open file TSP02-62 and determine the fault.

63. Open file TSP02-63 and determine the fault.

64. Open file TSP02-64 and determine the fault.

65. Open file TSP02-65 and determine the fault.

66. Open file TSP02-66 and determine the fault.

67. Open file TSP02-67 and determine the fault.

68. Open file TSP02-68 and determine the fault.

69. Open file TSP02-69 and determine the fault.

70. Open file TSP02-70 and determine the fault.

71. Open file TSP02-71 and determine the fault.

72. Open file TSP02-72 and determine the fault.

73. Open file TSP02-73 and determine the fault.

74. Open file TSP02-74 and determine the fault.

75. Open file TSP02-75 and determine the fault.

76. Open file TSP02-76 and determine the fault.

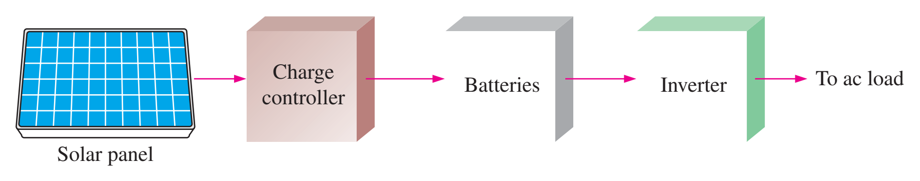
77. Open file TSP02-77 and determine the fault.

78. Open file TSP02-78 and determine the fault.

79. Open file TSP02-79 and determine the fault.

GreenTech Application 2: *Solar Power*

In GreenTech Application 1, the photovoltaic cell and a basic solar power system were introduced. The block diagram is shown again in Figure GA2–1. You learned that the basic components of a solar-powered system were the solar panel, the charge controller, the batteries, and the inverter. Now we will continue the solar power coverage by focusing on the charge controller and batteries.



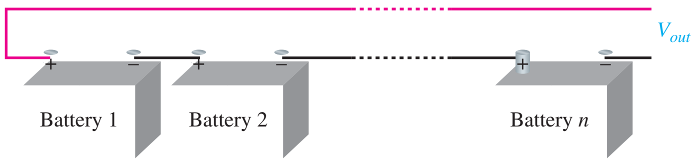
◀ **FIGURE GA2–1**

The Batteries

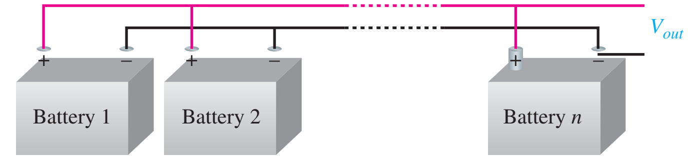
Deep-cycle (deep discharge) sealed lead-acid batteries are the most common batteries in solar power systems because their initial cost is lower and they are readily available. Unlike automobile batteries, which are shallow-cycle, deep-cycle batteries can be repeatedly discharged by as much as 80 percent of their capacity, although they will have a longer life if the cycles are shallower.

Deep-cycle batteries are required in solar power systems simply because the sunlight is not at its maximum all of the time—it is an intermittent energy source. When the light intensity from the sun decreases because of clouds or goes away entirely at night, the output from a solar panel drops drastically or goes to zero. During the periods of low light or no light, the batteries will discharge significantly when a load is connected. Typically, the voltage output of a solar panel must be at least 13.6 V to charge a 12 V battery. Solar panels are usually rated at voltages higher than the nominal output. For example, most 12 V solar panels produce 16 V to 20 V at optimal light conditions. The higher voltage outputs are necessary so that the solar panel will still produce a sufficient charging voltage during some nonoptimal conditions.

Battery Connections Batteries can be connected in series to increase the output voltage and in parallel to increase the ampere-hour capacity, as illustrated in Figure GA2–2 for any number of batteries. Several series connections of batteries can be connected in parallel to achieve both an increase in amp-hrs and output voltage. For example, assume a system uses 12 V, 200 Ah batteries. If the system requires 12 V and 600 Ah, three parallel-connected batteries are used. If the system requires 24 V and 200 Ah, two series-connected batteries are used. If 24 V and 600 Ah are needed, three pairs of series batteries are connected in parallel.



(a) Series batteries



(b) Parallel batteries

◀ **FIGURE GA2–2**

The Charge Controller

A solar charge controller is needed in solar power systems that use batteries to store the energy, with the exception of very low-power systems. The solar charge controller regulates the power from the solar panels primarily to prevent overcharging the batteries. Overcharging batteries reduce battery life and may damage the batteries.

Generally, there is no need for a charge controller with trickle-charge solar panels, such as those that produce five watts or less. A good rule-of-thumb is that if the solar panel produces about two watts or less for each 50 battery amp-hrs (Ah), then you don't need one. A charge controller is required if the solar panel produces more than two watts for each 50 Ah of battery rating. For example, a 12 V battery rated at 120 Ah will not require a charge controller, as the following calculation shows, because the solar power is less than 5 W.

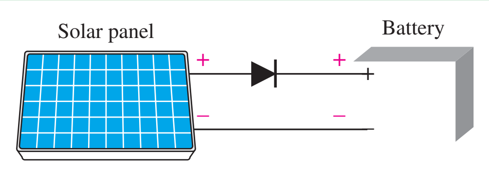
$$\left(\frac{\text{Specified Ah}}{50\text{ Ah}}\right)2\text{ W} = \text{Solar panel power}$$

$$\left(\frac{120\text{ Ah}}{50\text{ Ah}}\right)2\text{ W} = (2.4)2\text{ W} = \mathbf{4.8\text{ W}}$$

In this case, the charging circuit is shown in Figure GA2–3. The diode prevents the battery from discharging back through the solar panel when the panel voltage drops below the battery voltage. For example, when the solar panel is producing 16 V, the diode is forward-biased and the battery is charging. When the battery voltage is 12 V and the panel output drops to less than 12.7 V, the diode is reverse-biased and the battery cannot discharge back through the solar cells.

▶ FIGURE GA2–3

Simple trickle charging in a small solar system (less than 5 W).

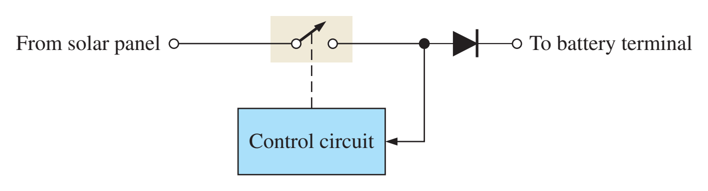


For solar systems of more than about 5 W, a charge controller is necessary. Basically, charge controllers regulate the 16–20 V output of the typical 12 V solar panel down to what the battery needs depending on the amount of battery charge, the type of battery, and the temperature. Solar panels produce more voltage at cooler temperatures.

Types of Charge Controllers Three basic types of charge controllers are on/off, PWM, and MPPT. The most basic controller is the *on/off* type, which simply monitors the battery voltage and stops the charging when the battery voltage reaches a specified level in order to prevent overcharging. It then restarts the charging once the battery voltage drops below a predetermined value. Figure GA2–4 shows the basic concept. The switch shown represents a transistor that is turned on and off. (You will study transistors beginning in Chapter 4.) The voltage of the battery is fed back to the control circuit. When the voltage is below a set low value, the control circuit turns the switch *on* to charge the battery. When the battery charges to a set high value, the control circuit turns the switch *off*. The diode prevents discharge back through the control circuit when the output of the panel is lower than the battery.

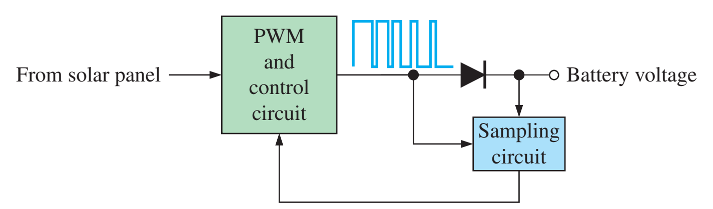
▶ FIGURE GA2–4

Basic concept of the on/off charge controller.

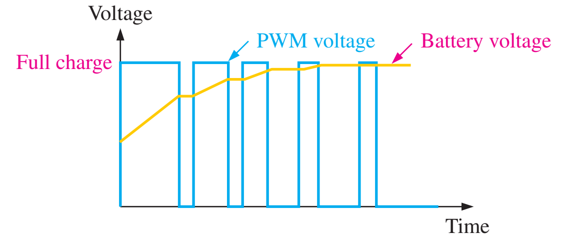


PWM (pulse width modulation) charge controllers gradually reduce the amount of power applied to the batteries as the batteries get closer to full charge. This type of controller allows the batteries to be more fully charged with less stress on the batteries. This extends the life of the batteries and constantly maintains the batteries in a fully charged state (called "float") during sunlight hours. The PWM controller produces a series of pulses to charge the batteries instead of a constant charge. The battery voltage is constantly monitored to determine how to adjust the frequency of the pulses and the pulse widths. When the batteries are fully charged and there is no load to drain them, the controller produces very short pulses at a low rate or no pulses at all. When the batteries are discharged, long pulses at a high rate are sent or the controller may go into a constant-charging mode, depending on the amount of discharge.

Figure GA2–5 shows the basic concept of a PWM charge controller. In part (a), the PWM and control circuit produces pulses based on the input from the sampling circuit. The sampling circuit determines the actual battery voltage by sampling the voltage between pulses. The diode acts as a rectifier and also blocks discharge of the battery back through the charger at night. Part (b) demonstrates how the battery charges during each pulse and how the width and the time between pulses change as the battery charges.



(a) Block diagram



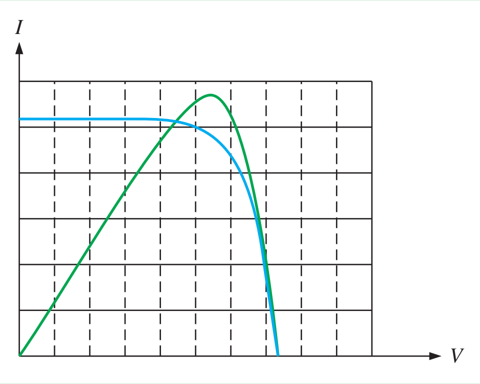
(b) Waveforms

FIGURE GA2–5

Basic concept of a PWM charge controller.

As you have learned, the output voltage of a solar panel varies greatly with the amount of sunlight and with the air temperature. For this reason, solar panels with voltage ratings higher than the battery voltage must be used in order to provide sufficient charging voltage to the battery under less than optimum conditions. As mentioned earlier, a 12 V solar panel may produce 20 V under optimum conditions but can produce only a certain amount of current. For example, if a solar panel can produce 8 A at 20 V, it is rated at 160 W. Batteries like to be charged at a voltage a little higher than their rated voltage. If a 12 V battery is being charged at 14 V, and it is drawing the maximum 8 A from the solar panel, the power delivered to the battery is $8\text{ A} \times 14\text{ V} = 112\text{ W}$ instead of the 160 W produced by the solar panel at 20 V. The batteries only stored 70% of the available energy because the 12 V battery cannot operate at 20 V.

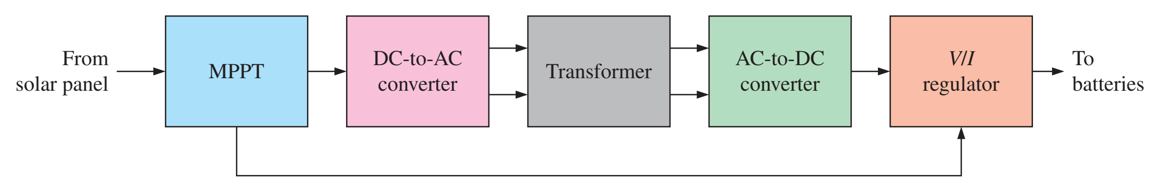
MPPT (maximum power point tracker) charge controllers eliminate much of the energy loss found in the other types of controllers and produce much higher efficiencies. The MPPT continuously tracks the input voltage and current from the solar panel to determine when the peak input power occurs and then adjusts the voltage to the battery to optimize the charging. This results in a maximum power transfer from the solar panel to the battery. In Figure GA2–6, the blue curve is the voltage-current characteristic for a certain solar panel under a specified condition of incident light. The green curve is the power showing where the peak occurs, which is in the knee of the *V-I* curve. If the incident light decreases, the curves will shift down.



▶ FIGURE GA2–6

Example of a solar panel *V-I* and power curves.

The MPPT is basically a DC-to-DC converter. A simplified block diagram showing the basic functional concept is shown in Figure GA2–7. Although there are several ways in which the MPPT can be implemented, the figure illustrates the basic functions. The DC/AC converter, the transformer, and the AC/DC converter isolate the dc input from the dc output, so the output can be adjusted for maximum power. For example, if a 160 W solar panel produces 20 V at 8 A, it needs to be reduced to approximately 13.6 V to charge a 12 V battery. A normal charger will not be able to provide more than 8 A at 13.6 V (or 109 W), which means the panel is not being used efficiently and only 76% of the available power from the solar panel is used. An MPPT charge controller can supply about 11 A at 13.6 V (150 W), thus decreasing the charging time and producing a better match between the panel and the battery. In this case, the panel is being used more efficiently because it is able to deliver about 94% of the available power to the battery.



▲ FIGURE GA2–7

Basic concept of an MPPT charge controller.

QUESTIONS

Some questions may require research beyond the content of this coverage. Answers can be found at www.pearsonhighered.com/floyd.

1. Why must deep-cycle batteries be used in solar power systems?
2. Why should a 12 V battery be charged at a higher than its rated voltage?
3. Which type of charge controller is the most efficient?
4. What range in terms of power is commercially available in charge controllers?
5. Two 12 V, 250 Ah batteries are connected in series and then connected in parallel with two more series-connected batteries of the same type. What is the total output voltage and Ah rating of the battery array?

The following websites are recommended for viewing charge controllers in action. Many other websites are also available.

http://www.youtube.com/watch?v=iifz1DxeaDQ

http://www.youtube.com/watch?v=P2XSbDRi6wo

http://www.youtube.com/watch?v=ITDh4aKXd80&feature=related

3 SPECIAL-PURPOSE DIODES

CHAPTER OUTLINE

3–1 The Zener Diode
3–2 Zener Diode Applications
3–3 The Varactor Diode
3–4 Optical Diodes
3–5 Other Types of Diodes
3–6 Troubleshooting
Application Activity
Green Tech Application 3: *Solar Power*

CHAPTER OBJECTIVES

- Describe the characteristics of a zener diode and analyze its operation
- Apply a zener diode in voltage regulation
- Describe the varactor diode characteristic and analyze its operation
- Discuss the characteristics, operation, and applications of LEDs, quantum dots, and photodiodes
- Discuss the basic characteristics of several types of diodes
- Troubleshoot zener diode regulators

KEY TERMS

- Zener diode
- Zener breakdown
- Varactor
- Light-emitting diode (LED)
- Electroluminescence
- Pixel
- Photodiode
- Laser

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

Chapter 2 was devoted to general-purpose and rectifier diodes, which are the most widely used types. In this chapter, we will cover several other types of diodes that are designed for specific applications, including the zener, varactor (variable-capacitance), light-emitting, photo, laser, Schottky, tunnel, *pin,* step-recovery, and current regulator diodes.

APPLICATION ACTIVITY PREVIEW

The Application Activity in this chapter is the expansion of the 16 V power supply developed in Chapter 2 into a 12 V regulated power supply with an LED power-on indicator. The new circuit will incorporate a voltage regulator IC, which is introduced in this chapter.

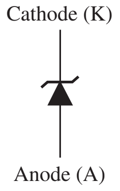
3–1 THE ZENER DIODE

A major application for zener diodes is as a type of voltage regulator for providing stable reference voltages for use in power supplies, voltmeters, and other instruments. In this section, you will see how the zener diode maintains a nearly constant dc voltage under the proper operating conditions. You will learn the conditions and limitations for properly using the zener diode and the factors that affect its performance.

After completing this section, you should be able to

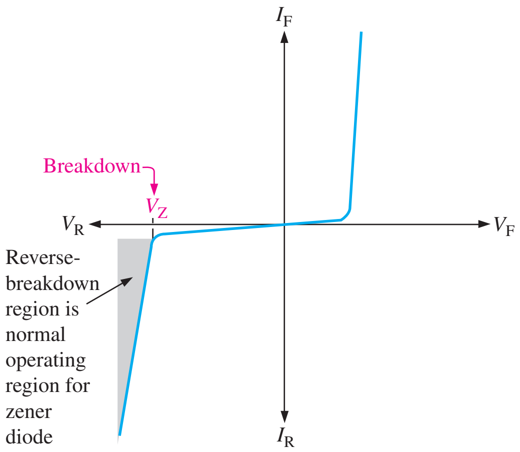
- ❑ **Describe the characteristics of a zener diode and analyze its operation**
- ❑ Recognize a zener diode by its schematic symbol
- ❑ Discuss zener breakdown
    - ◆ Define *avalanche breakdown*
- ❑ Explain zener breakdown characteristics
    - ◆ Describe zener regulation
- ❑ Discuss zener equivalent circuits
- ❑ Define *temperature coefficient*
    - ◆ Analyze zener voltage as a function of temperature
- ❑ Discuss zener power dissipation and derating
    - ◆ Apply power derating to a zener diode
- ❑ Interpret zener diode datasheets

The symbol for a zener diode is shown in Figure 3–1. Instead of a straight line representing the cathode, the zener diode has a bent line that reminds you of the letter Z (for zener). A **zener diode** is a silicon *pn* junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of a zener diode is set by carefully controlling the doping level during manufacture. Recall, from the discussion of the diode characteristic curve in Chapter 2, that when a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically, and this is the key to zener diode operation. This volt-ampere characteristic is shown again in Figure 3–2 with the normal operating region for zener diodes shown as a shaded area.



▲ FIGURE 3–1

Zener diode symbol.



◀ FIGURE 3–2

General zener diode *V-I* characteristic.

Zener Breakdown

Zener diodes are designed to operate in reverse breakdown. Two types of reverse breakdown in a zener diode are *avalanche* and *zener*. The avalanche effect, discussed in Chapter 2, occurs in both rectifier and zener diodes at a sufficiently high reverse voltage. **Zener breakdown** occurs in a zener diode at low reverse voltages. A zener diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (V_Z), the field is intense enough to pull electrons from their valence bands and create current.

Zener diodes with breakdown voltages of less than approximately 5 V operate predominately in zener breakdown. Those with breakdown voltages greater than approximately 5 V operate predominately in **avalanche breakdown.** Both types, however, are called *zener diodes.* Zeners are commercially available with breakdown voltages from less than 1 V to more than 250 V with specified tolerances from 1% to 20%.

HISTORY NOTE

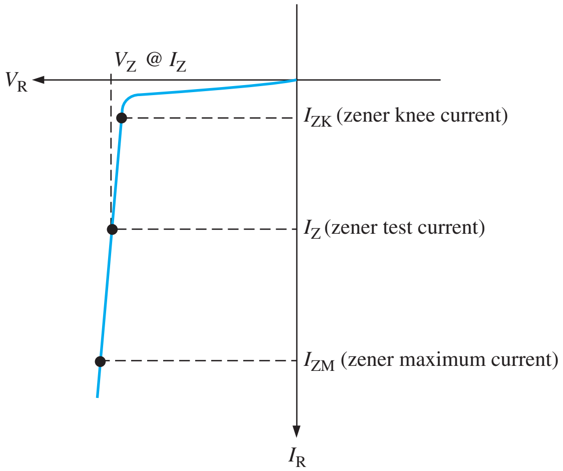
Clarence Melvin Zener, an American physicist, was born in Indianapolis and earned his PhD from Harvard in 1930. He was the first to describe the properties of reverse breakdown that are exploited by the zener diode. As a result, Bell Labs, where the device was developed, named the diode after him. He was also involved in areas of superconductivity, metallurgy, and geometric programming.

Breakdown Characteristics

Figure 3–3 shows the reverse portion of a zener diode's characteristic curve. Notice that as the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the zener breakdown voltage (V_Z) remains essentially constant although it increases slightly as the zener current, I_Z, increases.

▶ **FIGURE 3–3**

Reverse characteristic of a zener diode. V_Z is usually specified at a value of the zener current known as the test current.

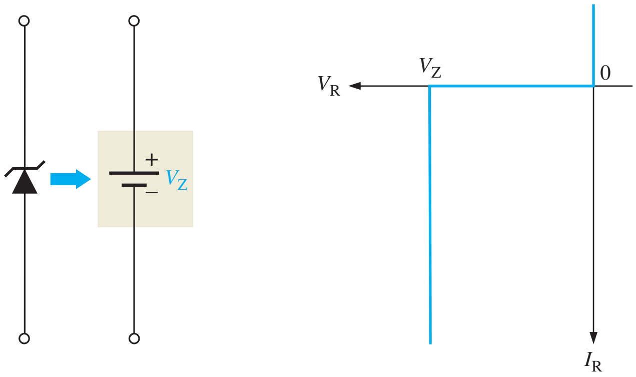


Zener Regulation The ability to keep the reverse voltage across its terminals essentially constant is the key feature of the zener diode. A zener diode operating in breakdown acts as a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse-current values.

A minimum value of reverse current, I_{ZK}, must be maintained in order to keep the diode in breakdown for voltage regulation. You can see on the curve in Figure 3–3 that when the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also, there is a maximum current, I_{ZM}, above which the diode may be damaged due to excessive power dissipation. So, basically, the zener diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from I_{ZK} to I_{ZM}. A nominal zener voltage, V_Z, is usually specified on a datasheet at a value of reverse current called the *zener test current.*

Zener Equivalent Circuits

Figure 3–4 shows the ideal model (first approximation) of a zener diode in reverse breakdown and its ideal characteristic curve. It has a constant voltage drop equal to the nominal zener voltage. This constant voltage drop across the zener diode produced by reverse breakdown is represented by a dc voltage symbol even though the zener diode does not produce a voltage.



(a) Ideal model (b) Ideal characteristic curve

FIGURE 3–4

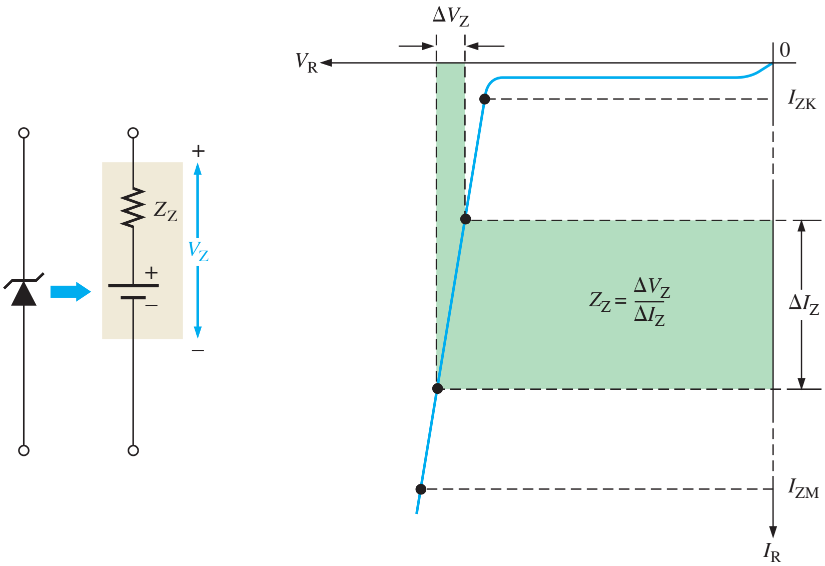
Ideal zener diode equivalent circuit model and the characteristic curve.

Figure 3–5(a) represents the practical model (second approximation) of a zener diode, where the zener impedance (resistance), Z_Z, is included. Since the actual voltage curve is not ideally vertical, a change in zener current (ΔI_Z) produces a small change in zener voltage (ΔV_Z), as illustrated in Figure 3–5(b). By Ohm's law, the ratio of ΔV_Z to ΔI_Z is the impedance, as expressed in the following equation:

$$\mathbf{Z_Z = \frac{\Delta V_Z}{\Delta I_Z}}$$

Equation 3–1

Normally, Z_Z is specified at the zener test current. In most cases, you can assume that Z_Z is a small constant over the full range of zener current values and is purely resistive. It is best to avoid operating a zener diode near the knee of the curve because the impedance changes dramatically in that area.



(a) Practical model (b) Characteristic curve. The slope is exaggerated for illustration.

FIGURE 3–5

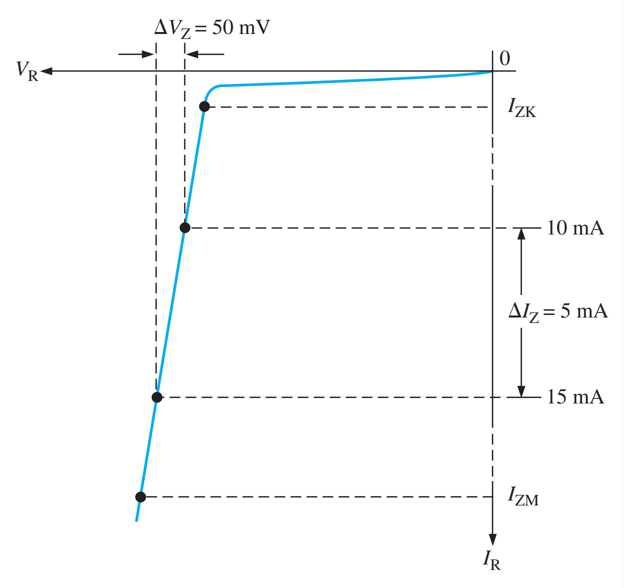
Practical zener diode equivalent circuit and the characteristic curve illustrating Z_Z.

For most circuit analysis and troubleshooting work, the ideal model will give very good results and is much easier to use than more complicated models. When a zener diode is operating normally, it will be in reverse breakdown and you should observe the nominal breakdown voltage across it. Most **schematics** will indicate on the drawing what this voltage should be.

EXAMPLE 3–1

A zener diode exhibits a certain change in V_Z for a certain change in I_Z on a portion of the linear characteristic curve between I_{ZK} and I_{ZM} as illustrated in Figure 3–6. What is the zener impedance?

▶ **FIGURE 3–6**



Solution

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{50\text{ mV}}{5\text{ mA}} = \mathbf{10\ \Omega}$$

Related Problem[*] Calculate the zener impedance if the change in zener voltage is 100 mV for a 20 mA change in zener current on the linear portion of the characteristic curve.

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Temperature Coefficient

The temperature coefficient specifies the percent change in zener voltage for each degree Celsius change in temperature. For example, a 12 V zener diode with a positive temperature coefficient of 0.01%/°C will exhibit a 1.2 mV increase in V_Z when the junction temperature increases one degree Celsius. The formula for calculating the change in zener voltage for a given junction temperature change, for a specified temperature coefficient, is

Equation 3–2

$$\Delta V_Z = V_Z \times TC \times \Delta T$$

where V_Z is the nominal zener voltage at the reference temperature of 25°C, TC is the temperature coefficient, and ΔT is the change in temperature from the reference temperature. A positive TC means that the zener voltage increases with an increase in temperature or decreases with a decrease in temperature. A negative TC means that the zener voltage decreases with an increase in temperature or increases with a decrease in temperature.

In some cases, the temperature coefficient is expressed in mV/°C rather than as %/°C. For these cases, ΔV_Z is calculated as

Equation 3–3

$$\Delta V_Z = TC \times \Delta T$$

EXAMPLE 3–2

An 8.2 V zener diode (8.2 V at 25°C) has a positive temperature coefficient of 0.05%/°C. What is the zener voltage at 60°C?

Solution The change in zener voltage is

$$\begin{aligned}\Delta V_Z = V_Z \times TC \times \Delta T &= (8.2\text{ V})(0.05\%/^\circ\text{C})(60^\circ\text{C} - 25^\circ\text{C})\\ &= (8.2\text{ V})(0.0005/^\circ\text{C})(35^\circ\text{C}) = 144\text{ mV}\end{aligned}$$

Notice that 0.05%/°C was converted to 0.0005/°C. The zener voltage at 60°C is

$$V_Z + \Delta V_Z = 8.2\text{ V} + 144\text{ mV} = \mathbf{8.34\text{ V}}$$

Related Problem A 12 V zener has a positive temperature coefficient of 0.075%/°C. How much will the zener voltage change when the junction temperature decreases 50 degrees Celsius?

Zener Power Dissipation and Derating

Zener diodes are specified to operate at a maximum power called the maximum dc power dissipation, $P_{D(max)}$. For example, the 1N746 zener is rated at a $P_{D(max)}$ of 500 mW and the 1N3305A is rated at a $P_{D(max)}$ of 50 W. The dc power dissipation is determined by the formula,

$$P_D = V_Z I_Z$$

Power Derating The maximum power dissipation of a zener diode is typically specified for temperatures at or below a certain value (50°C, for example). Above the specified temperature, the maximum power dissipation is reduced according to a derating factor. The derating factor is expressed in mW/°C. The maximum derated power can be determined with the following formula:

$$P_{D(derated)} = P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T$$

EXAMPLE 3–3

A certain zener diode has a maximum power rating of 400 mW at 50°C and a derating factor of 3.2 mW/°C. Determine the maximum power the zener can dissipate at a temperature of 90°C.

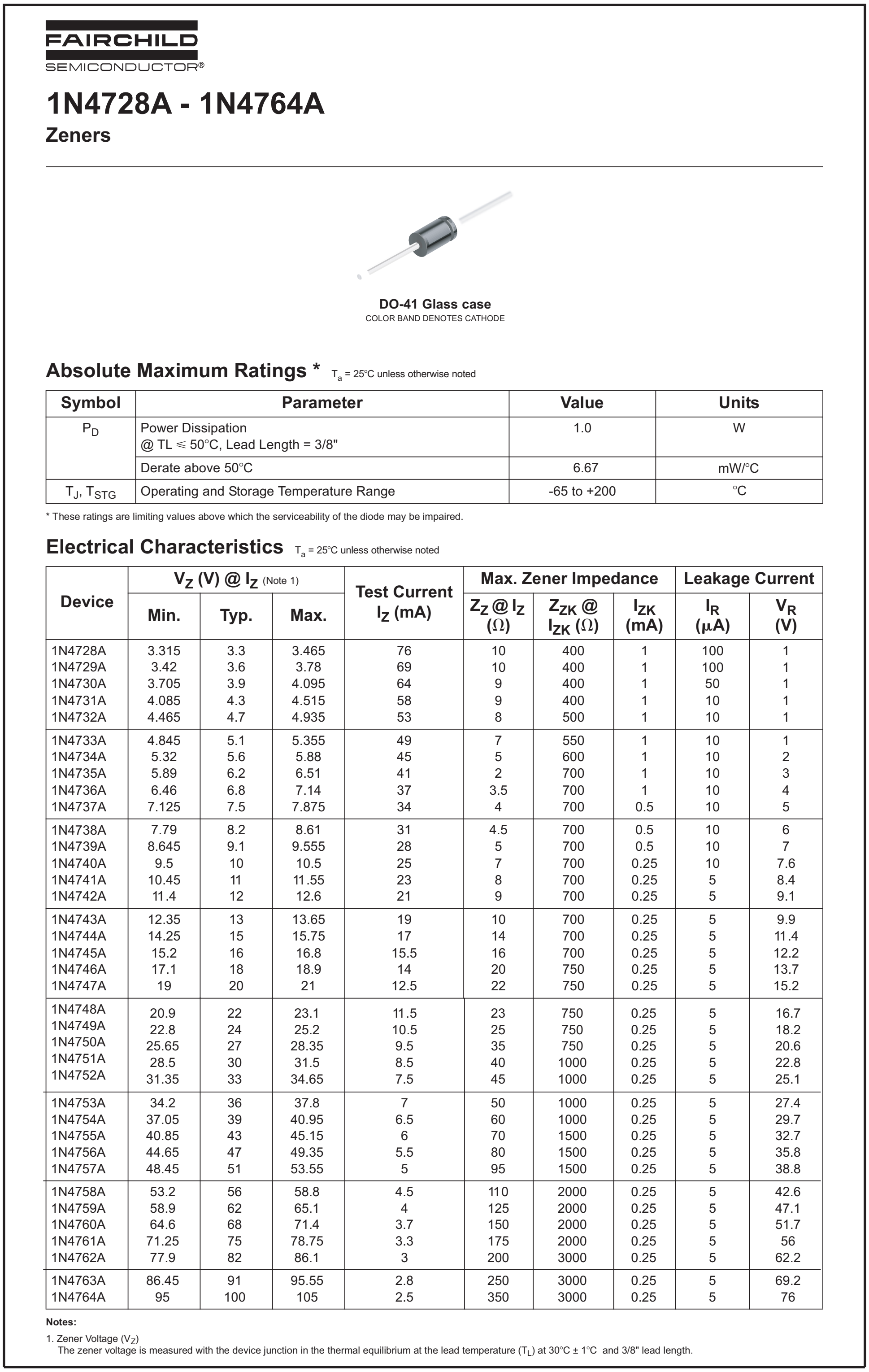
Solution

$$\begin{aligned}P_{D(derated)} &= P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T\\ &= 400\text{ mW} - (3.2\text{ mW}/^\circ\text{C})(90^\circ\text{C} - 50^\circ\text{C})\\ &= 400\text{ mW} - 128\text{ mW} = \mathbf{272\text{ mW}}\end{aligned}$$

Related Problem A certain 50 W zener diode must be derated with a derating factor of 0.5 W/°C above 75°C. Determine the maximum power it can dissipate at 160°C.

Zener Diode Datasheet Information

The amount and type of information found on datasheets for zener diodes (or any category of electronic device) varies from one type of diode to the next. The datasheet for some zeners contains more information than for others. Figure 3–7 gives an example of the type of information you have studied that can be found on a typical datasheet. This particular information is for a zener series, the 1N4728A–1N4764A.



FAIRCHILD
SEMICONDUCTOR®

1N4728A - 1N4764A

Zeners

DO-41 Glass case
COLOR BAND DENOTES CATHODE

Absolute Maximum Ratings * T_a = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
P_D	Power Dissipation @ TL ≤ 50°C, Lead Length = 3/8"	1.0	W
	Derate above 50°C	6.67	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to +200	°C

* These ratings are limiting values above which the serviceability of the diode may be impaired.

Electrical Characteristics T_a = 25°C unless otherwise noted

Device	V_Z (V) @ I_Z (Note 1)			Test Current I_Z (mA)	Max. Zener Impedance			Leakage Current	
	Min.	Typ.	Max.		Z_Z @ I_Z (Ω)	Z_{ZK} @ I_{ZK} (Ω)	I_{ZK} (mA)	I_R (μA)	V_R (V)
1N4728A	3.315	3.3	3.465	76	10	400	1	100	1
1N4729A	3.42	3.6	3.78	69	10	400	1	100	1
1N4730A	3.705	3.9	4.095	64	9	400	1	50	1
1N4731A	4.085	4.3	4.515	58	9	400	1	10	1
1N4732A	4.465	4.7	4.935	53	8	500	1	10	1
1N4733A	4.845	5.1	5.355	49	7	550	1	10	1
1N4734A	5.32	5.6	5.88	45	5	600	1	10	2
1N4735A	5.89	6.2	6.51	41	2	700	1	10	3
1N4736A	6.46	6.8	7.14	37	3.5	700	1	10	4
1N4737A	7.125	7.5	7.875	34	4	700	0.5	10	5
1N4738A	7.79	8.2	8.61	31	4.5	700	0.5	10	6
1N4739A	8.645	9.1	9.555	28	5	700	0.5	10	7
1N4740A	9.5	10	10.5	25	7	700	0.25	10	7.6
1N4741A	10.45	11	11.55	23	8	700	0.25	5	8.4
1N4742A	11.4	12	12.6	21	9	700	0.25	5	9.1
1N4743A	12.35	13	13.65	19	10	700	0.25	5	9.9
1N4744A	14.25	15	15.75	17	14	700	0.25	5	11.4
1N4745A	15.2	16	16.8	15.5	16	700	0.25	5	12.2
1N4746A	17.1	18	18.9	14	20	750	0.25	5	13.7
1N4747A	19	20	21	12.5	22	750	0.25	5	15.2
1N4748A	20.9	22	23.1	11.5	23	750	0.25	5	16.7
1N4749A	22.8	24	25.2	10.5	25	750	0.25	5	18.2
1N4750A	25.65	27	28.35	9.5	35	750	0.25	5	20.6
1N4751A	28.5	30	31.5	8.5	40	1000	0.25	5	22.8
1N4752A	31.35	33	34.65	7.5	45	1000	0.25	5	25.1
1N4753A	34.2	36	37.8	7	50	1000	0.25	5	27.4
1N4754A	37.05	39	40.95	6.5	60	1000	0.25	5	29.7
1N4755A	40.85	43	45.15	6	70	1500	0.25	5	32.7
1N4756A	44.65	47	49.35	5.5	80	1500	0.25	5	35.8
1N4757A	48.45	51	53.55	5	95	1500	0.25	5	38.8
1N4758A	53.2	56	58.8	4.5	110	2000	0.25	5	42.6
1N4759A	58.9	62	65.1	4	125	2000	0.25	5	47.1
1N4760A	64.6	68	71.4	3.7	150	2000	0.25	5	51.7
1N4761A	71.25	75	78.75	3.3	175	2000	0.25	5	56
1N4762A	77.9	82	86.1	3	200	3000	0.25	5	62.2
1N4763A	86.45	91	95.55	2.8	250	3000	0.25	5	69.2
1N4764A	95	100	105	2.5	350	3000	0.25	5	76

Notes:

1. Zener Voltage (V_Z)
The zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature (T_L) at 30°C ± 1°C and 3/8" lead length.

▲ FIGURE 3–7

Partial datasheet for the 1N4728A–1N4764A series 1 W zener diodes. Copyright Fairchild Semiconductor Corporation. Used by permission. Datasheets are available at www.fairchildsemi.com.

Absolute Maximum Ratings The maximum power dissipation, P_D, is specified as 1.0 W up to 50°C. Generally, the zener diode should be operated at least 20% below this maximum to assure reliability and longer life. The power dissipation is derated as shown on the datasheet at 6.67 mW for each degree above 50°C. For example, using the procedure illustrated in Example 3–3, the maximum power dissipation at 60°C is

$$P_D = 1\text{ W} - 10°\text{C}(6.67\text{ mW/°C}) = 1\text{ W} - 66.7\text{ mW} = 0.9933\text{ W}$$

At 125°C, the maximum power dissipation is

$$P_D = 1\text{ W} - 75°\text{C}(6.67\text{ mW/°C}) = 1\text{ W} - 500.25\text{ mW} = 0.4998\text{ W}$$

Notice that a maximum reverse current is not specified but can be determined from the maximum power dissipation for a given value of V_Z. For example, at 50°C, the maximum zener current for a zener voltage of 3.3 V is

$$I_{ZM} = \frac{P_D}{V_Z} = \frac{1\text{ W}}{3.3\text{ V}} = 303\text{ mA}$$

The operating junction temperature, T_J, and the storage temperature, T_{STG}, have a range of from −65°C to 200°C.

Electrical Characteristics The first column in the datasheet lists the zener type numbers, 1N4728A through 1N4764A.

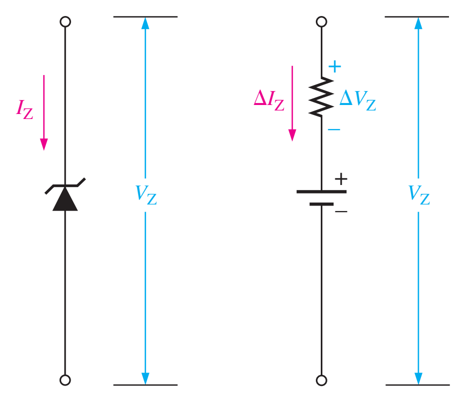
Zener voltage, V_Z, and zener test current, I_Z For each device type, the minimum, typical, and maximum zener voltages are listed. V_Z is measured at the specified zener test current, I_Z. For example, the zener voltage for a 1N4728A can range from 3.315 V to 3.465 V with a typical value of 3.3 V at a test current of 76 mA.

Maximum zener impedance Z_Z is the maximum zener impedance at the specified test current, I_Z. For example, for a 1N4728A, Z_Z is 10 Ω at 76 mA. The maximum zener impedance, Z_{ZK}, at the knee of the characteristic curve is specified at I_{ZK}, which is the current at the knee of the curve. For example, Z_{ZK} is 400 Ω at 1 mA for a 1N4728A.

Leakage current Reverse leakage current is specified for a reverse voltage that is less than the knee voltage. This means that the zener is not in reverse breakdown for these measurements. For example I_R is 100 μA for a reverse voltage of 1 V in a 1N4728A.

EXAMPLE 3–4

From the datasheet in Figure 3–7, a 1N4736A zener diode has a Z_Z of 3.5 Ω. The datasheet gives V_Z = 6.8 V at a test current, I_Z, of 37 mA. What is the voltage across the zener terminals when the current is 50 mA? When the current is 25 mA? Figure 3–8 represents the zener diode.



▲ FIGURE 3–8

Solution For $I_Z = 50$ mA: The 50 mA current is a 13 mA increase above the test current, I_Z, of 37 mA.

$$\Delta I_Z = I_Z - 37\text{ mA} = 50\text{ mA} - 37\text{ mA} = +13\text{ mA}$$
$$\Delta V_Z = \Delta I_Z Z_Z = (13\text{ mA})(3.5\ \Omega) = +45.5\text{ mV}$$

The change in voltage due to the increase in current above the I_Z value causes the zener terminal voltage to increase. The zener voltage for $I_Z = 50$ mA is

$$V_Z = 6.8\text{ V} + \Delta V_Z = 6.8\text{ V} + 45.5\text{ mV} = \mathbf{6.85\ V}$$

For $I_Z = 25$ mA: The 25 mA current is a 12 mA decrease below the test current, I_Z, of 37 mA.

$$\Delta I_Z = -12\text{ mA}$$
$$\Delta V_Z = \Delta I_Z Z_Z = (-12\text{ mA})(3.5\ \Omega) = -42\text{ mV}$$

The change in voltage due to the decrease in current below the test current causes the zener terminal voltage to decrease. The zener voltage for $I_Z = 25$ mA is

$$V_Z = 6.8\text{ V} - \Delta V_Z = 6.8\text{ V} - 42\text{ mV} = \mathbf{6.76\ V}$$

Related Problem Repeat the analysis for $I_Z = 10$ mA and for $I_Z = 30$ mA using a 1N4742A zener with $V_Z = 12$ V at $I_Z = 21$ mA and $Z_Z = 9\ \Omega$.

SECTION 3–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. In what region of their characteristic curve are zener diodes operated?
2. At what value of zener current is the zener voltage normally specified?
3. How does the zener impedance affect the voltage across the terminals of the device?
4. What does a positive temperature coefficient of **0.05%/°C** mean?
5. Explain power derating.

3–2 ZENER DIODE APPLICATIONS

The zener diode can be used as a type of voltage regulator for providing stable reference voltages. In this section, you will see how zeners can be used as voltage references, regulators, and as simple limiters or clippers.

After completing this section, you should be able to

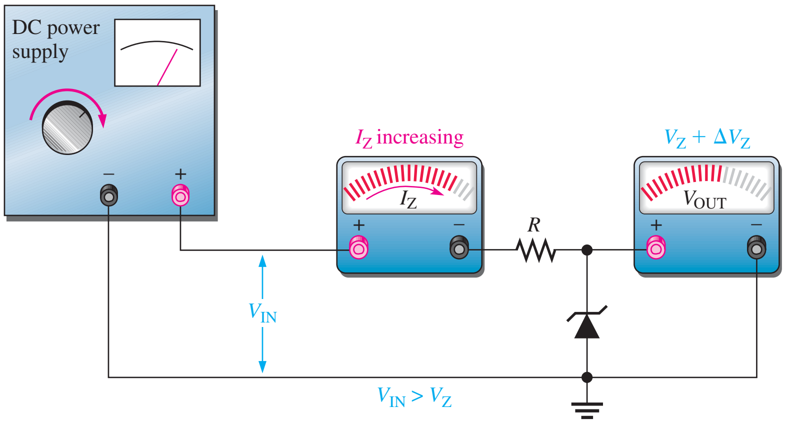
- ❑ **Apply a zener diode in voltage regulation**
- ❑ Analyze zener regulation with a variable input voltage
- ❑ Discuss zener regulation with a variable load
- ❑ Describe zener regulation from no load to full load
- ❑ Discuss zener limiting

Zener Regulation with a Variable Input Voltage

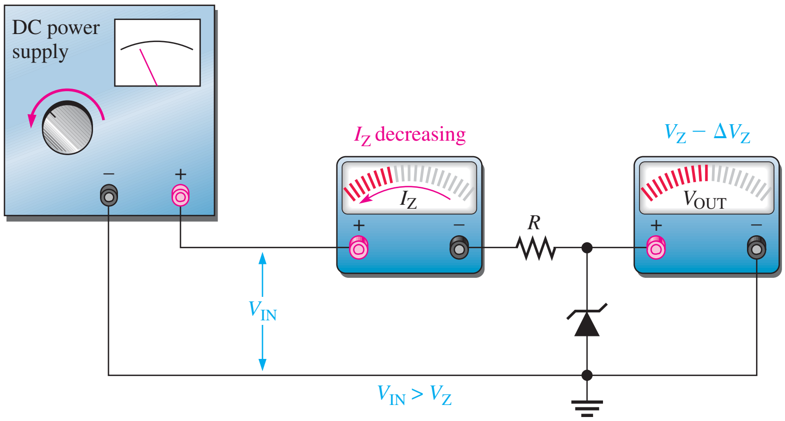
Zener diode regulators can provide a reasonably constant dc level at the output, but they are not particularly efficient. For this reason, they are limited to applications that require only low current to the load. Figure 3–9 illustrates how a zener diode can be used to regulate a dc

FIGURE 3–9

Zener regulation of a varying input voltage.



(a) As the input voltage increases, the output voltage remains nearly constant ($I_{ZK} < I_Z < I_{ZM}$).



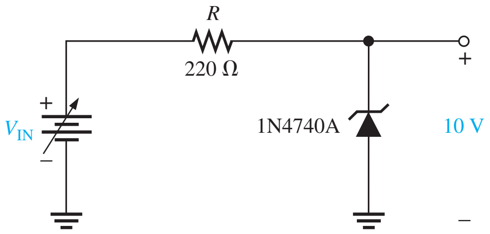
(b) As the input voltage decreases, the output voltage remains nearly constant ($I_{ZK} < I_Z < I_{ZM}$).

voltage. As the input voltage varies (within limits), the zener diode maintains a nearly constant output voltage across its terminals. However, as V_{IN} changes, I_Z will change proportionally so that the limitations on the input voltage variation are set by the minimum and maximum current values (I_{ZK} and I_{ZM}) with which the zener can operate. Resistor R is the series current-limiting resistor. The meters indicate the relative values and trends.

To illustrate regulation, let's use the ideal model of the 1N4740A zener diode (ignoring the zener resistance) in the circuit of Figure 3–10. The absolute lowest current that will maintain regulation is specified at I_{ZK}, which for the 1N4740A is 0.25 mA and represents the no-load current. The maximum current is not given on the datasheet but can be calculated from the power specification of 1 W, which is given on the datasheet. Keep in mind that both the minimum and maximum values are at the operating extremes and represent worst-case operation.

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{10\text{ V}} = 100\text{ mA}$$

FIGURE 3–10



For the minimum zener current, the voltage across the 220 Ω resistor is

$$V_R = I_{ZK}R = (0.25\text{ mA})(220\ \Omega) = 55\text{ mV}$$

Since $V_R = V_{IN} - V_Z$,

$$V_{IN(min)} = V_R + V_Z = 55\text{ mV} + 10\text{ V} = 10.055\text{ V}$$

For the maximum zener current, the voltage across the 220 Ω resistor is

$$V_R = I_{ZM}R = (100\text{ mA})(220\ \Omega) = 22\text{ V}$$

Therefore,

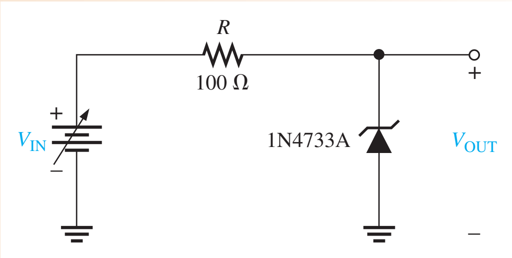
$$V_{IN(max)} = 22\text{ V} + 10\text{ V} = 32\text{ V}$$

This shows that this zener diode can ideally regulate an input voltage from 10.055 V to 32 V and maintain an approximate 10 V output. The output will vary slightly because of the zener impedance, which has been neglected in these calculations.

EXAMPLE 3–5

Determine the minimum and the maximum input voltages that can be regulated by the zener diode in Figure 3–11.

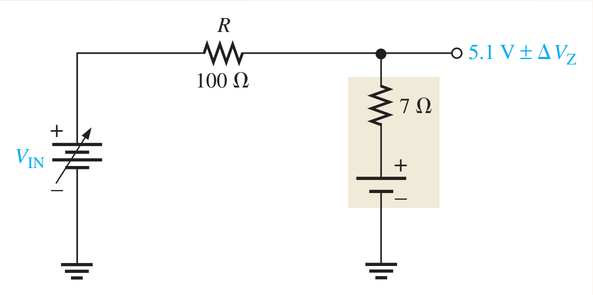
▶ FIGURE 3–11



Solution From the datasheet in Figure 3–7 for the 1N4733A: $V_Z = 5.1$ V at $I_Z = 49$ mA, $I_{ZK} = 1$ mA, and $Z_Z = 7\ \Omega$ at I_Z. For simplicity, assume this value of Z_Z over the range of current values. The equivalent circuit is shown in Figure 3–12.

▶ FIGURE 3–12

Equivalent of circuit in Figure 3–11.



At $I_{ZK} = 1$ mA, the output voltage is

$$V_{OUT} \cong 5.1\text{ V} - \Delta V_Z = 5.1\text{ V} - (I_Z - I_{ZK})Z_Z = 5.1\text{ V} - (49\text{ mA} - 1\text{ mA})(7\ \Omega)$$
$$= 5.1\text{ V} - (48\text{ mA})(7\ \Omega) = 5.1\text{ V} - 0.336\text{ V} = 4.76\text{ V}$$

Therefore,

$$V_{IN(min)} = I_{ZK}R + V_{OUT} = (1\text{ mA})(100\ \Omega) + 4.76\text{ V} = \mathbf{4.86\ V}$$

To find the maximum input voltage, first calculate the maximum zener current. Assume the temperature is 50°C or below; so from Figure 3–7, the power dissipation is 1 W.

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{5.1\text{ V}} = 196\text{ mA}$$

At I_{ZM}, the output voltage is

$$V_{OUT} \cong 5.1\text{ V} + \Delta V_Z = 5.1\text{ V} + (I_{ZM} - I_Z)Z_Z$$
$$= 5.1\text{ V} + (147\text{ mA})(7\ \Omega) = 5.1\text{ V} + 1.03\text{ V} = 6.13\text{ V}$$

Therefore,

$$V_{IN(max)} = I_{ZM}R + V_{OUT} = (196\text{ mA})(100\ \Omega) + 6.13\text{ V} = \mathbf{25.7\ V}$$

Related Problem Determine the minimum and maximum input voltages that can be regulated if a 1N4736A zener diode is used in Figure 3–11.

Open the Multisim file E03-05 in the Examples folder on the companion website. For the calculated minimum and maximum dc input voltages, measure the resulting output voltages. Compare with the calculated values.

Zener Regulation with a Variable Load

Figure 3–13 shows a zener voltage regulator with a variable load resistor across the terminals. The zener diode maintains a nearly constant voltage across R_L as long as the zener current is greater than I_{ZK} and less than I_{ZM}.

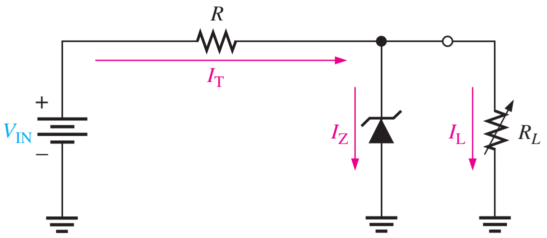


FIGURE 3–13

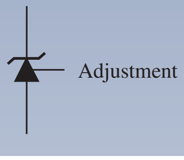
Zener regulation with a variable load.

From No Load to Full Load

When the output terminals of the zener regulator are open ($R_L = \infty$), the load current is zero and *all* of the current is through the zener; this is a no-load condition. When a load resistor (R_L) is connected, part of the total current is through the zener and part through R_L. The total current through R remains essentially constant as long as the zener is regulating. As R_L is decreased, the load current, I_L, increases and I_Z decreases. The zener diode continues to regulate the voltage until I_Z reaches its minimum value, I_{ZK}. At this point the load current is maximum, and a full-load condition exists. The following example will illustrate this.

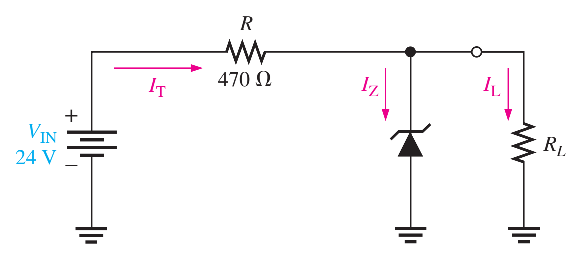
F Y I

One type of temperature sensor uses the zener diode breakdown voltage as a temperature indicator. The breakdown voltage of a zener is directly proportional to the Kelvin temperature. This type of sensor is small, accurate, and linear. The LM125/LM235/LM335 is an integrated circuit that is more complex than a simple zener diode. However, it displays a very precise zener characteristic. In addition to the anode and cathode terminals, this device has an adjustment for calibration purposes. The symbol is shown below.



EXAMPLE 3–6 Determine the minimum and the maximum load currents for which the zener diode in Figure 3–14 will maintain regulation. What is the minimum value of R_L that can be used? $V_Z = 12$ V, $I_{ZK} = 1$ mA, and $I_{ZM} = 50$ mA. Assume an ideal zener diode where $Z_Z = 0\ \Omega$ and V_Z remains a constant 12 V over the range of current values, for simplicity.

▶ FIGURE 3–14



Solution When $I_L = 0$ A ($R_L = \infty$), I_Z is maximum and equal to the total circuit current I_T.

$$I_{Z(max)} = I_T = \frac{V_{IN} - V_Z}{R} = \frac{24\text{ V} - 12\text{ V}}{470\ \Omega} = 25.5\text{ mA}$$

If R_L is removed from the circuit, the load current is 0 A. Since $I_{Z(max)}$ is less than I_{ZM}, 0 A is an acceptable minimum value for I_L because the zener can handle all of the 25.5 mA.

$$I_{L(min)} = \mathbf{0\ A}$$

The maximum value of I_L occurs when I_Z is minimum ($I_Z = I_{ZK}$), so

$$I_{L(max)} = I_T - I_{ZK} = 25.5\text{ mA} - 1\text{ mA} = \mathbf{24.5\ mA}$$

The minimum value of R_L is

$$R_{L(min)} = \frac{V_Z}{I_{L(max)}} = \frac{12\text{ V}}{24.5\text{ mA}} = \mathbf{490\ \Omega}$$

Therefore, if R_L is less than 490 Ω, R_L will draw more of the total current away from the zener and I_Z will be reduced below I_{ZK}. This will cause the zener to lose regulation. Regulation is maintained for any value of R_L between 490 Ω and infinity.

Related Problem Find the minimum and maximum load currents for which the circuit in Figure 3–14 will maintain regulation. Determine the minimum value of R_L that can be used. $V_Z = 3.3$ V (constant), $I_{ZK} = 1$ mA, and $I_{ZM} = 150$ mA. Assume an ideal zener.

Open the Multisim file E03-06 in the Examples folder on the companion website. For the calculated minimum value of load resistance, verify that regulation occurs.

In the last example, we assumed that Z_Z was zero and, therefore, the zener voltage remained constant over the range of currents. We made this assumption to demonstrate the concept of how the regulator works with a varying load. Such an assumption is often acceptable and in many cases produces results that are reasonably accurate. In Example 3–7, we will take the zener impedance into account.

EXAMPLE 3–7

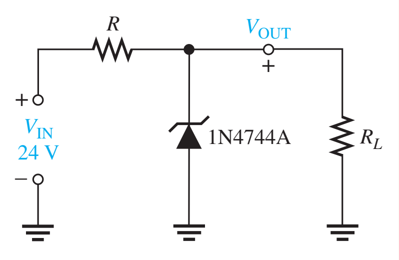
For the circuit in Figure 3–15:

(a) Determine V_{OUT} at I_{ZK} and at I_{ZM}.

(b) Calculate the value of R that should be used.

(c) Determine the minimum value of R_L that can be used.

▶ FIGURE 3–15



Solution The 1N4744A zener used in the regulator circuit of Figure 3–15 is a 15 V diode. The datasheet in Figure 3–7 gives the following information:
$V_Z = 15\text{ V}$ @ $I_Z = 17\text{ mA}$, $I_{ZK} = 0.25\text{ mA}$, and $Z_Z = 14\ \Omega$.

(a) For I_{ZK}:

$$\begin{aligned} V_{OUT} &= V_Z - \Delta I_Z Z_Z = 15\text{ V} - \Delta I_Z Z_Z = 15\text{ V} - (I_Z - I_{ZK})Z_Z \\ &= 15\text{ V} - (16.75\text{ mA})(14\ \Omega) = 15\text{ V} - 0.235\text{ V} = \mathbf{14.76\text{ V}} \end{aligned}$$

Calculate the zener maximum current. The maximum power dissipation is 1 W.

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{15\text{ V}} = 66.7\text{ mA}$$

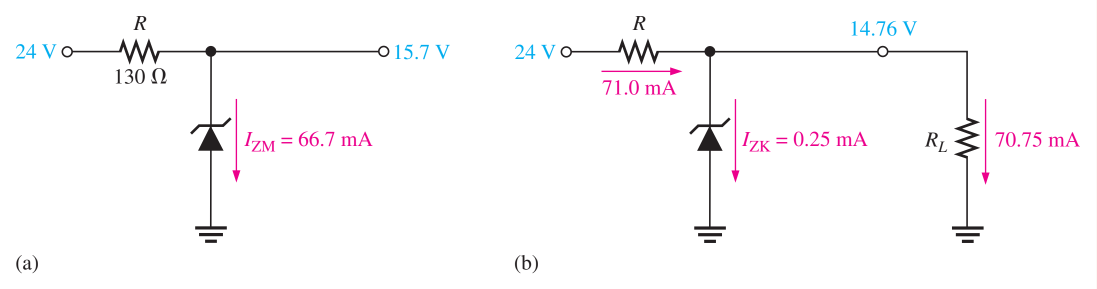
For I_{ZM}:

$$\begin{aligned} V_{OUT} &= V_Z + \Delta I_Z Z_Z = 15\text{ V} + \Delta I_Z Z_Z \\ &= 15\text{ V} + (I_{ZM} - I_Z)Z_Z = 15\text{ V} + (49.7\text{ mA})(14\ \Omega) = \mathbf{15.7\text{ V}} \end{aligned}$$

(b) Calculate the value of R for the maximum zener current that occurs when there is no load as shown in Figure 3–16(a).

$$R = \frac{V_{IN} - V_{OUT}}{I_{ZK}} = \frac{24\text{ V} - 15.7\text{ V}}{66.7\text{ mA}} = 124\ \Omega$$

$R = \mathbf{130\ \Omega}$ (nearest larger standard value).



▲ FIGURE 3–16

(c) For the minimum load resistance (maximum load current), the zener current is minimum ($I_{ZK} = 0.25\text{ mA}$) as shown in Figure 3–16(b).

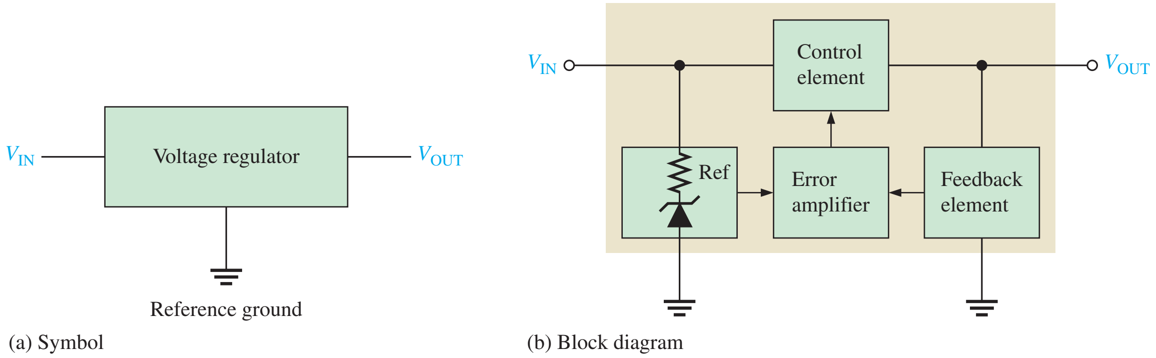
$$I_T = \frac{V_{IN} - V_{OUT}}{R} = \frac{24\text{ V} - 14.76\text{ V}}{130\ \Omega} = 71.0\text{ mA}$$

$$I_L = I_T - I_{ZK} = 71.0\text{ mA} - 0.25\text{ mA} = 70.75\text{ mA}$$

$$R_{L(min)} = \frac{V_{OUT}}{I_L} = \frac{14.76\text{ V}}{70.75\text{ mA}} = \mathbf{209\ \Omega}$$

Related Problem Repeat each part of the preceding analysis if the zener is changed to a 1N4742A 12 V device.

You have seen how the zener diode regulates voltage. Its regulating ability is somewhat limited by the change in zener voltage over a range of current values, which restricts the load current that it can handle. To achieve better regulation and provide for greater variations in load current, the zener diode is combined as a key element with other circuit components to create a 3-terminal linear voltage regulator. Three-terminal voltage regulators that were introduced in Chapter 2 are IC devices that use the zener to provide a reference voltage for an internal amplifier. For a given dc input voltage, the 3-terminal regulator maintains an essentially constant dc voltage over a range of input voltages and load currents. The dc output voltage is always less than the input voltage. The details of this type of regulator are covered in Chapter 17. Figure 3–17 illustrates a basic 3-terminal regulator showing where the zener diode is used.



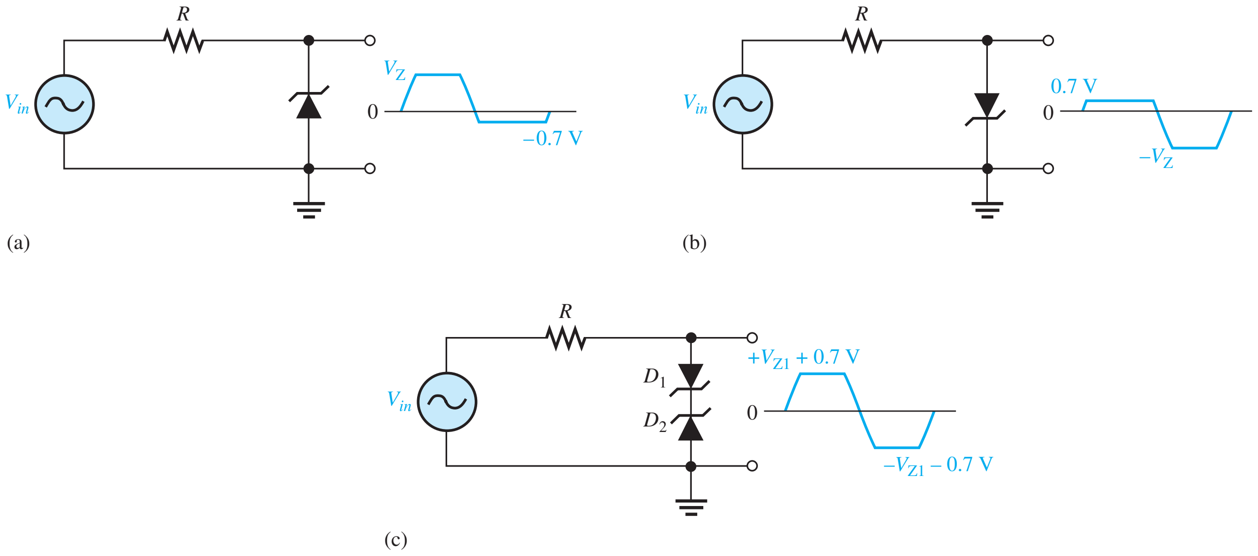
(a) Symbol (b) Block diagram

▲ FIGURE 3–17

Three-terminal voltage regulators.

Zener Limiter

In addition to voltage regulation applications, zener diodes can be used in ac applications to limit voltage swings to desired levels. Figure 3–18 shows three basic ways the limiting action of a zener diode can be used. Part (a) shows a zener used to limit the positive peak of a signal voltage to the selected zener voltage. During the negative alternation, the zener acts as a forward-biased diode and limits the negative voltage to −0.7 V. When the zener



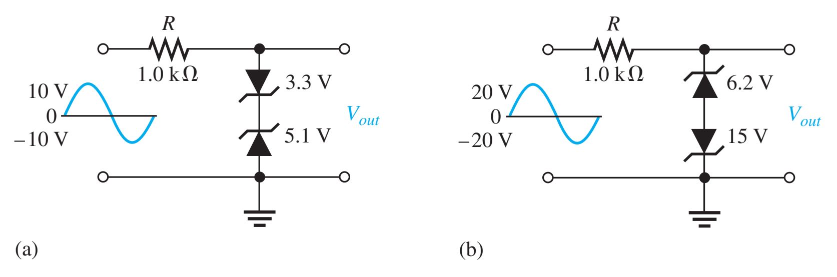
▲ FIGURE 3–18

Basic zener limiting action with a sinusoidal input voltage.

is turned around, as in part (b), the negative peak is limited by zener action and the positive voltage is limited to +0.7 V. Two back-to-back zeners limit both peaks to the zener voltage ±0.7 V, as shown in part (c). During the positive alternation, D_2 is functioning as the zener limiter and D_1 is functioning as a forward-biased diode. During the negative alternation, the roles are reversed.

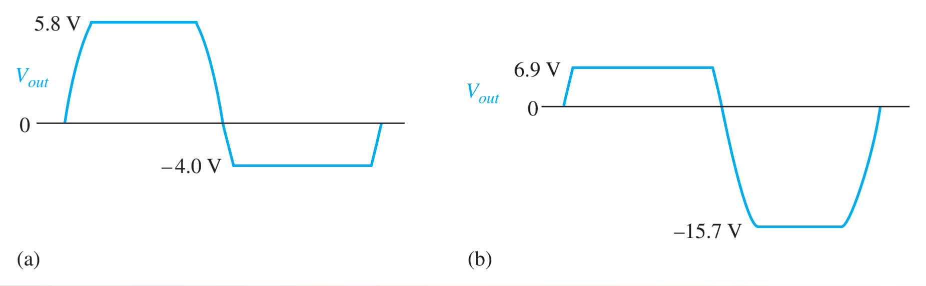
EXAMPLE 3–8

Determine the output voltage for each zener limiting circuit in Figure 3–19.



▲ FIGURE 3–19

Solution See Figure 3–20 for the resulting output voltages. Remember, when one zener is operating in breakdown, the other one is forward-biased with approximately 0.7 V across it.



▲ FIGURE 3–20

Related Problem

(a) What is the output in Figure 3–19(a) if the input voltage is increased to a peak value of 20 V?

(b) What is the output in Figure 3–19(b) if the input voltage is decreased to a peak value of 5 V?

Open the Multisim file E03-08 in the Examples folder on the companion website. For the specified input voltages, measure the resulting output waveforms. Compare with the waveforms shown in the example.

SECTION 3–2 CHECKUP

1. In a zener diode regulator, what value of load resistance results in the maximum zener current?
2. Explain the terms *no load* and *full load*.
3. How much voltage appears across a zener diode when it is forward-biased?

3–3 THE VARACTOR DIODE

The junction capacitance of diodes varies with the amount of reverse bias. Varactor diodes are specially designed to take advantage of this characteristic and are used as voltage-controlled capacitors rather than traditional diodes. These devices are commonly used in communication systems. Varactor diodes are also referred to as *varicaps* or *tuning diodes.*

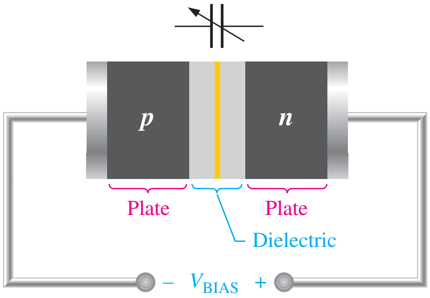
After completing this section, you should be able to

- ❑ **Describe the varactor diode characteristic and analyze its operation**
- ❑ Discuss the basic operation of a varactor
  - ◆ Explain why a reverse-biased varactor acts as a capacitor ◆ Calculate varactor capacitance ◆ Identify the varactor schematic symbol
- ❑ Interpret a varactor diode datasheet
  - ◆ Define and discuss capacitance tolerance range ◆ Define and discuss capacitance ratio ◆ Discuss the back-to-back configuration
- ❑ Discuss and analyze the application of a varactor in a resonant band-pass filter

A **varactor** is a diode that always operates in reverse bias and is doped to maximize the inherent capacitance of the depletion region. The depletion region acts as a capacitor dielectric because of its nonconductive characteristic. The *p* and *n* regions are conductive and act as the capacitor plates, as illustrated in Figure 3–21.

▶ FIGURE 3–21

The reverse-biased varactor diode acts as a variable capacitor.



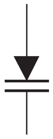
Basic Operation

Recall that capacitance is determined by the parameters of plate area (A), dielectric constant (ϵ), and plate separation (d), as expressed in the following formula:

$$C = \frac{A\epsilon}{d}$$

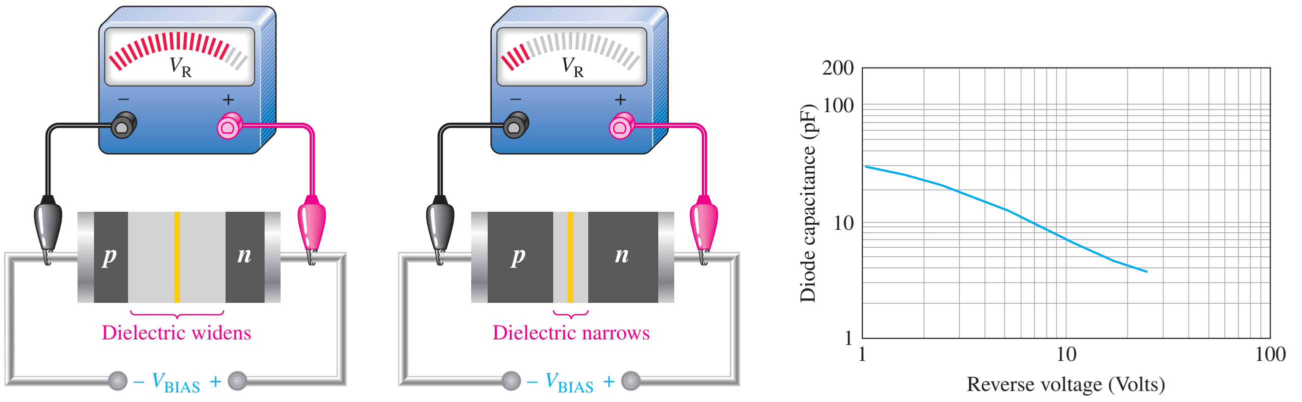
As the reverse-bias voltage increases, the depletion region widens, effectively increasing the plate separation, thus decreasing the capacitance. When the reverse-bias voltage decreases, the depletion region narrows, thus increasing the capacitance. This action is shown in Figure 3–22(a) and (b). A graph of diode capacitance (C_T) versus reverse voltage for a certain varactor is shown in Figure 3–22(c). For this particular device, C_T varies from 30 pF to slightly less than 4 pF as V_R varies from 1 V to 30 V.

In a varactor diode, these capacitance parameters are controlled by the method of doping near the *pn* junction and the size and geometry of the diode's construction. Nominal varactor capacitances are typically available from a few picofarads to several hundred picofarads. Figure 3–23 shows a common symbol for a varactor.



▲ FIGURE 3–23

Varactor diode symbol.



(a) Greater reverse bias, less capacitance

(b) Less reverse bias, greater capacitance

(c) Example of a diode capacitance versus reverse voltage graph

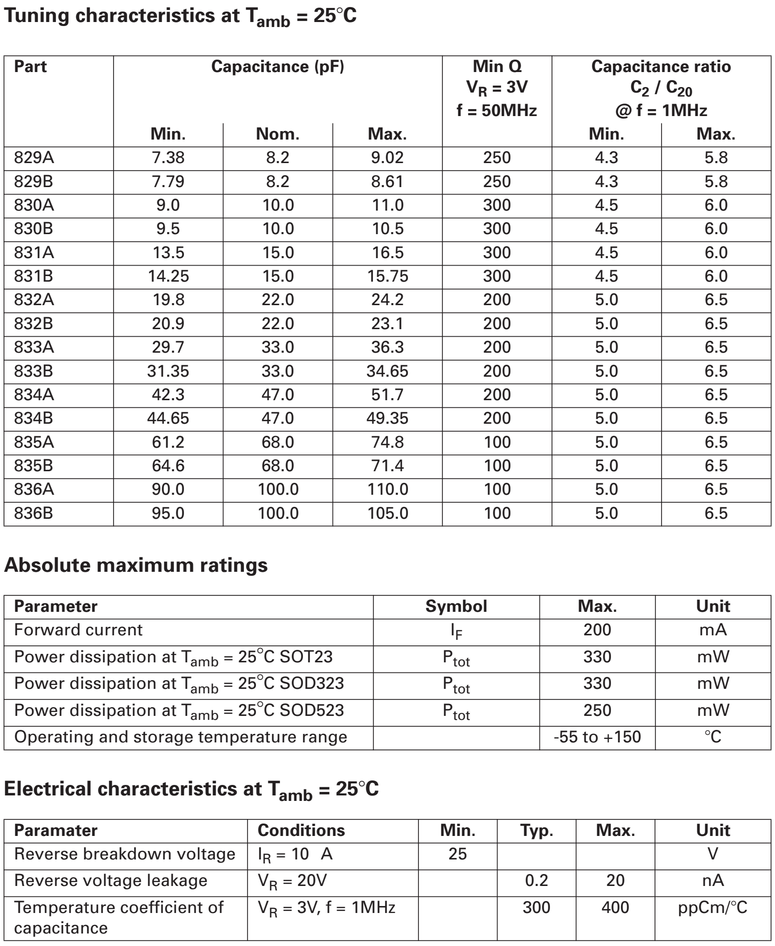
▲ **FIGURE 3–22**

Varactor diode capacitance varies with reverse voltage.

Varactor Datasheet Information

A partial datasheet for a specific series of varactor diode (Zetex 830 series) is shown in Figure 3–24.

Capacitance Tolerance Range The minimum, nominal, and maximum values of capacitance are shown on the datasheet. For example, when reverse-biased at 3 V, the 832A can



Tuning characteristics at T_{amb} = 25°C

Part	Capacitance (pF)			Min Q V_R = 3V f = 50MHz	Capacitance ratio C_2 / C_{20} @ f = 1MHz	
	Min.	Nom.	Max.		Min.	Max.
829A	7.38	8.2	9.02	250	4.3	5.8
829B	7.79	8.2	8.61	250	4.3	5.8
830A	9.0	10.0	11.0	300	4.5	6.0
830B	9.5	10.0	10.5	300	4.5	6.0
831A	13.5	15.0	16.5	300	4.5	6.0
831B	14.25	15.0	15.75	300	4.5	6.0
832A	19.8	22.0	24.2	200	5.0	6.5
832B	20.9	22.0	23.1	200	5.0	6.5
833A	29.7	33.0	36.3	200	5.0	6.5
833B	31.35	33.0	34.65	200	5.0	6.5
834A	42.3	47.0	51.7	200	5.0	6.5
834B	44.65	47.0	49.35	200	5.0	6.5
835A	61.2	68.0	74.8	100	5.0	6.5
835B	64.6	68.0	71.4	100	5.0	6.5
836A	90.0	100.0	110.0	100	5.0	6.5
836B	95.0	100.0	105.0	100	5.0	6.5

Absolute maximum ratings

Parameter	Symbol	Max.	Unit
Forward current	I_F	200	mA
Power dissipation at T_{amb} = 25°C SOT23	P_{tot}	330	mW
Power dissipation at T_{amb} = 25°C SOD323	P_{tot}	330	mW
Power dissipation at T_{amb} = 25°C SOD523	P_{tot}	250	mW
Operating and storage temperature range		-55 to +150	°C

Electrical characteristics at T_{amb} = 25°C

Paramater	Conditions	Min.	Typ.	Max.	Unit
Reverse breakdown voltage	I_R = 10 A	25			V
Reverse voltage leakage	V_R = 20V		0.2	20	nA
Temperature coefficient of capacitance	V_R = 3V, f = 1MHz		300	400	ppCm/°C

◀ **FIGURE 3–24**

Partial datasheet for the Zetex 830 series varactor diodes. Courtesy of Zetex Semiconductors PLC. Datasheets are available at www.datasheetcatalog/zetexsemiconductors/1/.

exhibit a capacitance anywhere between 19.8 pF and 24.2 pF. This tolerance range should not be confused with the range of capacitance values that result from varying the reverse bias as determined by the capacitance ratio.

Capacitance Ratio The varactor **capacitance ratio** is also known as the *tuning ratio*. It is the ratio of the diode capacitance at a minimum reverse voltage to the diode capacitance at a maximum reverse voltage. For the varactor diodes represented in Figure 3–24, the capacitance ratio is the ratio of C measured at a V_R of 2 V divided by C measured at a V_R of 20 V. The capacitance ratio is designated as C_2/C_{20} in this case.

For the 832A, the minimum capacitance ratio is 5.0. This means that the capacitance value decreases by a factor of 5.0 as V_R is increased from 2 V to 20 V. The following calculation illustrates how to use the capacitance ratio (CR) to find the capacitance range for the 832A. If $C_2 = 22$ pF and the minimum $CR = C_2/C_{20} = 5.0$,

$$C_{20} = \frac{C_2}{CR} = \frac{22\text{ pF}}{5} = 4.4\text{ pF}$$

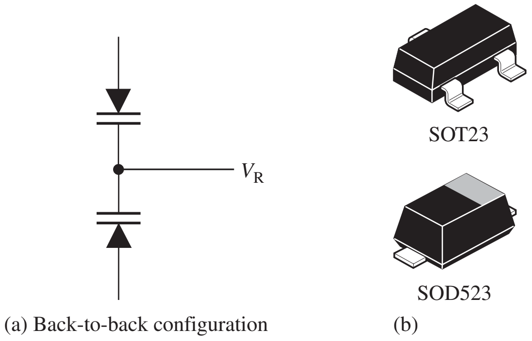
The diode capacitance varies from 22 pF to 4.4 pF when V_R is increased from 2 V to 20 V.

The Zetex 830 series of varactor diodes are hyper-abrupt junction devices. The doping in the n and p regions is made uniform so that at the pn junction there is a very abrupt change from n to p instead of the more gradual change found in the rectifier diodes. The abruptness of the pn junction determines the capacitance ratio.

Back-to-Back Configuration One of the drawbacks of using just a single varactor diode in certain applications, such as rf tuning, is that if the diode is forward-biased by the rf signal during part of the ac cycle, its reverse leakage will increase momentarily. Also, a type of distortion called *harmonic distortion* is produced if the varactor is alternately biased positively and negatively. To avoid harmonic distortion, you will often see two varactor diodes back to back, as shown in Figure 3–25(a) with the reverse dc voltage applied to both devices simultaneously. The two tuning diodes will be driven alternately into high and low capacitance, and the net capacitance will remain constant and is unaffected by the rf signal amplitude. The Zetex 832A varactor diode is available in a back-to-back configuration in an SOT23 package or as a single diode in an SOD523 package, as shown in Figure 3–25(b). Although the cathodes in the back-to-back configuration are connected to a common pin, each diode can also be used individually.

▶ FIGURE 3–25

Varactor diodes and typical packages.



(a) Back-to-back configuration (b)

An Application

A major application of varactors is in tuning circuits. For example, VHF, UHF, and satellite receivers utilize varactors. Varactors are also used in cellular communications. When used in a parallel resonant circuit, as illustrated in Figure 3–26, the varactor acts as a

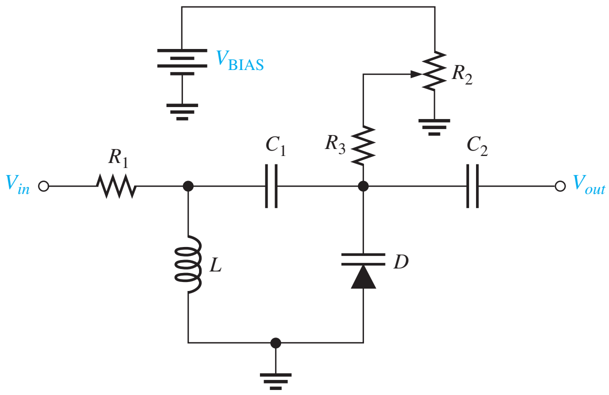


FIGURE 3–26

A resonant band-pass filter using a varactor diode for adjusting the resonant frequency over a specified range.

variable capacitor, thus allowing the resonant frequency to be adjusted by a variable voltage level. The varactor diode provides the total variable capacitance in the parallel resonant band-pass filter. The varactor diode and the inductor form a parallel resonant circuit from the output to ac ground. The capacitors C_1 and C_2 have no effect on the filter's frequency response because their reactances are negligible at the resonant frequencies. C_1 prevents a dc path from the potentiometer wiper back to the ac source through the inductor and R_1. C_2 prevents a dc path from the wiper of the potentiometer to a load on the output. The potentiometer R_2 forms a variable dc voltage for biasing the varactor. The reverse-bias voltage across the varactor can be varied with the potentiometer.

Recall that the parallel resonant frequency is

$$f_r \cong \frac{1}{2\pi\sqrt{LC}}$$

EXAMPLE 3–8

(a) Given that the capacitance of a Zetex 832A varactor is approximately 40 pF at 0 V bias and that the capacitance at a 2 V reverse bias is 22 pF, determine the capacitance at a reverse bias of 20 V using the specified minimum capacitance ratio.

(b) Using the capacitances at bias voltages of 0 V and 20 V, calculate the resonant frequencies at the bias extremes for the circuit in Figure 3–26 if $L = 2$ mH.

(c) Verify the frequency calculations by simulating the circuit in Figure 3–26 for the following component values: $R_1 = 47\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_3 = 5.1\ \text{M}\Omega$, $C_1 = 10$ nF, $C_2 = 10$ nF, $L = 2$ mH, and $V_{BIAS} = 20$ V.

Solution

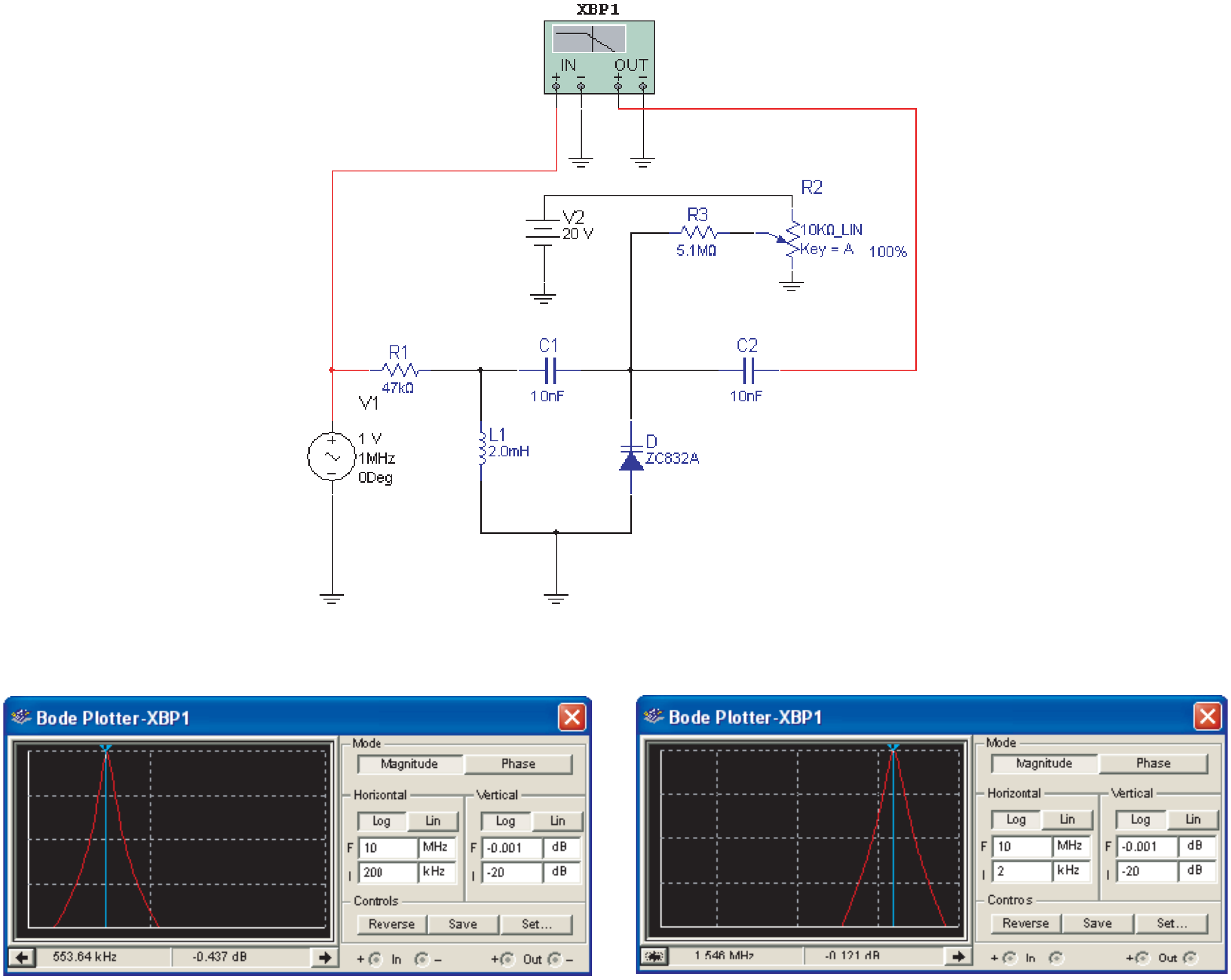
(a) $C_{20} = \dfrac{C_2}{CR} = \dfrac{22\text{ pF}}{5.0} = \mathbf{4.4\ pF}$

(b)

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(2\text{ mH})(40\text{ pF})}} = \mathbf{563\ kHz}$$

$$f_{20} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(2\text{ mH})(4.4\text{ pF})}} = \mathbf{1.7\ MHz}$$

(c) The Multsim simulation of the circuit is shown in Figure 3–27. The Bode plotters show the frequency responses at 0 V and 20 V reverse bias. The center of the 0 V bias response curve is at 553.64 kHz and the center of the 20 V bias response curve is at 1.548 MHz. These results agree reasonably well with the calculated values.


XBP1
IN
OUT
R2
V2
20 V
R3
5.1MΩ
10KΩ_LIN
Key = A
100%
R1
47kΩ
C1
10nF
C2
10nF
V1
1 V
1MHz
0Deg
L1
2.0mH
D
ZC832A
Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out

Horizontal: F 10 MHz, I 200 kHz; Vertical: F -0.001 dB, I -20 dB
553.64 kHz -0.437 dB

Frequency response for 0 V varactor bias

Horizontal: F 10 MHz, I 2 kHz; Vertical: F -0.001 dB, I -20 dB
1.546 MHz -0.121 dB

Frequency response for 20 V reverse varactor bias

▲ FIGURE 3–27

Multisim simulation.

These results show that this circuit can be tuned over most of the AM broadcast band.

Related Problem How could you increase the tuning range of the circuit?

SECTION 3–3 CHECKUP

1. What is the key feature of a varactor diode?
2. Under what bias condition is a varactor operated?
3. What part of the varactor produces the capacitance?
4. Based on the graph in Figure 3–22(c), what happens to the diode capacitance when the reverse voltage is increased?
5. Define *capacitance ratio*.

3–4 OPTICAL DIODES

In this section, three types of optoelectronic devices are introduced: the light-emitting diode, quantum dots, and the photodiode. As the name implies, the light-emitting diode is a light emitter. Quantum dots are very tiny light emitters made from silicon with great promise for various devices, including light-emitting diodes. On the other hand, the photodiode is a light detector.

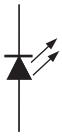
After completing this section, you should be able to

- ❑ **Discuss the basic characteristics, operation, and applications of LEDs, quantum dots, and photodiodes**
- ❑ Describe the light-emitting diode (LED)
  - ◆ Identify the LED schematic symbol ◆ Discuss the process of electroluminescence ◆ List some LED semiconductor materials ◆ Discuss LED biasing ◆ Discuss light emission
- ❑ Interpret an LED datasheet
  - ◆ Define and discuss radiant intensity and irradiance
- ❑ Describe some LED applications
- ❑ Discuss high-intensity LEDs and applications
  - ◆ Explain how high-intensity LEDs are used in traffic lights ◆ Explain how high-intensity LEDs are used in displays
- ❑ Describe the organic LED (OLED)
- ❑ Discuss quantum dots and their application
- ❑ Describe the photodiode and interpret a typical datasheet
  - ◆ Discuss photodiode sensitivity

The Light-Emitting Diode (LED)

The symbol for an LED is shown in Figure 3–28.

The basic operation of the **light-emitting diode (LED)** is as follows. When the device is forward-biased, electrons cross the *pn* junction from the *n*-type material and recombine with holes in the *p*-type material. Recall from Chapter 1 that these free electrons are in the conduction band and at a higher energy than the holes in the valence band. The difference in energy between the electrons and the holes corresponds to the energy of visible light. When recombination takes place, the recombining electrons release energy in the form of **photons.** The emitted light tends to be monochromatic (one color) that depends on the band gap (and other factors). A large exposed surface area on one layer of the semiconductive material permits the photons to be emitted as visible light. This process, called **electroluminescence**, is illustrated in Figure 3–29. Various impurities are added during the doping process to establish the **wavelength** of the emitted light. The wavelength determines the color of visible light. Some LEDs emit photons that are not part of the visible spectrum but have longer wavelengths and are in the **infrared** (IR) portion of the spectrum.



▲ FIGURE 3–28

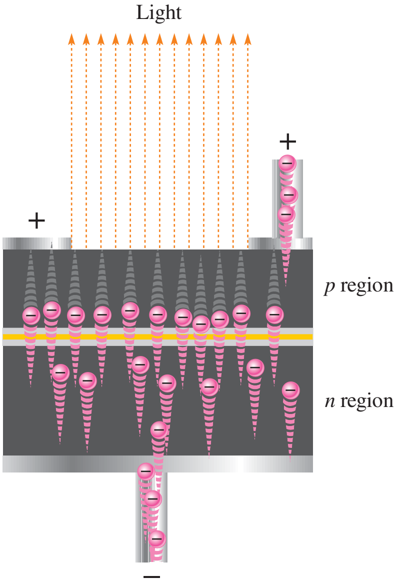
Symbol for an LED. When forward-biased, it emits light.

LED Semiconductor Materials The semiconductor gallium arsenide (GaAs) was used in early LEDs and emits IR radiation, which is invisible. The first visible red LEDs were produced using gallium arsenide phosphide (GaAsP) on a GaAs substrate. The efficiency was increased using a gallium phosphide (GaP) substrate, resulting in brighter red LEDs and also allowing orange LEDs.

Later, GaP was used as the light-emitter to achieve pale green light. By using a red and a green chip, LEDs were able to produce yellow light. The first super-bright red, yellow, and green LEDs were produced using gallium aluminum arsenide phosphide (GaAlAsP). By the early 1990s ultrabright LEDs using indium gallium aluminum phosphide (InGaAlP) were available in red, orange, yellow, and green.

▶ FIGURE 3–29

Electroluminescence in a forward-biased LED.



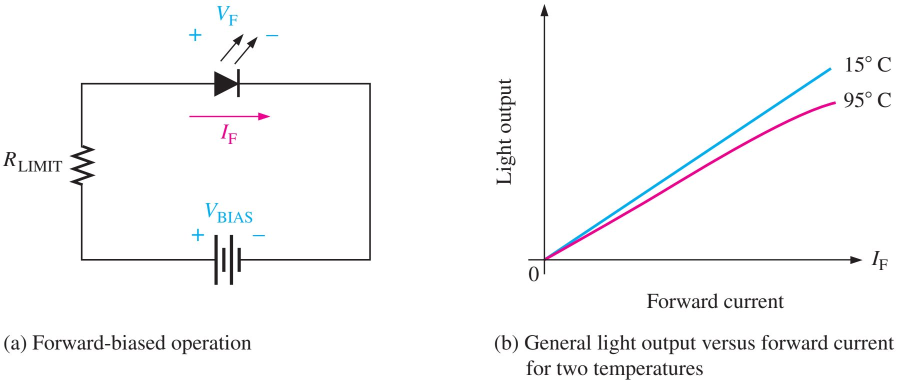
FYI

Efficiency is a term used in many fields to show how well a particular process works. It is the ratio of the output to the input and is a dimensionless number, often expressed as a percentage. An efficiency of 100% is the theoretical maximum that can never be achieved in real systems. For lighting, the term *efficacy* is used with units of lumens per watt and is related to the efficiency of converting input power (in watts) to light that can be seen by the human eye (lumens). The theoretical maximum efficacy is 683 lumens/watt.

Blue LEDs using silicon carbide (SiC) and ultrabright blue LEDs made of gallium nitride (GaN) became available. High intensity LEDs that produce green and blue are also made using indium gallium nitride (InGaN). High-intensity white LEDs are formed using ultrabright blue GaN coated with fluorescent phosphors that absorb the blue light and reemit it as white light.

LED Biasing The forward voltage across an LED is considerably greater than for a silicon diode. Typically, the maximum V_F for LEDs is between 1.2 V and 3.2 V, depending on the material. Reverse breakdown for an LED is much less than for a silicon rectifier diode (3 V to 10 V is typical).

The LED emits light in response to a sufficient forward current, as shown in Figure 3–30(a). The amount of power output translated into light is directly proportional to the forward current, as indicated in Figure 3–30(b). An increase in I_F corresponds proportionally to an increase in light output. The light output (both intensity and color) is also dependent on temperature. Light intensity goes down with higher temperature as indicated in the figure.



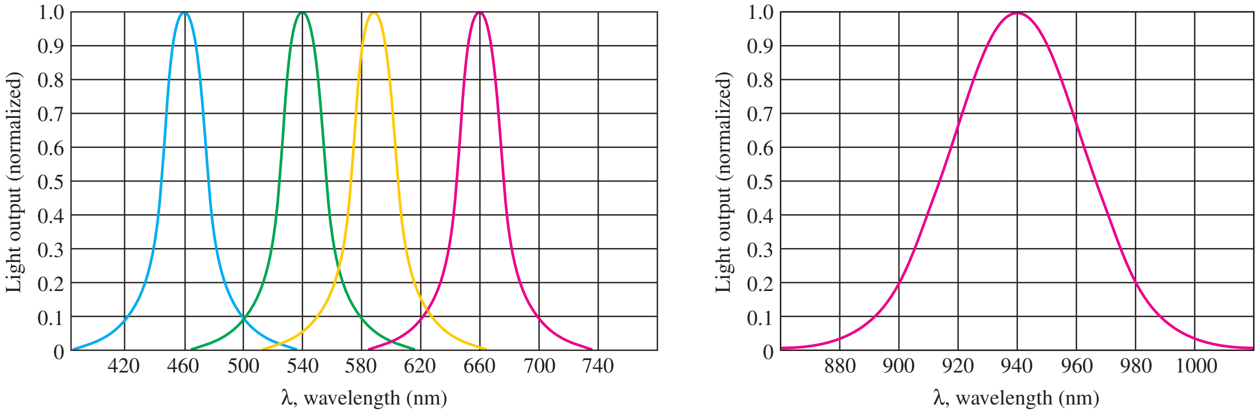
(a) Forward-biased operation

(b) General light output versus forward current for two temperatures

▲ FIGURE 3–30

Basic operation of an LED.

Light Emission An LED emits light over a specified range of wavelengths as indicated by the **spectral** output curves in Figure 3–31. The curves in part (a) represent the light output versus wavelength for typical visible LEDs, and the curve in part (b) is for a typical infrared LED. The wavelength (λ) is expressed in nanometers (nm). The normalized output of the visible red LED peaks at 660 nm, the yellow at 590 nm, green at 540 nm, and blue at 460 nm. The output for the infrared LED peaks at 940 nm.



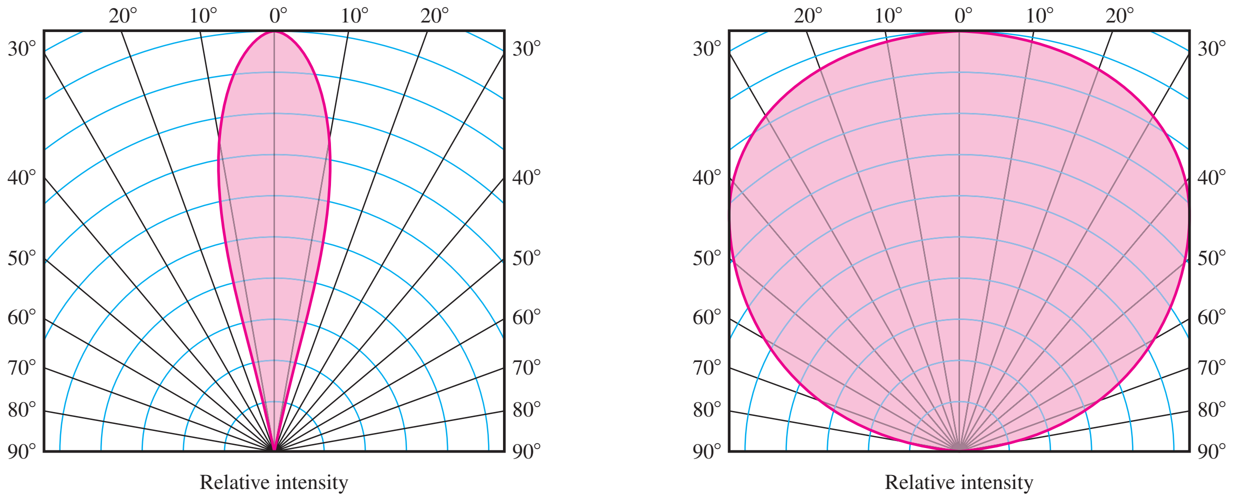
(a) Visible light

(b) Infrared (IR)

▲ **FIGURE 3–31**

Examples of typical spectral output curves for LEDs.

The graphs in Figure 3–32 show typical **radiation** patterns for small LEDs. LEDs are directional light sources (unlike filament or fluorescent bulbs). The radiation pattern is generally perpendicular to the emitting surface; however, it can be altered by the shape of the emitter surface and by lenses and diffusion films to favor a specific direction. Directional patterns can be an advantage for certain applications, such as traffic lights, where the light is intended to be seen only by certain drivers. Figure 3–32(a) shows the pattern for a forward-directed LED such as used in small panel indicators. Figure 3–32(b) shows the pattern for a wider viewing angle such as found in many super-bright LEDs. A wide variety of patterns are available from manufacturers; one variation is to design the LED to emit nearly all the light to the side in two lobes.



(a) A narrow viewing angle LED

(b) A wide viewing angle LED

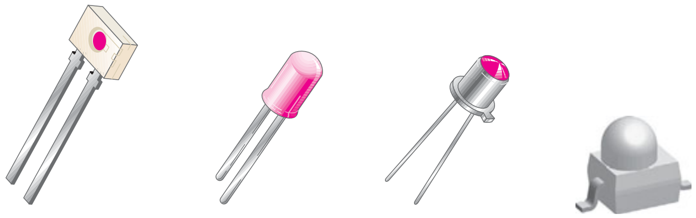
▲ **FIGURE 3–32**

Radiation patterns for two different LEDs.

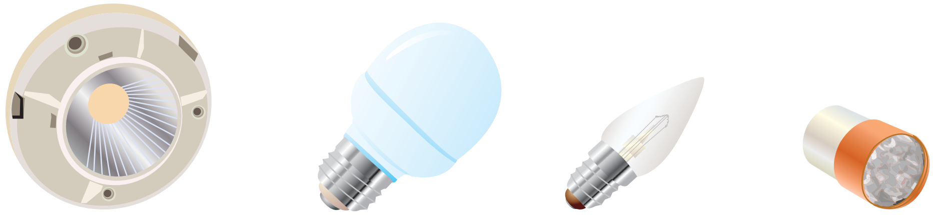
Typical small LEDs for indicators are shown in Figure 3–33(a). In addition to small LEDs for indicators, bright LEDs are becoming popular for lighting because of their superior efficiency and long life. A typical LED for lighting can deliver 50–60 lumens per watt, which is approximately five times greater efficiency than a standard incandescent bulb. LEDs for lighting are available in a variety of configurations, including even flexible tubes for decorative lighting and low-wattage bulbs for outdoor walkways and gardens. Many

FIGURE 3–33

Typical LEDs.



(a) Typical small LEDs for indicators



Helion 12 V overhead light with socket and module

120 V, 3.5 W screw base for low-level illumination

120 V, 1 W small screw base candelabra style

6 V, bayonet base for flashlights, etc.

(b) Typical LEDs for lighting applications

LED lamps are designed to work in 120 V standard fixtures. A few representative configurations are shown in Figure 3–33(b).

LED Datasheet Information

A partial datasheet for an TSMF1000 infrared (IR) light-emitting diode is shown in Figure 3–34. Notice that the maximum reverse voltage is only 5 V, the maximum forward current is 100 mA, and the forward voltage drop is approximately 1.3 V for $I_F = 20$ mA.

From the graph in part (c), you can see that the peak power output for this device occurs at a wavelength of 870 nm; its radiation pattern is shown in part (d).

Radiant Intensity and Irradiance In Figure 3–34(a), the **radiant intensity,** I_e (symbol not to be confused with current), is the output power per steradian and is specified as 5 mW/sr at $I_F = 20$ mA. The steradian (sr) is the unit of solid angular measurement. **Irradiance,** E, is the power per unit area at a given distance from an LED source expressed in mW/cm^2. Irradiance is important because the response of a detector (photodiode) used in conjunction with an LED depends on the irradiance of the light it receives.

EXAMPLE 3–10

From the LED datasheet in Figure 3–34 determine the following:

(a) The radiant power at 910 nm if the maximum output is 35 mW.

(b) The forward voltage drop for $I_F = 20$ mA.

(c) The radiant intensity for $I_F = 40$ mA.

Solution

(a) From the graph in Figure 3–34(c), the relative radiant power at 910 nm is approximately 0.25 and the peak radiant power is 35 mW. Therefore, the radiant power at 910 nm is

$$\phi_e = 0.25(35\text{ mW}) = \mathbf{8.75\ mW}$$

(b) From the graph in part (b), $V_F \cong$ **1.25 V** for $I_F = 20$ mA.

(c) From the graph in part (e), $I_e \cong$ **10 mW/sr** for $I_F = 40$ mA.

Related Problem

Determine the relative radiant power at 850 nm.

Absolute Maximum Ratings

T_{amb} = 25°C, unless otherwise specified

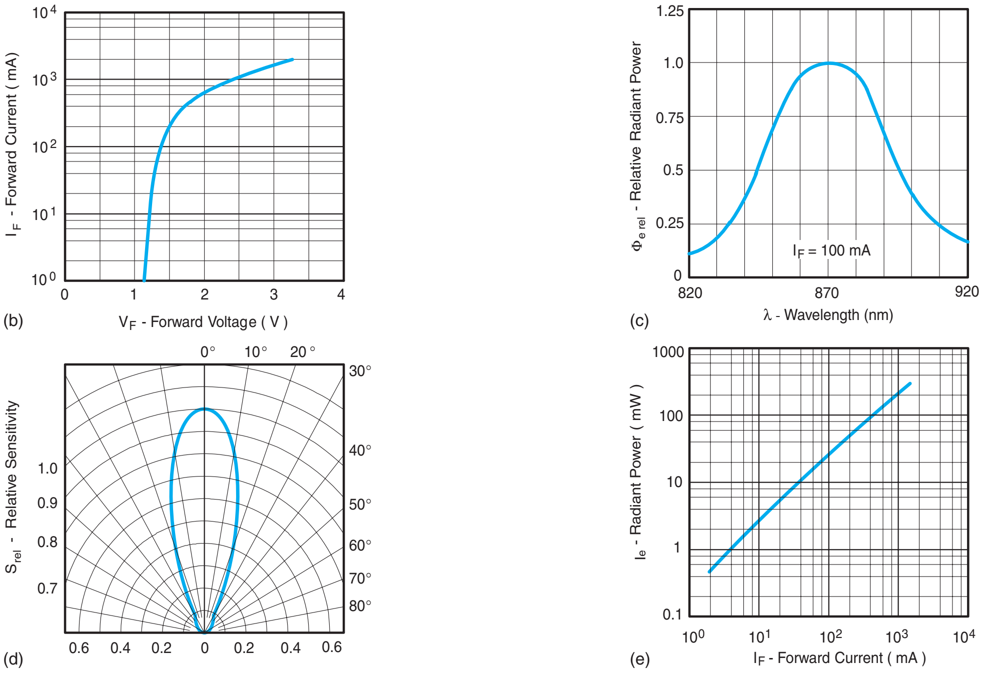
Parameter	Test condition	Symbol	Value	Unit
Reverse Voltage		V_R	5	V
Forward current		I_F	100	mA
Peak Forward Current	$t_p/T = 0.5$, $t_p = 100\ \mu s$	I_{FM}	200	mA
Surge Forward Current	$t_p = 100\ \mu s$	I_{FSM}	0.8	A
Power Dissipation		P_V	190	mW
Junction Temperature		T_j	100	°C
Operating Temperature Range		T_{amb}	- 40 to + 85	°C

Basic Characteristics

T_{amb} = 25°C, unless otherwise specified
T_{amb} = 25°C, unless otherwise specified

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward Voltage	$I_F = 20$ mA	V_F		1.3	1.5	V
	$I_F = 1$ A, $t_p = 100\ \mu s$	V_F		2.4		V
Temp. Coefficient of V_F	$I_F = 1.0$ mA	TK_{VF}		- 1.7		mV/K
Reverse Current	$V_R = 5$ V	I_R			10	μA
Junction capacitance	$V_R = 0$ V, f = 1 MHz, E = 0	C_j		160		pF
Radiant Intensity	$I_F = 20$ mA	I_e	2.5	5	13	mW/sr
	$I_F = 100$ mA, $t_p = 100\ \mu s$	I_e		25		mW/sr
Radiant Power	$I_F = 100$ mA, $t_p = 20$ ms	ϕ_e		35		mW
Temp. Coefficient of ϕ_e	$I_F = 20$ mA	$TK\phi_e$		- 0.6		%/K
Angle of Half Intensity		ϕ		± 17		deg
Peak Wavelength	$I_F = 20$ mA	λ_p		870		nm
Spectral Bandwidth	$I_F = 20$ mA	$\Delta\lambda$		40		nm
Temp. Coefficient of λ_p	$I_F = 20$ mA	$TK\lambda_p$		0.2		nm/K
Rise Time	$I_F = 20$ mA	t_r		30		ns
Fall Time	$I_F = 20$ mA	t_f		30		ns
Virtual Source Diameter		∅		1.2		mm

(a)

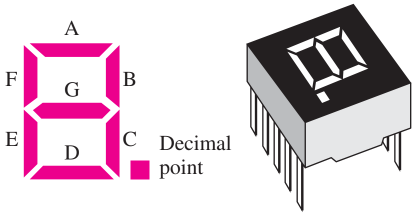


▲ FIGURE 3–34

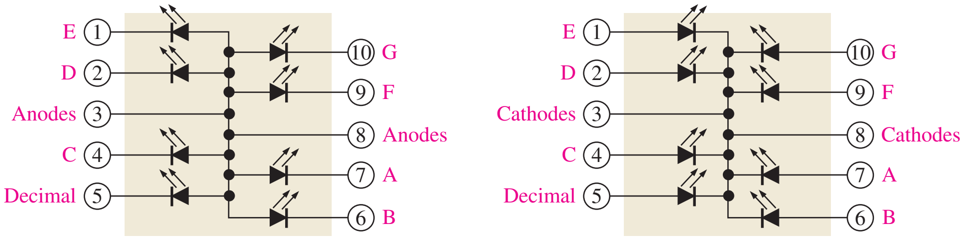
Partial datasheet for an TSMF1000 IR light-emitting diode. Datasheet courtesy of Vishay Intertechnology, Inc. Datasheets are available at www.vishay.com.

Applications

Standard LEDs are used for indicator lamps and readout displays on a wide variety of instruments, ranging from consumer appliances to scientific apparatus. A common type of display device using LEDs is the seven-segment display. Combinations of the segments form the ten decimal digits as illustrated in Figure 3–35. Each segment in the display is an LED. By forward-biasing selected combinations of segments, any decimal digit and a decimal point can be formed. Two types of LED circuit arrangements are the common anode and common cathode as shown.



(a) LED segment arrangement and typical device



(b) Common anode

(c) Common cathode

▲ **FIGURE 3–35**

The 7-segment LED display.

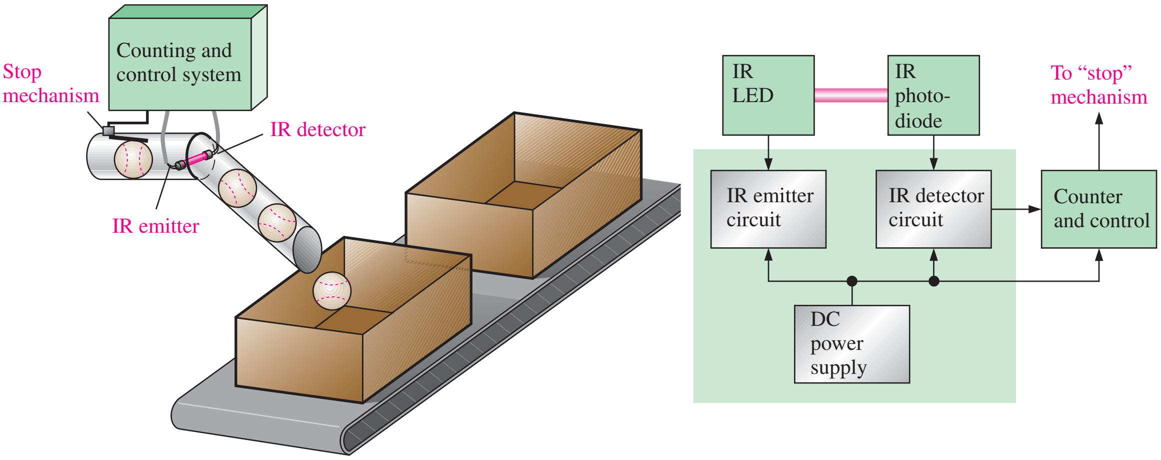
One common application of an infrared LED is in remote control units for TV, DVD, gate openers, etc. The IR LED sends out a beam of invisible light that is sensed by the receiver in your TV, for example. For each button on the remote control unit, there is a unique code. When a specific button is pressed, a coded electrical signal is generated that goes to the LED, which converts the electrical signal to a coded infrared light signal. The TV receiver recognizes the code and takes appropriate action, such as changing the channel or increasing the volume.

Also, IR light-emitting diodes are used in optical coupling applications, often in conjunction with fiber optics. Areas of application include industrial processing and control, position encoders, bar graph readers, and optical switching.

An example of how an IR LED could be used in an industrial application is illustrated in Figure 3–36. This particular system is used to count baseballs as they are fed down a chute into a box for shipping. As each ball passes through the chute, the IR beam emitted by the LED is interrupted. This is detected by the photodiode (discussed later) and the resulting change in current is sensed by a detector circuit. An electronic circuit counts each time that the beam is interrupted; and when a preset number of balls pass through the chute, the “stop” mechanism is activated to stop the flow of balls until the next empty box is automatically moved into place on the conveyor. When the next box is in place, the “stop” mechanism is deactivated and the balls begin to roll again. This idea can also be applied to inventory and packing control for many other types of products.

High-Intensity LEDs

LEDs that produce much greater light outputs than standard LEDs are found in many applications including traffic lights, automotive lighting, indoor and outdoor advertising and informational signs, and home lighting.


Stop mechanism
Counting and control system
IR detector
IR emitter
IR LED
IR photo-diode
To "stop" mechanism
IR emitter circuit
IR detector circuit
Counter and control
DC power supply

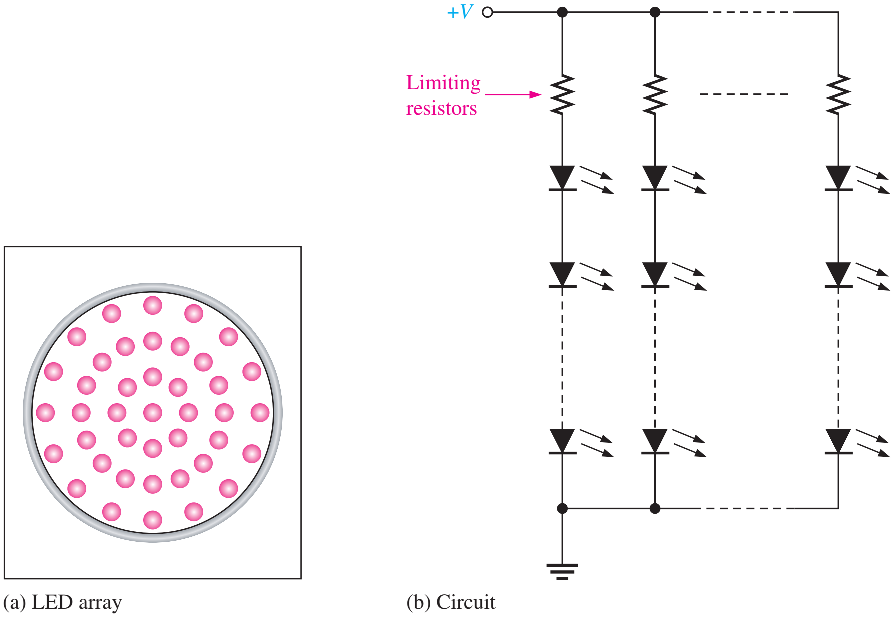
▲ FIGURE 3–36

Basic concept and block diagram of a counting and control system.

Traffic Lights LEDs are quickly replacing the traditional incandescent bulbs in traffic signal applications. Arrays of tiny LEDs form the red, yellow, and green lights in a traffic light unit. An LED array has three major advantages over the incandescent bulb: brighter light, longer lifetime (years vs. months), and less energy consumption (about 90% less).

LED traffic lights are constructed in arrays with lenses that optimize and direct the light output. Figure 3–37(a) illustrates the concept of a traffic light array using red LEDs. A relatively low density of LEDs is shown for illustration. The actual number and spacing of the LEDs in a traffic light unit depends on the diameter of the unit, the type of lens, the color, and the required light intensity. With an appropriate LED density and a lens, an 8- or 12-inch traffic light will appear essentially as a solid-color circle.

LEDs in an array are usually connected either in a series-parallel or a parallel arrangement. A series connection is not practical because if one LED fails open, then all the LEDs are disabled. For a parallel connection, each LED requires a limiting resistor. To reduce the number of limiting resistors, a series-parallel connection can be used, as shown in Figure 3–37(b).


+V
Limiting resistors

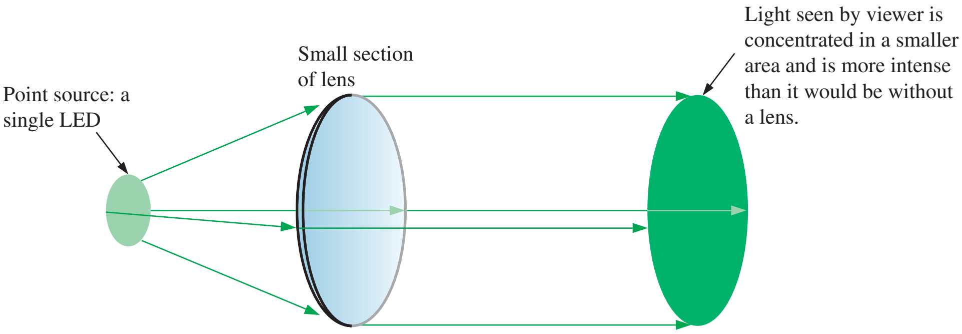
(a) LED array (b) Circuit

▲ FIGURE 3–37

LED traffic light.

▶ FIGURE 3–38

The lens directs the light emitted from the LED to optimize visibility.

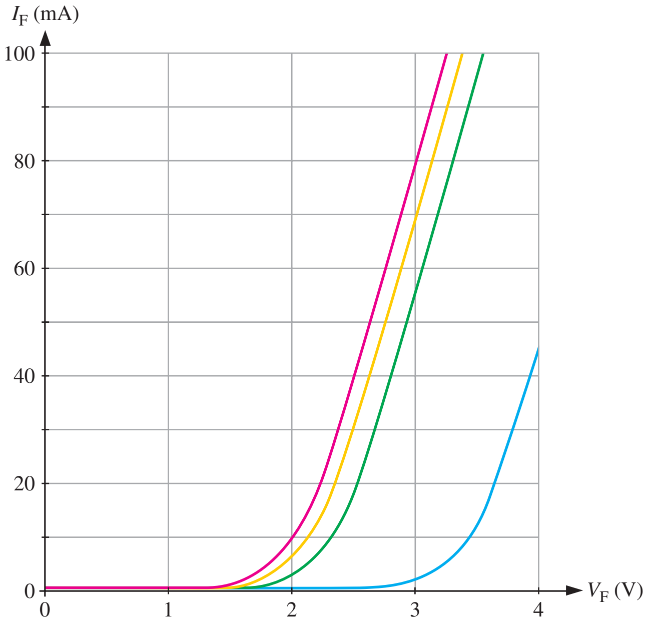

Point source: a single LED
Small section of lens
Light seen by viewer is concentrated in a smaller area and is more intense than it would be without a lens.

Some LED traffic arrays use small reflectors for each LED to help maximize the effect of the light output. Also, an optical lens covers the front of the array to direct the light from each individual diode to prevent improper dispersion of light and to optimize the visibility. Figure 3–38 illustrates how a lens is used to direct the light toward the viewer.

The particular LED circuit configuration depends on the voltage and the color of the LED. Different color LEDs require different forward voltages to operate. Red LEDs take the least; and as the color moves up the color spectrum toward blue, the voltage requirement increases. Typically, a red LED requires about 2 V, while blue LEDs require between 3 V and 4 V. Generally, LEDs, however, need 20 mA to 30 mA of current, regardless of their voltage requirements. Typical *V-I* curves for red, yellow, green, and blue LEDs are shown in Figure 3–39.

▶ FIGURE 3–39

V-I characteristic curves for visible-light LEDs.



EXAMPLE 3–11 Using the graph in Figure 3–39, determine the green LED forward voltage for a current of 20 mA. Design a 12 V LED circuit to minimize the number of limiting resistors for an array of 60 diodes.

Solution From the graph, a green LED has a forward voltage of approximately 2.5 V for a forward current of 20 mA. The maximum number of series LEDs is 3. The total voltage across three LEDs is

$$V = 3 \times 2.5\text{ V} = 7.5\text{ V}$$

The voltage drop across the series-limiting resistor is

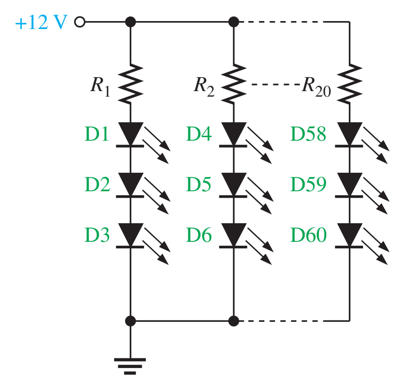
$$V = 12\text{ V} - 7.5\text{ V} = 4.5\text{ V}$$

The value of the limiting resistor is

$$R_{\text{LIMIT}} = \frac{4.5\text{ V}}{20\text{ mA}} = 225\ \Omega$$

The LED array has 20 parallel branches each with a limiting resistor and three LEDs, as shown in Figure 3–40.

▶ FIGURE 3–40



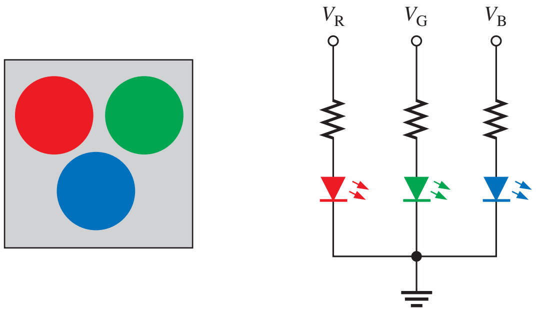
Related Problem Design a 12 V red LED array with minimum limiting resistors, a forward current of 30 mA, and containing 64 diodes.

LED Displays LEDs are widely used in large and small signs and message boards for both indoor and outdoor uses, including large-screen television. Signs can be single-color, multicolor, or full-color. Full-color screens use a tiny grouping of high-intensity red, green, and blue LEDs to form a **pixel**. A typical screen is made of thousands of RGB pixels with the exact number determined by the sizes of the screen and the pixel.

Red, green, and blue (RGB) are primary colors and when mixed together in varying amounts, can be used to produce any color in the visible spectrum. A basic pixel formed by three LEDs is shown in Figure 3–41. The light emission from each of the three diodes can be varied independently by varying the amount of forward current. Yellow is added to the three primary colors (RGBY) in some TV screen applications.

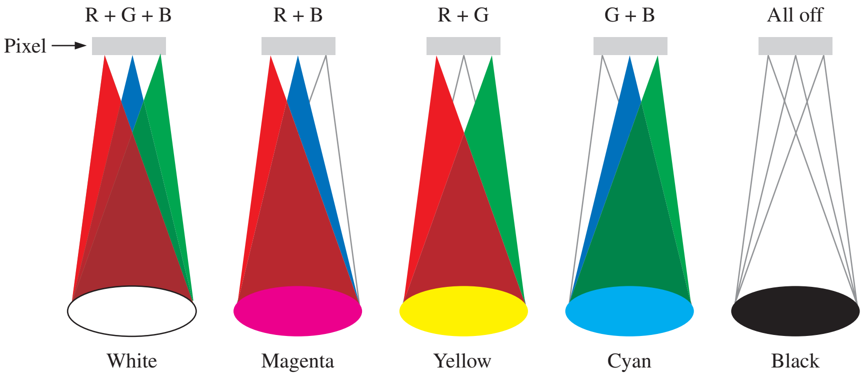
Other Applications High-intensity LEDs are becoming more widely used in automotive lighting for taillights, brakelights, turn signals, back-up lights, and interior applications. LED arrays are expected to replace most incandescent bulbs in automotive lighting. Eventually, headlights may also be replaced by white LED arrays. LEDs can be seen better in poor weather and can last 100 times longer than an incandescent bulb.

LEDs are also finding their way into interior home and business lighting applications. Arrays of white LEDs may eventually replace incandescent light bulbs and flourescent lighting in interior living and work areas. As previously mentioned, most white LEDs use a blue GaN (gallium nitride) LED covered by a yellowish phosphor coating made of a certain type of crystals that have been powdered and bound in a type of viscous adhesive. Since yellow light stimulates the red and green receptors of the eye, the resulting mix of blue and yellow light gives the appearance of white.



(a) Basic pixel

(b) Pixel circuit



R + G + B
R + B
R + G
G + B
All off
Pixel
White
Magenta
Yellow
Cyan
Black

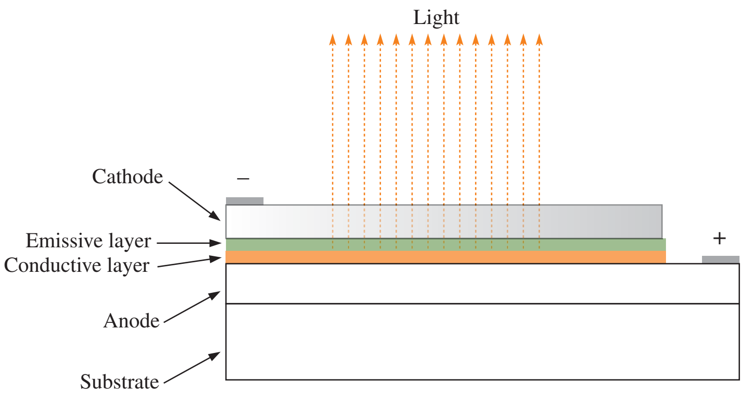
(c) Examples of different combinations of equal amounts of primary colors

▲ FIGURE 3–41

The concept of an RGB pixel used in LED display screens.

The Organic LED (OLED)

An **OLED** is a device that consists of two or three layers of materials composed of organic molecules or polymers that emit light with the application of voltage. OLEDs produce light through the process of electrophosphorescence. The color of the light depends on the type of organic molecule in the emissive layer. The basic structure of a 2-layer OLED is shown in Figure 3–42.



Light
Cathode
–
Emissive layer
Conductive layer
+
Anode
Substrate

▲ FIGURE 3–42

Basic structure of a top-emitting 2-layer OLED.

Electrons are provided to the emissive layer and removed from the conductive layer when there is current between the cathode and anode. This removal of electrons from the conductive layer leaves holes. The electrons from the emissive layer recombine with the holes from the conductive layer near the junction of the two layers. When this recombination occurs, energy is released in the form of light that passes through the transparent cathode material. If the anode and substrate are also made from transparent materials, light is emitted in both directions, making the OLED useful in applications such as heads-up displays.

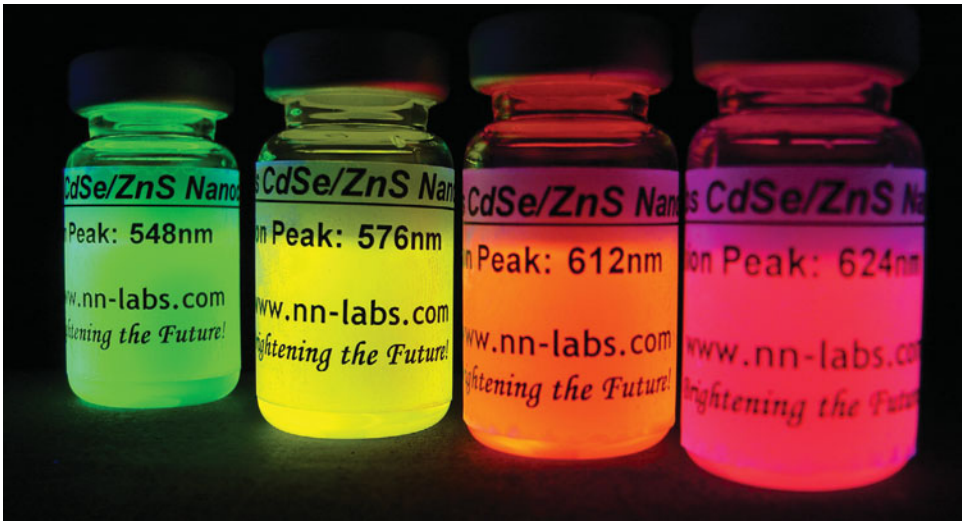
OLEDs can be sprayed onto substrates just like inks are sprayed onto paper during printing. Inkjet technology greatly reduces the cost of OLED manufacturing and allows OLEDs to be printed onto very large films for large displays like 80-inch TV screens or electronic billboards.

FYI

OLED technology was developed by Eastman Kodak. It is beginning to replace LCD (liquid crystal display) technology in handheld devices such as PDAs and cellular phones. OLEDs are brighter, thinner, faster, and lighter than conventional LEDs or LCDs. They also use less power and are cheaper to manufacture.

Quantum Dots

Quantum dots are a form of nanocrystals that are made from semiconductor material such as silicon, germanium, cadmium sulfide, cadmium selenide, and indium phosphide. Quantum dots are only 1 nm to 12 nm in diameter (a nm is one billionth of a meter). Billions of dots could fit on the head of a pin! Because of their small size, quantum effects arise due to the confinement of electrons and holes; as a result, material properties are very different than the normal material. One important property is that the band gap is dependent on the size of the dots. When excited from an external source, dots formed from semiconductors emit light in the visible range as well as infrared and ultraviolet, depending on their size. The higher-frequency blue light is emitted by smaller dots suspended in solution (larger band gap); red light is emitted from solutions with larger dots (smaller band gap). Solutions containing the quantum dots glow eerily with specific colors as shown in the photograph in Figure 3–43.



◀ FIGURE 3–43

Solutions containing quantum dots glow with specific colors that depend on the size of the dots. Courtesy of NN-Labs.

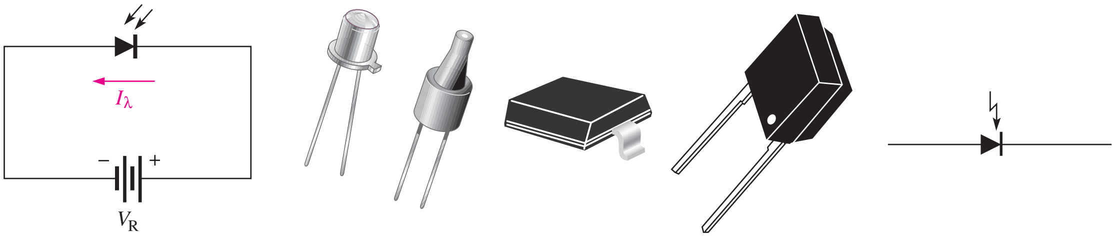
Although quantum dots are not diodes themselves, they can be used in construction of light-emitting diodes as well as display devices and a variety of other applications. As you know, LEDs work by generating a specific frequency (color) of light, which is determined by the band gap. To produce white light, blue LEDs are coated with a phosphor that adds yellow light to the blue, forming white. The result is not a pure white, but tends to be harsh and makes colors appear unnatural. While this is satisfactory for displays and signs, many people do not like it for home lighting.

Quantum dots can be used to modify the basic color of LEDs by converting higher energy photons (blue) to photons of lower energy. The result is a color that more closely approximates an incandescent bulb. Quantum dot filters can be designed to contain combinations of colors, giving designers control of the spectrum. The important advantage of quantum dot technology is that it does not lose the incoming light; it merely absorbs the light and reradiates it at a different frequency. This enables control of color without giving up efficiency. By placing a quantum dot filter in front of a white LED, the spectrum can be made to look like that of an incandescent bulb. The resulting light is more satisfactory for general illumination, while retaining the advantages of LEDs.

There are other promising applications, particularly in medical applications. Water-soluble quantum dots are used as a biochemical luminescent marker for cellular imaging and medical research. Research is also being done on quantum dots as the basic device units for information processing by manipulating two energy levels within the quantum dot.

The Photodiode

The **photodiode** is a device that operates in reverse bias, as shown in Figure 3–44(a), where I_λ is the reverse light current. The photodiode has a small transparent window that allows light to strike the *pn* junction. Some typical photodiodes are shown in Figure 3–44(b). An alternate photodiode symbol is shown in Figure 3–44(c).



(a) Reverse-bias operation using standard symbol

(b) Typical devices

(c) Alternate symbol

▲ FIGURE 3–44

Photodiode.

Recall that when reverse-biased, a rectifier diode has a very small reverse leakage current. The same is true for a photodiode. The reverse-biased current is produced by thermally generated electron-hole pairs in the depletion region, which are swept across the *pn* junction by the electric field created by the reverse voltage. In a rectifier diode, the reverse leakage current increases with temperature due to an increase in the number of electron-hole pairs.

A photodiode differs from a rectifier diode in that when its *pn* junction is exposed to light, the reverse current increases with the light intensity. When there is no incident light, the reverse current, I_λ, is almost negligible and is called the **dark current.** An increase in the amount of light intensity, expressed as irradiance (mW/cm^2), produces an increase in the reverse current, as shown by the graph in Figure 3–45(a).

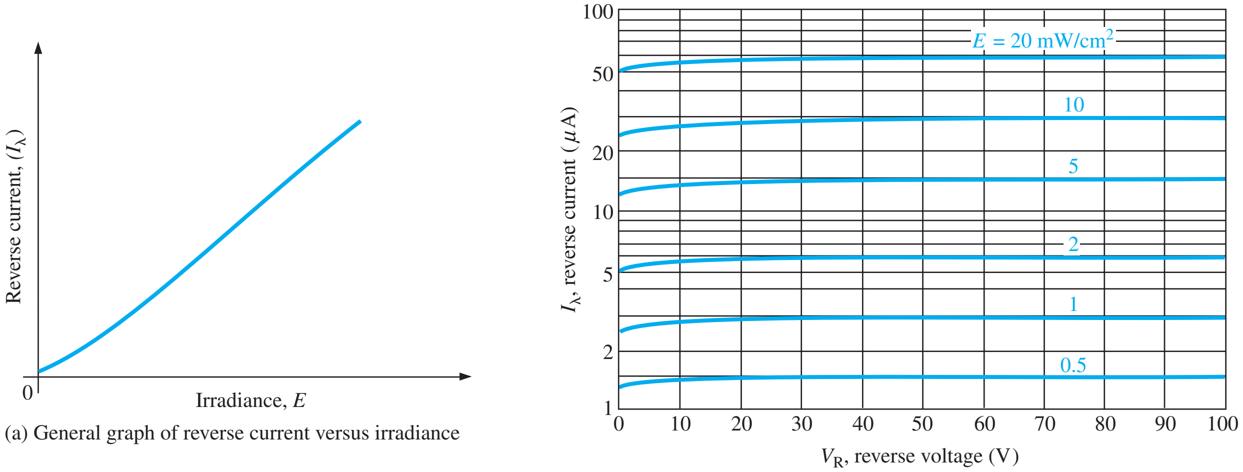
From the graph in Figure 3–45(b), you can see that the reverse current for this particular device is approximately 1.4 μA at a reverse-bias voltage of 10 V with an irradiance of 0.5 mW/cm^2. Therefore, the resistance of the device is

$$R_R = \frac{V_R}{I_\lambda} = \frac{10\text{ V}}{1.4\ \mu\text{A}} = 7.14\text{ M}\Omega$$

At 20 mW/cm^2, the current is approximately 55 μA at $V_R = 10$ V. The resistance under this condition is

$$R_R = \frac{V_R}{I_\lambda} = \frac{10\text{ V}}{55\ \mu\text{A}} = 182\text{ k}\Omega$$

These calculations show that the photodiode can be used as a variable-resistance device controlled by light intensity.



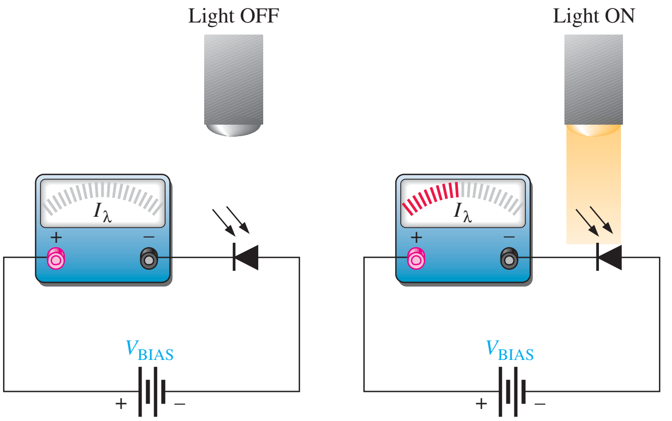
(a) General graph of reverse current versus irradiance

(b) Example of a graph of reverse current versus reverse voltage for several values of irradiance

▲ **FIGURE 3–45**

Typical photodiode characteristics.

Figure 3–46 illustrates that the photodiode allows essentially no reverse current (except for a very small dark current) when there is no incident light. When a light beam strikes the photodiode, it conducts an amount of reverse current that is proportional to the light intensity (irradiance).



(a) No light, no current except negligible dark current

(b) Where there is incident light, resistance decreases and there is reverse current.

▲ **FIGURE 3–46**

Operation of a photodiode.

Photodiode Datasheet Information

A partial datasheet for an TEMD1000 photodiode is shown in Figure 3–47. Notice that the maximum reverse voltage is 60 V and the dark current (reverse current with no light) is typically 1 nA for a reverse voltage of 10 V. The dark current increases with an increase in reverse voltage and also with an increase in temperature.

Sensitivity From the graph in part (b), you can see that the maximum sensitivity for this device occurs at a wavelength of 950 nm. The angular response graph in part (c) shows an area of response measured as relative sensitivity. At 10° on either side of the maximum orientation, the sensitivity drops to approximately 82% of maximum.

Absolute Maximum Ratings

Tamb = 25°C, unless otherwise specified

Parameter	Test condition	Symbol	Value	Unit
Reverse Voltage		V_R	60	V
Power Dissipation	$T_{amb} \leq 25°C$	P_V	75	mW
Junction Temperature		T_j	100	°C
Storage Temperature Range		T_{stg}	- 40 to + 100	°C
Operating Temperature Range		T_{stg}	- 40 to + 85	°C
Soldering Temperature	$t \leq 5$ s	T_{sd}	< 260	°C

Basic Characteristics

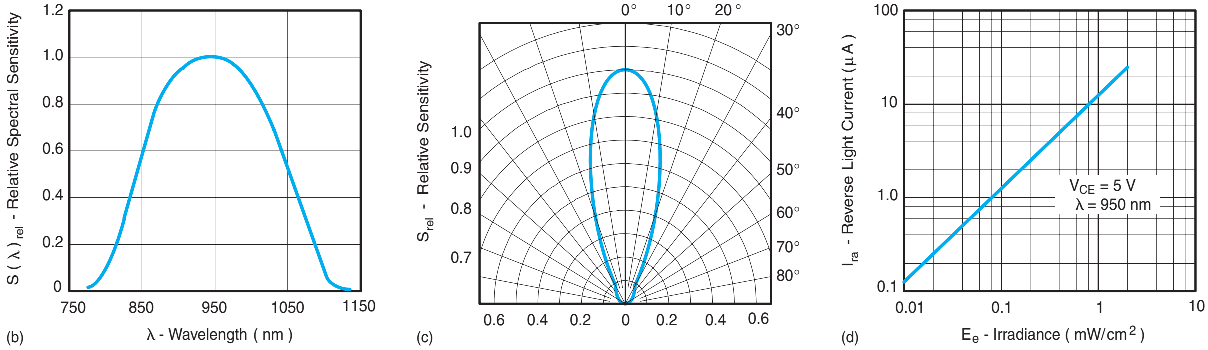
T_{amb} = 25 °C, unless otherwise specified

T_{amb} = 25 °C, unless otherwise specified

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward Voltage	I_F = 50 mA	V_F		1.0	1.3	V
Breakdown Voltage	I_R = 100 μA, E = 0	$V_{(BR)}$	60			V
Reverse Dark Current	V_R = 10 V, E = 0	I_{ro}		1	10	nA
Diode capacitance	V_R = 5 V, f = 1 MHz, E = 0	C_D		1.8		pF
Reverse Light Current	E_e = 1 mW/cm^2, λ = 870 nm, V_R = 5 V	I_{ra}		10		μA
	E_e = 1 mW/cm^2, λ = 950 nm, V_R = 5 V	I_{ra}	5	12		μA

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Temp. Coefficient of I_{ra}	V_R = 5 V, = 870 nm	TK_{Ira}		0.2		%/K
Absolute Spectral Sensitivity	V_R = 5 V, = 870 nm	s(λ)		0.60		A/W
	V_R = 5 V, = 950 nm	s(λ)		0.55		A/W
Angle of Half Sensitivity		ϕ		±15		deg
Wavelength of Peak Sensitivity		λ_p		900		nm
Range of Spectral Bandwidth		$\lambda_{0.5}$		840 to 1050		nm
Rise Time	V_R = 10 V, R_L = 50, Ω λ = 820 nm	t_r		4		ns
Fall Time	V_R = 10 V, R_L = 50, Ω λ = 820 nm	t_f		4		ns

(a)



▲ **FIGURE 3–47**

Partial datasheet for the TEMD1000 photodiode. Datasheet courtesy of Vishay Intertechnology, Inc.

EXAMPLE 3–12

For a TEMD1000 photodiode,

(a) Determine the maximum dark current for $V_R = 10$ V.

(b) Determine the reverse light current for an irradiance of 1 mW/cm^2 at a wavelength of 850 nm if the device angle is oriented at 10° with respect to the maximum irradiance and the reverse voltage is 5 V.

Solution **(a)** From Figure 3–47(a), the maximum dark current $I_{ro} =$ **10 nA.**

(b) From the graph in Figure 3–47(d), the reverse light current is 12 μ A at 950 nm. From Figure 3–47(b), the relative sensitivity is 0.6 at 850 nm. Therefore, the reverse light current is

$$I_{\lambda} = I_{ra} = 0.6(12\ \mu\text{A}) = 72\ \mu\text{A}$$

For an angle of 10°, the relative sensitivity is reduced to 0.92 of its value at 0°.

$$I_{\lambda} = I_{ra} = 0.92\,(7.2\ \mu\text{A}) = \mathbf{6.62\ \mu A}$$

Related Problem What is the reverse current if the wavelength is 1050 nm and the angle is 0°?

SECTION 3–4 CHECKUP

1. Name two types of LEDs in terms of their light-emission spectrum.
2. Which has the greater wavelength, visible light or infrared?
3. In what bias condition is an LED normally operated?
4. What happens to the light emission of an LED as the forward current increases?
5. The forward voltage drop of an LED is 0.7 V. (true or false)
6. What is a pixel?
7. In what bias condition is a photodiode normally operated?
8. When the intensity of the incident light (irradiance) on a photodiode increases, what happens to its internal reverse resistance?
9. What is *dark current*?

3–5 OTHER TYPES OF DIODES

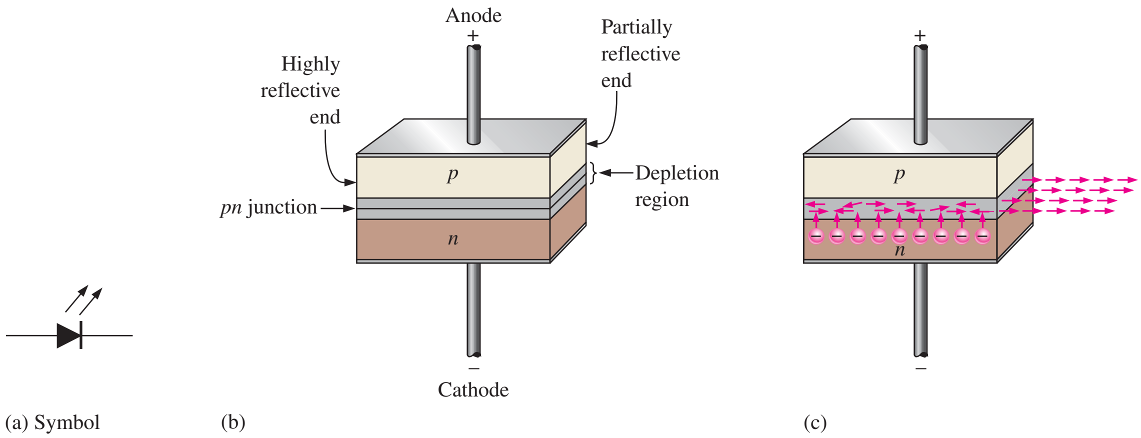
In this section, several types of diodes that you are less likely to encounter as a technician but are nevertheless important are introduced. Among these are the laser diode, the Schottky diode, the *pin* diode, the step-recovery diode, the tunnel diode, and the current regulator diode.

After completing this section, you should be able to

- **Discuss the basic characteristics of several types of diodes**
- Discuss the laser diode and an application
  - Identify the schematic symbol
- Discuss the Schottky diode
  - Identify the schematic symbol
- Discuss the *pin* diode
- Discuss the step-recovery diode
  - Identify the schematic symbol
- Discuss the tunnel diode
  - Identify the schematic symbol
  - Describe a tunnel diode application
- Discuss the current regulation diode
  - Identify the schematic symbol

The Laser Diode

The term **laser** stands for *l*ight *a*mplification by *s*timulated *e*mission of *r*adiation. Laser light is **monochromatic,** which means that it consists of a single color and not a mixture of colors. Laser light is also called **coherent light,** a single wavelength, as compared to incoherent light, which consists of a wide band of wavelengths. The laser diode normally emits coherent light, whereas the LED emits incoherent light. The symbols are the same as shown in Figure 3–48(a).



(a) Symbol (b) (c)

▲ FIGURE 3–48

Basic laser diode construction and operation.

The basic construction of a laser diode is shown in Figure 3–48(b). A *pn* junction is formed by two layers of doped gallium arsenide. The length of the *pn* junction bears a precise relationship with the wavelength of the light to be emitted. There is a highly reflective surface at one end of the *pn* junction and a partially reflective surface at the other end, forming a resonant cavity for the photons. External leads provide the anode and cathode connections.

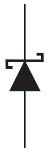
The basic operation is as follows. The laser diode is forward-biased by an external voltage source. As electrons move through the junction, recombination occurs just as in an ordinary diode. As electrons fall into holes to recombine, photons are released. A released photon can strike an atom, causing another photon to be released. As the forward current is increased, more electrons enter the depletion region and cause more photons to be emitted. Eventually some of the photons that are randomly drifting within the depletion region strike the reflected surfaces perpendicularly. These reflected photons move along the depletion region, striking atoms and releasing additional photons due to the avalanche effect. This back-and-forth movement of photons increases as the generation of photons "snowballs" until a very intense beam of laser light is formed by the photons that pass through the partially reflective end of the *pn* junction.

Each photon produced in this process is identical to the other photons in energy level, phase relationship, and frequency. So a single wavelength of intense light emerges from the laser diode, as indicated in Figure 3–48(c). Laser diodes have a threshold level of current above which the laser action occurs and below which the diode behaves essentially as an LED, emitting incoherent light.

An Application Laser diodes and photodiodes are used in the pick-up system of compact disk (CD) players. Audio information (sound) is digitally recorded in stereo on the surface of a compact disk in the form of microscopic "pits" and "flats." A lens arrangement focuses the laser beam from the diode onto the CD surface. As the CD rotates, the lens and beam follow the track under control of a servomotor. The laser light, which is altered by the pits and flats along the recorded track, is reflected back from the track through a lens and optical system to infrared photodiodes. The signal from the photodiodes is then used to reproduce the digitally recorded sound. Laser diodes are also used in laser printers and fiber-optic systems.

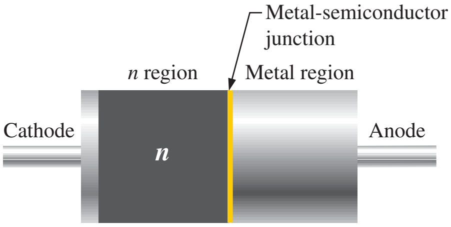
The Schottky Diode

Schottky diodes are high-current diodes used primarily in high-frequency and fast-switching applications. They are also known as *hot-carrier diodes.* The term *hot-carrier* is derived from the higher energy level of electrons in the *n* region compared to those in the metal region. A Schottky diode symbol is shown in Figure 3–49. A Schottky diode is formed by joining a doped semiconductor region (usually *n*-type) with a metal such as gold, silver, or platinum. Rather than a *pn* junction, there is a metal-to-semiconductor junction, as shown in Figure 3–50. The forward voltage drop is typically around 0.3 V because there is no depletion region as in a *pn* junction diode.



▲ **FIGURE 3–49**

Schottky diode symbol.



◀ **FIGURE 3–50**

Basic internal construction of a Schottky diode.

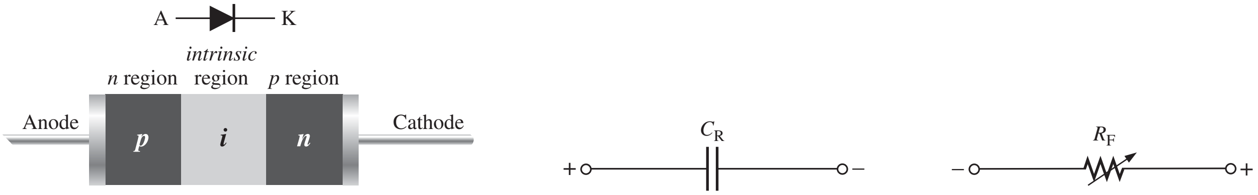
The Schottky diode operates only with majority carriers. There are no minority carriers and thus no reverse leakage current as in other types of diodes. The metal region is heavily occupied with conduction-band electrons, and the *n*-type semiconductor region is lightly doped. When forward-biased, the higher energy electrons in the *n* region are injected into the metal region where they give up their excess energy very rapidly. Since there are no minority carriers, as in a conventional rectifier diode, there is a very rapid response to a change in bias. The Schottky is a fast-switching diode, and most of its applications make use of this property. It can be used in high-frequency applications and in many digital circuits to decrease switching times. The LS family of TTL logic (LS stands for low-power Schottky) is one type of digital integrated circuit that uses the Schottky diode.

GREENTECH NOTE

Thin-film PV solar panels, a relatively new development, use a somewhat different concept for the diodes than a standard crystalline silicon panel uses. The thin films are based on amorphous silicon, rather than crystalline silicon, as standard PV panels are. The *p* and *n* layers are separated by an intrinsic layer forming a *p-i-n* diode. Because they are very thin, light can penetrate the entire layer and multiple layers can be added with different band gaps to capture a larger percentage of the light spectrum. This is a promising method for forming large flexible panels.

The *PIN* Diode

The *pin* diode consists of heavily doped *p* and *n* regions separated by an intrinsic (*i*) region, as shown in Figure 3–51(a). When reverse-biased, the *pin* diode acts like a nearly constant capacitance. When forward-biased, it acts like a current-controlled variable resistance. This is shown in Figure 3–51(b) and (c). The low forward resistance of the intrinsic region decreases with increasing current.



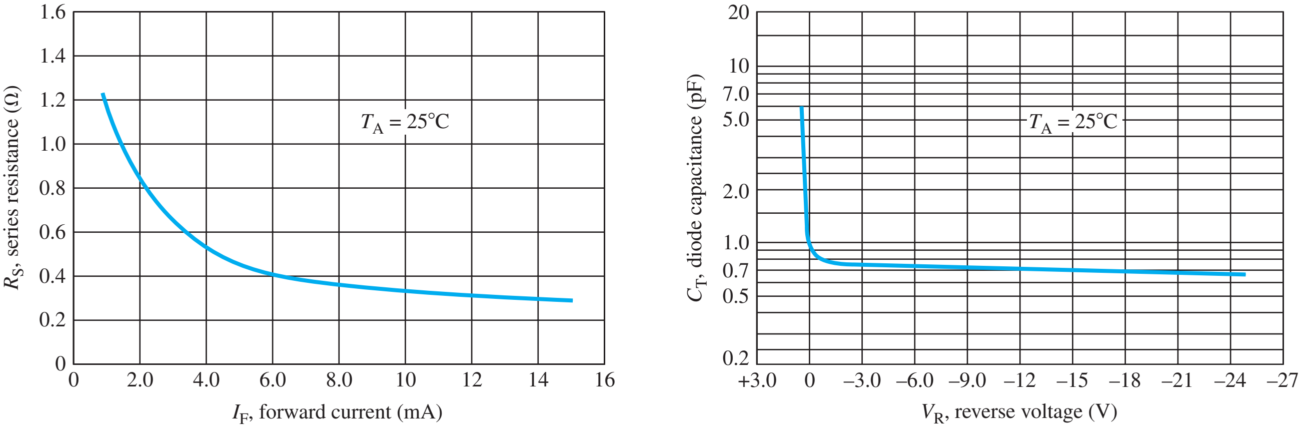
(a) Construction (b) Reverse-biased (c) Forward-biased

▲ **FIGURE 3–51**

PIN diode.

The forward series resistance characteristic and the reverse capacitance characteristic are shown graphically in Figure 3–52 for a typical *pin* diode.

The *pin* diode is used as a dc-controlled microwave switch operated by rapid changes in bias or as a modulating device that takes advantage of the variable forward-resistance characteristic. Since no rectification occurs at the *pn* junction, a high-frequency signal can be modulated (varied) by a lower-frequency bias variation. A *pin* diode can also be used in attenuator applications because its resistance can be controlled by the amount of current. Certain types of *pin* diodes are used as photodetectors in fiber-optic systems.



▲ FIGURE 3–52

PIN diode characteristics.

The Step-Recovery Diode

The step-recovery diode uses graded doping where the doping level of the semiconductive materials is reduced as the *pn* junction is approached. This produces an abrupt turn-off time by allowing a fast release of stored charge when switching from forward to reverse bias. It also allows a rapid re-establishment of forward current when switching from reverse to forward bias. This diode is used in very high frequency (VHF) and fast-switching applications.

The Tunnel Diode

The tunnel diode exhibits a special characteristic known as *negative resistance.* This feature makes it useful in oscillator and microwave amplifier applications. Two alternate symbols are shown in Figure 3–53. Tunnel diodes are constructed with germanium or gallium arsenide by doping the *p* and *n* regions much more heavily than in a conventional rectifier diode. This heavy doping results in an extremely narrow depletion region. The heavy doping allows conduction for all reverse voltages so that there is no breakdown effect as with the conventional rectifier diode. This is shown in Figure 3–54.

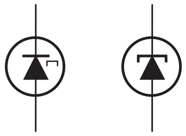
Also, the extremely narrow depletion region permits electrons to "tunnel" through the *pn* junction at very low forward-bias voltages, and the diode acts as a conductor. This is shown in Figure 3–54 between points *A* and *B*. At point *B*, the forward voltage begins to develop a barrier, and the current begins to decrease as the forward voltage continues to increase. This is the *negative-resistance region.*

$$R_F = \frac{\Delta V_F}{\Delta I_F}$$

This effect is opposite to that described in Ohm's law, where an increase in voltage results in an increase in current. At point *C,* the diode begins to act as a conventional forward-biased diode.

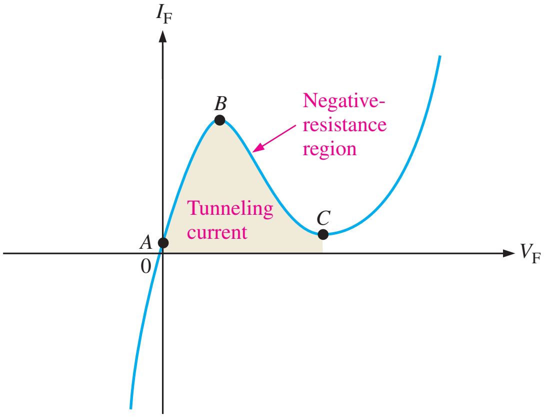
HISTORY NOTE

Leo Esaki won the Nobel Prize in physics in 1973 for the invention of the tunnel diode in the late 1950s. Surprisingly, in 1976 Robert Noyce, cofounder of Intel Corp., revealed in a talk before the MIT Club of New York that he had in his notebooks from 1956 a complete description of the tunnel diode. However, credit for the invention is given to Esaki and the tunnel diode is also known as the Esaki diode in his honor.



▲ FIGURE 3–53

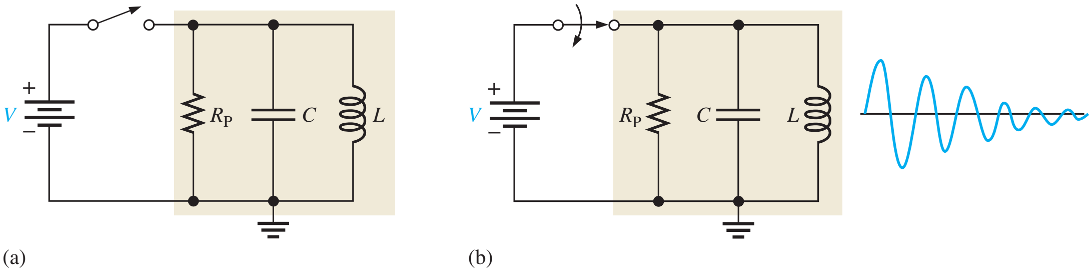
Tunnel diode symbols.



◀ **FIGURE 3–54**

Tunnel diode characteristic curve.

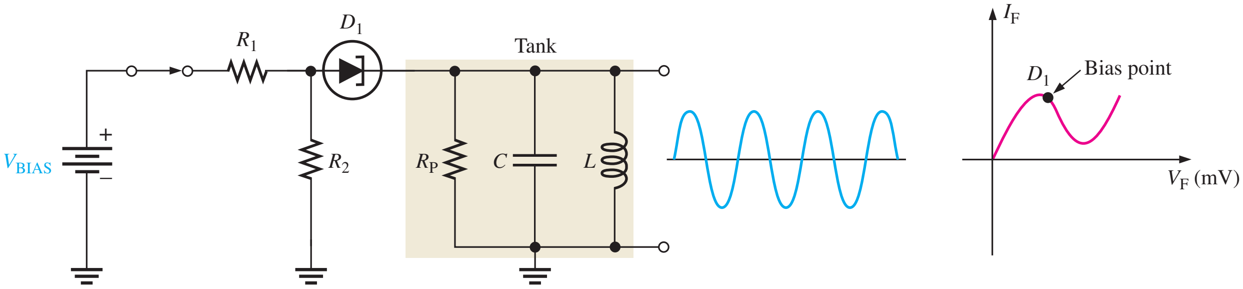
An Application A parallel resonant circuit can be represented by a capacitance, inductance, and resistance in parallel, as in Figure 3–55(a). R_P is the parallel equivalent of the series winding resistance of the coil. When the tank circuit is "shocked" into oscillation by an application of voltage as in Figure 3–55(b), a damped sinusoidal output results. The damping is due to the resistance of the tank, which prevents a sustained oscillation because energy is lost when there is current through the resistance.



▲ **FIGURE 3–55**

Parallel resonant circuit.

If a tunnel diode is placed in series with the tank circuit and biased at the center of the negative-resistance portion of its characteristic curve, as shown in Figure 3–56, a sustained oscillation (constant sinusoidal voltage) will result on the output. This is because the negative-resistance characteristic of the tunnel diode counteracts the positive-resistance characteristic of the tank resistance. The tunnel diode is only used at very high frequencies.



▲ **FIGURE 3–56**

Basic tunnel diode oscillator.

Current Regulator Diode

The current regulator diode is often referred to as a constant-current diode. Rather than maintaining a constant voltage, as the zener diode does, this diode maintains a constant current. The symbol is shown in Figure 3–57.

▶ FIGURE 3–57

Symbol for a current regulator diode.

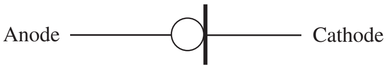
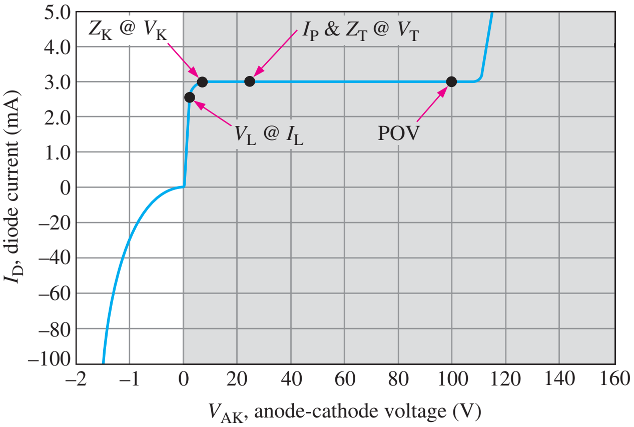


Figure 3–58 shows a typical characteristic curve. The current regulator diode operates in forward bias (shaded region), and the forward current becomes a specified constant value at forward voltages ranging from about 1.5 V to about 6 V, depending on the diode type. The constant forward current is called the *regulator current* and is designated I_P. For example, the 1N5283–1N5314 series of diodes have nominal regulator currents ranging from 220 μA to 4.7 mA. These diodes may be used in parallel to obtain higher currents. This diode does not have a sharply defined reverse breakdown, so the reverse current begins to increase for V_{AK} values of less than 0 V (unshaded region of the figure). This device should never be operated in reverse bias.

▶ FIGURE 3–58

Typical characteristic curve for a current regulator diode.



In forward bias, the diode regulation begins at the limiting voltage, V_L, and extends up to the POV (peak operating voltage). Notice that between V_K and POV, the current is essentially constant. V_T is the test voltage at which I_P and the diode impedance, Z_T, are specified on a datasheet. The impedance Z_T has very high values ranging from 235 kΩ to 25 MΩ for the diode series mentioned before.

SECTION 3–5 CHECKUP

1. What does *laser* mean?
2. What is the difference between incoherent and coherent light and which is produced by a laser diode?
3. What are the primary application areas for Schottky diodes?
4. What is a hot-carrier diode?
5. What is the key characteristic of a tunnel diode?
6. What is one application for a tunnel diode?
7. Name the three regions of a *pin* diode.
8. Between what two voltages does a current regulator diode operate?

3–6 TROUBLESHOOTING

In this section, you will see how a faulty zener diode can affect the output of a regulated dc power supply. Although IC regulators are generally used for power supply outputs, the zener is occasionally used when less precise regulation and low current is acceptable. Like other diodes, the zener can fail open, it can exhibit degraded performance, or it can short out.

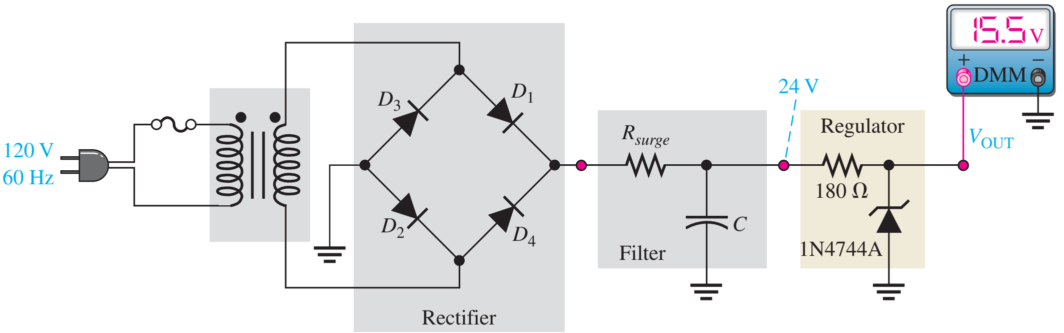
After completing this section, you should be able to

❑ **Troubleshoot zener diode regulators**
  ◆ Recognize the effects of an open zener ◆ Recognize the effects of a zener with degraded performance or shorted

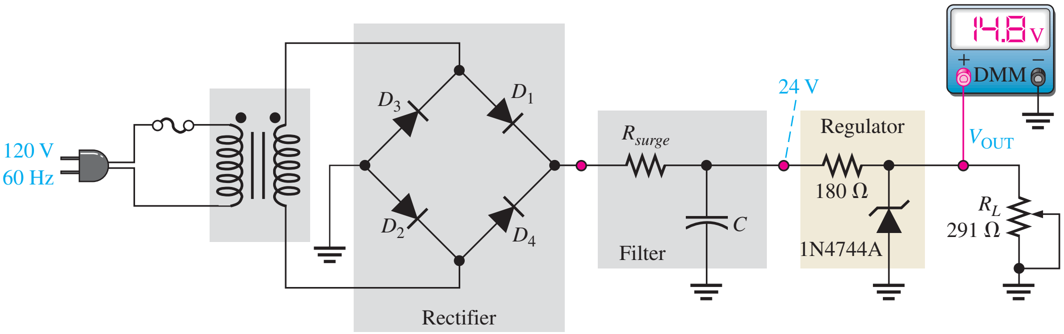
Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

A Zener-Regulated DC Power Supply

Figure 3–59 shows a filtered dc power supply that produces a constant 24 V before it is regulated down to 15 V by the zener regulator. The 1N4744A zener diode is the same as the one in Example 3–7. A no-load check of the regulated output voltage shows 15.5 V as indicated in part (a). The typical voltage expected at the zener test current for this particular


15.5 V
+
DMM
−
24 V
V_{OUT}
120 V
60 Hz
D_3
D_1
D_2
D_4
R_{surge}
C
Filter
Regulator
180 Ω
1N4744A
Rectifier

(a) Correct output voltage with no load


14.8 V
+
DMM
−
24 V
V_{OUT}
120 V
60 Hz
D_3
D_1
D_2
D_4
R_{surge}
C
Filter
Regulator
180 Ω
1N4744A
R_L
291 Ω
Rectifier

(b) Correct output voltage with full load

▲ FIGURE 3–59

Zener-regulated power supply test.

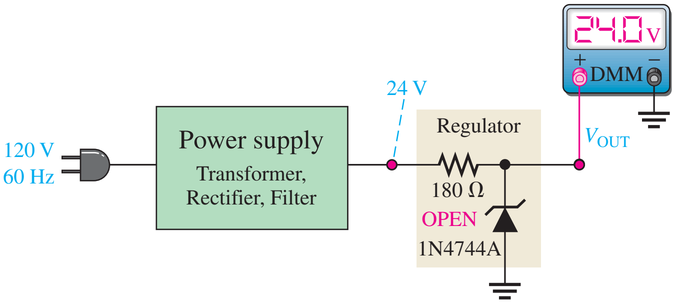
diode is 15 V. In part (b), a potentiometer is connected to provide a variable load resistance. It is adjusted to a minimum value for a full-load test as determined by the following calculations. The full-load test is at minimum zener current (I_{ZK}). The meter reading of 14.8 V indicates approximately the expected output voltage of 15.0 V.

$$I_T = \frac{24\text{ V} - 14.8\text{ V}}{180\ \Omega} = 51.1\text{ mA}$$

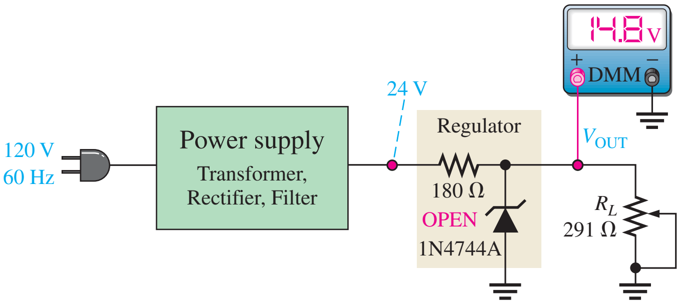
$$I_L = I_T - I_Z = 51.1\text{ mA} - 0.25\text{ mA} = 50.9\text{ mA}$$

$$R_{L(\min)} = \frac{14.8\text{ V}}{50.9\text{ mA}} = 291\ \Omega$$

Case 1: Zener Diode Open If the zener diode fails open, the power supply test gives the approximate results indicated in Figure 3–60. In the no-load check shown in part (a), the output voltage is 24 V because there is no voltage dropped between the filtered output of the power supply and the output terminal. This definitely indicates an open between the output terminal and ground. In the full-load check, the voltage of 14.8 V results from the voltage-divider action of the 180 Ω series resistor and the 291 Ω load. In this case, the result is too close to the normal reading to be a reliable fault indication but the no-load check will verify the problem. Also, if R_L is varied, V_{OUT} will vary if the zener diode is open.


24.0 V
+
DMM
−
24 V
Regulator
V_{OUT}
120 V
60 Hz
Power supply
Transformer,
Rectifier, Filter
180 Ω
OPEN
1N4744A

(a) Open zener diode with no load

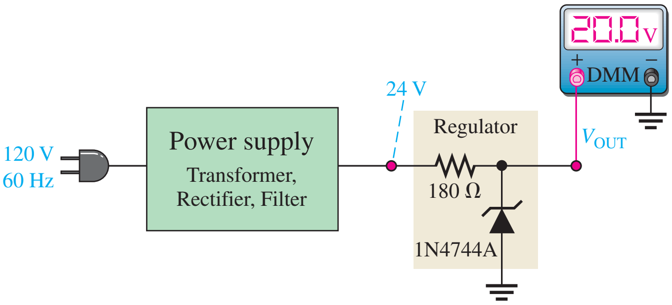

14.8 V
+
DMM
−
24 V
Regulator
V_{OUT}
120 V
60 Hz
Power supply
Transformer,
Rectifier, Filter
180 Ω
OPEN
1N4744A
R_L
291 Ω

(b) Open zener diode cannot be detected by full-load measurement in this case.

▲ FIGURE 3–60

Indications of an open zener.

Case 2: Incorrect Zener Voltage As indicated in Figure 3–61, a no-load check that results in an output voltage greater than the maximum zener voltage but less than the power supply output voltage indicates that the zener has failed such that its internal impedance is more than it should be. The 20 V output in this case is 4.5 V higher than the expected value of 15.5 V. That additional voltage indicates the zener is faulty or the wrong type has been installed. A 0 V output, of course, indicates that there is a short.



▲ FIGURE 3–61

Indication of faulty or wrong zener.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE03-01
2. Multisim file TSE03-02
3. Multisim file TSE03-03
4. Multisim file TSE03-04
5. Multisim file TSE03-05

SECTION 3–6 CHECKUP

1. In a zener regulator, what are the symptoms of an open zener diode?
2. If a zener regulator fails so that the zener impedance is greater than the specified value, is the output voltage more or less than it should be?
3. If you measure 0 V at the output of a zener-regulated power supply, what is the most likely fault(s)?
4. The zener diode regulator in a power supply is open. What will you observe on the output with a voltmeter if the load resistance is varied within its specified range?

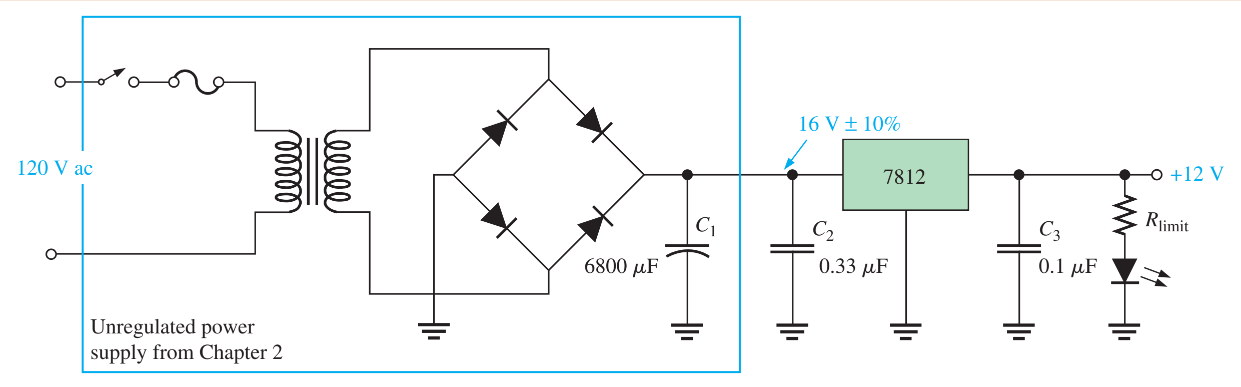
Application Activity: *Regulated DC Power Supply*

The unregulated 16 V dc power supply developed in Chapter 2 is to be upgraded to a regulated power supply with a fixed output voltage of 12 V. An integrated circuit 3–terminal voltage regulator is to be used and a red LED incorporated to indicate when the power is on. The printed circuit board for the unregulated power supply was designed to accommodate these additions.

The Circuit

Practical considerations for the circuit are the type of regulator, the selection of the LED power-on indicator and limiting resistor, and the value and placement of the fuse.

The Regulator The 78XX series of linear voltage regulators provide positive fixed output voltages for a range of values. The last two digits in the part number indicate the output voltage. The 7812 provides a 12 V regulated output. The change in output voltage for a specified change in input voltage is called the *line regulation.* The change in output voltage for a specified change in load current is called the *load regulation.* These parameters are specified on the datasheet. It is recommended by the manufacturer that a 0.33 μF capacitor be connected from the input terminal to ground and a 0.1 μF connected from the output terminal to ground, as shown in Figure 3–62 to prevent high-frequency oscillations and improve the performance. You may wonder about putting a small-value capacitor in parallel with a large one; the reason is that the large filter capacitor has an internal equivalent series resistance, which affects the high frequency response of the system. The effect is cancelled with the small capacitor.



▲ FIGURE 3–62

12 V regulated power supply.

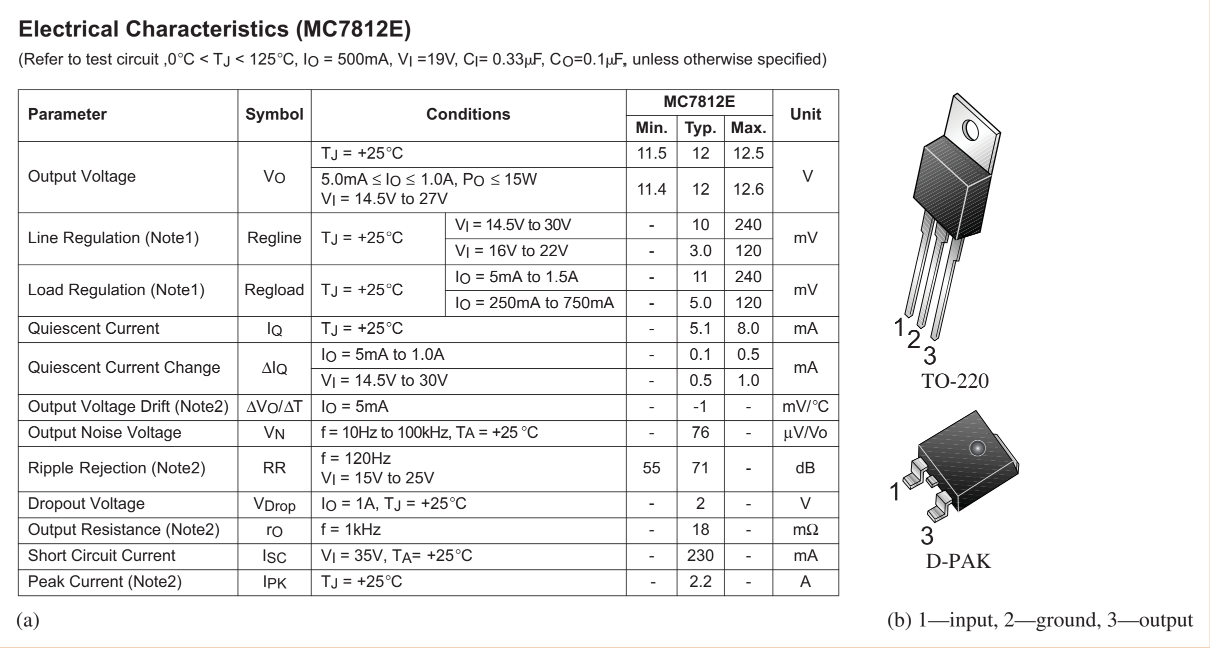
A partial datasheet for a 7812 is shown in Figure 3–63(a) Notice that there is a range of nominal output voltages, but it is typically 12 V. The line and load regulation specify how much the output can vary about the nominal output value. For example, the typical 12 V output will change no more than 11 mV (typical) as the load current changes from 5 mA to 1. 5 A. Package configurations are shown in part (b).

1. From the datasheet, determine the maximum output voltage if the input voltage to the regulator increases to 22 V, assuming a nominal output of 12 V.
2. From the datasheet, determine how much the typical output voltage changes when the load current changes from 250 mA to 750 mA.

The LED A typical partial datasheet for a visible red LED is shown in Figure 3–64. As the datasheet shows, a forward current of 10 mA to 20 mA is used for the test data.

3. Determine the value of the resistor shown in Figure 3–62 for limiting the LED current to 20 mA and use the next higher standard value. Also specify the power rating of the limiting resistor.

The Fuse The fuse will be in series with the primary winding of the transformer, as shown in Figure 3–62. The fuse should be calculated based on the maximum allowable primary current. Recall from your dc/ac circuits course that if the voltage is stepped



Electrical Characteristics (MC7812E)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =19V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

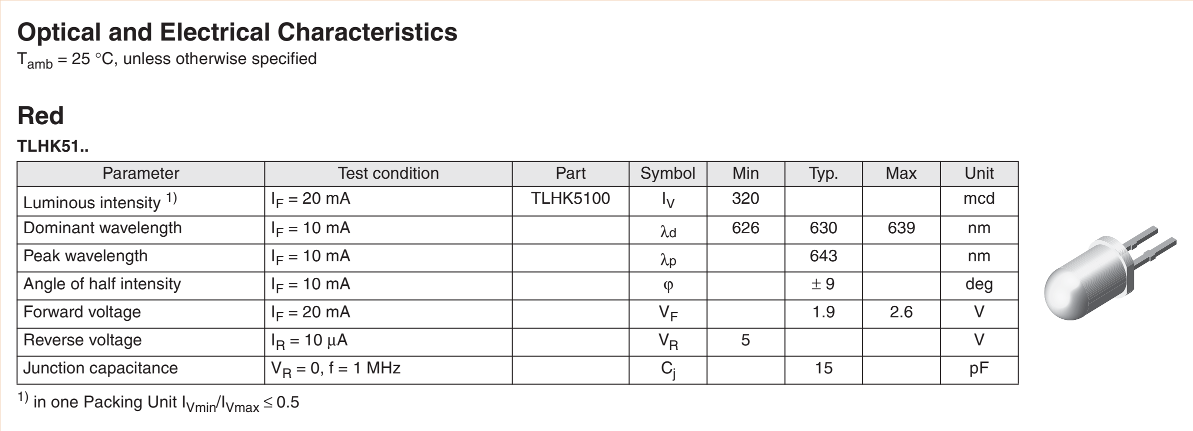
Parameter	Symbol	Conditions		MC7812E			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J = +25°C		11.5	12	12.5	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 14.5V to 27V		11.4	12	12.6	
Line Regulation (Note1)	Regline	T_J = +25°C	V_I = 14.5V to 30V	-	10	240	mV
			V_I = 16V to 22V	-	3.0	120	
Load Regulation (Note1)	Regload	T_J = +25°C	I_O = 5mA to 1.5A	-	11	240	mV
			I_O = 250mA to 750mA	-	5.0	120	
Quiescent Current	I_Q	T_J = +25°C		-	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.1	0.5	mA
		V_I = 14.5V to 30V		-	0.5	1.0	
Output Voltage Drift (Note2)	$\Delta V_O/\Delta T$	I_O = 5mA		-	-1	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100kHz, T_A = +25 °C		-	76	-	μV/Vo
Ripple Rejection (Note2)	RR	f = 120Hz V_I = 15V to 25V		55	71	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J = +25°C		-	2	-	V
Output Resistance (Note2)	r_O	f = 1kHz		-	18	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A= +25°C		-	230	-	mA
Peak Current (Note2)	I_{PK}	T_J = +25°C		-	2.2	-	A

(a)

(b) 1—input, 2—ground, 3—output

▲ FIGURE 3–63

Partial datasheet and packages for a 7812 regulator. You can view an entire datasheet at *www.fairchildsemiconductor.com*. Copyright Fairchild Semiconductor Corporation. Used by permission.



Optical and Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified

Red

TLHK51..

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Luminous intensity [1)]	I_F = 20 mA	TLHK5100	I_V	320			mcd
Dominant wavelength	I_F = 10 mA		λ_d	626	630	639	nm
Peak wavelength	I_F = 10 mA		λ_p		643		nm
Angle of half intensity	I_F = 10 mA		φ		± 9		deg
Forward voltage	I_F = 20 mA		V_F		1.9	2.6	V
Reverse voltage	I_R = 10 μA		V_R	5			V
Junction capacitance	V_R = 0, f = 1 MHz		C_j		15		pF

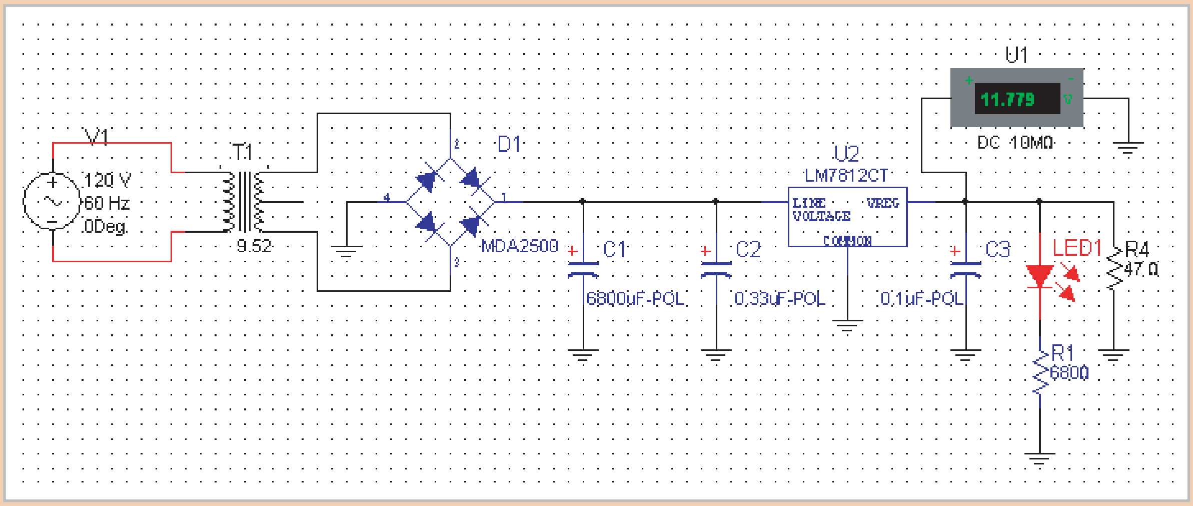
[1)] in one Packing Unit $I_{Vmin}/I_{Vmax} \leq 0.5$

▲ FIGURE 3–64

Partial datasheet and package for a typical red LED. To view a complete datasheet, go to *www. vishay.com*. Datasheet courtesy of Vishay Intertechnology, Inc.

down, the current is stepped up. From the specifications for the unregulated power supply, the maximum load current is 250 mA. The current required for the power-on LED indicator is 15 mA. So, the total secondary current is 265 mA. The primary current will be the secondary current divided by the turns ratio.

4. Calculate the primary current and use this value to select a fuse rating.



▲ FIGURE 3–65

Simulation of the regulated 12 V power supply circuit.

Simulation

In the development of a new circuit, it is helpful to simulate the circuit using a software program before actually building it and committing it to hardware. We will use Multisim to simulate this power supply circuit. Figure 3–65 shows the simulated regulated power supply circuit. The unregulated power supply was previously tested, so you need only to verify that the regulated output is correct. A load resistor value is chosen to draw a current equal to or greater than the specified maximum load current.

$$R_L = \frac{12\text{ V}}{250\text{ mA}} = 48\ \Omega$$

The closest standard value is 47 Ω, which draws 255 mA at 12 V.

5. Determine the power rating for the load resistor.

Simulate the circuit using your Multisim software. Verify the operation with the virtual voltmeter.

Prototyping and Testing

Now that all the components have been selected and the circuit has been simulated, the new components are added to the power supply protoboard from Experiment 2 and the circuit is tested.

Lab Experiment

To build and test a similar circuit, go to Experiment 3 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

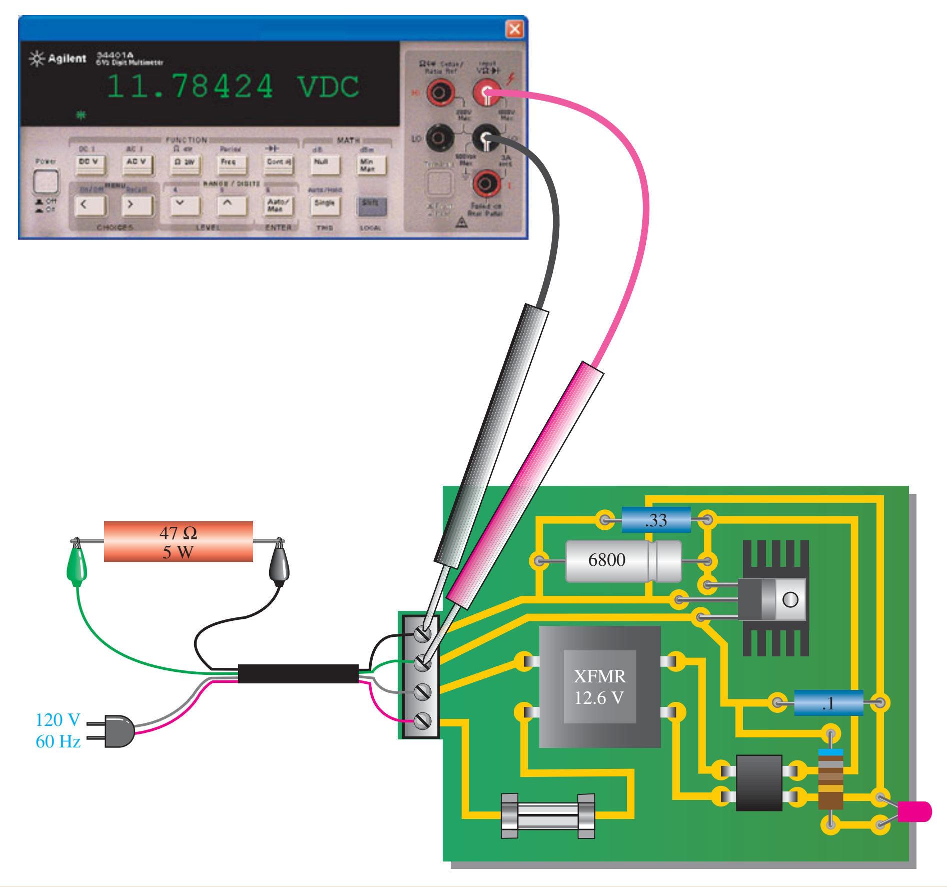
Printed Circuit Board

The 12 V regulated power supply prototype has been built and tested. It is now committed to a printed circuit layout, as shown in Figure 3–66. Notice that a heat sink is used with the regulator IC to increase its ability to dissipate power. With the ac line voltage and load resistor connected, the output voltage is measured.

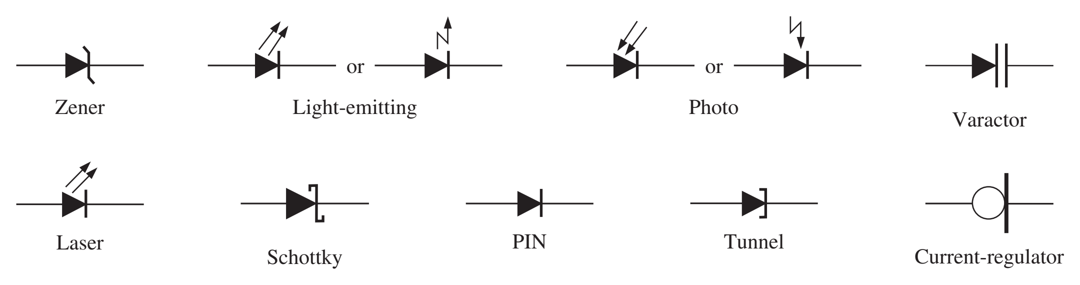
6. Compare the printed circuit board to the schematic in Figure 3–65.
7. Calculate the power dissipated by the regulator for an output of 12 V.

FIGURE 3–66

Regulated 12 V power supply on the printed circuit (PC) board.


Agilent 34401A
11.78424 VDC
47 Ω
5 W
120 V
60 Hz
.33
6800
XFMR
12.6 V
.1

SUMMARY OF DIODE SYMBOLS


Zener
or
Light-emitting
or
Photo
Varactor
Laser
Schottky
PIN
Tunnel
Current-regulator

SUMMARY

Section 3–1

- The zener diode operates in reverse breakdown.
- There are two breakdown mechanisms in a zener diode: avalanche breakdown and zener breakdown.
- When $V_Z < 5$ V, zener breakdown is predominant.

- When $V_Z > 5$ V, avalanche breakdown is predominant.
- A zener diode maintains a nearly constant voltage across its terminals over a specified range of zener currents.
- Zener diodes are available in many voltage ratings ranging from less than 1 V to more than 250 V.

Section 3–2

- Zener diodes are used as voltage references, regulators, and limiters.

Section 3–3

- A varactor diode acts as a variable capacitor under reverse-bias conditions.
- The capacitance of a varactor varies inversely with reverse-bias voltage.
- The current regulator diode keeps its forward current at a constant specified value.

Section 3–4

- An LED emits light when forward-biased.
- LEDs are available for either infrared or visible light.
- High-intensity LEDs are used in large-screen displays, traffic lights, automotive lighting, and home lighting.
- An organic LED (OLED) uses two or three layers of organic material to produce light.
- Quantum dots are semiconductor devices that emit light when energized from an external source.
- The photodiode exhibits an increase in reverse current with light intensity.

Section 3–5

- The Schottky diode has a metal-to-semiconductor junction. It is used in fast-switching applications.
- The tunnel diode is used in oscillator circuits.
- The *pin* diode has a *p* region, an *n* region, and an intrinsic (*i*) region and displays a variable resistance characteristic when forward-biased and a constant capacitance when reverse-biased.
- A laser diode is similar to an LED except that it emits coherent (single wavelength) light when the forward current exceeds a threshold value.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Electroluminescence The process of releasing light energy by the recombination of electrons in a semiconductor.

Laser *L*ight *a*mplification by *s*timulated *e*mission of *r*adiation.

Light-emitting diode (LED) A type of diode that emits light when there is forward current.

Photodiode A diode in which the reverse current varies directly with the amount of light.

Pixel In an LED display screen, the basic unit for producing colored light and consisting of red, green, and blue LEDs.

Varactor A variable capacitance diode.

Zener breakdown The lower voltage breakdown in a zener diode.

Zener diode A diode designed for limiting the voltage across its terminals in reverse bias.

KEY FORMULAS

3–1	$Z_Z = \dfrac{\Delta V_Z}{\Delta I_Z}$	Zener impedance
3–2	$\Delta V_Z = V_Z \times TC \times \Delta T$	V_Z temperature change when TC is %/°C
3–3	$\Delta V_Z = TC \times \Delta T$	V_Z temperature change when TC is mV/°C

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. The zener diode normally operates in reverse breakdown.
2. A zener diode can be used as a voltage regulator.
3. There is no current when a zener is in reverse breakdown.
4. The varactor diode normally operates in forward bias.
5. The varactor diode is used as a variable capacitor.
6. The capacitance of a varactor varies directly with reverse voltage.
7. The LED is based on the process of electroluminescence.
8. The LED is normally operated in forward bias.
9. OLED stands for operational light-emitting diode.
10. The photodiode operates in reverse bias.
11. The reverse current of a photodiode increases as the incident light increases.
12. The light emitted by a laser diode is monochromatic.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the input voltage in Figure 3–11 is increased from 5 V to 10 V, ideally the output voltage will
   (a) increase **(b)** decrease **(c)** not change
2. If the input voltage in Figure 3–14 is reduced by 2 V, the zener current will
   (a) increase **(b)** decrease **(c)** not change
3. If R_L in Figure 3–14 is removed, the current through the zener diode will
   (a) increase **(b)** decrease **(c)** not change
4. If the zener opens in Figure 3–14, the output voltage will
   (a) increase **(b)** decrease **(c)** not change
5. If R in Figure 3–14 is increased, the current to the load resistor will
   (a) increase **(b)** decrease **(c)** not change
6. If the input voltage amplitude in Figure 3–18(a) is increased, the positive output voltage will
   (a) increase **(b)** decrease **(c)** not change
7. If the input voltage amplitude in Figure 3–19(a) is reduced, the amplitude of the output voltage will
   (a) increase **(b)** decrease **(c)** not change
8. If the varactor capacitance is increased in Figure 3–26, the resonant frequency will
   (a) increase **(b)** decrease **(c)** not change
9. If the reverse voltage across the varactor in Figure 3–26 is increased, the frequency will
   (a) increase **(b)** decrease **(c)** not change
10. If the bias voltage in Figure 3–30 is increased, the light output of the LED will
    (a) increase **(b)** decrease **(c)** not change
11. If the bias voltage in Figure 3–30 is reversed, the light output of the LED will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 3–1

1. The cathode of a zener diode in a voltage regulator is normally
   (a) more positive than the anode **(b)** more negative than the anode
   (c) at +0.7 V **(d)** grounded

2. If a certain zener diode has a zener voltage of 3.6 V, it operates in

(a) regulated breakdown **(b)** zener breakdown

(c) forward conduction **(d)** avalanche breakdown

3. For a certain 12 V zener diode, a 10 mA change in zener current produces a 0.1 V change in zener voltage. The zener impedance for this current range is

(a) 1 Ω **(b)** 100 Ω **(c)** 10 Ω **(d)** 0.1 Ω

4. The datasheet for a particular zener gives $V_Z = 10$ V at $I_Z = 500$ mA. Z_Z for these conditions is

(a) 50 Ω **(b)** 20 Ω **(c)** 10 Ω **(d)** unknown

Section 3–2

5. A no-load condition means that

(a) the load has infinite resistance **(b)** the load has zero resistance

(c) the output terminals are open **(d)** answers(a) and (c)

Section 3–3

6. A varactor diode exhibits

(a) a variable capacitance that depends on reverse voltage

(b) a variable resistance that depends on reverse voltage

(c) a variable capacitance that depends on forward current

(d) a constant capacitance over a range of reverse voltages

Section 3–4

7. An LED

(a) emits light when reverse-biased **(b)** senses light when reverse-biased

(c) emits light when forward-biased **(d)** acts as a variable resistance

8. Compared to a visible red LED, an infrared LED

(a) produces light with shorter wavelengths **(b)** produces light of all wavelengths

(c) produces only one color of light **(d)** produces light with longer wavelengths

9. Compared to incandescent bulbs, high-intensity LEDs

(a) are brighter **(b)** have a much longer life

(c) use less power **(d)** all of the above

10. An OLED differs from a conventional LED in that it

(a) requires no bias voltage

(b) has layers of organic material in the place of a *pn* junction

(c) can be implemented using an inkjet printing process

(d) both (b) and (c)

11. An infrared LED is optically coupled to a photodiode. When the LED is turned off, the reading on an ammeter in series with the reverse-biased photodiode will

(a) not change **(b)** decrease

(c) increase **(d)** fluctuate

12. The internal resistance of a photodiode

(a) increases with light intensity when reverse-biased

(b) decreases with light intensity when reverse-biased

(c) increases with light intensity when forward-biased

(d) decreases with light intensity when forward-biased

Section 3–5

13. A laser diode produces

(a) incoherent light **(b)** coherent light

(c) monochromatic light **(d)** both (b) and (c)

14. A diode that has a negative resistance characteristic is the

(a) Schottky diode **(b)** tunnel diode **(c)** laser diode **(d)** hot-carrier diode

15. In order for a system to function properly, the various types of circuits that make up the system must be

(a) properly biased **(b)** properly connected **(c)** properly interfaced

(d) all of the above **(e)** answers(a) and (b)

PROBLEMS

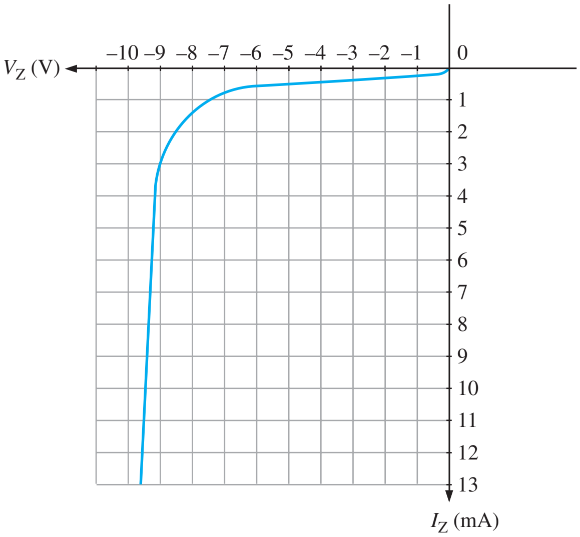
Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 3–1 The Zener Diode

1. A certain zener diode has a $V_Z = 7.5$ V and an $Z_Z = 5\ \Omega$ at a certain current. Draw the equivalent circuit.
2. From the characteristic curve in Figure 3–67, what is the approximate minimum zener current (I_{ZK}) and the approximate zener voltage at I_{ZK}?

▶ FIGURE 3–67

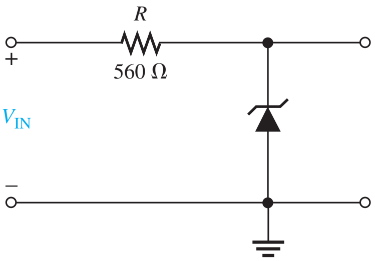


3. When the reverse current in a particular zener diode increases from 20 mA to 30 mA, the zener voltage changes from 5.6 V to 5.65 V. What is the impedance of this device?
4. A zener has an impedance of 15 Ω. What is its terminal voltage at 50 mA if $V_Z = 4.7$ V at $I_Z = 25$ mA?
5. A certain zener diode has the following specifications: $V_Z = 6.8$ V at 25°C and $TC = +0.04\%/°C$. Determine the zener voltage at 70°C.

Section 3–2 Zener Diode Applications

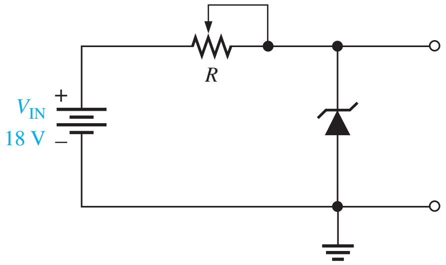
6. Determine the minimum input voltage required for regulation to be established in Figure 3–68. Assume an ideal zener diode with $I_{ZK} = 1.5$ mA and $V_Z = 14$ V.

▶ FIGURE 3–68



7. Repeat Problem 6 with $Z_Z = 20\ \Omega$ and $V_Z = 14$ V at 30 mA.

▶ FIGURE 3–69



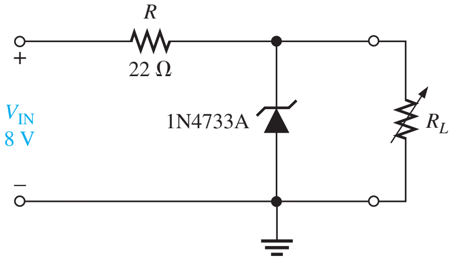
8. To what value must R be adjusted in Figure 3–69 to make $I_Z = 40$ mA? Assume $V_Z = 12$ V at 30 mA and $Z_Z = 30\ \Omega$.

9. A 20 V peak sinusoidal voltage is applied to the circuit in Figure 3–69 in place of the dc source. Draw the output waveform. Use the parameter values established in Problem 8.

10. A loaded zener regulator is shown in Figure 3–70. $V_Z = 5.1$ V at $I_Z = 49$ mA, $I_{ZK} = 1$ mA, $Z_Z = 7\ \Omega$, and $I_{ZM} = 70$ mA. Determine the minimum and maximum permissible load currents.

▶ FIGURE 3–70

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F03-70).



11. Find the load regulation expressed as a percentage in Problem 10. Refer to Chapter 2, Equation 2–15.

12. Analyze the circuit in Figure 3–70 for percent line regulation using an input voltage from 6 V to 12 V with no load. Refer to Chapter 2, Equation 2–14.

13. The no-load output voltage of a certain zener regulator is 8.23 V, and the full-load output is 7.98 V. Calculate the load regulation expressed as a percentage. Refer to Chapter 2, Equation 2–15.

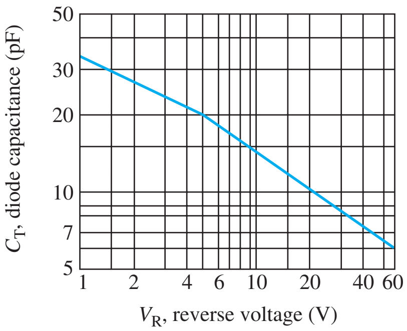
14. In a certain zener regulator, the output voltage changes 0.2 V when the input voltage goes from 5 V to 10 V. What is the input regulation expressed as a percentage? Refer to Chapter 2, Equation 2–14.

15. The output voltage of a zener regulator is 3.6 V at no load and 3.4 V at full load. Determine the load regulation expressed as a percentage. Refer to Chapter 2, Equation 2–15.

Section 3–3 The Varactor Diode

16. Figure 3–71 is a curve of reverse voltage versus capacitance for a certain varactor. Determine the change in capacitance if V_R varies from 5 V to 20 V.

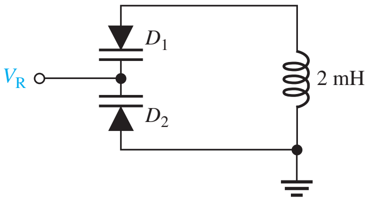
▶ FIGURE 3–71



17. Refer to Figure 3–71 and determine the approximate value of V_R that produces 25 pF.

18. What capacitance value is required for each of the varactors in Figure 3–72 to produce a resonant frequency of 1 MHz?

▶ FIGURE 3–72

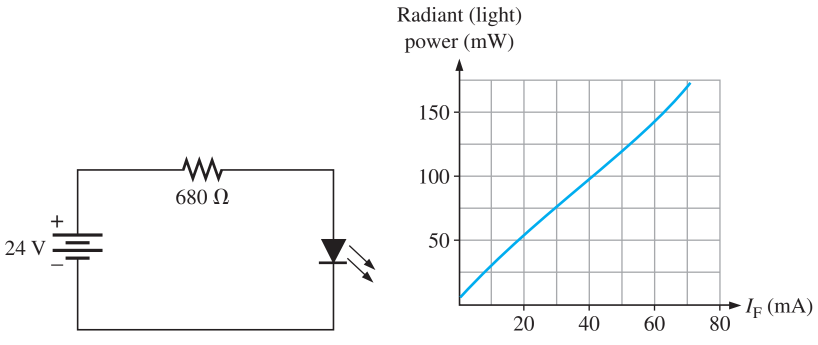


19. At what value must the voltage V_R be set in Problem 18 if the varactors have the characteristic curve in Figure 3–72?

Section 3–4 Optical Diodes

20. The LED in Figure 3–73(a) has a light-producing characteristic as shown in part (b). Neglecting the forward voltage drop of the LED, determine the amount of radiant (light) power produced in mW.

▶ FIGURE 3–73

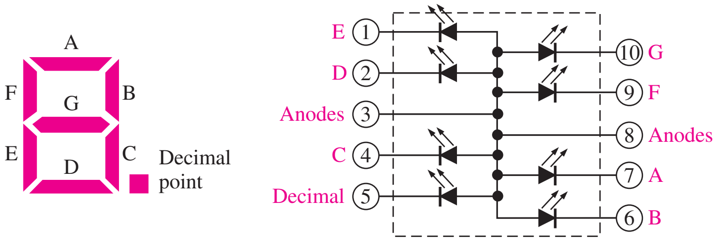


(a)

(b)

21. Determine how to connect the seven-segment display in Figure 3–74 to display “5.” The maximum continuous forward current for each LED is 30 mA and a +5 V dc source is to be used.

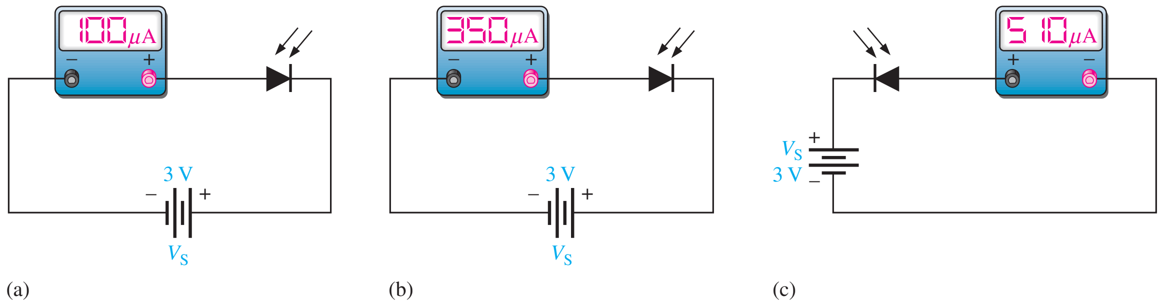
▶ FIGURE 3–74



22. Specify the number of limiting resistors and their value for a series-parallel array of 48 red LEDs using a 9 V dc source for a forward current of 20 mA.

23. Develop a yellow LED traffic-light array using a minimum number of limiting resistors that operates from a 24 V supply and consists of 100 LEDs with $I_F = 30$ mA and an equal number of LEDs in each parallel branch. Show the circuit and the resistor values.

24. For a certain photodiode at a given irradiance, the reverse resistance is 200 kΩ and the reverse voltage is 10 V. What is the current through the device?

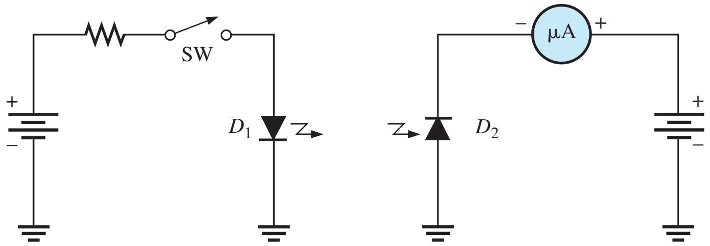


▲ FIGURE 3–75

25. What is the resistance of each photodiode in Figure 3–75?

26. When the switch in Figure 3–76 is closed, will the microammeter reading increase or decrease? Assume D_1 and D_2 are optically coupled.

▶ FIGURE 3–76



Section 3–5 Other Types of Diodes

27. The *V-I* characteristic of a certain tunnel diode shows that the current changes from 0.25 mA to 0.15 mA when the voltage changes from 125 mV to 200 mV. What is the resistance?

28. In what type of circuit are tunnel diodes commonly used?

29. What purpose do the reflective surfaces in the laser diode serve? Why is one end only partially reflective?

Section 3–6 Troubleshooting

30. For each set of measured voltages at the points (1, 2, and 3) indicated in Figure 3–77, determine if they are correct and if not, identify the most likely fault(s). State what you would do to correct the problem once it is isolated. The zener is rated at 12 V.

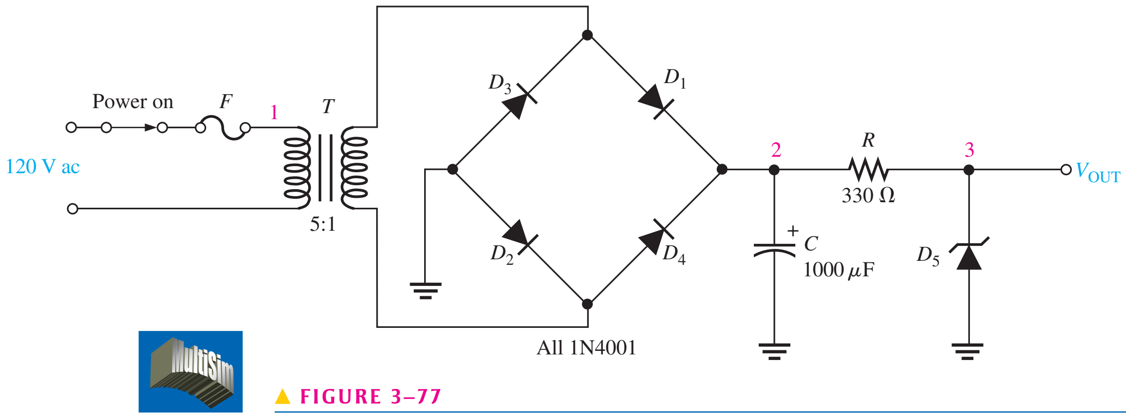
(a) $V_1 = 120$ V rms, $V_2 = 30$ V dc, $V_3 = 12$ V dc

(b) $V_1 = 120$ V rms, $V_2 = 30$ V dc, $V_3 = 30$ V dc

(c) $V_1 = 0$ V, $V_2 = 0$ V, $V_3 = 0$ V

(d) $V_1 = 120$ V rms, $V_2 = 30$ V peak full-wave 120 Hz, $V_3 = 12$ V, 120 Hz pulsating voltage

(e) $V_1 = 120$ V rms, $V_2 = 9$ V, $V_3 = 0$ V



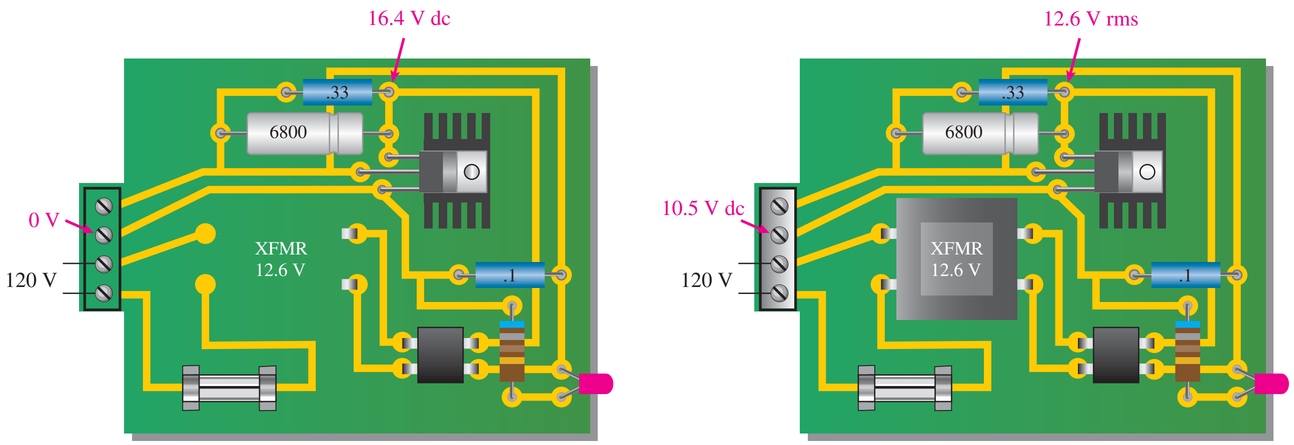
▲ FIGURE 3–77

31. What is the output voltage in Figure 3–77 for each of the following faults?

(a) D_5 open **(b)** *R* open **(c)** *C* leaky **(d)** *C* open
(e) D_3 open **(f)** D_2 open **(g)** *T* open **(h)** *F* open

APPLICATION ACTIVITY PROBLEMS

32. Based on the indicated voltage measurements with respect to ground in Figure 3–78(a), determine the probable fault(s).



(a) (b)

▲ FIGURE 3–78

33. Determine the probable fault(s) indicated by the voltage measurements in Figure 3–78(b).

34. List the possible reasons for the LED in Figure 3–78 not emitting light when the power supply is plugged in.

35. If a 1 kΩ load resistor is connected from the output pin to ground on a properly operating power supply circuit like shown in Figure 3–78, how much power will the 7812 regulator dissipate?

DATASHEET PROBLEMS

36. Refer to the zener diode datasheet in Figure 3–7.

(a) What is the maximum dc power dissipation at 25°C for a 1N4738A?

(b) Determine the maximum power dissipation at 70°C and at 100°C for a 1N4751A.

(c) What is the minimum current required by the 1N4738A for regulation?

(d) What is the maximum current for the 1N4750A at 25°C?

(e) The current through a 1N4740A changes from 25 mA to 0.25 mA. How much does the zener impedance change?

37. Refer to the varactor diode datasheet in Figure 3–24.

(a) What is the maximum forward current for the 832A?

(b) What is the maximum capacitance of an 830A at a reverse voltage of 2 V?

(c) What is the maximum capacitance range of an 836A?

38. Refer to the LED datasheet in Figure 3–34.

(a) Can 9 V be applied in reverse across an TSMF1000 LED?

(b) Determine the typical value of series resistor for the TSMF1000 when a voltage of 5.1 V is used to forward-bias the diode with $I_F = 20$ mA.

(c) Assume the forward current is 50 mA and the forward voltage drop is 1.5 V at an ambient temperature of 15°C. Is the maximum power rating exceeded?

(d) Determine the radiant intensity for a forward current of 40 mA.

(e) What is the radiant intensity at an angle of 20° from the axis if the forward current is 100 mA?

39. Refer to the photodiode datasheet in Figure 3–47.

(a) An TEMD1000 is connected in series with a 1 kΩ resistor and a reverse-bias voltage source. There is no incident light on the diode. What is the maximum voltage drop across the resistor?

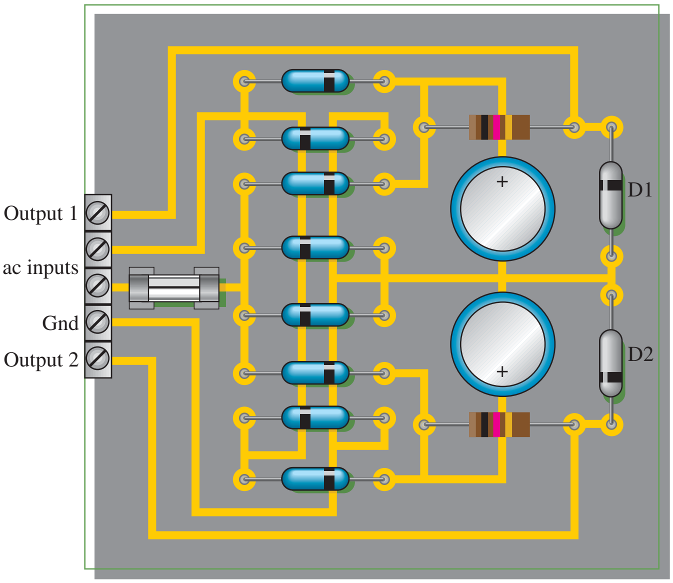
(b) At what wavelength will the reverse current be the greatest for a given irradiance?

(c) At what wavelength is relative spectral sensitivity of the TEMD1000 equal to 0.4?

ADVANCED PROBLEMS

40. Develop the schematic for the circuit board in Figure 3–79 and determine what type of circuit it is.

▶ FIGURE 3–79



Rectifier diodes: 1N4001A
Zener diodes: D1-1N4736A, D2-1N4749A
Filter capacitors: 100 μF

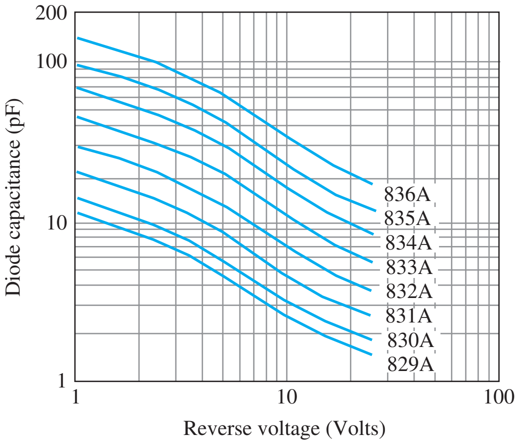
41. If a 30 V rms, 60 Hz input voltage is connected to the ac inputs, determine the output voltages on the circuit board in Figure 3–79.

42. If each output of the board in Figure 3–79 is loaded with 10 kΩ, what fuse rating should be used?

43. Design a zener voltage regulator to meet the following specifications: The input voltage is 24 V dc, the load current is 35 mA, and the load voltage is 8.2 V.

44. The varactor-tuned band-pass filter in Figure 3–27 is to be redesigned to produce a bandwidth of from 350 kHz to 850 kHz within a 10% tolerance. Specify what change you would have to make using the graph in Figure 3–80.

▶ FIGURE 3–80



45. Design a seven-segment red LED display circuit in which any of the ten digits can be displayed using a set of switches. Each LED segment is to have a current of 20 mA ± 10% from a 12 V source and the circuit must be designed with a minimum number of switches.

46. If you used a common-anode seven-segment display in Problem 45, redesign it for a common-cathode display or vice versa.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

47. Open file TSP03-47 and determine the fault.

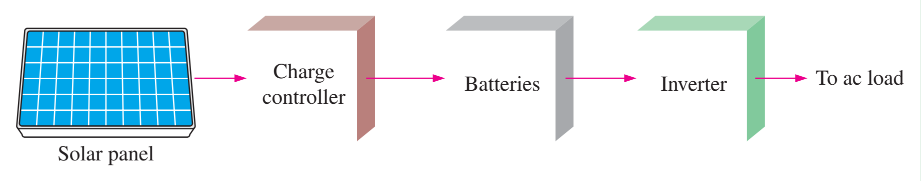
48. Open file TSP03-48 and determine the fault.

49. Open file TSP03-49 and determine the fault.

50. Open file TSP03-50 and determine the fault.

GreenTech Application 3: *Solar Power*

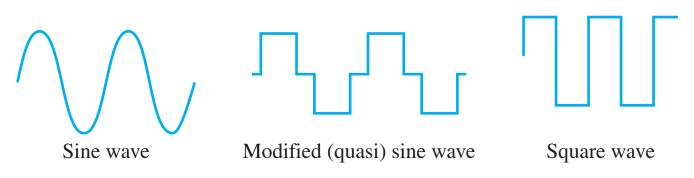
In GreenTech Application 1, the photovoltaic cell and a basic solar power system were introduced. In GreenTech Application 2, the charge controller was covered. In this chapter, the inverter is introduced. The system block diagram is shown again in Figure GA3–1.



▲ FIGURE GA3–1

The Inverter The inverter is a dc-to-ac converter that takes the output of the batteries in a solar power system and converts it to a standard 120 V, 60 Hz output voltage. This is the same as the voltage provided by the electric utilities companies. Some inverters can produce 240 V.

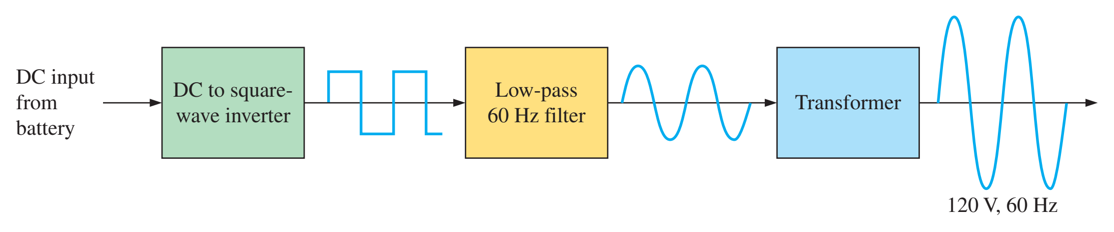
Basically, an inverter switches the dc output of the storage battery on and off and processes the result to create a pure sine wave, a stepped wave called a modified or quasi sine wave (sometimes called a modified square wave), or a square wave. Most inverters produce a pure sine wave, which is the type that the power company generates. Other outputs are found in cheaper inverters and are limited to providing power at lower efficiencies to only certain types of loads. The square wave inverter is seldom used, although it can be used as the basis for generating a pure sine wave. These three types of inverter outputs are shown in Figure GA3–2.



▲ FIGURE GA3–2

Types of inverter outputs.

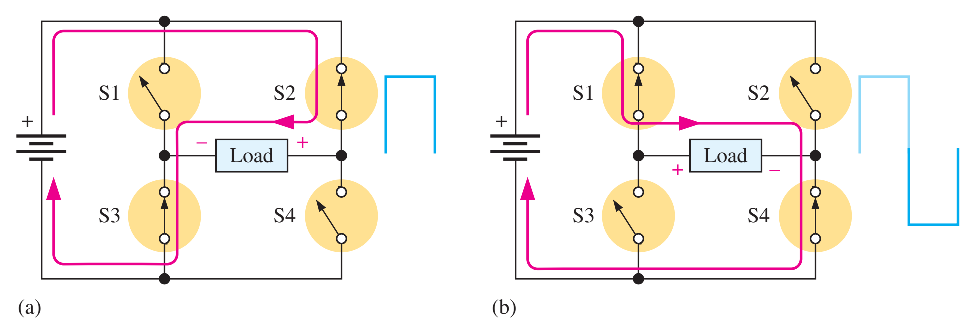
Recall from your dc/ac course that the harmonic content of a square wave includes a fundamental sine wave at the frequency of the square wave and a series of odd harmonics. One method of implementing a relatively pure sine wave inverter uses a dc to square wave inverter. The square wave is processed through a filter system to eliminate all of the odd harmonics, leaving only the fundamental sine wave, as illustrated in Figure GA3–3. A step-up transformer is used to produce the required 120 V, 60 Hz sine wave.



▲ FIGURE GA3–3

Basic concept of a pure sine wave inverter.

A switching circuit can be used in the conversion of dc voltage to an ac square wave voltage. One method is illustrated in Figure GA3–4 where switch symbols are used to represent switching transistors such as CMOS, which is discussed in Chapter 9. In part (a), switches S2 and S3 are on for a specified time and S1 and S4 are off. The direct current is through the load as shown creating a positive output voltage, as indicated. In part (b), opposite switches are on and off. The current is in the opposite direction through the load and the output voltage is negative. The complete on/off cycle of the switches produces an alternating square wave. The transistors are switched by a timing control circuit which is not shown for simplicity. The load is the filter in the pure sine wave inverter.



▲ FIGURE GA3–4

A method of producing a square wave from a dc voltage.

Inverters can have two types of interface: *stand-alone* and *grid-tie*. The stand-alone inverter is used in applications where all of the output power is used for a specified load, such as lighting, appliances, and motors, and is independent of the electrical power grid. Figure GA3–1 represents a stand-alone system. The grid-tie inverter is used in applications where all or part of the output power is provided to the electrical gird. For example, a home solar power system may share excess power not used in the home with the power company for credit if net metering is available. Some power companies have a net metering policy in which a special meter is installed and all power going to the electrical grid is deducted from power used by the on-site consumer. A large solar power system may be entirely devoted to producing power for the electrical gird.

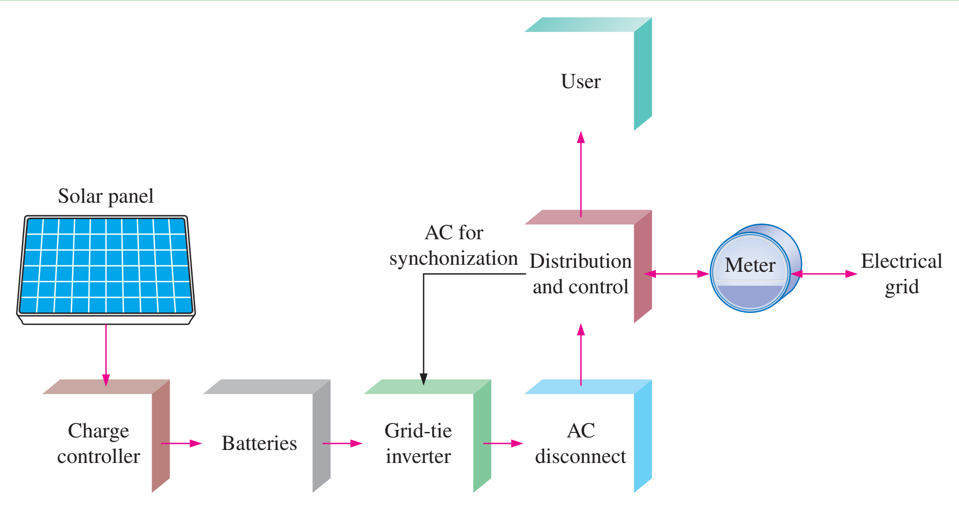
The Grid-Tie System A grid-tie inverter (GTI) must synchronize its ac output frequency (60 Hz) and phase with that of the grid, limit its amplitude for compatibility with the grid, and adjust its power factor to unity (voltage and current in phase). For safety reasons, grid-tie inverters have to disconnect from the grid if the grid goes down in a blackout. An option with grid-tie systems is that the solar panel can connect directly to the inverter with no battery backup. However, batteries allow the consumer to have energy available when they lose power from the grid. Figure GA3–5 shows the basic concept of a grid-tie solar power system with backup batteries.

During normal operation, the grid is supplying electrical power to the user and the power from the grid-tie inverter is fed back into the gird through the distribution and control circuits for credit from the power company. If the grid goes down, the ac disconnect prevents the power from the grid-tie inverter from feeding into the solar power is then switched directly to the user.

QUESTIONS

Some questions may require research beyond the content of this coverage. Answers can be found at www.pearsonhighered.com/floyd.

1. What is the difference between a stand-alone inverter and a grid-tie inverter?
2. What are two types of inverters in terms of the output waveforms?


User
Solar panel
AC for
synchronization
Distribution
and control
Meter
Electrical
grid
Charge
controller
Batteries
Grid-tie
inverter
AC
disconnect

▲ FIGURE GA3–5

Basic concept of grid-tie solar power system with battery backup.

3. How much average power should a solar power system for your home produce for the month of January? Hint: Use your utility bill.
4. Is net metering available in your area?
5. What is the range of inverters in terms of power that are commercially available?

The following websites are recommended for viewing solar inverters in action. Many other websites are also available.

http://www.youtube.com/watch?v=ra9gp21RpDU

http://www.youtube.com/watch?v=hANi5NbcY5g&feature=related

http://www.youtube.com/watch?v=mXi-sS7veFw&NR=1

BIPOLAR JUNCTION TRANSISTORS

4

CHAPTER OUTLINE

4–1 Bipolar Junction Transistor (BJT) Structure
4–2 Basic BJT Operation
4–3 BJT Characteristics and Parameters
4–4 The BJT as an Amplifier
4–5 The BJT as a Switch
4–6 The Phototransistor
4–7 Transistor Categories and Packaging
4–8 Troubleshooting
Application Activity
GreenTech Application 4: *Solar Power*

CHAPTER OBJECTIVES

- Describe the basic structure of the BJT
- Discuss basic BJT operation
- Discuss basic BJT parameters and characteristics and analyze transistor circuits
- Discuss how a BJT is used as a voltage amplifier
- Discuss how a BJT is used as a switch
- Discuss the phototransistor and its operation
- Identify various types of transistor packages
- Troubleshoot faults in transistor circuits

KEY TERMS

- BJT
- Emitter
- Base
- Collector
- Gain
- Beta
- Saturation
- Linear
- Cutoff
- Amplification
- Phototransistor

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

The invention of the transistor was the beginning of a technological revolution that is still continuing. All of the complex electronic devices and systems today are an outgrowth of early developments in semiconductor transistors.

Two basic types of transistors are the bipolar junction transistor (BJT), which we will begin to study in this chapter, and the field-effect transistor (FET), which we will cover in later chapters. The BJT is used in two broad areas—as a linear amplifier to boost or amplify an electrical signal and as an electronic switch. Both of these applications are introduced in this chapter.

APPLICATION ACTIVITY PREVIEW

Suppose you work for a company that makes a security alarm system for protecting homes and businesses against illegal entry. You are given the responsibility for final development and for testing each system before it is shipped out. The first step is to learn all you can about transistor operation. You will then apply your knowledge to the Application Activity at the end of the chapter.

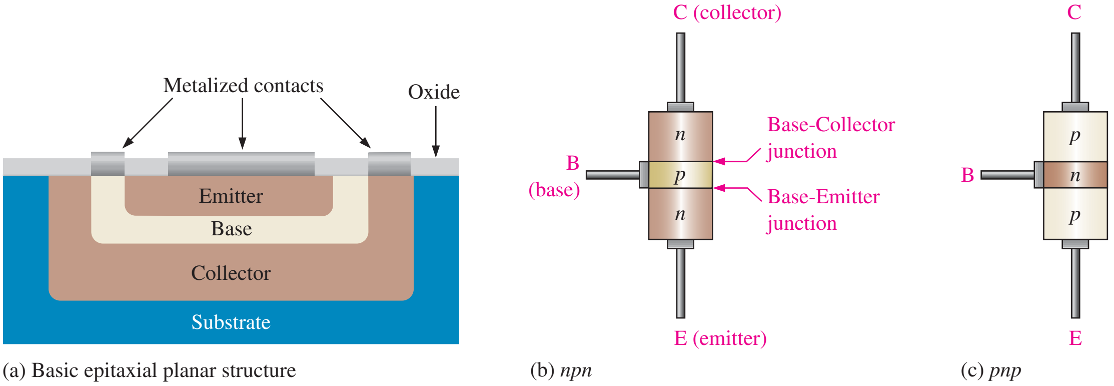
4–1 BIPOLAR JUNCTION TRANSISTOR (BJT) STRUCTURE

The basic structure of the bipolar junction transistor (BJT) determines its operating characteristics. In this section, you will see how semiconductive materials are used to form a BJT, and you will learn the standard BJT symbols.

After completing this section, you should be able to

- ☐ **Describe the basic structure of the BJT**
  - ◆ Explain the difference between the structure of an *npn* and a *pnp* transistor
  - ◆ Identify the symbols for *npn* and *pnp* transistors
  - ◆ Name the three regions of a BJT and their labels

The **BJT** is constructed with three doped semiconductor regions separated by two *pn* junctions, as shown in the epitaxial planar structure in Figure 4–1(a). The three regions are called **emitter**, **base**, and **collector**. Physical representations of the two types of BJTs are shown in Figure 4–1(b) and (c). One type consists of two *n* regions separated by a *p* region (*npn*), and the other type consists of two *p* regions separated by an *n* region (*pnp*). The term **bipolar** refers to the use of both holes and electrons as current carriers in the transistor structure.



(a) Basic epitaxial planar structure (b) *npn* (c) *pnp*

▲ **FIGURE 4–1**

Basic BJT construction.

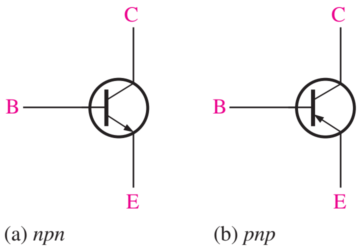
The *pn* junction joining the base region and the emitter region is called the *base-emitter junction*. The *pn* junction joining the base region and the collector region is called the *base-collector junction,* as indicated in Figure 4–1(b). A wire lead connects to each of the three regions, as shown. These leads are labeled E, B, and C for emitter, base, and collector, respectively. The base region is lightly doped and very thin compared to the heavily doped emitter and the moderately doped collector regions. (The reason for this is discussed in the next section.) Figure 4–2 shows the schematic symbols for the *npn* and *pnp* bipolar junction transistors.

HISTORY NOTE

The transistor was invented in 1947 by a team of scientists from Bell Laboratories. William Shockley, Walter Brattain, and John Bardeen developed the solid-state device that replaced the vacuum tube. Each received the Nobel prize in 1956. The transistor is arguably the most significant invention of the twentieth century.

▶ **FIGURE 4–2**

Standard BJT (bipolar junction transistor) symbols.



(a) *npn* (b) *pnp*

SECTION 4–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. Name the two types of BJTs according to their structure.
2. The BJT is a three-terminal device. Name the three terminals.
3. What separates the three regions in a BJT?

4–2 BASIC BJT OPERATION

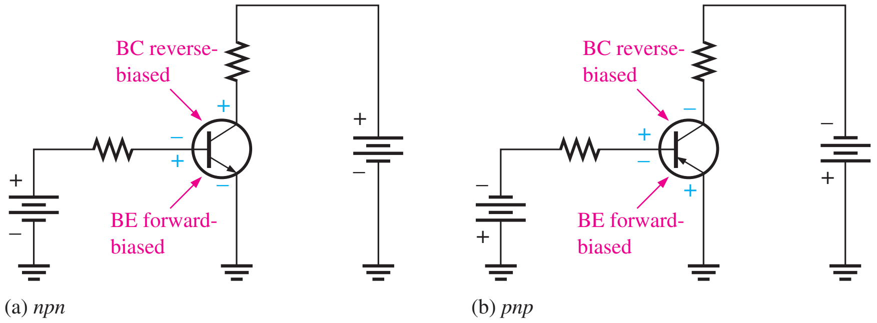
In order for a BJT to operate properly as an amplifier, the two *pn* junctions must be correctly biased with external dc voltages. In this section, we mainly use the *npn* transistor for illustration. The operation of the *pnp* is the same as for the *npn* except that the roles of the electrons and holes, the bias voltage polarities, and the current directions are all reversed.

After completing this section, you should be able to

- **Discuss basic BJT operation**
- Describe forward-reverse bias
    - Show how to bias *pnp* and *npn* BJTs with dc sources
- Explain the internal operation of a BJT
    - Discuss the hole and electron movement
- Discuss transistor currents
    - Calculate any of the transistor currents if the other two are known

Biasing

Figure 4–3 shows a bias arrangement for both *npn* and *pnp* BJTs for operation as an **amplifier.** Notice that in both cases the base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased. This condition is called *forward-reverse bias.*



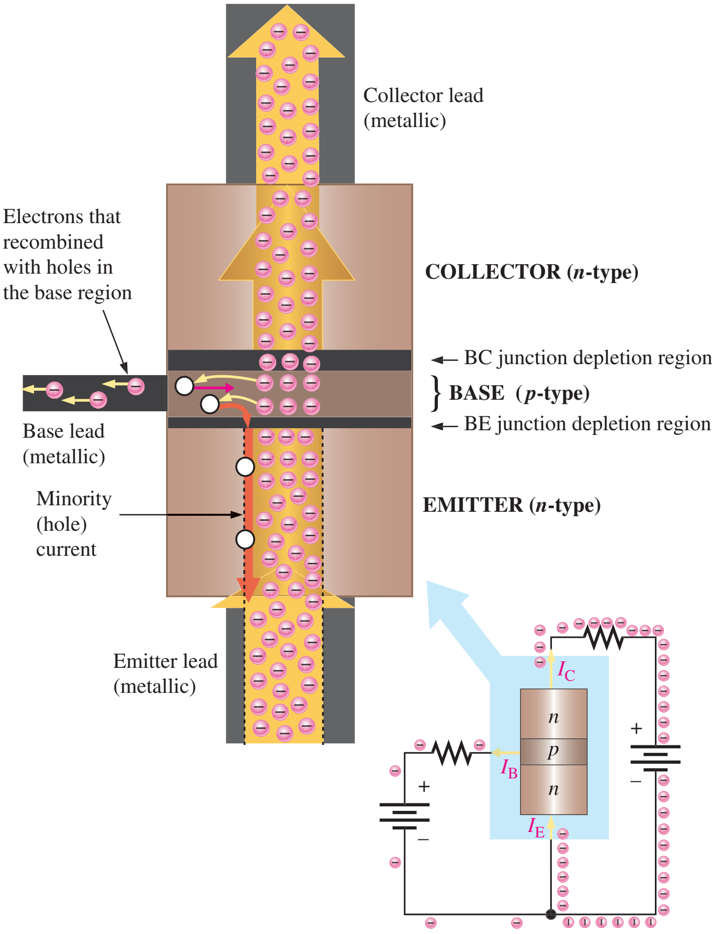
(a) *npn* (b) *pnp*

FIGURE 4–3

Forward-reverse bias of a BJT.

Operation

To understand how a transistor operates, let's examine what happens inside the *npn* structure. The heavily doped *n*-type emitter region has a very high density of conduction-band (free) electrons, as indicated in Figure 4–4. These free electrons easily diffuse through the forward-based BE junction into the lightly doped and very thin *p*-type base region, as indicated by the wide arrow. The base has a low density of holes, which are the majority carriers, as represented by the white circles. A small percentage of the total number of free electrons injected into the base region recombine with holes and move as valence electrons through the base region and into the emitter region as hole current, indicated by the red arrows.


Collector lead
(metallic)
Electrons that
recombined
with holes in
the base region
COLLECTOR (n-type)
BC junction depletion region
BASE (p-type)
BE junction depletion region
Base lead
(metallic)
Minority
(hole)
current
EMITTER (n-type)
Emitter lead
(metallic)
I_C
n
p
n
I_B
I_E
+
−
+
−

▲ FIGURE 4–4

BJT operation showing electron flow.

When the electrons that have recombined with holes as valence electrons leave the crystalline structure of the base, they become free electrons in the metallic base lead and produce the external base current. Most of the free electrons that have entered the base do not recombine with holes because the base is very thin. As the free electrons move toward the reverse-biased BC junction, they are swept across into the collector region by the attraction of the positive collector supply voltage. The free electrons move through the collector region, into the external circuit, and then return into the emitter region along with the base current, as indicated. The emitter current is slightly greater than the collector current because of the small base current that splits off from the total current injected into the base region from the emitter.

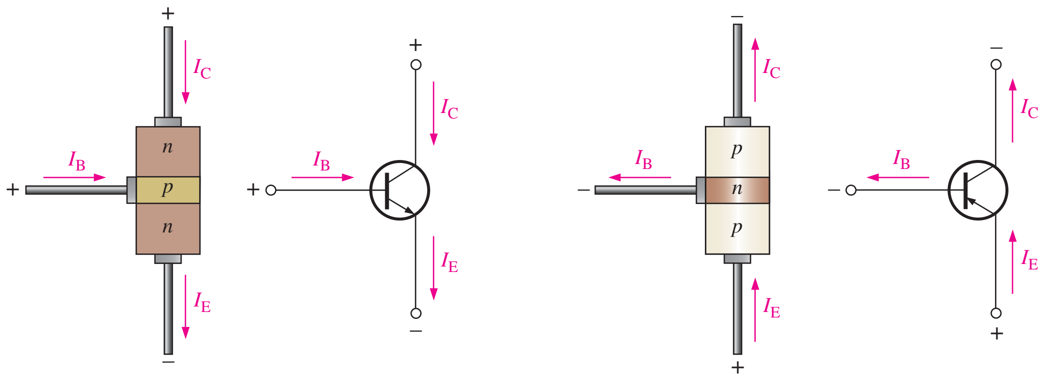
Transistor Currents

The directions of the currents in an *npn* transistor and its schematic symbol are as shown in Figure 4–5(a); those for a *pnp* transistor are shown in Figure 4–5(b). Notice that the arrow on the emitter inside the transistor symbols points in the direction of conventional current. These diagrams show that the emitter current (I_E) is the sum of the collector current (I_C) and the base current (I_B), expressed as follows:

Equation 4–1

$$\boldsymbol{I_E = I_C + I_B}$$

As mentioned before, I_B is very small compared to I_E or I_C. The capital-letter subscripts indicate dc values.



(a) *npn* (b) *pnp*

▲ **FIGURE 4–5**

Transistor currents.

SECTION 4–2 CHECKUP

1. What are the bias conditions of the base-emitter and base-collector junctions for a transistor to operate as an amplifier?
2. Which is the largest of the three transistor currents?
3. Is the base current smaller or larger than the emitter current?
4. Is the base region much thinner or much wider than the collector and emitter regions?
5. If the collector current is 1 mA and the base current is 10 μA, what is the emitter current?

4–3 BJT CHARACTERISTICS AND PARAMETERS

Two important parameters, β_{DC} (dc current gain) and α_{DC} are introduced and used to analyze a BJT circuit. Also, transistor characteristic curves are covered, and you will learn how a BJT's operation can be determined from these curves. Finally, maximum ratings of a BJT are discussed.

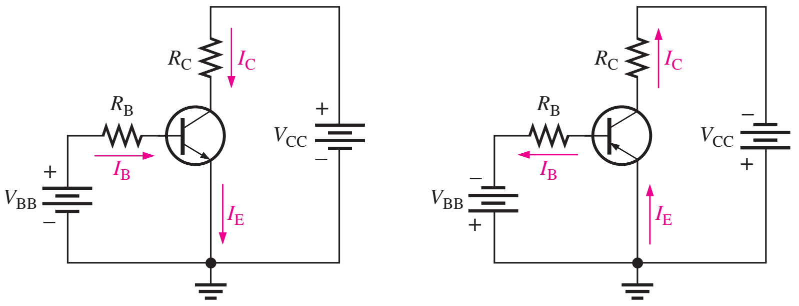
After completing this section, you should be able to

- **Discuss basic BJT parameters and characteristics and analyze transistor circuits**
- Define *dc beta* (β_{DC}) and *dc alpha* (α_{DC})
    - Calculate (β_{DC}) and (α_{DC}) based on transistor current
- Describe a basic dc model of a BJT
- Analyze BJT circuits
    - Identify transistor currents and voltages
    - Calculate each transistor current
    - Calculate each transistor voltage
- Interpret collector characteristic curves
    - Discuss the linear region
    - Explain saturation and cutoff in relation to the curves
- Describe the cutoff condition in a BJT circuit
- Describe the saturation condition in a BJT circuit
- Discuss the dc load line and apply it to circuit analysis
- Discuss how β_{DC} changes with temperature
- Explain and apply maximum transistor ratings
- Derate a transistor for power dissipation
- Interpret a BJT datasheet

When a transistor is connected to dc bias voltages, as shown in Figure 4–6 for both *npn* and *pnp* types, V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. Although in this chapter we are using separate battery symbols to represent the bias voltages, in practice the voltages are often derived from a single dc power supply. For example, V_{CC} is normally taken directly from the power supply output and V_{BB} (which is smaller) can be produced with a voltage divider. Bias circuits are examined thoroughly in Chapter 5.

FIGURE 4–6

Transistor dc bias circuits.



(a) *npn* (b) *pnp*

DC Beta (β_{DC}) and DC Alpha (α_{DC})

The dc current **gain** of a transistor is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated dc **beta** (β_{DC}).

Equation 4–2

$$\boldsymbol{\beta_{DC} = \frac{I_C}{I_B}}$$

Typical values of β_{DC} range from less than 20 to 200 or higher. β_{DC} is usually designated as an equivalent hybrid (h) parameter, h_{FE}, on transistor datasheets. h-parameters are covered in Chapter 6. All you need to know now is that

$$h_{FE} = \beta_{DC}$$

The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc **alpha** (α_{DC}). The alpha is a less-used parameter than beta in transistor circuits.

$$\alpha_{DC} = \frac{I_C}{I_E}$$

Typically, values of α_{DC} range from 0.95 to 0.99 or greater, but α_{DC} is always less than 1. The reason is that I_C is always slightly less than I_E by the amount of I_B. For example, if $I_E = 100$ mA and $I_B = 1$ mA, then $I_C = 99$ mA and $\alpha_{DC} = 0.99$.

EXAMPLE 4–1

Determine the dc current gain β_{DC} and the emitter current I_E for a transistor where $I_B = 50\ \mu$A and $I_C = 3.65$ mA.

Solution

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.65\text{ mA}}{50\ \mu\text{A}} = \mathbf{73}$$

$$I_E = I_C + I_B = 3.65\text{ mA} + 50\ \mu\text{A} = \mathbf{3.70\ mA}$$

Related Problem[*] A certain transistor has a β_{DC} of 200. When the base current is 50 μA, determine the collector current.

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[*] **Answers can be found at www.pearsonhighered.com/floyd**

Transistor DC Model

You can view the unsaturated BJT as a device with a current input and a dependent current source in the output circuit, as shown in Figure 4–7 for an *npn*.The input circuit is a forward-biased diode through which there is base current. The output circuit is a dependent current source (diamond-shaped element) with a value that is dependent on the base current, I_B, and equal to $\beta_{DC}I_B$. Recall that independent current source symbols have a circular shape.

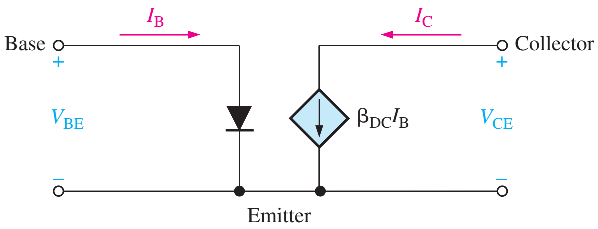


FIGURE 4–7

Ideal dc model of an *npn* transistor.

BJT Circuit Analysis

Consider the basic transistor bias circuit configuration in Figure 4–8. Three transistor dc currents and three dc voltages can be identified.

I_B: dc base current

I_E: dc emitter current

I_C: dc collector current

V_{BE}: dc voltage at base with respect to emitter

V_{CB}: dc voltage at collector with respect to base

V_{CE}: dc voltage at collector with respect to emitter

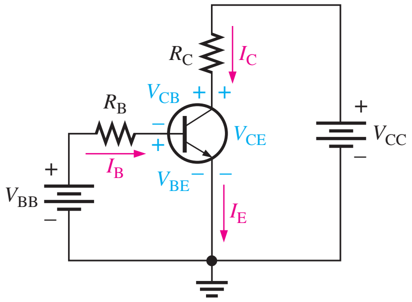


FIGURE 4–8

Transistor currents and voltages.

The base-bias voltage source, V_{BB}, forward-biases the base-emitter junction, and the collector-bias voltage source, V_{CC}, reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of

$$\mathbf{V_{BE} \cong 0.7\ V} \quad \text{Equation 4–3}$$

Although in an actual transistor V_{BE} can be as high as 0.9 V and is dependent on current, we will use 0.7 V throughout this text in order to simplify the analysis of the basic concepts. Keep in mind that the characteristic of the base-emitter junction is the same as a normal diode curve like the one in Figure 2-12.

Since the emitter is at ground (0 V), by Kirchhoff's voltage law, the voltage across R_B is

$$V_{R_B} = V_{BB} - V_{BE}$$

Also, by Ohm's law,

$$V_{R_B} = I_B R_B$$

Substituting for V_{R_B} yields

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for I_B,

Equation 4–4

$$\boldsymbol{I_B = \frac{V_{BB} - V_{BE}}{R_B}}$$

The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across R_C is

$$V_{R_C} = I_C R_C$$

the voltage at the collector with respect to the emitter can be written as

Equation 4–5

$$\boldsymbol{V_{CE} = V_{CC} - I_C R_C}$$

where $I_C = \beta_{DC} I_B$.

The voltage across the reverse-biased collector-base junction is

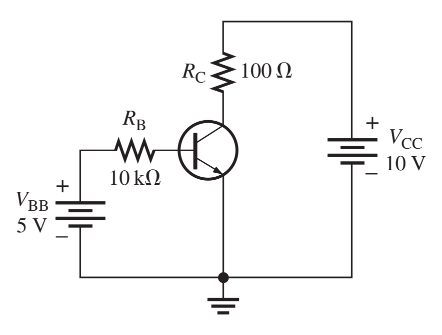
Equation 4–6

$$\boldsymbol{V_{CB} = V_{CE} - V_{BE}}$$

EXAMPLE 4–2

Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit of Figure 4–9. The transistor has a $\beta_{DC} = 150$.

▶ **FIGURE 4–9**



Solution From Equation 4–3, $V_{BE} \cong$ **0.7 V.** Calculate the base, collector, and emitter currents as follows:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = \mathbf{430\ \mu A}$$

$$I_C = \beta_{DC} I_B = (150)(430\ \mu\text{A}) = \mathbf{64.5\ mA}$$

$$I_E = I_C + I_B = 64.5\text{ mA} + 430\ \mu\text{A} = \mathbf{64.9\ mA}$$

Solve for V_{CE} and V_{CB}.

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (64.5\text{ mA})(100\ \Omega) = 10\text{ V} - 6.45\text{ V} = \mathbf{3.55\ V}$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55\text{ V} - 0.7\text{ V} = \mathbf{2.85\ V}$$

Since the collector is at a higher voltage than the base, the collector-base junction is reverse-biased.

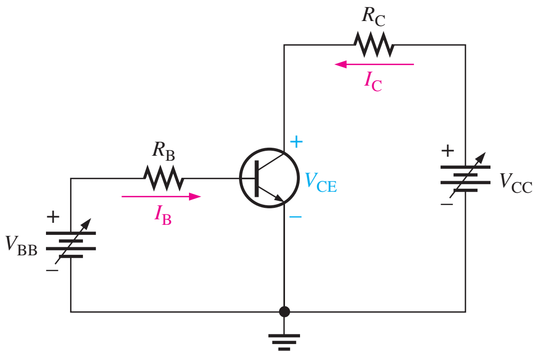
Related Problem Determine I_B, I_C, I_E, V_{CE}, and V_{CB} in Figure 4–9 for the following values: $R_B = 22\ \text{k}\Omega$, $R_C = 220\ \Omega$, $V_{BB} = 6$ V, $V_{CC} = 9$ V, and $\beta_{DC} = 90$.

Open the Multisim file E04-02 in the Examples folder on the companion website. Measure each current and voltage and compare with the calculated values.

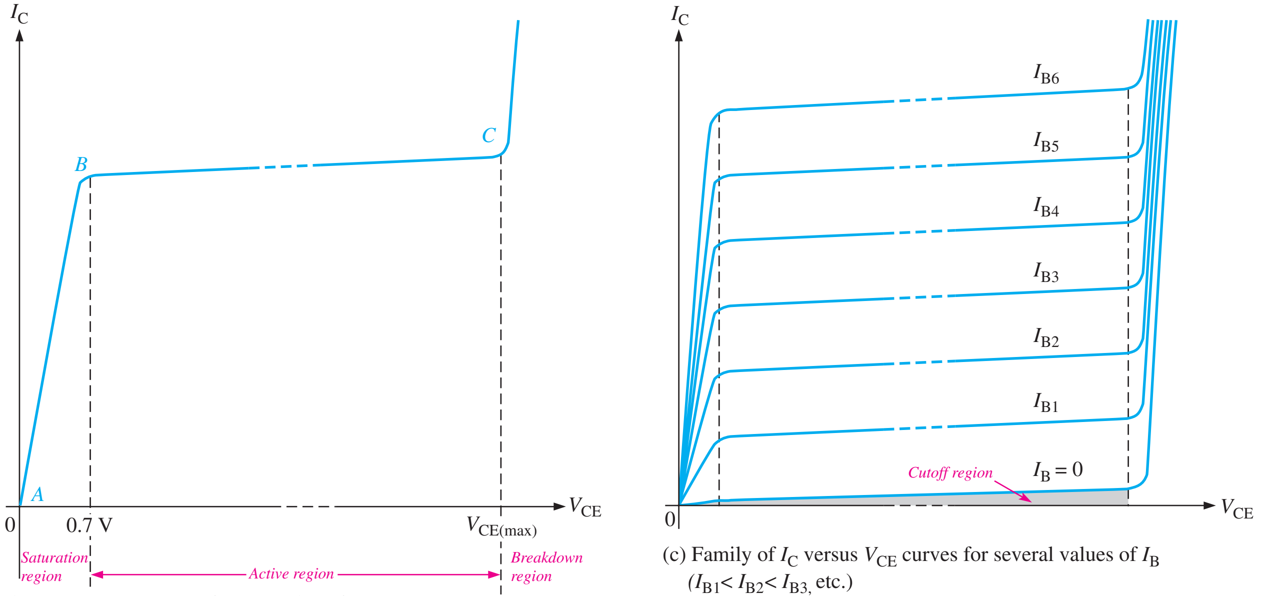
Collector Characteristic Curves

Using a circuit like that shown in Figure 4–10(a), a set of *collector characteristic curves* can be generated that show how the collector current, I_C, varies with the collector-to-emitter voltage, V_{CE}, for specified values of base current, I_B. Notice in the circuit diagram that both V_{BB} and V_{CC} are variable sources of voltage.

Assume that V_{BB} is set to produce a certain value of I_B and V_{CC} is zero. For this condition, both the base-emitter junction and the base-collector junction are forward-biased because the base is at approximately 0.7 V while the emitter and the collector are at 0 V. The base current is through the base-emitter junction because of the low impedance path to



(a) Circuit



(b) I_C versus V_{CE} curve for one value of I_B

(c) Family of I_C versus V_{CE} curves for several values of I_B ($I_{B1} < I_{B2} < I_{B3}$, etc.)

▲ **FIGURE 4–10**

Collector characteristic curves.

ground and, therefore, I_C is zero. When both junctions are forward-biased, the transistor is in the saturation region of its operation. **Saturation** is the state of a BJT in which the collector current has reached a maximum and is independent of the base current.

As V_{CC} is increased, V_{CE} increases as the collector current increases. This is indicated by the portion of the characteristic curve between points *A* and *B* in Figure 4–10(b). I_C increases as V_{CC} is increased because V_{CE} remains less than 0.7 V due to the forward-biased base-collector junction.

Ideally, when V_{CE} exceeds 0.7 V, the base-collector junction becomes reverse-biased and the transistor goes into the *active,* or **linear**, *region* of its operation. Once the base-collector junction is reverse-biased, I_C levels off and remains essentially constant for a given value of I_B as V_{CE} continues to increase. Actually, I_C increases very slightly as V_{CE} increases due to widening of the base-collector depletion region. This results in fewer holes for recombination in the base region which effectively causes a slight increase in β_{DC}. This is shown by the portion of the characteristic curve between points *B* and *C* in Figure 4–10(b). For this portion of the characteristic curve, the value of I_C is determined only by the relationship expressed as $I_C = \beta_{DC}I_B$.

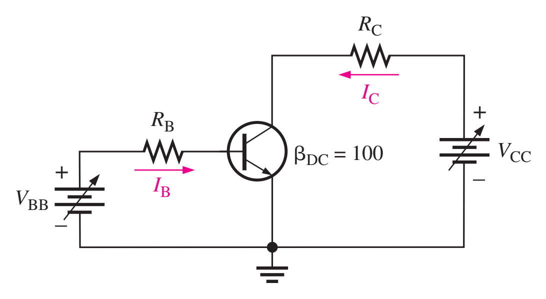
When V_{CE} reaches a sufficiently high voltage, the reverse-biased base-collector junction goes into breakdown; and the collector current increases rapidly as indicated by the part of the curve to the right of point *C* in Figure 4–10(b). A transistor should never be operated in this breakdown region.

A family of collector characteristic curves is produced when I_C versus V_{CE} is plotted for several values of I_B, as illustrated in Figure 4–10(c). When $I_B = 0$, the transistor is in the cutoff region although there is a very small collector leakage current as indicated. **Cutoff** is the nonconducting state of a transistor. The amount of collector leakage current for $I_B = 0$ is exaggerated on the graph for illustration.

EXAMPLE 4–3

Sketch an ideal family of collector curves for the circuit in Figure 4–11 for $I_B = 5\ \mu A$ to $25\ \mu A$ in $5\ \mu A$ increments. Assume $\beta_{DC} = 100$ and that V_{CE} does not exceed breakdown.

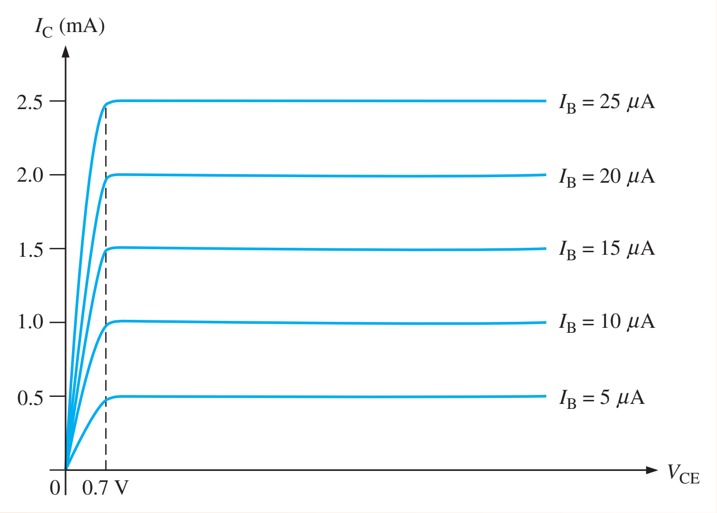
▶ FIGURE 4–11



Solution Using the relationship $I_C = \beta_{DC}I_B$, values of I_C are calculated and tabulated in Table 4–1. The resulting curves are plotted in Figure 4–12.

▶ TABLE 4–1

I_B	I_C
5 μA	0.5 mA
10 μA	1.0 mA
15 μA	1.5 mA
20 μA	2.0 mA
25 μA	2.5 mA

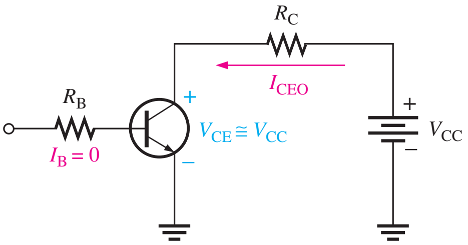


▲ **FIGURE 4–12**

Related Problem Where would the curve for $I_B = 0$ appear on the graph in Figure 4–12, neglecting collector leakage current?

Cutoff

As previously mentioned, when $I_B = 0$, the transistor is in the cutoff region of its operation. This is shown in Figure 4–13 with the base lead open, resulting in a base current of zero. Under this condition, there is a very small amount of collector leakage current, I_{CEO}, due mainly to thermally produced carriers. Because I_{CEO} is extremely small, it will usually be neglected in circuit analysis so that $V_{CE} = V_{CC}$. In cutoff, neither the base-emitter nor the base-collector junctions are forward-biased. The subscript CEO represents collector-to-emitter with the base open.



◀ **FIGURE 4–13**

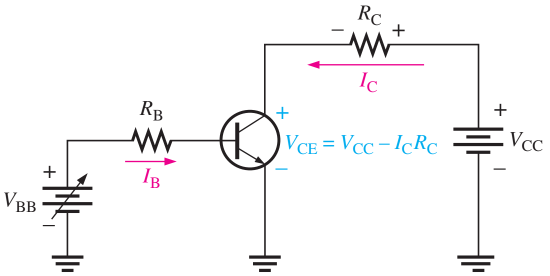
Cutoff: Collector leakage current (I_{CEO}) is extremely small and is usually neglected. Base-emitter and base-collector junctions are reverse-biased.

Saturation

When the base-emitter junction becomes forward-biased and the base current is increased, the collector current also increases ($I_C = \beta_{DC}I_B$) and V_{CE} decreases as a result of more drop across the collector resistor ($V_{CE} = V_{CC} - I_CR_C$). This is illustrated in Figure 4–14. When V_{CE} reaches its saturation value, $V_{CE(sat)}$, the base-collector junction becomes forward-biased and I_C can increase no further even with a continued increase in I_B. At the point of saturation, the relation $I_C = \beta_{DC}I_B$ is no longer valid. $V_{CE(sat)}$ for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt.

FIGURE 4–14

Saturation: As I_B increases due to increasing V_{BB}, I_C also increases and V_{CE} decreases due to the increased voltage drop across R_C. When the transistor reaches saturation, I_C can increase no further regardless of further increase in I_B. Base-emitter and base-collector junctions are forward-biased.

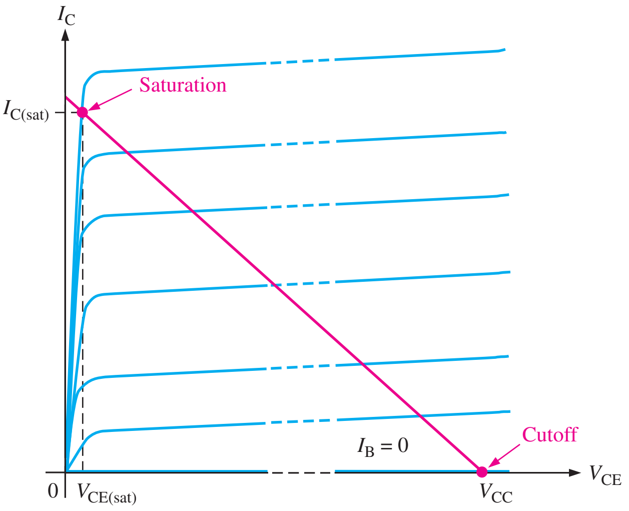


DC Load Line

Cutoff and saturation can be illustrated in relation to the collector characteristic curves by the use of a load line. Figure 4–15 shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point. The bottom of the load line is at ideal cutoff where $I_C = 0$ and $V_{CE} = V_{CC}$. The top of the load line is at saturation where $I_C = I_{C(sat)}$ and $V_{CE} = V_{CE(sat)}$. In between cutoff and saturation along the load line is the *active region* of the transistor's operation. Load line operation is discussed more in Chapter 5.

FIGURE 4–15

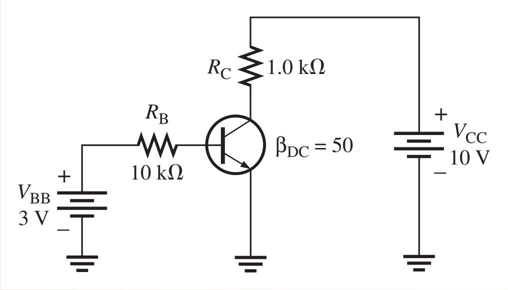
DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions.



EXAMPLE 4–4

Determine whether or not the transistor in Figure 4–16 is in saturation. Assume $V_{CE(sat)} = 0.2$ V.

FIGURE 4–16



Solution First, determine $I_{C(sat)}$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10\text{ V} - 0.2\text{ V}}{1.0\text{ k}\Omega} = \frac{9.8\text{ V}}{1.0\text{ k}\Omega} = 9.8\text{ mA}$$

Now, see if I_B is large enough to produce $I_{C(sat)}$.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = \frac{2.3\text{ V}}{10\text{ k}\Omega} = 0.23\text{ mA}$$

$$I_C = \beta_{DC}I_B = (50)(0.23\text{ mA}) = 11.5\text{ mA}$$

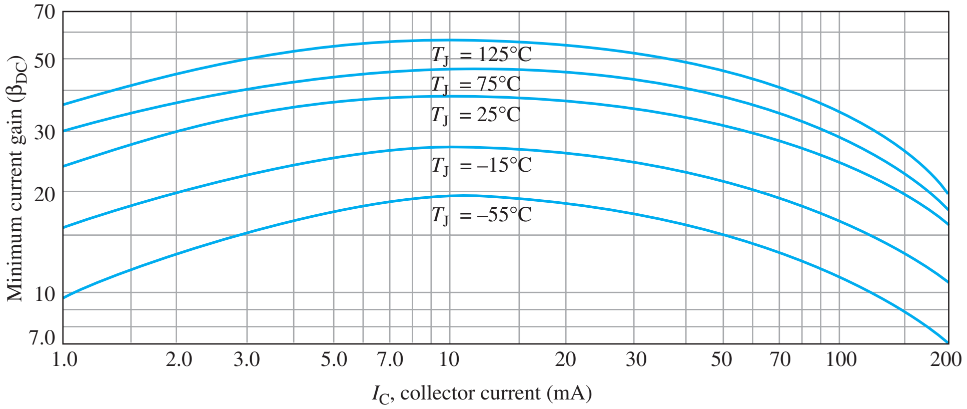
This shows that with the specified β_{DC}, this base current is capable of producing an I_C greater than $I_{C(sat)}$. Therefore, the **transistor is saturated,** and the collector current value of 11.5 mA is never reached. If you further increase I_B, the collector current remains at its saturation value of 9.8 mA.

Related Problem Determine whether or not the transistor in Figure 4–16 is saturated for the following values: $\beta_{DC} = 125$, $V_{BB} = 1.5$ V, $R_B = 6.8$ kΩ, $R_C = 180$ Ω, and $V_{CC} = 12$ V.

Open the Multisim file E04-04 in the Examples folder on the companion website. Determine if the transistor is in saturation and explain how you did this.

More About β_{DC}

The β_{DC} or h_{FE} is an important BJT parameter that we need to examine further. β_{DC} is not truly constant but varies with both collector current and with temperature. Keeping the junction temperature constant and increasing I_C causes β_{DC} to increase to a maximum. A further increase in I_C beyond this maximum point causes β_{DC} to decrease. If I_C is held constant and the temperature is varied, β_{DC} changes directly with the temperature. If the temperature goes up, β_{DC} goes up and vice versa. Figure 4–17 shows the variation of β_{DC} with I_C and junction temperature (T_J) for a typical BJT.



▲ FIGURE 4–17

Variation of β_{DC} with I_C for several temperatures.

A transistor datasheet usually specifies β_{DC} (h_{FE}) at specific I_C values. Even at fixed values of I_C and temperature, β_{DC} varies from one device to another for a given type of transistor due to inconsistencies in the manufacturing process that are unavoidable. The β_{DC} specified at a certain value of I_C is usually the minimum value, $\beta_{DC(min)}$, although the maximum and typical values are also sometimes specified.

Maximum Transistor Ratings

A BJT, like any other electronic device, has limitations on its operation. These limitations are stated in the form of maximum ratings and are normally specified on the manufacturer's datasheet. Typically, maximum ratings are given for collector-to-base voltage, collector-to-emitter voltage, emitter-to-base voltage, collector current, and power dissipation.

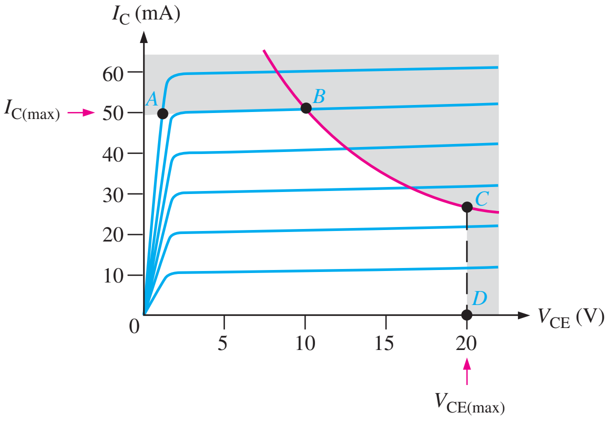
The product of V_{CE} and I_C must not exceed the maximum power dissipation. Both V_{CE} and I_C cannot be maximum at the same time. If V_{CE} is maximum, I_C can be calculated as

$$I_C = \frac{P_{D(max)}}{V_{CE}}$$

If I_C is maximum, V_{CE} can be calculated by rearranging the previous equation as follows:

$$V_{CE} = \frac{P_{D(max)}}{I_C}$$

For any given transistor, a maximum power dissipation curve can be plotted on the collector characteristic curves, as shown in Figure 4–18(a). These values are tabulated in Figure 4–18(b). Assume $P_{D(max)}$ is 500 mW, $V_{CE(max)}$ is 20 V, and $I_{C(max)}$ is 50 mA. The curve shows that this particular transistor cannot be operated in the shaded portion of the graph. $I_{C(max)}$ is the limiting rating between points *A* and *B*, $P_{D(max)}$ is the limiting rating between points *B* and *C*, and $V_{CE(max)}$ is the limiting rating between points *C* and *D*.



(a)

$P_{D(max)}$	V_{CE}	I_C
500 mW	5 V	100 mA
500 mW	10 V	50 mA
500 mW	15 V	33 mA
500 mW	20 V	25 mA

(b)

▲ **FIGURE 4–18**

Maximum power dissipation curve and tabulated values.

EXAMPLE 4–5

A certain transistor is to be operated with $V_{CE} = 6$ V. If its maximum power rating is 250 mW, what is the most collector current that it can handle?

Solution

$$I_C = \frac{P_{D(max)}}{V_{CE}} = \frac{250\text{ mW}}{6\text{ V}} = \mathbf{41.7\ mA}$$

This is the maximum current for this particular value of V_{CE}. The transistor can handle more collector current if V_{CE} is reduced, as long as $P_{D(max)}$ and $I_{C(max)}$ are not exceeded.

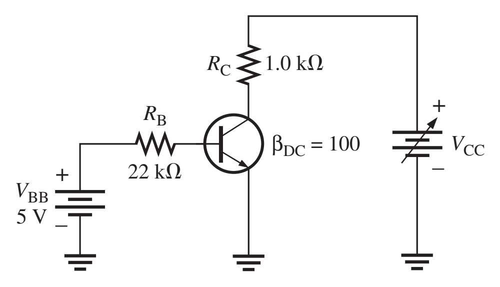
Related Problem

If $P_{D(max)} = 1$ W, how much voltage is allowed from collector to emitter if the transistor is operating with $I_C = 100$ mA?

EXAMPLE 4–6

The transistor in Figure 4–19 has the following maximum ratings: $P_{D(max)} = 800$ mW, $V_{CE(max)} = 15$ V, and $I_{C(max)} = 100$ mA. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?

▶ FIGURE 4–19



Solution First, find I_B so that you can determine I_C.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{22\text{ k}\Omega} = 195\ \mu\text{A}$$

$$I_C = \beta_{DC}I_B = (100)(195\ \mu\text{A}) = 19.5\text{ mA}$$

I_C is much less than $I_{C(max)}$ and ideally will not change with V_{CC}. It is determined only by I_B and β_{DC}.

The voltage drop across R_C is

$$V_{R_C} = I_CR_C = (19.5\text{ mA})(1.0\text{ k}\Omega) = 19.5\text{ V}$$

Now you can determine the value of V_{CC} when $V_{CE} = V_{CE(max)} = 15$ V.

$$V_{R_C} = V_{CC} - V_{CE}$$

So,

$$V_{CC(max)} = V_{CE(max)} + (V_{R_C} = 15\text{ V} + 19.5\text{ V} = \mathbf{34.5\ V}$$

V_{CC} can be increased to 34.5 V, under the existing conditions, before $V_{CE(max)}$ is exceeded. However, at this point it is not known whether or not $P_{D(max)}$ has been exceeded.

$$P_D = V_{CE(max)}I_C = (15\text{ V})(19.5\text{ mA}) = 293\text{ mW}$$

Since $P_{D(max)}$ is 800 mW, it is *not* exceeded when $V_{CC} = 34.5$ V. So, $V_{CE(max)} = 15$ V is the limiting rating in this case. If the base current is removed causing the transistor to turn off, $\boldsymbol{V_{CE(max)}}$ **will be exceeded first** because the entire supply voltage, V_{CC}, will be dropped across the transistor.

Related Problem The transistor in Figure 4–19 has the following maximum ratings: $P_{D(max)} = 500$ mW, $V_{CE(max)} = 25$ V, and $I_{C(max)} = 200$ mA. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?

Derating $P_{D(max)}$

$P_{D(max)}$ is usually specified at 25°C. For higher temperatures, $P_{D(max)}$ is less. Datasheets often give derating factors for determining $P_{D(max)}$ at any temperature above 25°C. For example, a derating factor of 2 mW/°C indicates that the maximum power dissipation is reduced 2 mW for each degree Celsius increase in temperature.

EXAMPLE 4–7

A certain transistor has a $P_{D(max)}$ of 1 W at 25°C. The derating factor is 5 mW/°C. What is the $P_{D(max)}$ at a temperature of 70°C?

Solution The change (reduction) in $P_{D(max)}$ is

$$\Delta P_{D(max)} = (5\text{ mW/°C})(70°\text{C} - 25°\text{C}) = (5\text{ mW/°C})(45°\text{C}) = 225\text{ mW}$$

Therefore, the $P_{D(max)}$ at 70°C is

$$1\text{ W} - 225\text{ mW} = \mathbf{775\text{ mW}}$$

Related Problem A transistor has a $P_{D(max)} = 5$ W at 25°C. The derating factor is 10 mW/°C. What is the $P_{D(max)}$ at 70°C?

BJT Datasheet

A partial datasheet for the 2N3904 *npn* transistor is shown in Figure 4–20. Notice that the maximum collector-emitter voltage (V_{CEO}) is 40 V. The CEO subscript indicates that the voltage is measured from collector (C) to emitter (E) with the base open (O). In the text, we use $V_{CE(max)}$ for this parameter. Also notice that the maximum collector current is 200 mA.

The β_{DC} (h_{FE}) is specified for several values of I_C. As you can see, h_{FE} varies with I_C as we previously discussed.

The collector-emitter saturation voltage, $V_{CE(sat)}$ is 0.2 V maximum for $I_{C(sat)} = 10$ mA and increases with the current.

EXAMPLE 4–8

A 2N3904 transistor is used in the circuit of Figure 4–19 (Example 4–6). Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first? Refer to the datasheet in Figure 4–20.

Solution From the datasheet,

$$P_{D(max)} = P_D = 625\text{ mW}$$
$$V_{CE(max)} = V_{CEO} = 40\text{ V}$$
$$I_{C(max)} = I_C = 200\text{ mA}$$

Assume $\beta_{DC} = 100$. This is a reasonably valid assumption based on the datasheet $h_{FE} = 100$ minimum for specified conditions (β_{DC} and h_{FE} are the same parameter). As you have learned, the β_{DC} has considerable variations for a given transistor, depending on circuit conditions. Under this assumption, $I_C = 19.5$ mA and $V_{R_C} = 19.5$ V from Example 4–6.

Since I_C is much less than $I_{C(max)}$ and, ideally, will not change with V_{CC}, the maximum value to which V_{CC} can be increased before $V_{CE(max)}$ is exceeded is

$$V_{CC(max)} = V_{CE(max)} + V_{R_C} = 40\text{ V} + 19.5\text{ V} = 59.5\text{ V}$$

However, at the maximum value of V_{CE}, the power dissipation is

$$P_D = V_{CE(max)}I_C = (40\text{ V})(19.5\text{ mA}) = 780\text{ mW}$$

Power dissipation exceeds the maximum of 625 mW specified on the datasheet.

Related Problem Use the datasheet in Figure 4–20 to find the maximum P_D at 50°C.

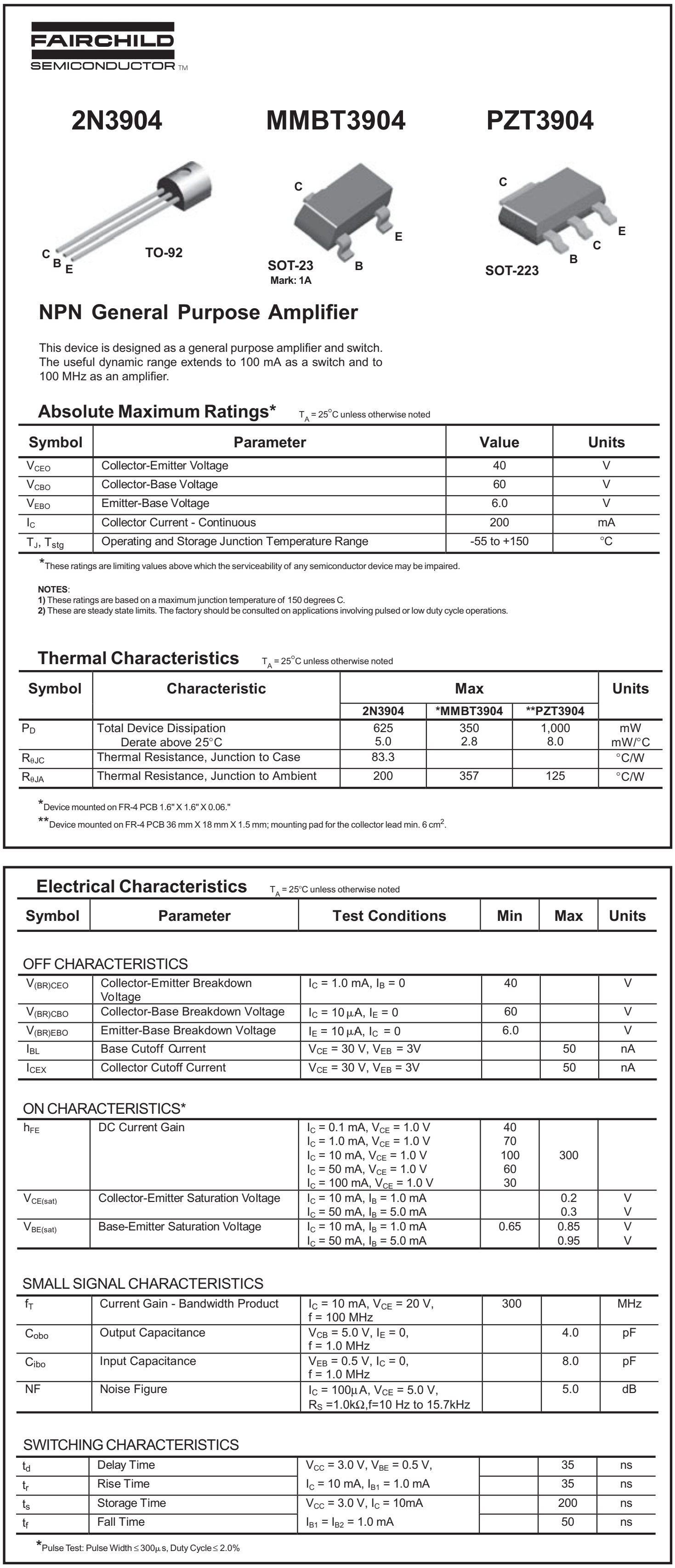


FIGURE 4–20

Partial datasheet. For a complete 2N3904 datasheet, go to *http://www.fairchildsemi.com/ds/2N%2F2N3904.pdf*. Copyright Fairchild Semiconductor Corporation. Used by permission.

FAIRCHILD
SEMICONDUCTOR TM

2N3904 **MMBT3904** **PZT3904**

C
B
E
TO-92
C
E
SOT-23
B
Mark: 1A
C
E
C
B
SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Absolute Maximum Ratings*

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3904	***MMBT3904**	****PZT3904**	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0$ mA, $I_B = 0$	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\ \mu A$, $I_C = 0$	6.0		V
I_{BL}	Base Cutoff Current	$V_{CE} = 30$ V, $V_{EB} = 3V$		50	nA
I_{CEX}	Collector Cutoff Current	$V_{CE} = 30$ V, $V_{EB} = 3V$		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	$I_C = 0.1$ mA, $V_{CE} = 1.0$ V	40		
		$I_C = 1.0$ mA, $V_{CE} = 1.0$ V	70		
		$I_C = 10$ mA, $V_{CE} = 1.0$ V	100	300	
		$I_C = 50$ mA, $V_{CE} = 1.0$ V	60		
		$I_C = 100$ mA, $V_{CE} = 1.0$ V	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1.0$ mA		0.2	V
		$I_C = 50$ mA, $I_B = 5.0$ mA		0.3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1.0$ mA	0.65	0.85	V
		$I_C = 50$ mA, $I_B = 5.0$ mA		0.95	V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	$I_C = 10$ mA, $V_{CE} = 20$ V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	$V_{CB} = 5.0$ V, $I_E = 0$, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	$V_{EB} = 0.5$ V, $I_C = 0$, f = 1.0 MHz		8.0	pF
NF	Noise Figure	$I_C = 100\ \mu A$, $V_{CE} = 5.0$ V, $R_S = 1.0 k\Omega$, f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	$V_{CC} = 3.0$ V, $V_{BE} = 0.5$ V,		35	ns
t_r	Rise Time	$I_C = 10$ mA, $I_{B1} = 1.0$ mA		35	ns
t_s	Storage Time	$V_{CC} = 3.0$ V, $I_C = 10$mA		200	ns
t_f	Fall Time	$I_{B1} = I_{B2} = 1.0$ mA		50	ns

*Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

SECTION 4–3 CHECKUP

1. Define β_{DC} and α_{DC}. What is h_{FE}?
2. If the dc current gain of a transistor is 100, determine β_{DC} and α_{DC}.
3. What two variables are plotted on a collector characteristic curve?
4. What bias conditions must exist for a transistor to operate as an amplifier?
5. Does β_{DC} increase or decrease with temperature?
6. For a given type of transistor, can β_{DC} be considered to be a constant?

4–4 THE BJT AS AN AMPLIFIER

Amplification is the process of linearly increasing the amplitude of an electrical signal and is one of the major properties of a transistor. As you learned, a BJT exhibits current gain (called β). When a BJT is biased in the active (or linear) region, as previously described, the BE junction has a low resistance due to forward bias and the BC junction has a high resistance due to reverse bias.

After completing this section, you should be able to

- ☐ **Discuss how a BJT is used as a voltage amplifier**
- ☐ List the dc and ac quantities in an amplifier
  - ◆ Describe how the dc and ac quantities are identified
- ☐ Describe voltage amplification
  - ◆ Draw the schematic for a basic BJT amplifier ◆ Define *current gain* and *voltage gain* ◆ Calculate voltage gain ◆ Calculate amplifier output voltage

DC and AC Quantities

Before discussing the concept of transistor amplification, the designations that we will use for the circuit quantities of current, voltage, and resistance must be explained because amplifier circuits have both dc and ac quantities.

In this text, italic capital letters are used for both dc and ac currents (I) and voltages (V). This rule applies to rms, average, peak, and peak-to-peak ac values. AC current and voltage values are always rms unless stated otherwise. Although some texts use lowercase i and v for ac current and voltage, we reserve the use of lowercase i and v only for instantaneous values. In this text, the distinction between a dc current or voltage and an ac current or voltage is in the subscript.

DC quantities always carry an uppercase roman (nonitalic) subscript. For example, I_B, I_C, and I_E are the dc transistor currents. V_{BE}, V_{CB}, and V_{CE} are the dc voltages from one transistor terminal to another. Single subscripted voltages such as V_B, V_C, and V_E are dc voltages from the transistor terminals to ground.

AC and all time-varying quantities always carry a lowercase italic subscript. For example, I_b, I_c, and I_e are the ac transistor currents. V_{be}, V_{cb}, and V_{ce} are the ac voltages from one transistor terminal to another. Single subscripted voltages such as V_b, V_c, and V_e are ac voltages from the transistor terminals to ground.

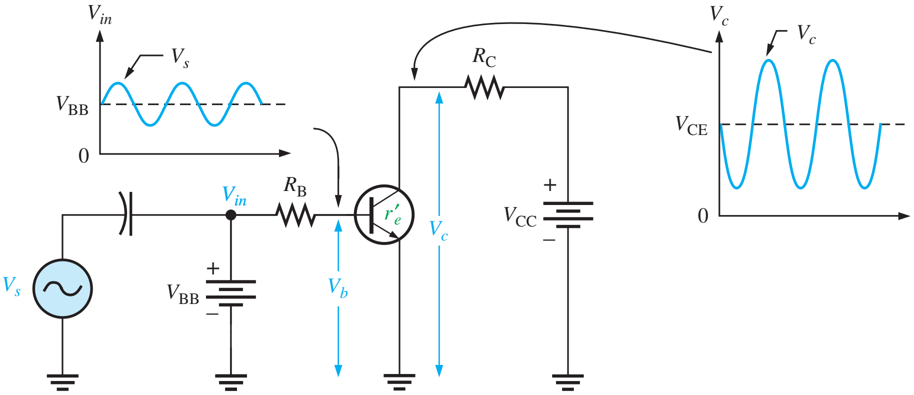
The rule is different for *internal* transistor resistances. As you will see later, transistors have internal ac resistances that are designated by lowercase r' with an appropriate subscript. For example, the internal ac emitter resistance is designated as r'_e.

Circuit resistances external to the transistor itself use the standard italic capital R with a subscript that identifies the resistance as dc or ac (when applicable), just as for current and voltage. For example R_E is an external dc emitter resistance and R_e is an external ac emitter resistance.

Voltage Amplification

As you have learned, a transistor amplifies current because the collector current is equal to the base current multiplied by the current gain, β. The base current in a transistor is very small compared to the collector and emitter currents. Because of this, the collector current is approximately equal to the emitter current.

With this in mind, let's look at the circuit in Figure 4–21. An ac voltage, V_s, is superimposed on the dc bias voltage V_{BB} by capacitive coupling as shown. The dc bias voltage V_{CC} is connected to the collector through the collector resistor, R_C.



◀ FIGURE 4–21

Basic transistor amplifier circuit with ac source voltage V_s and dc bias voltage V_{BB} superimposed.

The ac input voltage produces an ac base current, which results in a much larger ac collector current. The ac collector current produces an ac voltage across R_C, thus producing an amplified, but inverted, reproduction of the ac input voltage in the active region of operation, as illustrated in Figure 4–21.

The forward-biased base-emitter junction presents a very low resistance to the ac signal. This internal ac emitter resistance is designated r'_e in Figure 4–21 and appears in series with R_B. The ac base voltage is

$$V_b = I_e r'_e$$

The ac collector voltage, V_c, equals the ac voltage drop across R_C.

$$V_c = I_c R_C$$

Since $I_c \cong I_e$, the ac collector voltage is

$$V_c \cong I_e R_C$$

V_b can be considered the transistor ac input voltage where $V_b = V_s - I_b R_B$. V_c can be considered the transistor ac output voltage. Since *voltage gain* is defined as the ratio of the output voltage to the input voltage, the ratio of V_c to V_b is the ac voltage gain, A_v, of the transistor.

$$A_v = \frac{V_c}{V_b}$$

Substituting $I_e R_C$ for V_c and $I_e r'_e$ for V_b yields

$$A_v = \frac{V_c}{V_b} \cong \frac{I_e R_C}{I_e r'_e}$$

The I_e terms cancel; therefore,

$$\boldsymbol{A_v \cong \frac{R_C}{r'_e}}$$

Equation 4–7

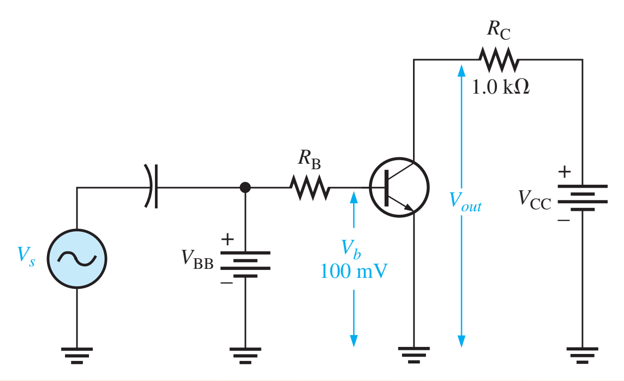
Equation 4–7 shows that the transistor in Figure 4–21 provides amplification in the form of voltage gain, which is dependent on the values of R_C and r'_e.

Since R_C is always considerably larger in value than r'_e, the output voltage for this configuration is greater than the input voltage. Various types of amplifiers are covered in detail in later chapters.

EXAMPLE 4–9

Determine the voltage gain and the ac output voltage in Figure 4–22 if $r'_e = 50\ \Omega$.

▶ FIGURE 4–22



Solution The voltage gain is

$$A_v \cong \frac{R_C}{r'_e} = \frac{1.0\ \text{k}\Omega}{50\ \Omega} = \mathbf{20}$$

Therefore, the ac output voltage is

$$V_{out} = A_v V_b = (20)(100\ \text{mV}) = \mathbf{2\ V\ rms}$$

Related Problem What value of R_C in Figure 4–22 will it take to have a voltage gain of 50?

SECTION 4–4 CHECKUP

1. What is amplification?
2. How is voltage gain defined?
3. Name two factors that determine the voltage gain of an amplifier.
4. What is the voltage gain of a transistor amplifier that has an output of 5 V rms and an input of 250 mV rms?
5. A transistor connected as in Figure 4–22 has an $r'_e = 20\ \Omega$. If R_C is 1200 Ω, what is the voltage gain?

4–5 THE BJT AS A SWITCH

In the previous section, you saw how a BJT can be used as a linear amplifier. The second major application area is switching applications. When used as an electronic switch, a BJT is normally operated alternately in cutoff and saturation. Many digital circuits use the BJT as a switch.

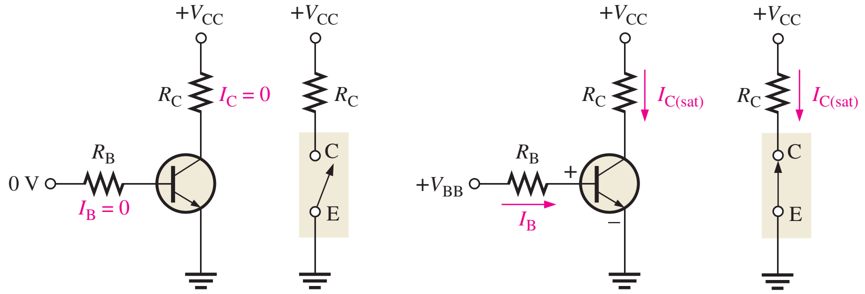
After completing this section, you should be able to

- **Discuss how a BJT is used as a switch**
- Describe BJT switching operation
- Explain the conditions in cutoff
  - Determine the cutoff voltage in terms of the dc supply voltage

- Explain the conditions in saturation
  - Calculate the collector current and the base current in saturation
- Describe a simple application

Switching Operation

Figure 4–23 illustrates the basic operation of a BJT as a switching device. In part (a), the transistor is in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an *open* between collector and emitter, as indicated by the switch equivalent. In part (b), the transistor is in the saturation region because the base-emitter junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector current to reach its saturation value. In this condition, there is, ideally, a *short* between collector and emitter, as indicated by the switch equivalent. Actually, a small voltage drop across the transister of up to a few tenths of a volt normally occurs, which is the saturation voltage, $V_{CE(sat)}$.



(a) Cutoff — open switch (b) Saturation — closed switch

FIGURE 4–23

Switching action of an ideal transistor.

Conditions in Cutoff As mentioned before, a transistor is in the cutoff region when the base-emitter junction is not forward-biased. Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC}.

$$V_{CE(cutoff)} = V_{CC}$$

Equation 4–8

Conditions in Saturation As you have learned, when the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

Equation 4–9

Since $V_{CE(sat)}$ is very small compared to V_{CC}, it can usually be neglected.

The minimum value of base current needed to produce saturation is

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

Equation 4–10

Normally, I_B should be significantly greater than $I_{B(min)}$ to ensure that the transistor is saturated.

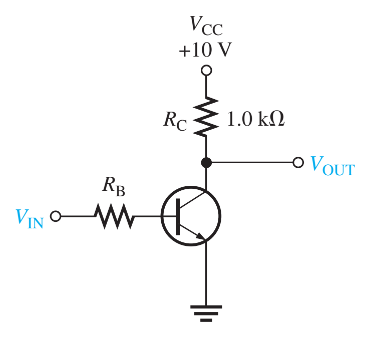
EXAMPLE 4–10

(a) For the transistor circuit in Figure 4–24, what is V_{CE} when $V_{IN} = 0$ V?

(b) What minimum value of I_B is required to saturate this transistor if β_{DC} is 200? Neglect $V_{CE(sat)}$.

(c) Calculate the maximum value of R_B when $V_{IN} = 5$ V.

▶ FIGURE 4–24



Solution **(a)** When $V_{IN} = 0$ V, the transistor is in cutoff (acts like an open switch) and

$$V_{CE} = V_{CC} = \mathbf{10\ V}$$

(b) Since $V_{CE(sat)}$ is neglected (assumed to be 0 V),

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10\text{ V}}{1.0\text{ k}\Omega} = 10\text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{10\text{ mA}}{200} = \mathbf{50\ \mu A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation. Any further increase in I_B will ensure the transistor remains in saturation but there cannot be any further increase in I_C.

(c) When the transistor is on, $V_{BE} \cong 0.7$ V. The voltage across R_B is

$$V_{R_B} = V_{IN} - V_{BE} \cong 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

Calculate the maximum value of R_B needed to allow a minimum I_B of 50 μA using Ohm's law as follows:

$$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}} = \frac{4.3\text{ V}}{50\ \mu\text{A}} = \mathbf{86\ k\Omega}$$

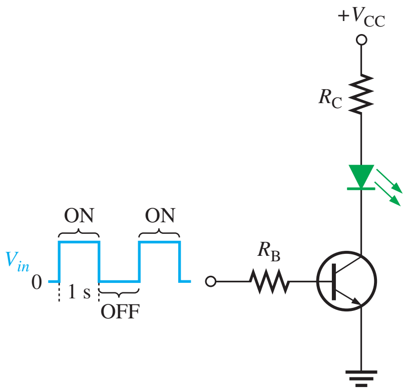
Related Problem Determine the minimum value of I_B required to saturate the transistor in Figure 4–24 if β_{DC} is 125 and $V_{CE(sat)}$ is 0.2 V.

A Simple Application of a Transistor Switch

The transistor in Figure 4–25 is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated. When

▶ FIGURE 4–25

A transistor used to switch an LED on and off.



the square wave is at 0 V, the transistor is in cutoff; and since there is no collector current, the LED does not emit light. When the square wave goes to its high level, the transistor saturates. This forward-biases the LED, and the resulting collector current through the LED causes it to emit light. Thus, the LED is on for 1 second and off for 1 second.

EXAMPLE 4–11

The LED in Figure 4–25 requires 30 mA to emit a sufficient level of light. Therefore, the collector current should be approximately 30 mA. For the following circuit values, determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of base current as a safety margin to ensure saturation. $V_{CC} = 9\text{ V}$, $V_{CE(sat)} = 0.3\text{ V}$, $R_C = 220\ \Omega$, $R_B = 3.3\text{ k}\Omega$, $\beta_{DC} = 50$, and $V_{LED} = 1.6\text{ V}$.

Solution

$$I_{C(sat)} = \frac{V_{CC} - V_{LED} - V_{CE(sat)}}{R_C} = \frac{9\text{ V} - 1.6\text{ V} - 0.3\text{ V}}{220\ \Omega} = 32.3\text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{32.3\text{ mA}}{50} = 646\ \mu\text{A}$$

To ensure saturation, use twice the value of $I_{B(min)}$, which is 1.29 mA. Use Ohm's law to solve for V_{in}.

$$I_B = \frac{V_{R_B}}{R_B} = \frac{V_{in} - V_{BE}}{R_B} = \frac{V_{in} - 0.7\text{ V}}{3.3\text{ k}\Omega}$$

$$V_{in} - 0.7\text{ V} = 2I_{B(min)}R_B = (1.29\text{ mA})(3.3\text{ k}\Omega)$$

$$V_{in} = (1.29\text{ mA})(3.3\text{ k}\Omega) + 0.7\text{ V} = \mathbf{4.96\text{ V}}$$

Related Problem

If you change the LED in Figure 4–25 to one that requires 50 mA for a specified light emission and you can't increase the input amplitude above 5 V or V_{CC} above 9 V, how would you modify the circuit? Specify the component(s) to be changed and the value(s).

Open the Multisim file E04-11 in the Examples folder on the companion website. Using a 0.5 Hz square wave input with the calculated amplitude, verify that the transistor is switching between cutoff and saturation and that the LED is alternately turning on and off.

SECTION 4–5 CHECKUP

1. When a transistor is used as a switch, in what two states is it operated?
2. When is the collector current maximum?
3. When is the collector current approximately zero?
4. Under what condition is $V_{CE} = V_{CC}$?
5. When is V_{CE} minimum?

4–6 THE PHOTOTRANSISTOR

A phototransistor is similar to a regular BJT except that the base current is produced and controlled by light instead of a voltage source. The phototransistor effectively converts light energy to an electrical signal.

After completing this section, you should be able to

- **Discuss the phototransistor and its operation**
  - Identify the schematic symbol
  - Calculate the collector current
  - Interpret a set of collector characteristic curves
- Describe a simple application
- Discuss optocouplers
  - Define *current transfer ratio*
  - Give examples of how optocouplers are used

In a **phototransistor** the base current is produced when light strikes the photosensitive semiconductor base region. The collector-base *pn* junction is exposed to incident light through a lens opening in the transistor package. When there is no incident light, there is only a small thermally generated collector-to-emitter leakage current, I_{CEO}; this dark current is typically in the nA range. When light strikes the collector-base *pn* junction, a base current, I_λ, is produced that is directly proportional to the light intensity. This action produces a collector current that increases with I_λ. Except for the way base current is generated, the phototransistor behaves as a conventional BJT. In many cases, there is no electrical connection to the base.

The relationship between the collector current and the light-generated base current in a phototransistor is

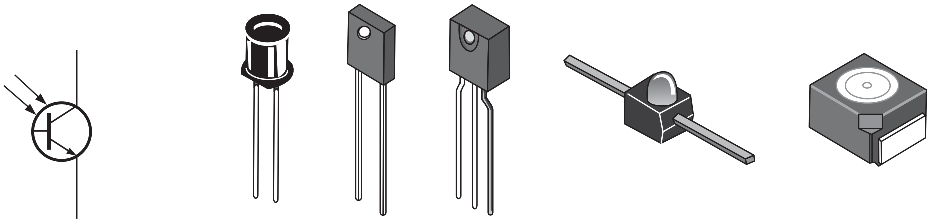
Equation 4–11

$$I_C = \beta_{DC} I_\lambda$$

The schematic symbol and some typical phototransistors are shown in Figure 4–26. Since the actual photogeneration of base current occurs in the collector-base region, the larger the physical area of this region, the more base current is generated. Thus, a typical phototransistor is designed to offer a large area to the incident light, as the simplified structure diagram in Figure 4–27 illustrates.

▶ FIGURE 4–26

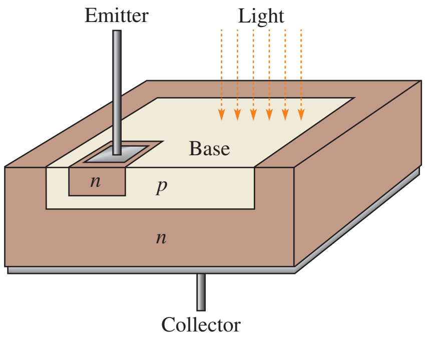
Phototransistor.



(a) Schematic symbol (b) Typical packages

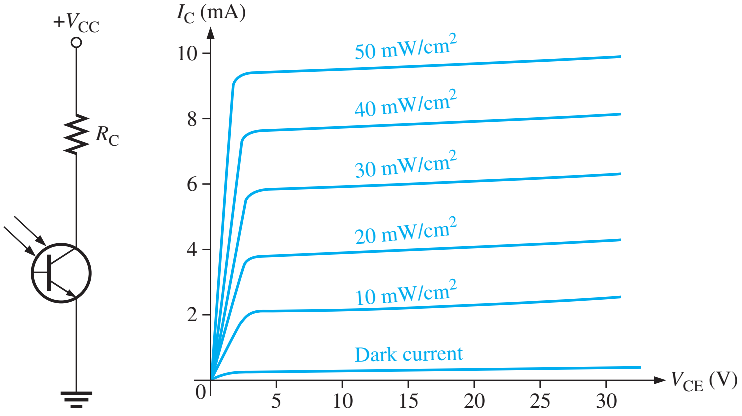
▶ FIGURE 4–27

Typical phototransistor structure.



A phototransistor can be either a two-lead or a three-lead device. In the three-lead configuration, the base lead is brought out so that the device can be used as a conventional BJT with or without the additional light-sensitivity feature. In the two-lead configuration, the base is not electrically available, and the device can be used only with light as the input. In many applications, the phototransistor is used in the two-lead version.

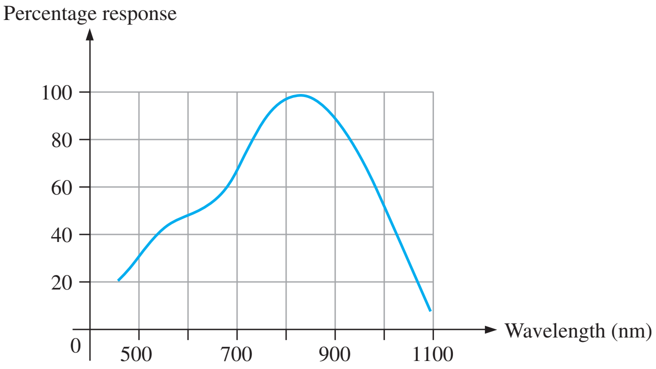
Figure 4–28 shows a phototransistor with a biasing circuit and typical collector characteristic curves. Notice that each individual curve on the graph corresponds to a certain value of light intensity (in this case, the units are mW/cm^2) and that the collector current in creases with light intensity.



◀ **FIGURE 4–28**

Phototransistor circuit and typical collector characteristic curves.

Phototransistors are not sensitive to all light but only to light within a certain range of wavelengths. They are most sensitive to particular wavelengths in the red and infrared part of the spectrum, as shown by the peak of the infrared spectral response curve in Figure 4–29.



◀ **FIGURE 4–29**

Typical phototransistor spectral response.

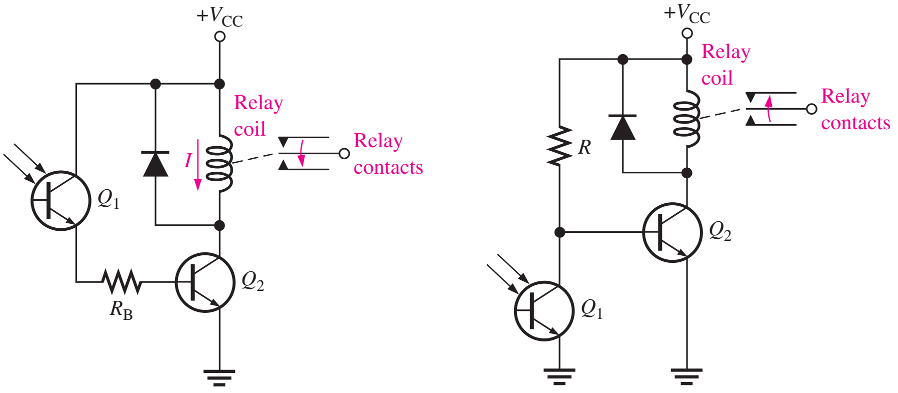
Applications

Phototransistors are used in a variety of applications. A light-operated relay circuit is shown in Figure 4–30(a). The phototransistor Q_1 drives the BJT Q_2. When there is sufficient incident light on Q_1, transistor Q_2 is driven into saturation, and collector current through the relay coil energizes the relay. The diode across the relay coil prevents, by its limiting action, a large voltage transient from occurring at the collector of Q_2 when the transistor turns off.

Figure 4–30(b) shows a circuit in which a relay is deactivated by incident light on the phototransistor. When there is insufficient light, transistor Q_2 is biased on, keeping the relay energized. When there is sufficient light, phototransistor Q_1 turns on; this pulls the base of Q_2 low, thus turning Q_2 off and de-energizing the relay.

FIGURE 4–30

Relay circuits driven by a phototransistor.



(a) Light activated

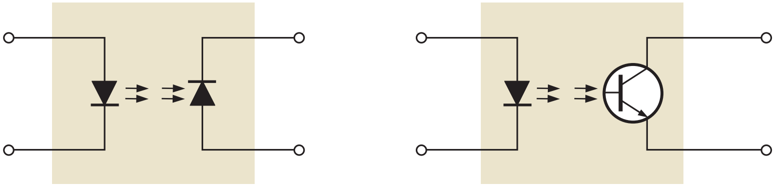
(b) Light deactivated

Optocouplers

An **optocoupler** uses an LED optically coupled to a photodiode or a phototransistor in a single package. Two basic types are LED-to-photodiode and LED-to-phototransistor, as shown in Figure 4–31. Examples of typical packages are shown in Figure 4–32.

FIGURE 4–31

Basic optocouplers.

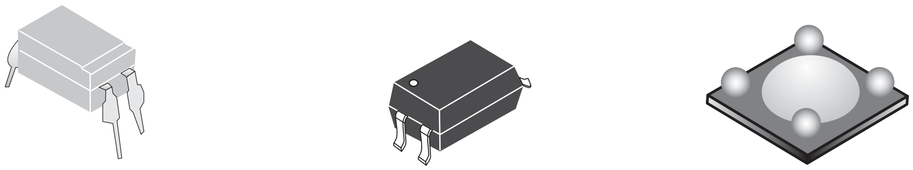


(a) LED-to-photodiode

(b) LED-to-phototransistor

FIGURE 4–32

Examples of optocoupler packages.



(a) Dual-in-line

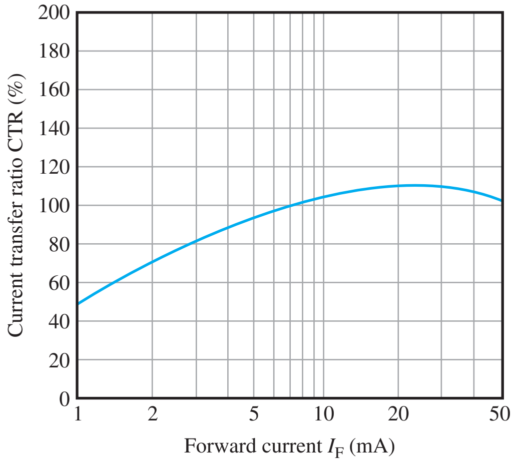
(b) Surface-mount

(c) Ball-grid

A key parameter in optocouplers is the **CTR** (current transfer ratio). The CTR is an indication of how efficiently a signal is coupled from input to output and is expressed as the ratio of a change in the LED current to the corresponding change in the photodiode or phototransistor current. It is usually expressed as a percentage. Figure 4–33 shows a

FIGURE 4–33

CTR versus I_F for a typical optocoupler.



typical graph of CTR versus forward LED current. For this case, it varies from about 50% to about 110%.

Optocouplers are used to isolate sections of a circuit that are incompatible in terms of the voltage levels or currents required. For example, they are used to protect hospital patients from shock when they are connected to monitoring instruments or other devices. They are also used to isolate low-current control or signal circuits from noisy power supply circuits or higher-current motor and machine circuits.

SECTION 4–6 CHECKUP

1. How does a phototransistor differ from a conventional BJT?
2. A three-lead phototransistor has an external (emitter, base, collector) lead.
3. The collector current in a phototransistor circuit depends on what two factors?
4. What is the optocoupler parameter, OTR?

4–7 TRANSISTOR CATEGORIES AND PACKAGING

BJTs are available in a wide range of package types for various applications. Those with mounting studs or heat sinks are usually power transistors. Low-power and medium-power transistors are usually found in smaller metal or plastic cases. Still another package classification is for high-frequency devices. You should be familiar with common transistor packages and be able to identify the emitter, base, and collector terminals.

After completing this section, you should be able to

- ❑ **Identify various types of transistor packages**
- ❑ List three broad transistor categories
  - ◆ Identify package pin configurations

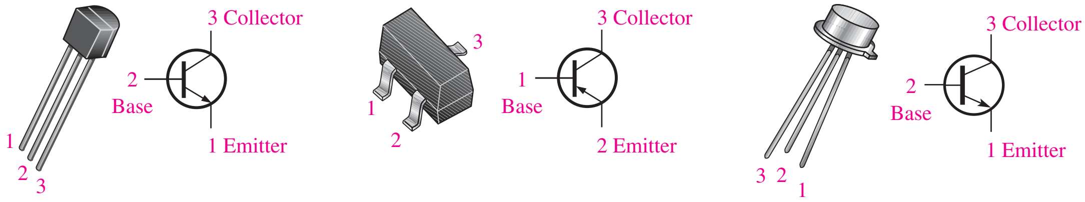
Transistor Categories

Manufacturers generally classify bipolar junction transistors into three broad categories: general-purpose/small-signal devices, power devices, and RF (radio frequency/microwave) devices. Although each of these categories, to a large degree, has its own unique package types, you will find certain types of packages used in more than one device category. Let's look at transistor packages for each of the three categories so that you will be able to recognize a transistor when you see one on a circuit board and have a good idea of what general category it is in.

General-Purpose/Small-Signal Transistors General-purpose/small-signal transistors are generally used for low- or medium-power amplifiers or switching circuits. The packages are either plastic or metal cases. Certain types of packages contain multiple transistors. Figure 4–34 illustrates two common plastic cases and a metal can package.

Figure 4–35 shows multiple-transistor packages. Some of the multiple-transistor packages such as the dual in-line (DIP) and the small-outline (SO) are the same as those used for many integrated circuits. Typical pin connections are shown so you can identify the emitter, base, and collector.

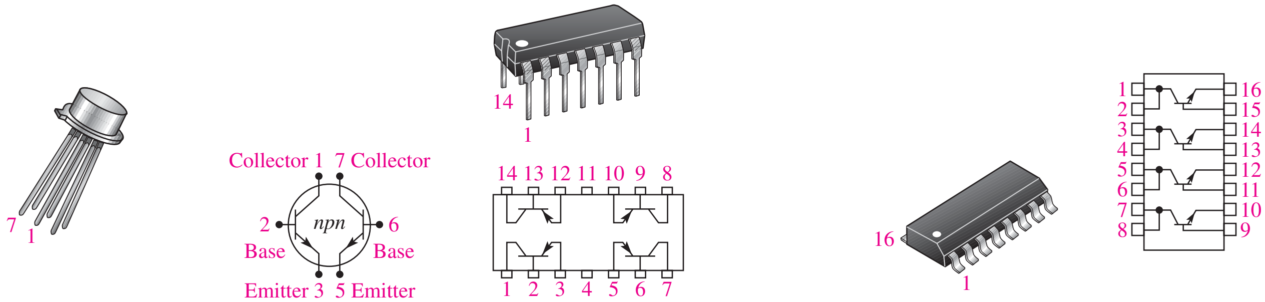
Power Transistors Power transistors are used to handle large currents (typically more than 1 A) and/or large voltages. For example, the final audio stage in a stereo system uses a power transistor amplifier to drive the speakers. Figure 4–36 shows some common package


3 Collector
2
Base
1 Emitter
1
2
3
3
1
2
3 Collector
1
Base
2 Emitter
3 Collector
2
Base
1 Emitter
3
2
1

(a) TO-92 (b) SOT-23 (c) TO-18. Emitter is closest to tab.

▲ **FIGURE 4–34**

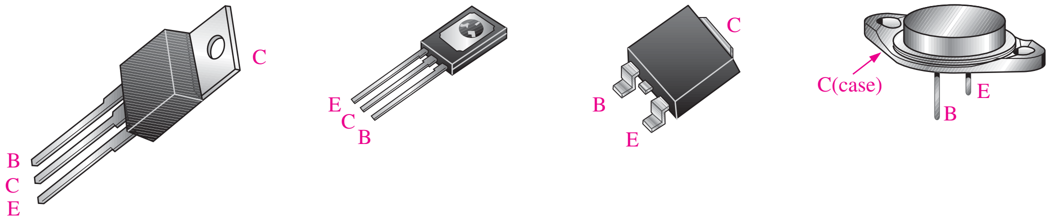
Plastic and metal cases for general-purpose/small-signal transistors. Pin configurations may vary. Always check the datasheet (*http://fairchildsemiconductor.com/*).


7
1
Collector 1
7 Collector
2
Base
npn
6
Base
Emitter 3
5 Emitter
14
1
14 13 12 11 10 9 8
1 2 3 4 5 6 7
16
1
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9

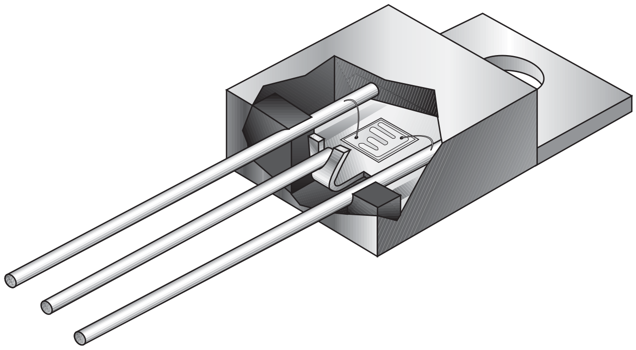
(a) Dual metal can. Emitters are closest to tab. (b) Quad dual in-line (DIP) and quad flat-pack. Dot indicates pin 1. (c) Quad small outline (SO) package for surface-mount technology

▲ **FIGURE 4–35**

Examples of multiple-transistor packages.


C
B
C
E
E
C
B
C
B
E
C(case)
E
B

(a) TO-220 (b) TO-225 (c) D-Pack (d) TO-3



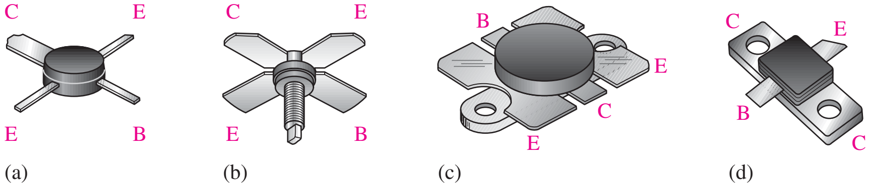
(e) Greatly enlarged cutaway view of tiny transistor chip mounted in the encapsulated package

▲ **FIGURE 4–36**

Examples of power transistors and packages.

configurations. The metal tab or the metal case is common to the collector and is thermally connected to a heat sink for heat dissipation. Notice in part (e) how the small transistor chip is mounted inside the much larger package.

RF Transistors RF transistors are designed to operate at extremely high frequencies and are commonly used for various purposes in communications systems and other high-frequency applications. Their unusual shapes and lead configurations are designed to optimize certain high-frequency parameters. Figure 4–37 shows some examples.



▲ **FIGURE 4–37**

Examples of RF transistor packages.

SECTION 4–7 CHECKUP

1. List the three broad categories of bipolar junction transistors.
2. In a metal can package of a general-purpose BJT, how is the emitter identified?
3. In power transistors, the metal mounting tab or case is connected to which transistor region?

4–8 TROUBLESHOOTING

As you already know, a critical skill in electronics work is the ability to identify a circuit malfunction and to isolate the failure to a single component if necessary. In this section, the basics of troubleshooting transistor bias circuits and testing individual transistors are covered.

After completing this section, you should be able to

- ❑ **Troubleshoot faults in transistor circuits**
- ❑ Troubleshoot a biased transistor
  - ◆ Calculate what the readings should be ◆ Define *floating point*
- ❑ Test a transistor using a DMM
  - ◆ Discuss the DMM diode test position ◆ Describe testing using the OHMs function
- ❑ Describe the transistor tester
- ❑ Discuss in-circuit and out-of-circuit testing
  - ◆ Explain point-of-measurement troubleshooting ◆ Describe leakage measurement and gain measurement
- ❑ Explain what a curve tracer is

Chapter 18 Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

Troubleshooting a Biased Transistor

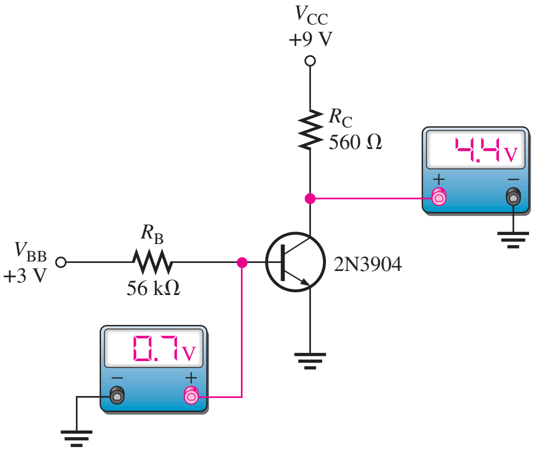
Several faults can occur in a simple transistor bias circuit. Possible faults are open bias resistors, open or resistive connections, shorted connections, and opens or shorts internal to the transistor itself. Figure 4–38 is a basic transistor bias circuit with all voltages referenced to ground. The two bias voltages are $V_{BB} = 3\text{ V}$ and $V_{CC} = 9\text{ V}$. The correct voltage measurements at the base and collector are shown. Analytically, these voltages are verified as follows. A $\beta_{DC} = 200$ is taken as midway between the minimum and maximum values of h_{FE} given on the datasheet for the 2N3904 in Figure 4–20. A different h_{FE} (β_{DC}), of course, will produce different results for the given circuit.

$$V_B = V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{56\text{ k}\Omega} = \frac{2.3\text{ V}}{56\text{ k}\Omega} = 41.1\ \mu\text{A}$$

$$I_C = \beta_{DC}I_B = 200(41.1\ \mu\text{A}) = 8.2\text{ mA}$$

$$V_C = 9\text{ V} - I_CR_C = 9\text{ V} - (8.2\text{ mA})(560\ \Omega) = 4.4\text{ V}$$



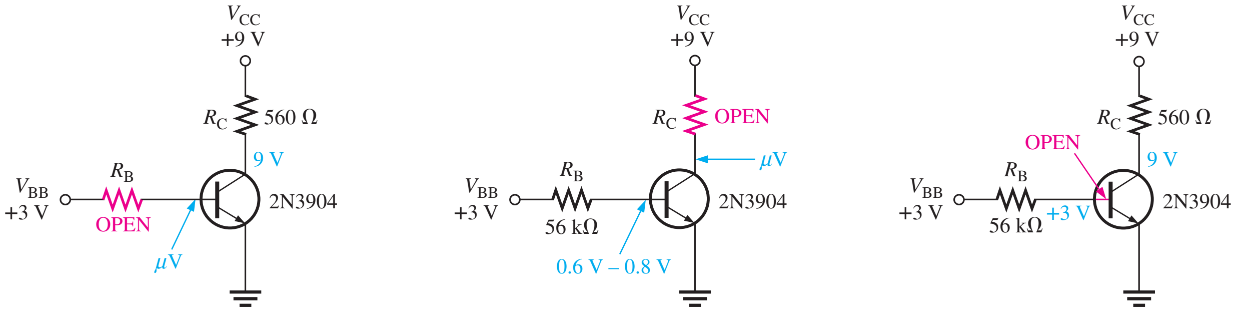
▲ **FIGURE 4–38**

A basic transistor bias circuit.

Several faults that can occur in the circuit and the accompanying symptoms are illustrated in Figure 4–39. Symptoms are shown in terms of measured voltages that are incorrect. If a transistor circuit is not operating correctly, it is a good idea to verify that V_{CC} and ground are connected and operating. A simple check at the top of the collector resistor and at the collector itself will quickly ascertain if V_{CC} is present and if the transistor is conducting normally or is in cutoff or saturation. If it is in cutoff, the collector voltage will equal V_{CC}; if it is in saturation, the collector voltage will be near zero. Another faulty measurement can be seen if there is an open in the collector path. The term **floating point** refers to a point in the circuit that is not electrically connected to ground or a "solid" voltage. Normally, very small and sometimes fluctuating voltages in the μV to low mV range are generally measured at floating points. The faults in Figure 4–39 are typical but do not represent all possible faults that may occur.

Testing a Transistor with a DMM

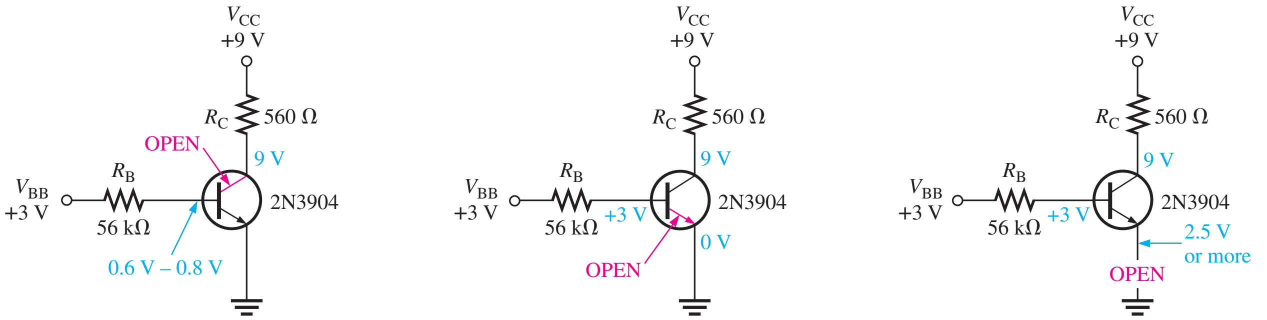
A digital multimeter can be used as a fast and simple way to check a transistor for open or shorted junctions. For this test, you can view the transistor as two diodes connected as shown in Figure 4–40 for both *npn* and *pnp* transistors. The base-collector junction is one diode and the base-emitter junction is the other.



(a) ***Fault:*** Open base resistor.
Symptoms: Readings from μV to a few mV at base due to floating point. 9 V at collector because transistor is in cutoff.

(b) ***Fault:*** Open collector resistor.
Symptoms: A very small voltage may be observed at the collector when a meter is connected due to the current path through the BC junction and the meter resistance.

(c) ***Fault:*** Base internally open.
Symptoms: 3 V at base lead. 9 V at collector because transistor is in cutoff.



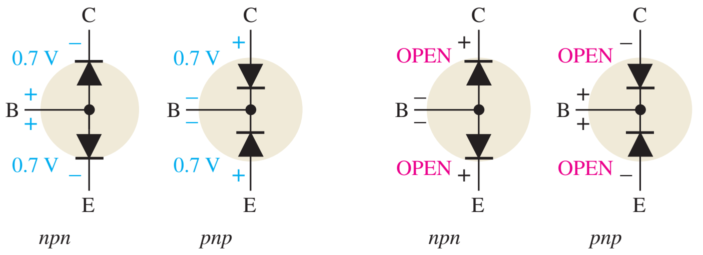
(d) ***Fault:*** Collector internally open.
Symptoms: 0.6 V – 0.8 V at base lead due to forward voltage drop across base-emitter junction. 9 V at collector because the open prevents collector current.

(e) ***Fault:*** Emitter internally open.
Symptoms: 3 V at base lead. 9 V at collector because there is no collector current. 0 V at the emitter as normal.

(f) ***Fault:*** Open ground connection.
Symptoms: 3 V at base lead. 9 V at collector because there is no collector current. 2.5 V or more at the emitter due to the forward voltage drop across the base-emitter junction. The measuring voltmeter provides a forward current path through its internal resistance.

▲ **FIGURE 4–39**

Examples of faults and symptoms in the basic transistor bias circuit.



(a) Both junctions should typically read 0.7 V when forward-biased.

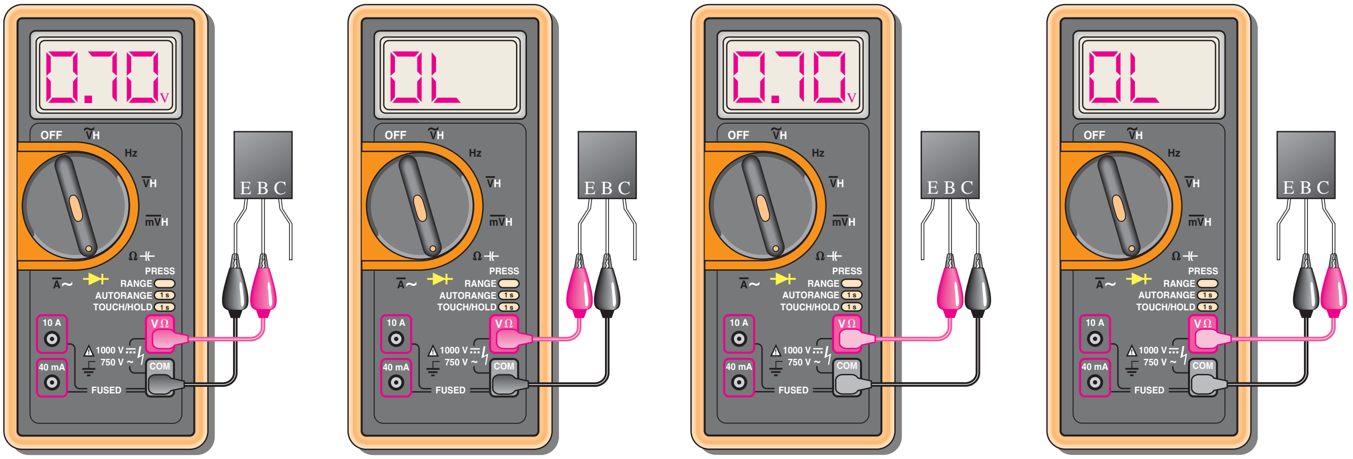
(b) Both junctions should ideally read OPEN when reverse-biased.

◀ **FIGURE 4–40**

A transistor viewed as two diodes.

Recall that a good diode will show an extremely high resistance (or open) with reverse bias and a very low resistance with forward bias. A defective open diode will show an extremely high resistance (or open) for both forward and reverse bias. A defective shorted or resistive diode will show zero or a very low resistance for both forward and reverse bias. An open diode is the most common type of failure. Since the transistor *pn* junctions are, in effect diodes, the same basic characteristics apply.

The DMM Diode Test Position Many digital multimeters (DMMs) have a *diode test* position that provides a convenient way to test a transistor. A typical DMM, as shown in Figure 4–41, has a small diode symbol to mark the position of the function switch. When set to diode test, the meter provides an internal voltage sufficient to forward-bias and reverse-bias a transistor junction.



(a) Forward-bias test of the BE junction

(b) Reverse-bias test of the BE junction

(c) Forward-bias test of the BC junction

(d) Reverse-bias test of the BC junction

▲ FIGURE 4–41

Typical DMM test of a properly functioning *npn* transistor. Leads are reversed for a *pnp* transistor.

When the Transistor Is Not Defective In Figure 4–41(a), the red (positive) lead of the meter is connected to the base of an *npn* transistor and the black (negative) lead is connected to the emitter to forward-bias the base-emitter junction. If the junction is good, you will get a reading of between approximately 0.6 V and 0.8 V, with 0.7 V being typical for forward bias.

In Figure 4–41(b), the leads are switched to reverse-bias the base-emitter junction, as shown. If the transistor is working properly, you will typically get an OL indication.

The process just described is repeated for the base-collector junction as shown in Figure 4–41(c) and (d). For a *pnp* transistor, the polarity of the meter leads are reversed for each test.

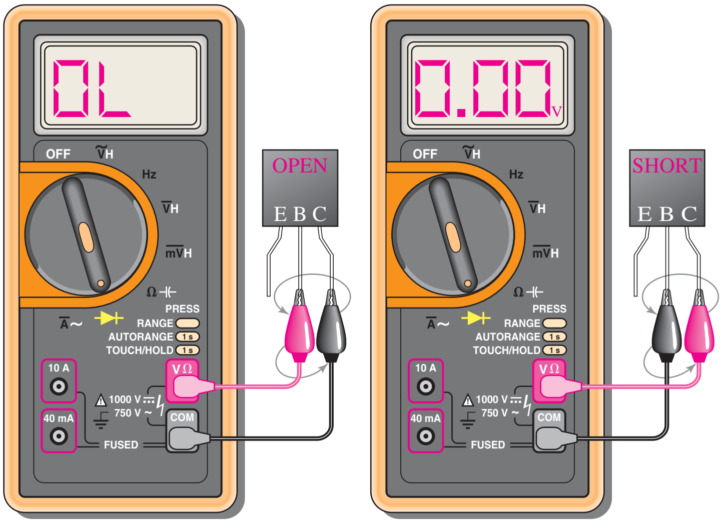
When the Transistor Is Defective When a transistor has failed with an open junction or internal connection, you get an open circuit voltage reading (OL) for both the forward-bias and the reverse-bias conditions for that junction, as illustrated in Figure 4–42(a). If a junction is shorted, the meter reads 0 V in both forward- and reverse-bias tests, as indicated in part (b).

Some DMMs provide a test socket on their front panel for testing a transistor for the h_{FE} (β_{DC}) value. If the transistor is inserted improperly in the socket or if it is not functioning properly due to a faulty junction or internal connection, a typical meter will flash a 1 or display a 0. If a value of β_{DC} within the normal range for the specific transistor is displayed, the device is functioning properly. The normal range of β_{DC} can be determined from the datasheet.

Checking a Transistor with the OHMs Function DMMs that do not have a diode test position or an h_{FE} socket can be used to test a transistor for open or shorted junctions by setting the function switch to an OHMs range. For the forward-bias check of a good transistor *pn* junction, you will get a resistance reading that can vary depending on the meter's internal battery. Many DMMs do not have sufficient voltage on the OHMs range to fully forward-bias a junction, and you may get a reading of from several hundred to several thousand ohms.

For the reverse-bias check of a good transistor, you will get an out-of-range indication on most DMMs because the reverse resistance is too high to measure. An out-of-range indication may be a flashing 1 or a display of dashes, depending on the particular DMM.

Even though you may not get accurate forward and reverse resistance readings on a DMM, the relative readings are sufficient to indicate a properly functioning transistor *pn* junction. The out-of-range indication shows that the reverse resistance is very high, as you


OL
OPEN
E B C
0.00 V
SHORT
E B C
OFF
Hz
mV
PRESS
RANGE
AUTORANGE
TOUCH/HOLD
10 A
40 mA
VΩ
COM
1000 V
750 V ~
FUSED

(a) Forward-bias test and reverse-bias test give the same reading (OL is typical) for an open BC junction.

(b) Forward- and reverse-bias tests for a shorted junction give the same 0 V reading.

FIGURE 4–42

Testing a defective *npn* transistor. Leads are reversed for a *pnp* transistor.

expect. The reading of a few hundred to a few thousand ohms for forward bias indicates that the forward resistance is small compared to the reverse resistance, as you expect.

Transistor Testers

An individual transistor can be tested either in-circuit or out-of-circuit with a transistor tester. For example, let's say that an amplifier on a particular printed circuit (PC) board has malfunctioned. Good troubleshooting practice dictates that you do not unsolder a component from a circuit board unless you are reasonably sure that it is bad or you simply cannot isolate the problem down to a single component. When components are removed, there is a risk of damage to the PC board contacts and traces.

You can perform an in-circuit check of the transistor using a transistor tester similar to the one shown in Figure 4–43. The three clip-leads are connected to the transistor terminals and the tester gives a positive indication if the transistor is good.

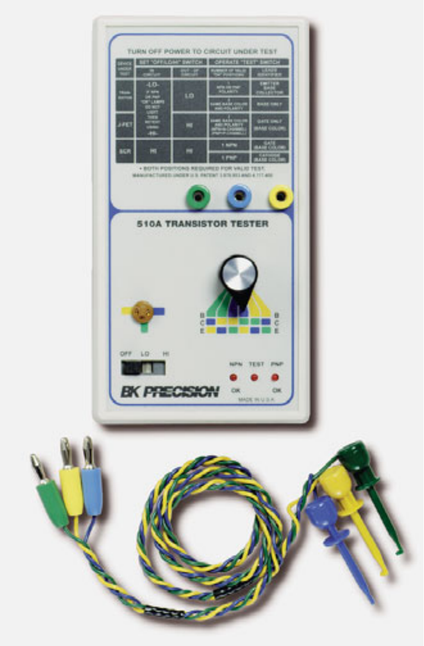

TURN OFF POWER TO CIRCUIT UNDER TEST
510A TRANSISTOR TESTER
OFF LO HI
NPN TEST PNP
OK OK
BK PRECISION
MADE IN U.S.A.

FIGURE 4–43

Transistor tester (courtesy of B + K Precision).

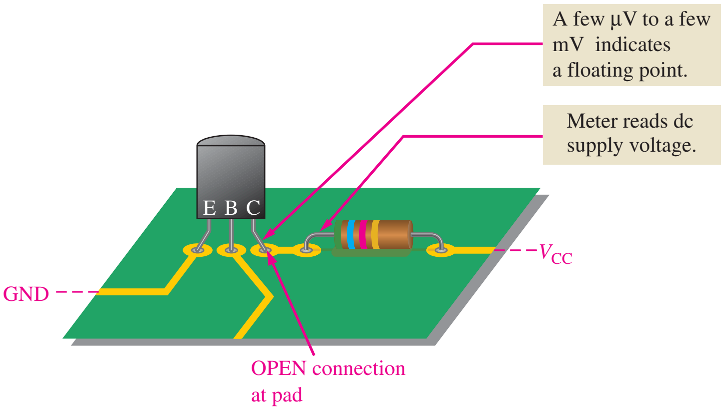
In-Circuit and Out-of-Circuit Tests

Case 1 If the transistor tests defective, it should be carefully removed and replaced with a known good one. An out-of-circuit check of the replacement device is usually a good idea, just to make sure it is OK. The transistor is plugged into the socket on the transistor tester for out-of-circuit tests.

Case 2 If the transistor tests good in-circuit but the circuit is not working properly, examine the circuit board for a poor connection at the collector pad or for a break in the connecting trace. A poor solder joint often results in an open or a highly resistive contact. The physical point at which you actually measure the voltage is very important in this case. For example, if you measure on the collector lead when there is an external open at the collector pad, you will measure a floating point. If you measure on the connecting trace or on the R_C lead, you will read V_{CC}. This situation is illustrated in Figure 4–44.

▶ **FIGURE 4–44**

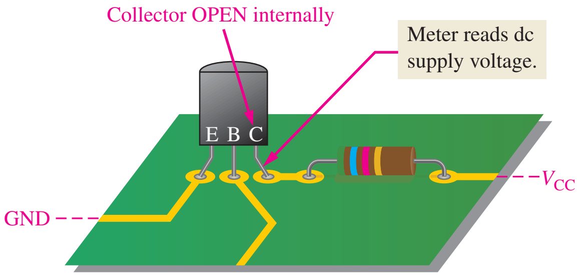
The indication of an open, when it is in the circuit external to the transistor, depends on where you measure.


A few µV to a few mV indicates a floating point.
Meter reads dc supply voltage.
E B C
V_{CC}
GND
OPEN connection at pad

Importance of Point-of-Measurement in Troubleshooting In case 2, if you had taken the initial measurement on the transistor lead itself and the open were *internal* to the transistor as shown in Figure 4–45, you would have measured V_{CC}. This indicates a defective transistor even before the tester was used, assuming the base-to-emitter voltage is normal. This simple concept emphasizes the importance of point-of-measurement in certain troubleshooting situations.

▶ **FIGURE 4–45**

Illustration of an internal open. Compare with Figure 4–44.



EXAMPLE 4–12 What fault do the measurements in Figure 4–46 indicate?

Solution The transistor is in cutoff, as indicated by the 10 V measurement on the collector lead. The base bias voltage of 3 V appears on the PC board contact but not on the transistor lead, as indicated by the floating point measurement. This shows that there is an open external to the transistor between the two measured base points. Check the solder joint at the base contact on the PC board. If the open were internal, there would be 3 V on the base lead.

Related Problem If the meter in Figure 4–46 that now reads 3 V indicates a floating point when touching the circuit board pad, what is the most likely fault?

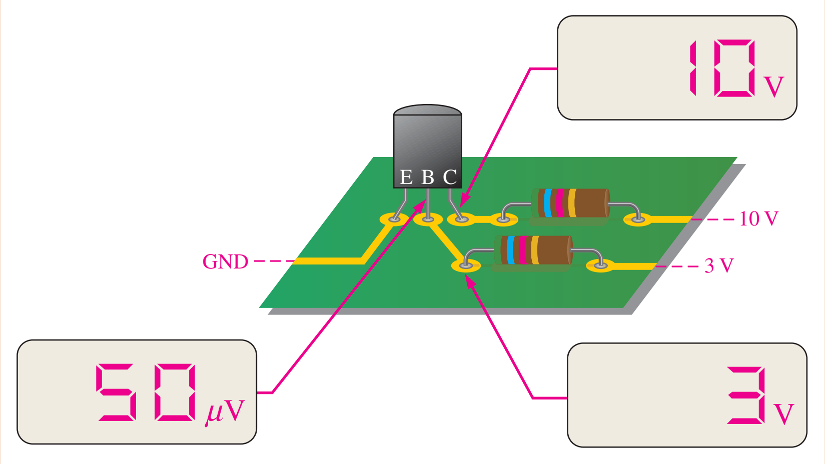


FIGURE 4–46

Leakage Measurement Very small leakage currents exist in all transistors and in most cases are small enough to neglect (usually nA). When a transistor is connected with the base open ($I_B = 0$), it is in cutoff. Ideally $I_C = 0$; but actually there is a small current from collector to emitter, as mentioned earlier, called I_{CEO} (collector-to-emitter current with base open). This leakage current is usually in the nA range. A faulty transistor will often have excessive leakage current and can be checked in a transistor tester. Another leakage current in transistors is the reverse collector-to-base current, I_{CBO}. This is measured with the emitter open. If it is excessive, a shorted collector-base junction is likely.

Gain Measurement In addition to leakage tests, the typical transistor tester also checks the β_{DC}. A known value of I_B is applied, and the resulting I_C is measured. The reading will indicate the value of the I_C/I_B ratio, although in some units only a relative indication is given. Most testers provide for an in-circuit β_{DC} check, so that a suspected device does not have to be removed from the circuit for testing.

Curve Tracers A *curve tracer* is an oscilloscope type of instrument that can display transistor characteristics such as a family of collector curves. In addition to the measurement and display of various transistor characteristics, diode curves can also be displayed.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE04-01
2. Multisim file TSE04-02
3. Multisim file TSE04-03
4. Multisim file TSE04-04

SECTION 4–8 CHECKUP

1. If a transistor on a circuit board is suspected of being faulty, what should you do?
2. In a transistor bias circuit, such as the one in Figure 4–38; what happens if R_B opens?
3. In a circuit such as the one in Figure 4–38, what are the base and collector voltages if there is an external open between the emitter and ground?

Application Activity: *Security Alarm System*

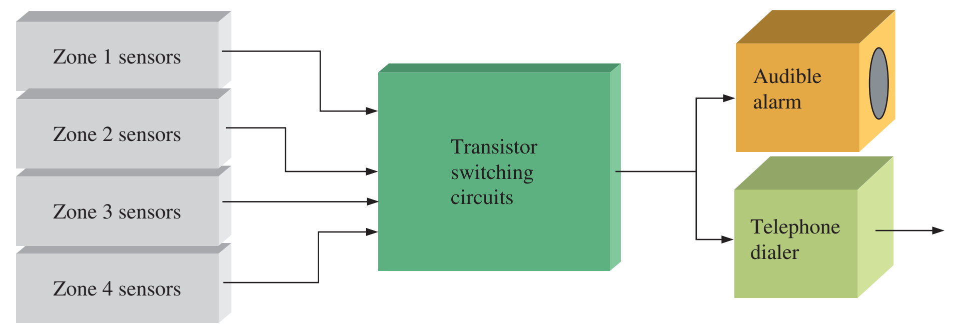
A circuit using transistor switches will be developed for use in an alarm system for detecting forced entry into a building. In its simplest form, the alarm system will accommodate four zones with any number of openings. It can be expanded to cover additional zones. For the purposes of this application, a zone is one room in a house or other building. The sensor used for each opening can be either a mechanical switch, a magnetically operated switch, or an optical sensor. Detection of an intrusion can be used to initiate an audible alarm signal and/or to initiate transmission of a signal over the phone line to a monitoring service.

Designing the Circuit

A basic block diagram of the system is shown in Figure 4–47. The sensors for each zone are connected to the switching circuits, and the output of the switching circuit goes to an audible alarm circuit and/or to a telephone dialing circuit. The focus of this application is the transistor switching circuits.

FIGURE 4–47

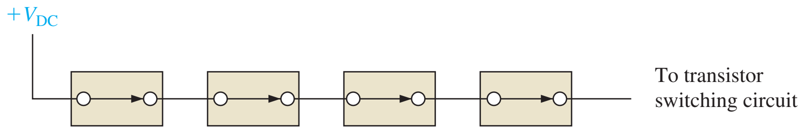
Block diagram of security alarm system.



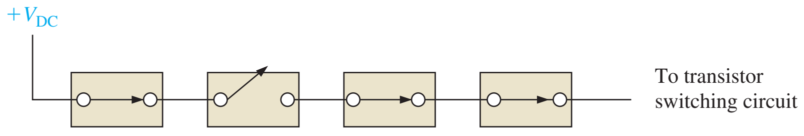
A zone sensor detects when a window or door is opened. They are normally in a closed position and are connected in series to a dc voltage source, as shown in Figure 4–48(a). When a window or door is opened, the corresponding sensor creates an open circuit, as shown in part (b). The sensors are represented by switch symbols.

FIGURE 4–48

Zone sensor configuration.



(a) Series zone sensors are normally closed.

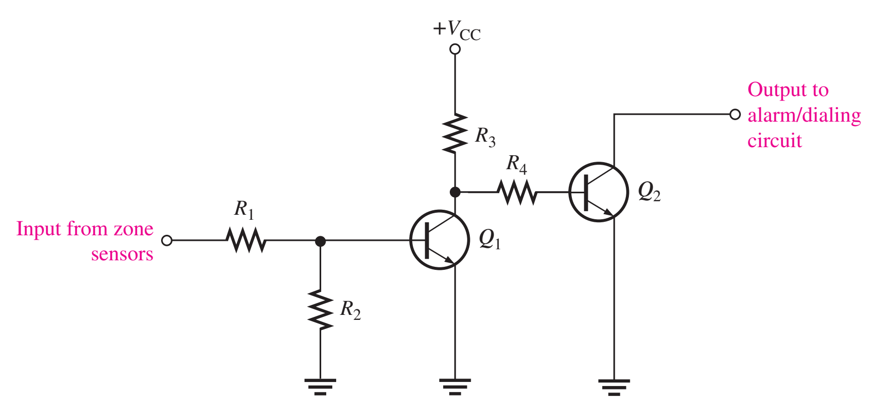


(b) Intrusion into the zone causes a sensor to open.

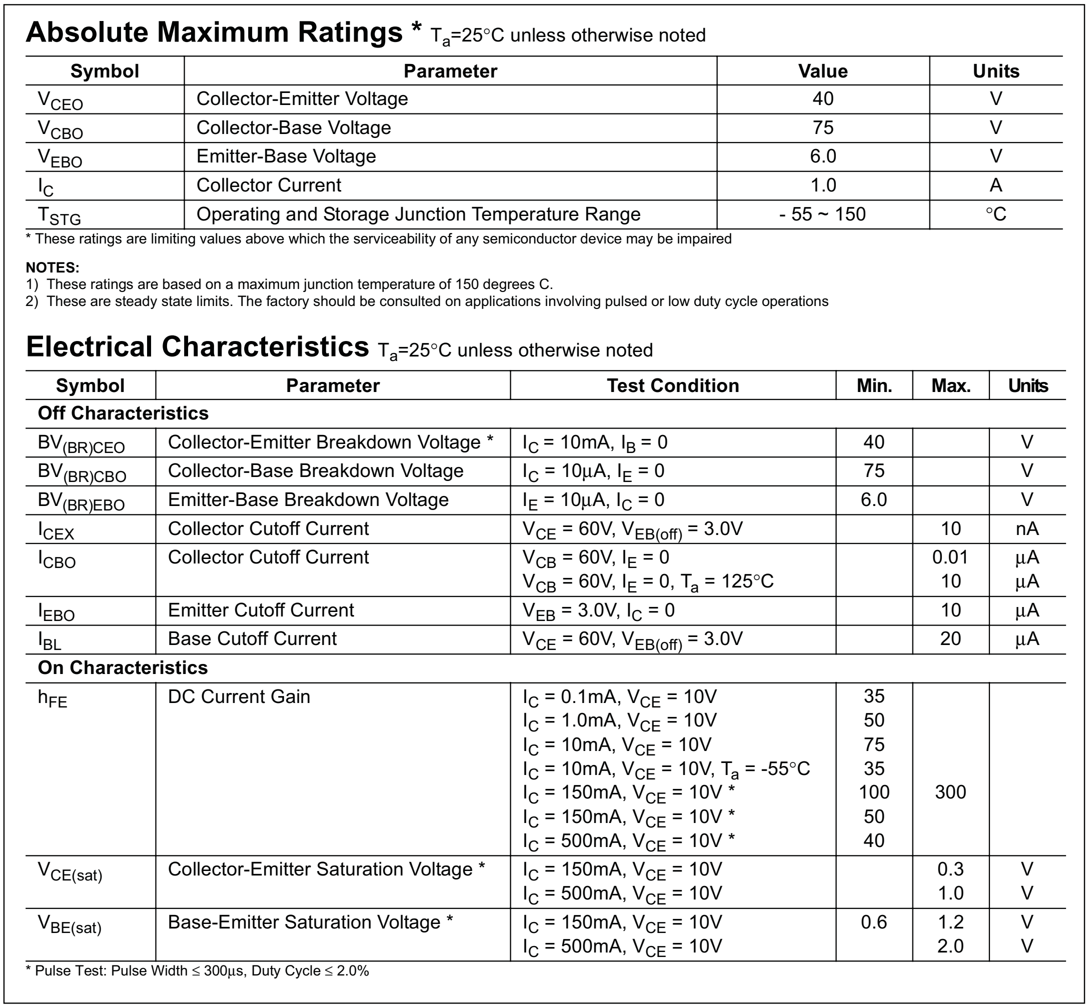
A circuit for one zone is shown in Figure 4–49. It consists of two BJTs, Q_1 and Q_2. As long as the zone sensors are closed, Q_1 is in the *on* state (saturated). The very low saturation voltage at the Q_1 collector keeps Q_2 *off.* Notice that the collector of Q_2 is left open with no load connected. This allows for all four of the zone circuit outputs to be tied together and a common load connected externally to drive the alarm and/or dialing circuits. If one of the zone sensors opens, indicating a break-in, Q_1 turns *off* and its collector voltage goes to V_{CC}. This turns on Q_2, causing it to saturate. The *on* state of Q_2 will then activate the audible alarm and the telephone dialing sequence.

FIGURE 4–49

One of the four identical transistor switching circuits.



1. Refer to the partial datasheet for the 2N2222A in Figure 4–50 and determine the value of the collector resistor R_3 to limit the current to 10 mA with a +12 V dc supply voltage.



Absolute Maximum Ratings * T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	75	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current	1.0	A
T_{STG}	Operating and Storage Junction Temperature Range	- 55 ~ 150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$BV_{(BR)CEO}$	Collector-Emitter Breakdown Voltage *	I_C = 10mA, I_B = 0	40		V
$BV_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10µA, I_E = 0	75		V
$BV_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10µA, I_C = 0	6.0		V
I_{CEX}	Collector Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		10	nA
I_{CBO}	Collector Cutoff Current	V_{CB} = 60V, I_E = 0 V_{CB} = 60V, I_E = 0, T_a = 125°C		0.01 10	µA µA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3.0V, I_C = 0		10	µA
I_{BL}	Base Cutoff Current	V_{CE} = 60V, $V_{EB(off)}$ = 3.0V		20	µA
On Characteristics					
h_{FE}	DC Current Gain	I_C = 0.1mA, V_{CE} = 10V I_C = 1.0mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V, T_a = -55°C I_C = 150mA, V_{CE} = 10V * I_C = 150mA, V_{CE} = 10V * I_C = 500mA, V_{CE} = 10V *	35 50 75 35 100 50 40	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V		0.3 1.0	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage *	I_C = 150mA, V_{CE} = 10V I_C = 500mA, V_{CE} = 10V	0.6	1.2 2.0	V V

* Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%

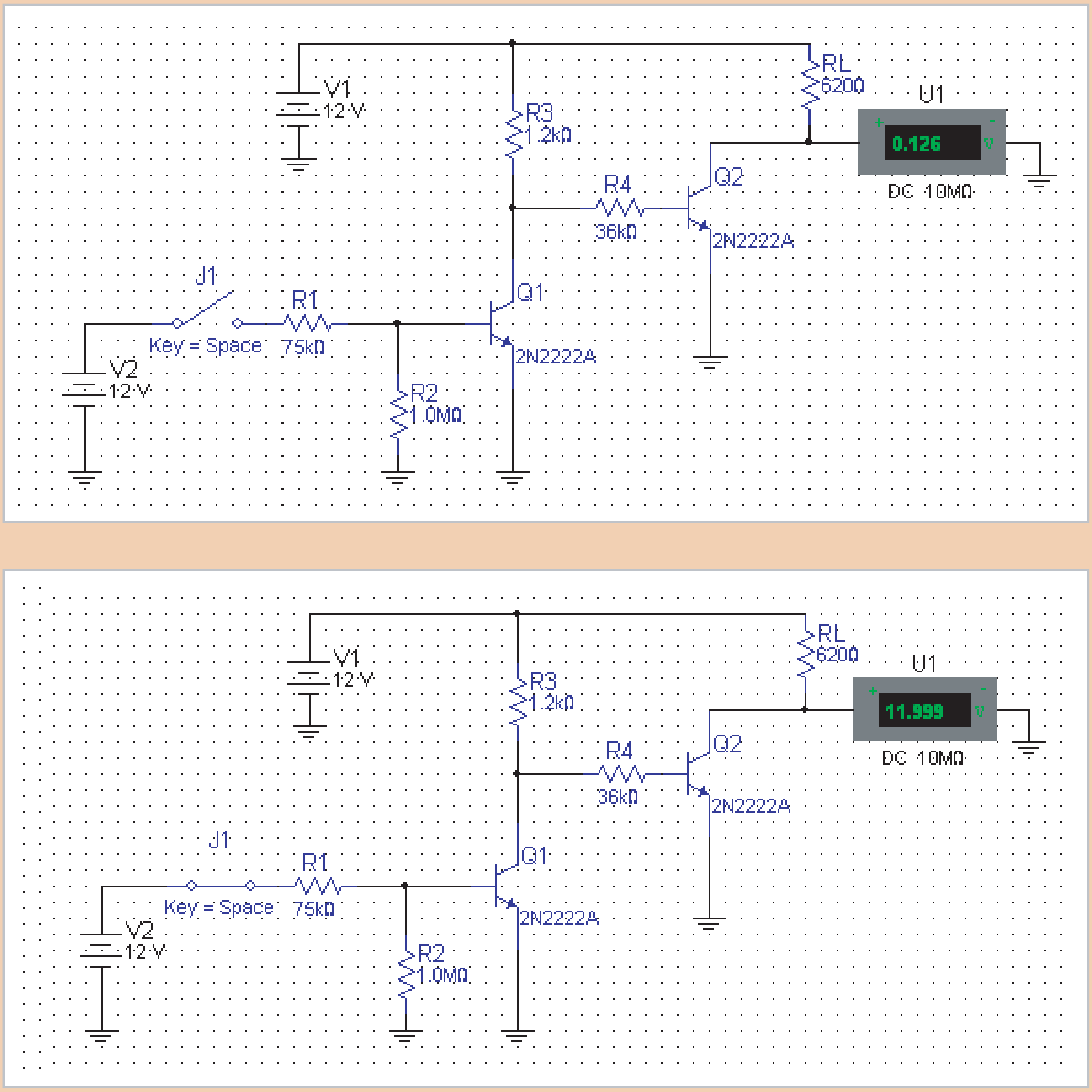
FIGURE 4–50

Partial datasheet for the 2N2222A transistor. Copyright Fairchild Semiconductor Corporation. Used by permission.

2. Using the minimum β_{DC} or h_{FE} from the datasheet, determine the base current required to saturate Q_1 at $I_C = 10$ mA.
3. To ensure saturation, calculate the value of R_1 necessary to provide sufficient base current to Q_1 from the +12 V sensor input. R_2 can be any arbitrarily high value to assure the base of Q_1 is near ground when there is no input voltage.
4. Calculate the value of R_4 so that a sufficient base current is supplied to Q_2 to ensure saturation for a load of 620 Ω. This simulates the actual load of the alarm and dialing circuits.

Simulation

The switching circuit is simulated with Multisim, as shown in Figure 4–51. A switch connected to a 12 V source simulates the zone input and a 620 Ω load resistor is connected to


V1
12 V
R3
1.2kΩ
RL
620Ω
U1
0.126
DC 10MΩ
R4
36kΩ
Q2
2N2222A
J1
R1
Key = Space
75kΩ
Q1
2N2222A
V2
12 V
R2
1.0MΩ
V1
12 V
R3
1.2kΩ
RL
620Ω
U1
11.999
DC 10MΩ
R4
36kΩ
Q2
2N2222A
J1
R1
Key = Space
75kΩ
Q1
2N2222A
V2
12 V
R2
1.0MΩ

▲ FIGURE 4–51

Simulation of the switching circuit.

the output to represent the actual load. When the zone switch is open, Q_2 is saturated as indicated by 0.126 V at its collector. When the zone switch is closed, Q_2 is *off* as indicated by the 11.999 V at its collector.

5. How does the Q_2 saturation voltage compare to the value specified on the datasheet?

Simulate the circuit using your Multisim software. Observe the operation with the virtual multimeter.

Prototyping and Testing

Now that the circuit has been simulated, it is connected on a protoboard and tested for proper operation.

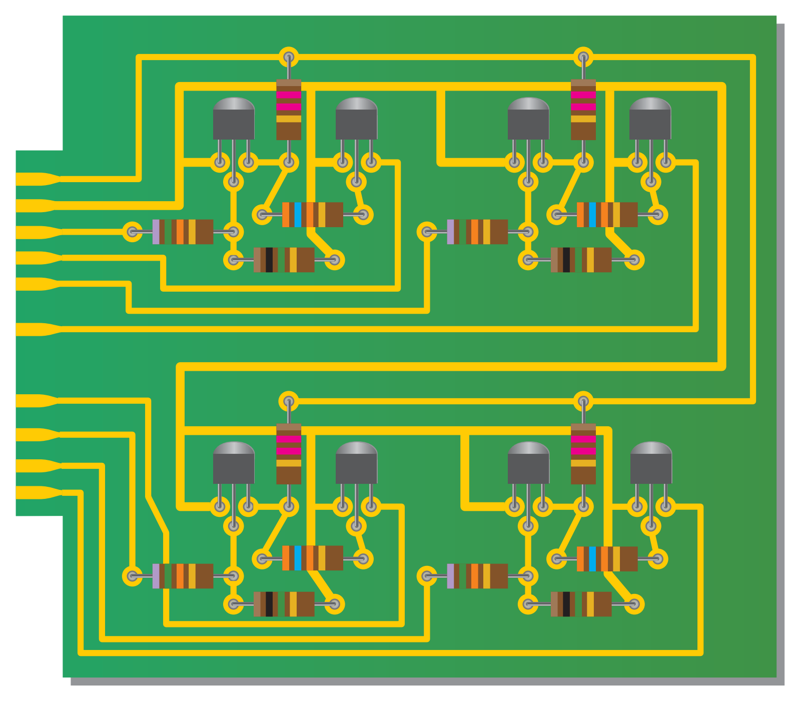
Lab Experiment

To build and test a similar circuit, go to Experiment 4 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Printed Circuit Board

The transistor switching circuit prototype has been built and tested. It is now committed to a printed circuit layout, as shown in Figure 4–52. Notice that there are four identical circuits on the board, one for each zone to be monitored. The outputs are externally connected to form a single input.

6. Compare the printed circuit board to the schematic in Figure 4–49 and verify that they agree. Identify each component.
7. Compare the resistor values on the printed circuit board to those that you calculated previously. They should closely agree.
8. Label the input and output pins on the printed circuit board according to their function.
9. Describe how you would test the circuit board.
10. Explain how the system can be expanded to monitor six zones instead of four.

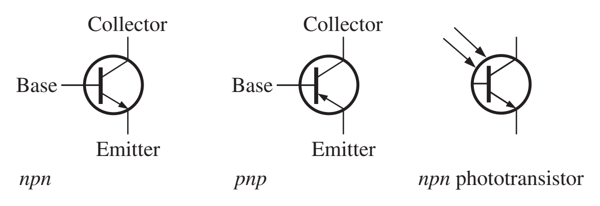


▶ FIGURE 4–52

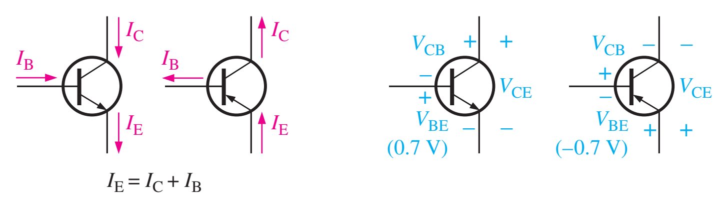
The 4-zone transistor switching circuit board.

SUMMARY OF BIPOLAR JUNCTION TRANSISTORS

SYMBOLS

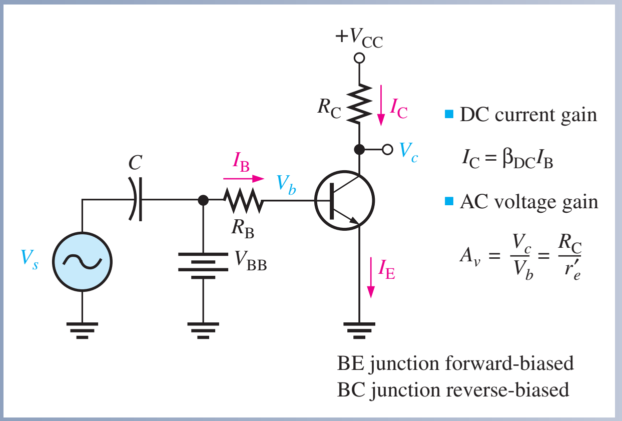

Collector
Base
Emitter
npn
Collector
Base
Emitter
pnp
npn phototransistor

CURRENTS AND VOLTAGES


I_B
I_C
I_E
I_B
I_C
I_E
V_{CB}
+
+
−
+
V_{CE}
V_{BE}
−
−
(0.7 V)
V_{CB}
−
−
+
−
V_{CE}
V_{BE}
+
+
(−0.7 V)

$I_E = I_C + I_B$

AMPLIFICATION


$+V_{CC}$
R_C
I_C
V_c
C
I_B
V_b
R_B
V_s
V_{BB}
I_E

- DC current gain

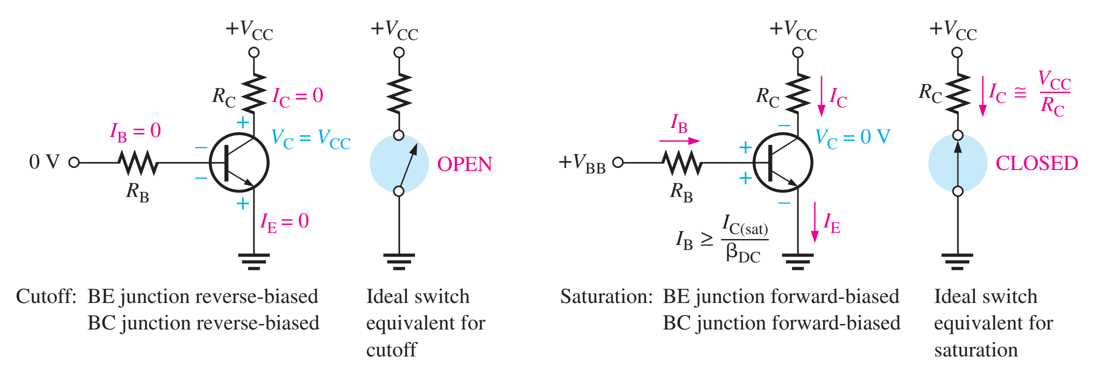
$I_C = \beta_{DC} I_B$

- AC voltage gain

$$A_v = \frac{V_c}{V_b} = \frac{R_C}{r'_e}$$

BE junction forward-biased
BC junction reverse-biased

SWITCHING


$+V_{CC}$
R_C
$I_C = 0$
+
$V_C = V_{CC}$
−
$I_B = 0$
0 V
R_B
−
+
$I_E = 0$
$+V_{CC}$
OPEN
$+V_{CC}$
R_C
I_C
−
$V_C = 0$ V
I_B
+
$+V_{BB}$
R_B
+
−
I_E
$+V_{CC}$
R_C
$I_C \cong \frac{V_{CC}}{R_C}$
CLOSED

$I_B \geq \frac{I_{C(sat)}}{\beta_{DC}}$

Cutoff: BE junction reverse-biased
BC junction reverse-biased

Ideal switch equivalent for cutoff

Saturation: BE junction forward-biased
BC junction forward-biased

Ideal switch equivalent for saturation

SUMMARY

Section 4–1

- The BJT (bipolar junction transistor) is constructed with three regions: base, collector, and emitter.
- The BJT has two *pn* junctions, the base-emitter junction and the base-collector junction.
- Current in a BJT consists of both free electrons and holes, thus the term *bipolar*.
- The base region is very thin and lightly doped compared to the collector and emitter regions.
- The two types of bipolar junction transistor are the *npn* and the *pnp*.

Section 4–2

- To operate as an amplifier, the base-emitter junction must be forward-biased and the base-collector junction must be reverse-biased. This is called *forward-reverse bias*.
- The three currents in the transistor are the base current (I_B), emitter current (I_E), and collector current (I_C).
- I_B is very small compared to I_C and I_E.

Section 4–3

- The dc current gain of a transistor is the ratio of I_C to I_B and is designated β_{DC}. Values typically range from less than 20 to several hundred.
- β_{DC} is usually referred to as h_{FE} on transistor datasheets.
- The ratio of I_C to I_E is called α_{DC}. Values typically range from 0.95 to 0.99.
- There is a variation in β_{DC} over temperature and also from one transistor to another of the same type.

Section 4–4

- When a transistor is forward-reverse biased, the voltage gain depends on the internal emitter resistance and the external collector resistance.
- Voltage gain is the ratio of output voltage to input voltage.
- Internal transistor resistances are represented by a lowercase *r*.

Section 4–5

- A transistor can be operated as an electronic switch in cutoff and saturation.
- In cutoff, both *pn* junctions are reverse-biased and there is essentially no collector current. The transistor ideally behaves like an open switch between collector and emitter.
- In saturation, both *pn* junctions are forward-biased and the collector current is maximum. The transistor ideally behaves like a closed switch between collector and emitter.

Section 4–6

- In a phototransistor, base current is produced by incident light.
- A phototransistor can be either a two-lead or a three-lead device.
- An optocoupler consists of an LED and a photodiode or phototransistor.
- Optocouplers are used to electrically isolate circuits.

Section 4–7

- There are many types of transistor packages using plastic, metal, or ceramic.
- Two basic package types are through-hole and surface mount.

Section 4–8

- It is best to check a transistor in-circuit before removing it.
- Common faults in transistor circuits are open junctions, low β_{DC}, excessive leakage currents, and external opens and shorts on the circuit board.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Amplification The process of increasing the power, voltage, or current by electronic means.

Base One of the semiconductor regions in a BJT. The base is very thin and lightly doped compared to the other regions.

Beta (β) The ratio of dc collector current to dc base current in a BJT; current gain from base to collector.

BJT A bipolar junction transistor constructed with three doped semiconductor regions separated by two *pn* junctions.

Collector The largest of the three semiconductor regions of a BJT.

Cutoff The nonconducting state of a transistor.

Emitter The most heavily doped of the three semiconductor regions of a BJT.

Gain The amount by which an electrical signal is increased or amplified.

Linear Characterized by a straight-line relationship of the transistor currents.

Phototransistor A transistor in which base current is produced when light strikes the photosensitive semiconductor base region.

Saturation The state of a BJT in which the collector current has reached a maximum and is independent of the base current.

KEY FORMULAS

4–1	$I_{\mathrm{E}} = I_{\mathrm{C}} + I_{\mathrm{B}}$	Transistor currents
4–2	$\beta_{\mathrm{DC}} = \dfrac{I_{\mathrm{C}}}{I_{\mathrm{B}}}$	DC current gain
4–3	$V_{\mathrm{BE}} \cong 0.7\ \mathrm{V}$	Base-to-emitter voltage (silicon)
4–4	$I_{\mathrm{B}} = \dfrac{V_{\mathrm{BB}} - V_{\mathrm{BE}}}{R_{\mathrm{B}}}$	Base current
4–5	$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}}$	Collector-to-emitter voltage (common-emitter)
4–6	$V_{\mathrm{CB}} = V_{\mathrm{CE}} - V_{\mathrm{BE}}$	Collector-to-base voltage
4–7	$A_v \cong \dfrac{R_{\mathrm{C}}}{r'_e}$	Approximate ac voltage gain
4–8	$V_{\mathrm{CE(cutoff)}} = V_{\mathrm{CC}}$	Cutoff condition
4–9	$I_{\mathrm{C(sat)}} = \dfrac{V_{\mathrm{CC}} - V_{\mathrm{CE(sat)}}}{R_{\mathrm{C}}}$	Collector saturation current
4–10	$I_{\mathrm{B(min)}} = \dfrac{I_{\mathrm{C(sat)}}}{\beta_{\mathrm{DC}}}$	Minimum base current for saturation
4–11	$I_{\mathrm{C}} = \beta_{\mathrm{DC}} I_{\lambda}$	Phototransistor collector current

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. A bipolar junction transistor has three terminals.

2. The three regions of a BJT are base, emitter, and cathode.

3. For operation in the linear or active region, the base-emitter junction of a transistor is forward-biased.

4. Two types of BJT are *npn* and *pnp*.

5. The base current and collector current are approximately equal.

6. The dc voltage gain of a transistor is designated β_{DC}.

7. Cutoff and saturation are the two normal states of a linear transistor amplifier.

8. When a transistor is saturated, the collector current is maximum.

9. β_{DC} and h_{FE} are two different transistor parameters.

10. Voltage gain of a transistor amplifier depends on the collector resistor and the internal ac resistance.

11. Amplification is the output voltage divided by the input current.

12. A transistor in cutoff acts as an open switch.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If a transistor with a higher β_{DC} is used in Figure 4–9, the collector current will

(a) increase **(b)** decrease **(c)** not change

2. If a transistor with a higher β_{DC} is used in Figure 4–9, the emitter current will

(a) increase **(b)** decrease **(c)** not change

3. If a transistor with a higher β_{DC} is used in Figure 4–9, the base current will
   (a) increase **(b)** decrease **(c)** not change
4. If V_{BB} is reduced in Figure 4–16, the collector current will
   (a) increase **(b)** decrease **(c)** not change
5. If V_{CC} in Figure 4–16 is increased, the base current will
   (a) increase **(b)** decrease **(c)** not change
6. If the amplitude of V_{in} in Figure 4–22 is decreased, the ac output voltage amplitude will
   (a) increase **(b)** decrease **(c)** not change
7. If the transistor in Figure 4–24 is saturated and the base current is increased, the collector current will
   (a) increase **(b)** decrease **(c)** not change
8. If R_C in Figure 4–24 is reduced in value, the value of $I_{C(sat)}$ will
   (a) increase **(b)** decrease **(c)** not change
9. If the transistor in Figure 4–38 is open from collector to emitter, the voltage across R_C will
   (a) increase **(b)** decrease **(c)** not change
10. If the transistor in Figure 4–38 is open from collector to emitter, the collector voltage will
    (a) increase **(b)** decrease **(c)** not change
11. If the base resistor in Figure 4–38 is open, the transistor collector voltage will
    (a) increase **(b)** decrease **(c)** not change
12. If the emitter in Figure 4–38 becomes disconnected from ground, the collector voltage will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 4–1

1. The three terminals of a bipolar junction transistor are called
   (a) *p*, *n*, *p* **(b)** *n*, *p*, *n* **(c)** input, output, ground **(d)** base, emitter, collector
2. In a *pnp* transistor, the *p* regions are
   (a) base and emitter **(b)** base and collector **(c)** emitter and collector

Section 4–2

3. For operation as an amplifier, the base of an *npn* transistor must be
   (a) positive with respect to the emitter **(b)** negative with respect to the emitter
   (c) positive with respect to the collector **(d)** 0 V
4. The emitter current is always
   (a) greater than the base current **(b)** less than the collector current
   (c) greater than the collector current **(d)** answers (a) and (c)

Section 4–3

5. The β_{DC} of a transistor is its
   (a) current gain **(b)** voltage gain **(c)** power gain **(d)** internal resistance
6. If I_C is 50 times larger than I_B, then β_{DC} is
   (a) 0.02 **(b)** 100 **(c)** 50 **(d)** 500
7. The approximate voltage across the forward-biased base-emitter junction of a silicon BJT is
   (a) 0 V **(b)** 0.7 V **(c)** 0.3 V **(d)** V_{BB}
8. The bias condition for a transistor to be used as a linear amplifier is called
   (a) forward-reverse **(b)** forward-forward **(c)** reverse-reverse **(d)** collector bias

Section 4–4

9. If the output of a transistor amplifier is 5 V rms and the input is 100 mV rms, the voltage gain is
   (a) 5 **(b)** 500 **(c)** 50 **(d)** 100
10. When a lowercase r' is used in relation to a transistor, it refers to
    (a) a low resistance **(b)** a wire resistance
    (c) an internal ac resistance **(d)** a source resistance

11. In a given transistor amplifier, $R_C = 2.2\ \text{k}\Omega$ and $r'_e = 20\ \Omega$, the voltage gain is
(a) 2.2 **(b)** 110 **(c)** 20 **(d)** 44

Section 4–5

12. When operated in cutoff and saturation, the transistor acts like a
(a) linear amplifier **(b)** switch **(c)** variable capacitor **(d)** variable resistor

13. In cutoff, V_{CE} is
(a) 0 V **(b)** minimum **(c)** maximum
(d) equal to V_{CC} **(e)** answers (a) and (b) **(f)** answers (c) and (d)

14. In saturation, V_{CE} is
(a) 0.7 V **(b)** equal to V_{CC} **(c)** minimum **(d)** maximum

15. To saturate a BJT,
(a) $I_B = I_{C(sat)}$ **(b)** $I_B > I_{C(sat)}/\beta_{DC}$
(c) V_{CC} must be at least 10 V **(d)** the emitter must be grounded

16. Once in saturation, a further increase in base current will
(a) cause the collector current to increase **(b)** not affect the collector current
(c) cause the collector current to decrease **(d)** turn the transistor off

Section 4–6

17. In a phototransistor, base current is
(a) set by a bias voltage **(b)** directly proportional to light intensity
(c) inversely proportional to light intensity **(d)** not a factor

18. The relationship between the collector current and a light-generated base current is
(a) $I_C = \beta_{DC} I_\lambda$ **(b)** $I_C = \alpha_{DC} I_\lambda$ **(c)** $I_C = \lambda I_\lambda$ **(d)** $I_C = \beta_{DC}^2 I_\lambda$

19. An optocoupler usually consists of
(a) two LEDs **(b)** an LED and a photodiode
(c) an LED and a phototransistor **(d)** both (b) and (c)

Section 4–8

20. In a transistor amplifier, if the base-emitter junction is open, the collector voltage is
(a) V_{CC} **(b)** 0 V **(c)** floating **(d)** 0.2 V

21. A DMM measuring on open transistor junction shows
(a) 0 V **(b)** 0.7 V **(c)** OL **(d)** V_{CC}

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 4–1

Bipolar Junction Transistor (BJT) Structure

1. What are the majority carriers in the base region of an *npn* transistor called?

2. Explain the purpose of a thin, lightly doped base region.

Section 4–2

Basic BJT Operation

3. Why is the base current in a transistor so much less than the collector current?

4. In a certain transistor circuit, the base current is 2 percent of the 30 mA emitter current. Determine the collector current.

5. For normal operation of a *pnp* transistor, the base must be (+ or −) with respect to the emitter, and (+ or −) with respect to the collector.

6. What is the value of I_C for $I_E = 5.34$ mA and $I_B = 475\ \mu$A?

Section 4–3

BJT Characteristics and Parameters

7. What is the α_{DC} when $I_C = 8.23$ mA and $I_E = 8.69$ mA?

8. A certain transistor has an $I_C = 25$ mA and an $I_B = 200\ \mu$A. Determine the β_{DC}.

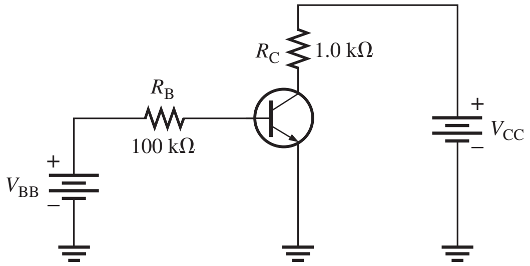
9. What is the β_{DC} of a transistor if $I_C = 20.3$ mA and $I_E = 20.5$ mA?

10. What is the α_{DC} if $I_C = 5.35$ mA and $I_B = 50\ \mu$A?

11. A certain transistor exhibits an α_{DC} of 0.96. Determine I_C when $I_E = 9.35$ mA.

12. A base current of 50 μA is applied to the transistor in Figure 4–53, and a voltage of 5 V is dropped across R_C. Determine the β_{DC} of the transistor.

▶ **FIGURE 4–53**


R_C
1.0 kΩ
R_B
100 kΩ
+
V_{CC}
–
+
V_{BB}
–

13. Calculate α_{DC} for the transistor in Problem 12.

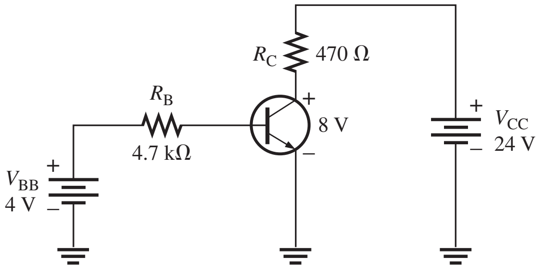
14. Assume that the transistor in the circuit of Figure 4–53 is replaced with one having a β_{dc} of 200. Determine I_B, I_C, I_E, and V_{CE} given that $V_{CC} = 10$ V and $V_{BB} = 3$ V.

15. If V_{CC} is increased to 15 V in Figure 4–53, how much do the currents and V_{CE} change?

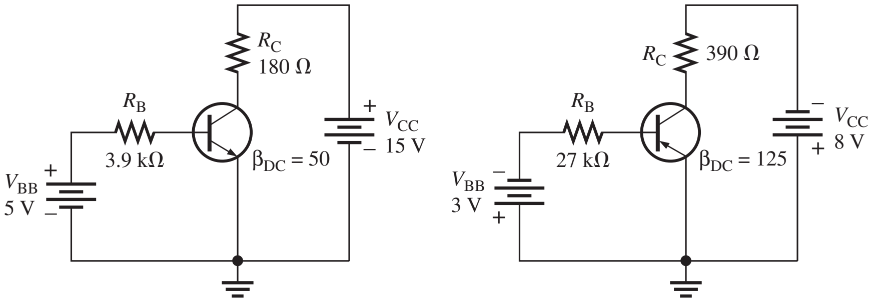
16. Determine each current in Figure 4–54. What is the β_{DC}?

▶ **FIGURE 4–54**

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F04-54).


R_C
470 Ω
R_B
4.7 kΩ
+
8 V
–
+
V_{CC}
24 V
–
+
V_{BB}
4 V
–

17. Find V_{CE}, V_{BE}, and V_{CB} in both circuits of Figure 4–55.


R_C
180 Ω
R_B
3.9 kΩ
$\beta_{DC} = 50$
+
V_{CC}
15 V
–
+
V_{BB}
5 V
–
R_C
390 Ω
R_B
27 kΩ
$\beta_{DC} = 125$
–
V_{CC}
8 V
+
–
V_{BB}
3 V
+

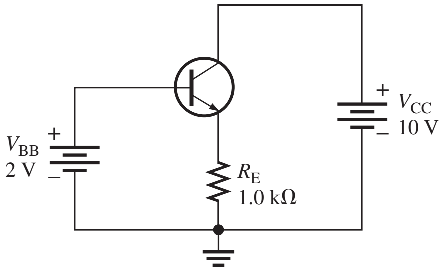
(a) (b)

▲ **FIGURE 4–55**

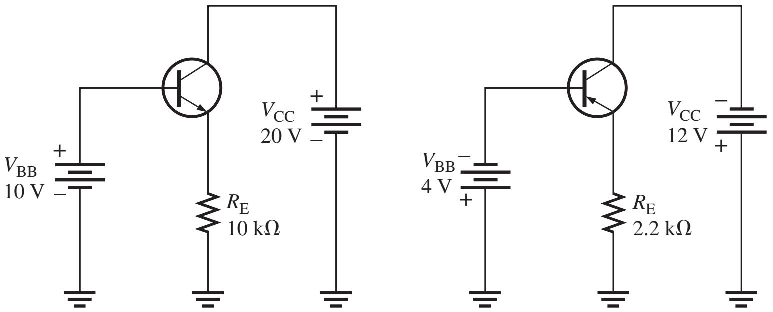
18. Determine whether or not the transistors in Figure 4–55 are saturated.

19. Find I_B, I_E, and I_C in Figure 4–56. $\alpha_{DC} = 0.98$.

▶ **FIGURE 4–56**


+
V_{CC}
10 V
–
+
V_{BB}
2 V
–
R_E
1.0 kΩ

20. Determine the terminal voltages of each transistor with respect to ground for each circuit in Figure 4–57. Also determine V_{CE}, V_{BE}, and V_{CB}.



(a) (b)

▲ **FIGURE 4–57**

21. If the β_{DC} in Figure 4–57(a) changes from 100 to 150 due to a temperature increase, what is the change in collector current?

22. A certain transistor is to be operated at a collector current of 50 mA. How high can V_{CE} go without exceeding a $P_{D(max)}$ of 1.2 W?

23. The power dissipation derating factor for a certain transistor is 1 mW/°C. The $P_{D(max)}$ is 0.5 W at 25°C. What is $P_{D(max)}$ at 100°C?

Section 4–4 The BJT as an Amplifier

24. A transistor amplifier has a voltage gain of 50. What is the output voltage when the input voltage is 100 mV?

25. To achieve an output of 10 V with an input of 300 mV, what voltage gain is required?

26. A 50 mV signal is applied to the base of a properly biased transistor with $r'_e = 10\ \Omega$ and $R_C = 560\ \Omega$. Determine the signal voltage at the collector.

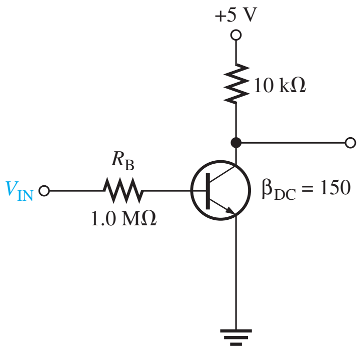
27. Determine the value of the collector resistor in an *npn* transistor amplifier with $\beta_{DC} = 250$, $V_{BB} = 2.5$ V, $V_{CC} = 9$ V, $V_{CE} = 4$ V, and $R_B = 100$ kΩ.

28. What is the dc current gain of each circuit in Figure 4–55?

Section 4–5 The BJT as a Switch

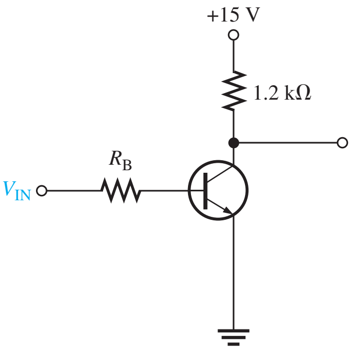
29. Determine $I_{C(sat)}$ for the transistor in Figure 4–58. What is the value of I_B necessary to produce saturation? What minimum value of V_{IN} is necessary for saturation? Assume $V_{CE(sat)} = 0$ V.

▶ **FIGURE 4–58**



30. The transistor in Figure 4–59 has a β_{DC} of 50. Determine the value of R_B required to ensure saturation when V_{IN} is 5 V. What must V_{IN} be to cut off the transistor? Assume $V_{CE(sat)} = 0$ V.

▶ FIGURE 4–59

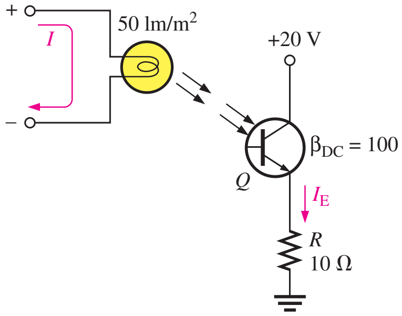


Section 4–6 The Phototransistor

31. A certain phototransistor in a circuit has a $\beta_{DC} = 200$. If $I_\lambda = 100\ \mu A$, what is the collector current?

32. Determine the emitter current in the phototransistor circuit in Figure 4–60 if, for each lm/m^2 of light intensity, 1 μA of base current is produced in the phototransistor.

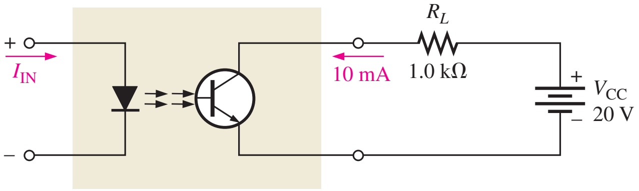
▶ FIGURE 4–60



33. A particular optical coupler has a current transfer ratio of 30 percent. If the input current is 100 mA, what is the output current?

34. The optical coupler shown in Figure 4–61 is required to deliver at least 10 mA to the external load. If the current transfer ratio is 60 percent, how much current must be supplied to the input?

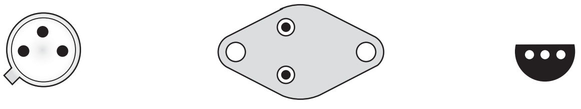
▶ FIGURE 4–61



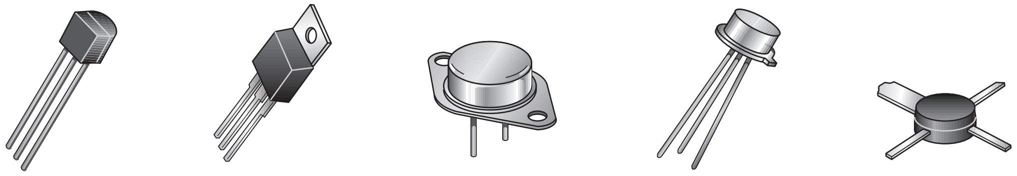
Section 4–7 Transistor Categories and Packaging

35. Identify the leads on the transistors in Figure 4–62. Bottom views are shown.

▶ FIGURE 4–62


(a) (b) (c)

36. What is the most probable category of each transistor in Figure 4–63?

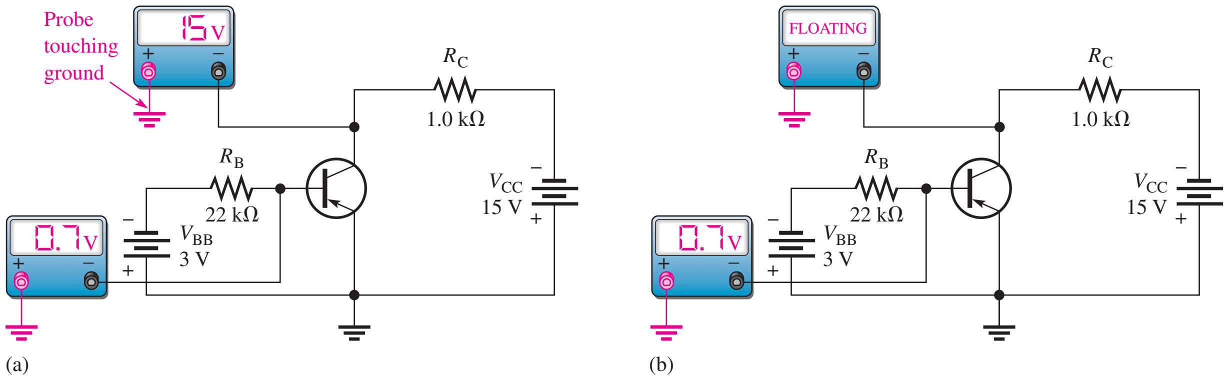

(a) (b) (c) (d) (e)

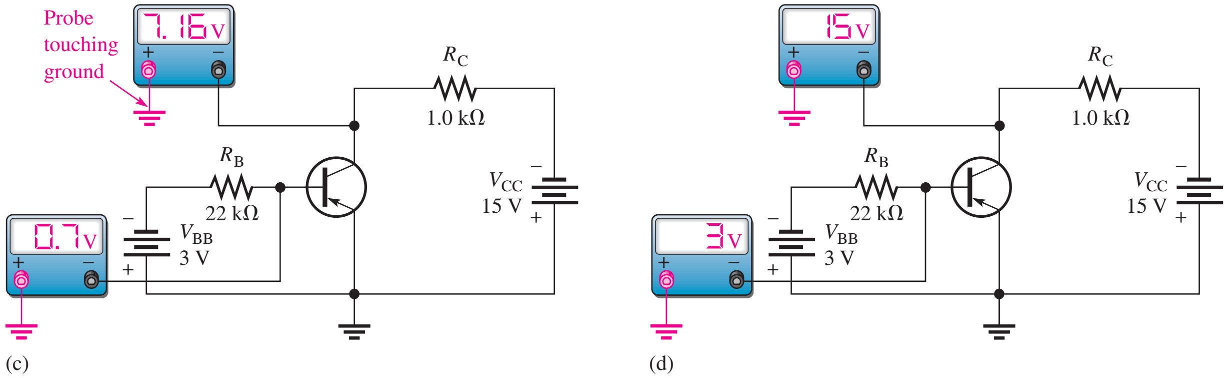
▲ FIGURE 4–63

Section 4–8 Troubleshooting

37. In an out-of-circuit test of a good *npn* transistor, what should an analog ohmmeter indicate when its positive probe is touching the emitter and the negative probe is touching the base? When its positive probe is touching the base and the negative probe is touching the collector?

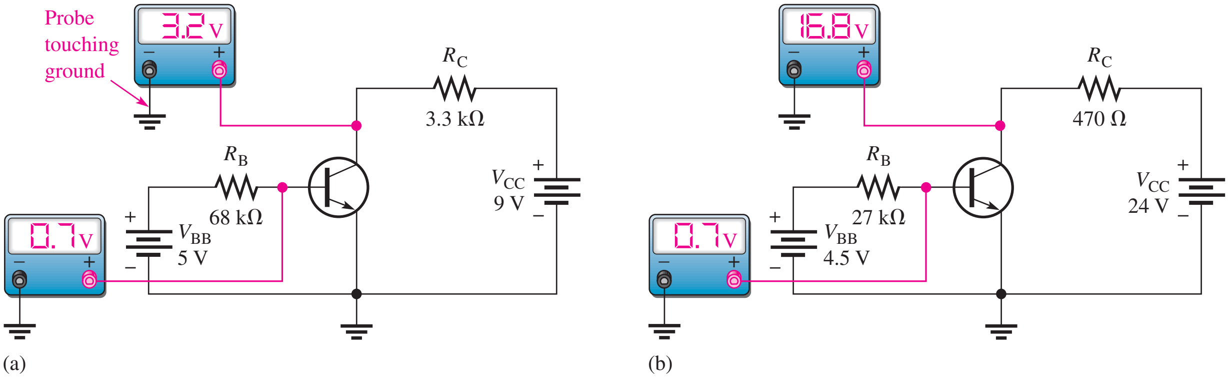
38. What is the most likely problem, if any, in each circuit of Figure 4–64? Assume a β_{DC} of 75.


Probe touching ground
15 V
R_C
1.0 kΩ
R_B
22 kΩ
V_{CC}
15 V
0.7 V
V_{BB}
3 V
(a)
FLOATING
(b)
7.16 V
(c)
3 V
(d)



▲ FIGURE 4–64

39. What is the value of the β_{DC} of each transistor in Figure 4–65?


Probe touching ground
3.2 V
R_C
3.3 kΩ
R_B
68 kΩ
V_{CC}
9 V
0.7 V
V_{BB}
5 V
(a)
16.8 V
470 Ω
27 kΩ
24 V
4.5 V
(b)

▲ FIGURE 4–65

APPLICATION ACTIVITY PROBLEMS

40. Calculate the power dissipation in each resistor in Figure 4–51 for both states of the circuit.

41. Determine the minimum value of load resistance that Q_2 can drive without exceeding the maximum collector current specified on the datasheet.

42. Develop a wiring diagram for the printed circuit board in Figure 4–52 for connecting it in the security alarm system. The input/output pins are numbered from 1 to 10 starting at the top.

DATASHEET PROBLEMS

43. Refer to the partial transistor datasheet in Figure 4–20.

(a) What is the maximum collector-to-emitter voltage for a 2N3904?

(b) How much continuous collector current can the 2N3904 handle?

(c) How much power can a 2N3904 dissipate if the ambient temperature is 25°C?

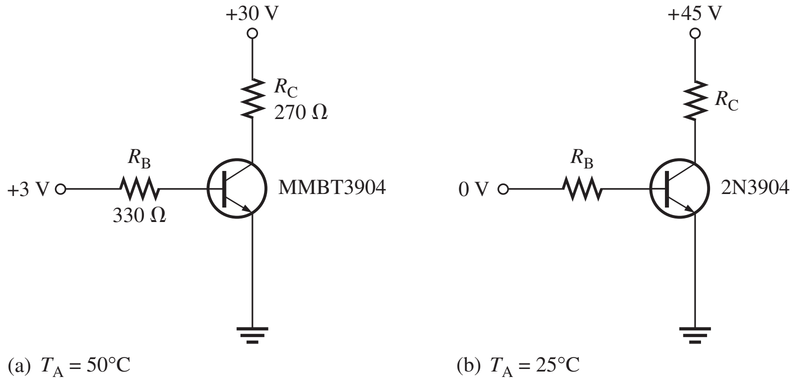
(d) How much power can a 2N3904 dissipate if the ambient temperature is 50°C?

(e) What is the minimum h_{FE} of a 2N3904 if the collector current is 1 mA?

44. Refer to the transistor datasheet in Figure 4–20. A MMBT3904 is operating in an environment where the ambient temperature is 65°C. What is the most power that it can dissipate?

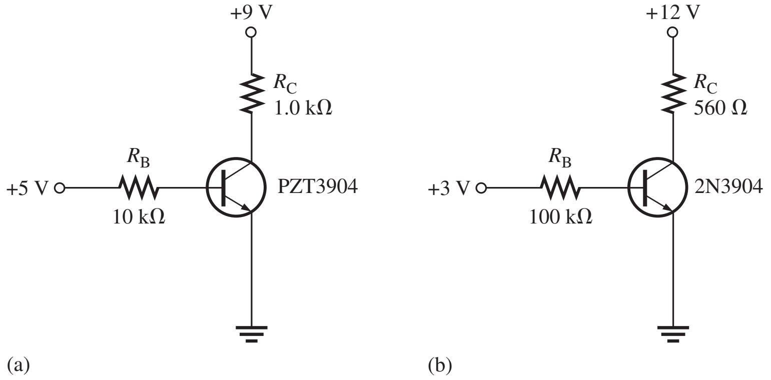
45. Refer to the transistor datasheet in Figure 4–20. A PZT3904 is operating with an ambient temperature of 45°C. What is the most power that it can dissipate?

46. Refer to the transistor datasheet in Figure 4–20. Determine if any rating is exceeded in each circuit of Figure 4–66 based on minimum specified values.



▲ FIGURE 4–66

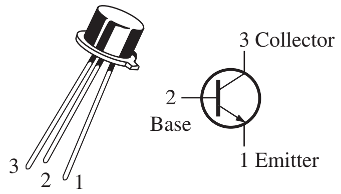
47. Refer to the transistor datasheet in Figure 4–20. Determine whether or not the transistor is saturated in each circuit of Figure 4–67 based on the maximum specified value of h_{FE}.



▲ FIGURE 4–67

48. Refer to the partial transistor datasheet in Figure 4–68. Determine the minimum and maximum base currents required to produce a collector current of 10 mA in a 2N3946. Assume that the transistor is not in saturation and $V_{CE} = 1$ V.

2N3946
2N3947



General-Purpose
Transistors

NPN Silicon

Maximum Ratings

Rating	Symbol	Value	Unit
Collector-Emitter voltage	V_{CEO}	40	V dc
Collector-Base voltage	V_{CBO}	60	V dc
Emitter-Base voltage	V_{EBO}	6.0	V dc
Collector current — continuous	I_C	200	mA dc
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.36 2.06	Watts mW/°C
Total device dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.2 6.9	Watts mW/°C
Operating and storage junction Temperature range	T_J, T_{stg}	–65 to +200	°C

Thermal Characteristics

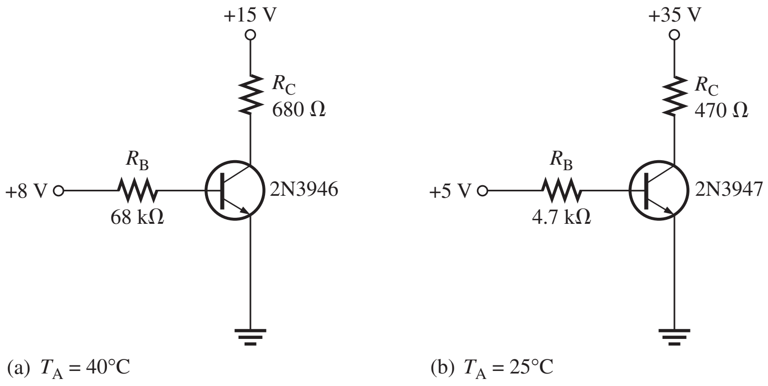
Characteristic	Symbol	Max	Unit
Thermal resistance, junction to case	$R_{\theta JC}$	0.15	°C/mW
Thermal resistance, junction to ambient	$R_{\theta JA}$	0.49	°C/mW

Electrical Characteristics ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF Characteristics					
Collector-Emitter breakdown voltage ($I_C = 10$ mA dc)		$V_{(BR)CEO}$	40	–	V dc
Collector-Base breakdown voltage ($I_C = 10\ \mu$A dc, $I_E = 0$)		$V_{(BR)CBO}$	60	–	V dc
Emitter-Base breakdown voltage ($I_E = 10\ \mu$A dc, $I_C = 0$)		$V_{(BR)EBO}$	6.0	–	V dc
Collector cutoff current		I_{CEX}			μA dc
($V_{CE} = 40$ V dc, $V_{OB} = 3.0$ V dc)			–	0.010	
($V_{CE} = 40$ V dc, $V_{OB} = 3.0$ V dc, $T_A = 150°C$)			–	15	
Base cutoff current ($V_{CE} = 40$ V dc, $V_{OB} = 3.0$ V dc)		I_{BL}	–	.025	μA dc
ON Characteristics					
DC current gain		h_{FE}			–
($I_C = 0.1$ mA dc, $V_{CE} = 1.0$ V dc)	2N3946		30	–	
	2N3947		60	–	
($I_C = 1.0$ mA dc, $V_{CE} = 1.0$ V dc)	2N3946		45	–	
	2N3947		90	–	
($I_C = 10$ mA dc, $V_{CE} = 1.0$ V dc)	2N3946		50	150	
	2N3947		100	300	
($I_C = 50$ mA dc, $V_{CE} = 1.0$ V dc)	2N3946		20	–	
	2N3947		40	–	
Collector-Emitter saturation voltage		$V_{CE(sat)}$			V dc
($I_C = 10$ mA dc, $I_B = 1.0$ mA dc)			–	0.2	
($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)			–	0.3	
Base-Emitter saturation voltage		$V_{BE(sat)}$			V dc
($I_C = 10$ mA dc, $I_B = 1.0$ mA dc)			0.6	0.9	
($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)			–	1.0	
Small-Signal Characteristics					
Current gain — Bandwidth product		f_T			MHz
($I_C = 10$ mA dc, $V_{CE} = 20$ V dc, $f = 100$ MHz)	2N3946		250	–	
	2N3947		300	–	
Output capacitance ($V_{CB} = 10$ V dc, $I_E = 0$, $f = 100$ kHz)		C_{obo}	–	4.0	pF

▲ FIGURE 4–68

49. For each of the circuits in Figure 4–69, determine if there is a problem based on the datasheet information in Figure 4–68. Use the maximum specified h_{FE}.



(a) $T_A = 40°C$ (b) $T_A = 25°C$

▲ FIGURE 4–69

ADVANCED PROBLEMS

50. Derive a formula for α_{DC} in terms of β_{DC}.

51. A certain 2N3904 dc bias circuit with the following values is in saturation. $I_B = 500\ \mu A$, $V_{CC} = 10$ V, and $R_C = 180\ \Omega$, $h_{FE} = 150$. If you increase V_{CC} to 15 V, does the transistor come out of saturation? If so, what is the collector-to-emitter voltage and the collector current?

52. Design a dc bias circuit for a 2N3904 operating from a collector supply voltage of 9 V and a base-bias voltage of 3 V that will supply 150 mA to a resistive load that acts as the collector resistor. The circuit must not be in saturation. Assume the minimum specified β_{DC} from the datasheet.

53. Modify the design in Problem 52 to use a single 9 V dc source rather than two different sources. Other requirements remain the same.

54. Design a dc bias circuit for an amplifier in which the voltage gain is to be a minimum of 50 and the output signal voltage is to be "riding" on a dc level of 5 V. The maximum input signal voltage at the base is 10 mV rms. $V_{CC} = 12$ V, and $V_{BB} = 4$ V. Assume $r'_e = 8\ \Omega$.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

55. Open file TSP04-55 and determine the fault.

56. Open file TSP04-56 and determine the fault.

57. Open file TSP04-57 and determine the fault.

58. Open file TSP04-58 and determine the fault.

59. Open file TSP04-59 and determine the fault.

60. Open file TSP04-60 and determine the fault.

61. Open file TSP04-61 and determine the fault.

62. Open file TSP04-62 and determine the fault.

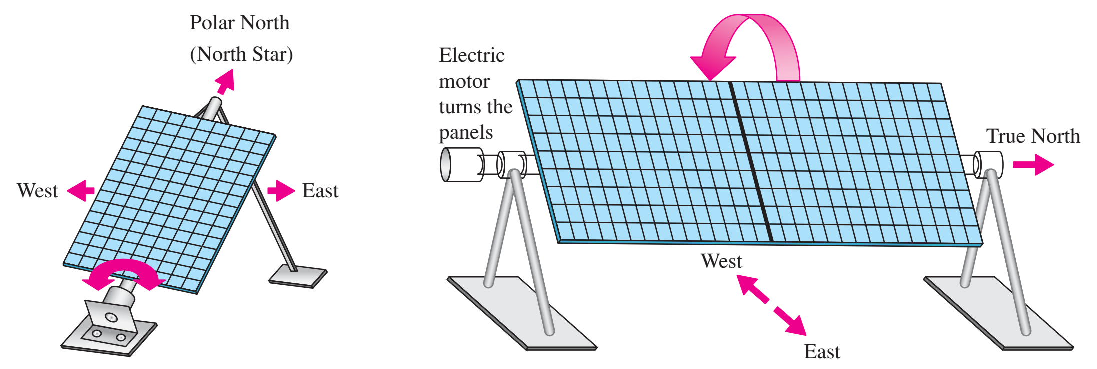
GreenTech Application 4: *Solar Power*

In this GreenTech Application, solar tracking is examined. Solar tracking is the process of moving the solar panel to track the daily movement of the sun and the seasonal changes in elevation of the sun in the southern sky. The purpose of a solar tracker is to increase the amount of solar energy that can be collected by the system. For flat-panel collectors, an increase of 30% to 50% in collected energy can be realized with sun tracking compared to fixed solar panels.

Before looking at methods for tracking, let's review how the sun moves across the sky. The daily motion of the sun follows the arc of a circle from east to west that has its axis pointed north near the location of the North Star. As the seasons change from the winter solstice to the summer solstice, the sun rises a little further to the north each day. Between the summer solstice and the winter solstice, the sun moves further south each day. The amount of the north-south motion depends on your location.

Single-Axis Solar Tracking

For flat-panel solar collectors, the most economical and generally most practical solution to tracking is to follow the daily east-west motion, and not the annual north-south motion. The daily east-to-west motion can be followed with a single-axis tracking system. There are two basic single-axis systems: polar and azimuth. In a polar system, the main axis is pointed to the polar north (North Star), as shown in Figure GA4–1(a). (In telescope terminology, this is called an equatorial mounting.) The advantage is that the solar panel is kept at an angle facing the sun at all times because it tracks the sun from east to west and is angled toward the southern sky. In an azimuth tracking system, the motor drives the solar panel and frequently multiple panels. The panels can be oriented horizontally but still track the east-to-west motion of the sun. Although this does not intercept as much of the sunlight during the seasons, it has less wind loading and is more feasible for long rows of solar panels. Figure GA4–1(b) shows a solar array that is oriented horizontally with the axis pointing to true north and uses azimuth tracking (east to west). As you can see, sunlight will strike the polar-aligned panel more directly during the seasonal movement of the sun than it will with the horizontal orientation of the azimuth tracker.



(a) A single-axis polar-aligned tracker

(b) Single-axis azimuth tracker

▲ FIGURE GA4–1

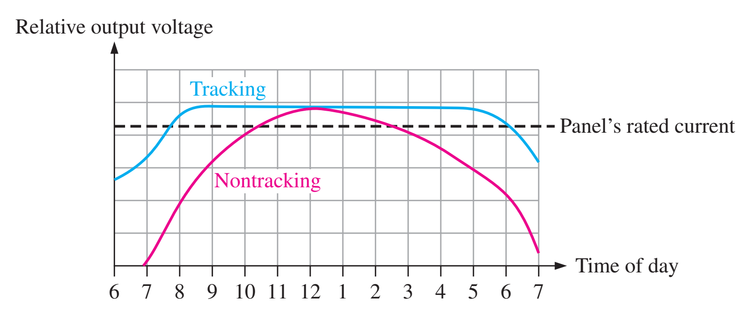
Types of single-axis solar tracking.

Some solar tracking systems combine both the azimuth and the elevation tracking, which is known as dual-axis tracking. Ideally, the solar panel should always face directly toward the sun so that the sun light rays are perpendicular to the panel. With dual-axis tracking, the annual north-south motion of the sun can be followed in addition to the daily east-to-west movement. This is particularly important with concentrating collectors that need to be oriented correctly to focus the sun on the active region.

Figure GA4–2 is an example showing the improvement in energy collection of a typical tracking panel versus a nontracking panel for a flat solar collector. As you can see, tracking extends the time that a given output can be maintained.

▶ FIGURE GA4–2

Graphs of voltages in tracking and nontracking (fixed) solar panels.

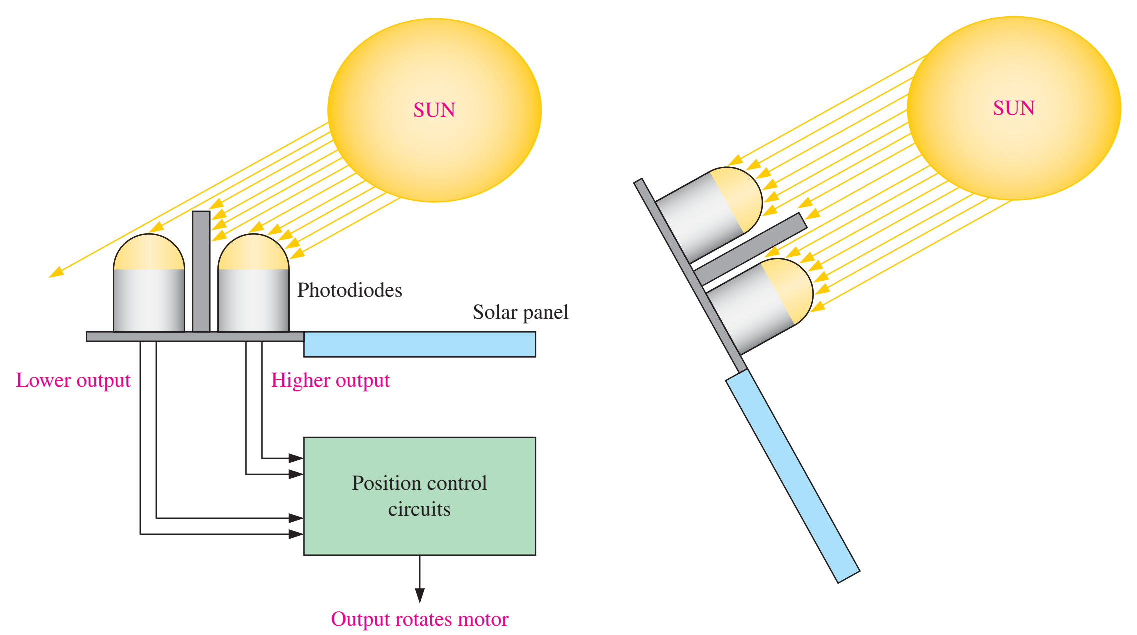


There are several methods of implementing solar tracking. Two main ones are sensor controlled and timer controlled.

Sensor-Controlled Solar Tracking

This type of tracking control uses photosensitive devices such as photodiodes or photoresistors. Typically, there are two light sensors for the azimuth control and two for the elevation control. Each pair senses the direction of light from the sun and activates the motor control to move the solar panel to align perpendicular to the sun's rays.

Figure GA4–3 shows the basic idea of a sensor-controlled tracker. Two photodiodes with a light-blocking partition between them are mounted on the same plane as the solar panel.



(a) Outputs of the photodiodes are unequal if solar panel is not directly facing the sun.

(b) Outputs of the photodiodes are equal when solar panel orientation is optimum.

▲ FIGURE GA4–3

Simplified illustration of a light-sensing control for a solar-tracking system. Relative sizes are exaggerated to demonstrate the concept.

If the solar panel is not facing directly toward the sun, the light strikes the panel and the photodiode assembly at an angle so that one of the diodes is shaded or partially shaded by the partition and receives less light than the other, as illustrated in Figure GA4–3(a). As a result, the photodiode with the most light produces a higher current than the partially-shaded device. The difference in currents from the two diodes is sensed by an operational amplifier and sends an output voltage to the motor. The motor rotates the solar panel until both photodiodes produce the same current and then is stopped by the control circuit, as illustrated in Figure GA4–3(b). The light-blocking partition between the diodes is oriented vertically for azimuth tracking and horizontally for elevation tracking. The photodiode assemblies must face in the same direction as the solar panel, so they are mounted on the solar panel frame.

Dual-Axis Solar Tracking As mentioned, a dual-axis system tracks the sun in both azimuth and elevation. It requires two photo-sensing elements and two motors, as shown in Figure GA4–4. The outputs from the two pairs of sensors go to the position-control circuits. A circuit detects the differential between the two azimuth sensor outputs and, if the differential is sufficient, the azimuth motor is advanced westward until a balance occurs between the two sensors. Similarly, another circuit detects the differential between the two elevation sensor outputs and, correspondingly, advances the elevation motor to rotate the solar panel either up or down until a balance occurs between the two sensors. When night falls and the solar panel is at its western-most position, the position-control circuits detect no output from the azimuth sensors and send a reset command to the azimuth motor to cause it to turn the soar panel back to its eastmost position to await sunrise the next day. The system must be sensitive enough to detect very small differences in photodiode output because the more closely the sun is tracked, the better the energy collection efficiency.

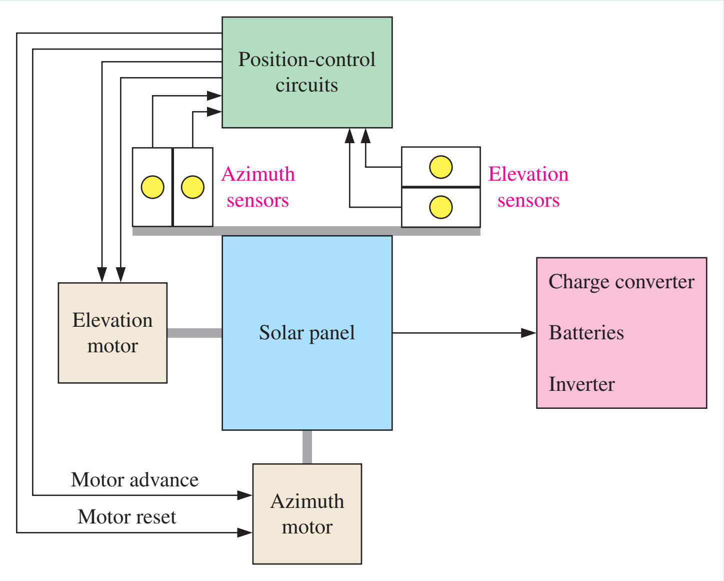


FIGURE GA4–4

Block diagram of a dual-axis sensor-controlled tracking solar power system.

A drawback of the sensor-controlled system is its sensitivity requirement for cloudy days or a passing cloud, when the differences in detected light are much smaller. The system must be able to distinguish between two low-light levels. Also, a certain amount of energy must be diverted to power the electronics and motors, although this is a requirement of most types of tracking systems.

Timer-Controlled Solar Tracking

Solar tracking can also be accomplished by using an electronic timer that causes the motors to move incrementally in azimuth and elevation. During the day the sun moves from east-to-west and this takes approximately 12 hours at summer solstice. The sun moves at a rate of approximately 15° per hour. A timer-controlled tracking system can be designed to follow the sun at desired increments. For example, the panel azimuth position could advance every minute (60 times an hour), every 5 minutes (12 times an hour), or every 15 minutes (4 times an hour), depending on the tracking accuracy desired.

The sun moves slowly in elevation as it progresses from winter solstice to summer solstice and back again, traversing an angle of 47° in six months. This is a rate of 8° per month. The tracking system could make one adjustment in the elevation or tilt of the solar panel each week or each month, depending on the accuracy desired.

Generally, a timer-controlled tracker uses an accurate time source, such as a crystal oscillator, a microprocessor with associated timing and control circuits, and motor interface circuits. The advantage of this type of tracking is that it is independent of the amount of sunlight that is striking the solar panel. Like the sensor-controlled system, the electronics and motors use extra energy. A simple block diagram is shown in Figure GA4–5.

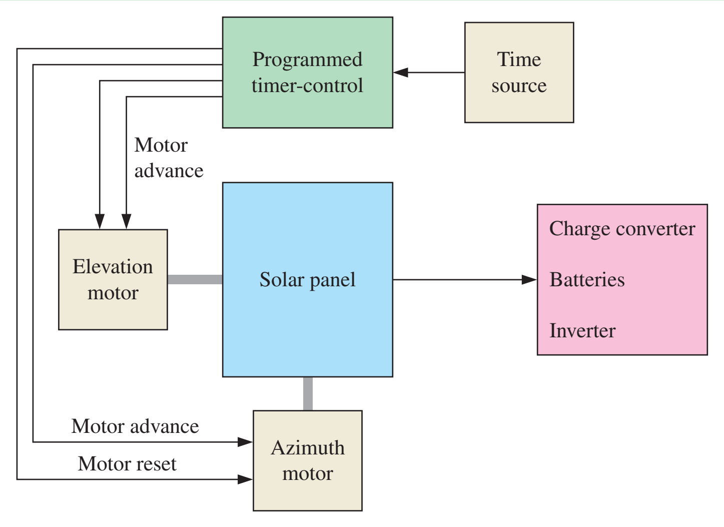


FIGURE GA4–5

Block diagram of a dual-axis timer-controlled tracking solar power system.

Questions

Some questions may require research beyond the content of this coverage. Answers can be found at www.pearsonhighered.com/floyd.

1. What are two types of solar trackers in terms of the way they move?
2. What is the difference between azimuth and elevation?
3. On what date does the winter solstice occur?
4. On what date does the summer solstice occur?
5. Would you recommend a single-axis or a dual-axis tracker for a flat-panel collector? Why?

The following recommended websites are for viewing solar tracking in action. Many other websites are also available.

http://www.youtube.com/watch?v=L4zwQbWrW-A

http://www.youtube.com/watch?v=jdPTyPIwap0

http://www.youtube.com/watch?v=jG942sw31mI

http://www.youtube.com/watch?v=Uzm5LWeTomY

http://www.youtube.com/watch?v=HrnlfiG6KTI

http://www.youtube.com/watch?v=sRqmTpozPYA

http://www.youtube.com/watch?v=E9r1UScgGnE

5

Transistor Bias Circuits

CHAPTER OUTLINE

5–1 The DC Operating Point
5–2 Voltage-Divider Bias
5–3 Other Bias Methods
5–4 Troubleshooting
Application Activity
GreenTech Application 5: *Wind Power*

CHAPTER OBJECTIVES

- Discuss and determine the dc operating point of a linear amplifier
- Analyze a voltage-divider biased circuit
- Analyze an emitter bias circuit, a base bias circuit, an emitter-feedback bias circuit, and a collector-feedback bias circuit
- Troubleshoot faults in transistor bias circuits

KEY TERMS

- Q-point
- DC load line
- Linear region
- Stiff voltage divider
- Feedback

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

As you learned in Chapter 4, a transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish fixed dc values for the transistor currents and voltages called the *dc operating point* or *quiescent point* (*Q-point*). In this chapter, several types of bias circuits are discussed. This material lays the groundwork for the study of amplifiers, and other circuits that require proper biasing.

APPLICATION ACTIVITY PREVIEW

The Application Activity focuses on a system for controlling temperature in an industrial chemical process. You will be dealing with a circuit that converts a temperature measurement to a proportional voltage that is used to adjust the temperature of a liquid in a storage tank. The first step is to learn all you can about transistor operation. You will then apply your knowledge to the Application Activity at the end of the chapter.

5–1 THE DC OPERATING POINT

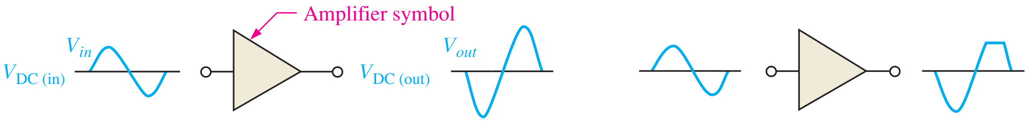
A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. As you learned in Chapter 4, when you bias a transistor, you establish the dc voltage and current values. This means, for example, that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point).

After completing this section, you should be able to

- ☐ **Discuss and determine the dc operating point of a linear amplifier**
- ☐ Explain the purpose of dc bias
  - ◆ Define *Q-point* and describe how it affects the output of an amplifier
  - ◆ Explain how collector characteristic curves are produced ◆ Describe and draw a dc load line ◆ State the conditions for linear operation ◆ Explain what causes waveform distortion

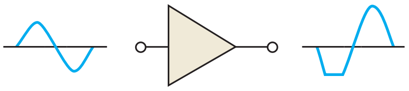
DC Bias

Bias establishes the dc operating point (**Q-point**) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper dc biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of phase with the input. The output signal swings equally above and below the dc bias level of the output, $V_{DC(out)}$. Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.



(a) Linear operation: larger output has same shape as input except that it is inverted

(b) Nonlinear operation: output voltage limited (clipped) by cutoff

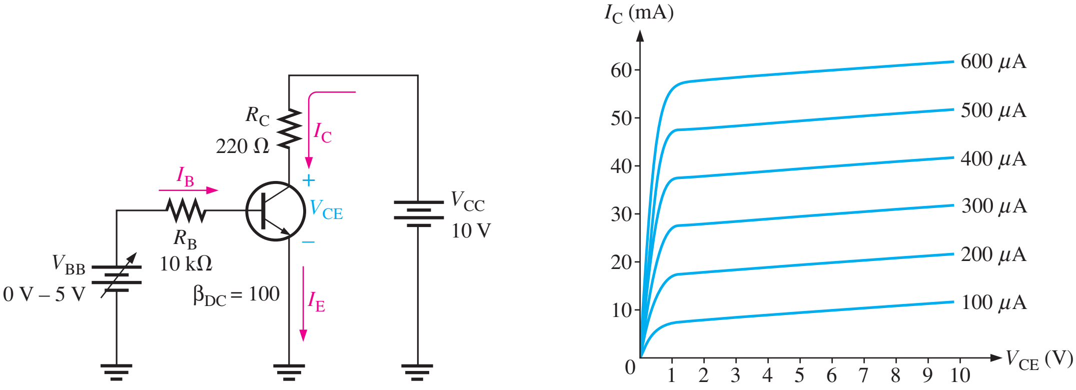


(c) Nonlinear operation: output voltage limited (clipped) by saturation

▲ FIGURE 5–1

Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Graphical Analysis The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.



(a) DC biased circuit

(b) Collector characteristic curves

▲ **FIGURE 5–2**

A dc-biased transistor circuit with variable bias voltage (V_{BB}) for generating the collector characteristic curves shown in part (b).

F Y I

In 1965, a single transistor cost more than a dollar. By 1975, the cost of a transistor had dropped to less than a penny, while transistor size allowed for almost 100,000 transistors on a single chip. From 1979 to 1999, processor performance went from about 1.5 million instructions per second (MIPS) to over 1,000 MIPS. Today's processors, some topping out at well above one billion transistors, run at 3.2 GHz and higher, deliver over 10,000 MIPS, and can be manufactured in high volumes with transistors that cost less than 1/10,000th of a cent.

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

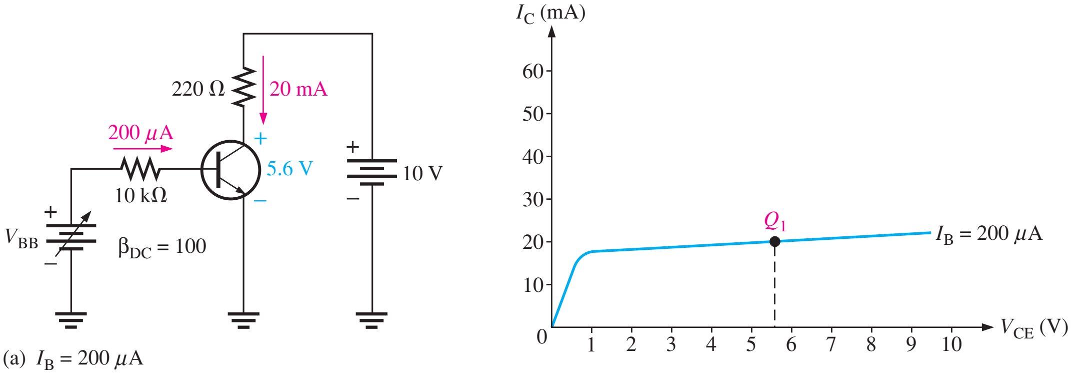
Q_3 is the corresponding Q-point on the graph.

DC Load Line The dc operation of a transistor circuit can be described graphically using a **dc load line**. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the *y*-axis to the cutoff value where $V_{CE} = V_{CC}$ on the *x*-axis, as shown in Figure 5–4(a). The load line is determined by the external circuit (V_{CC} and R_C), not the transistor itself, which is described by the characteristic curves.

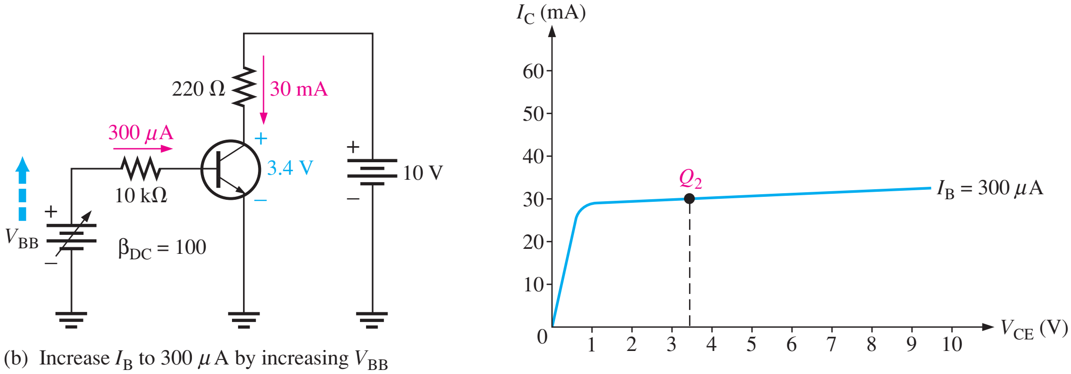
In Figure 5–3, the equation for I_C is

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

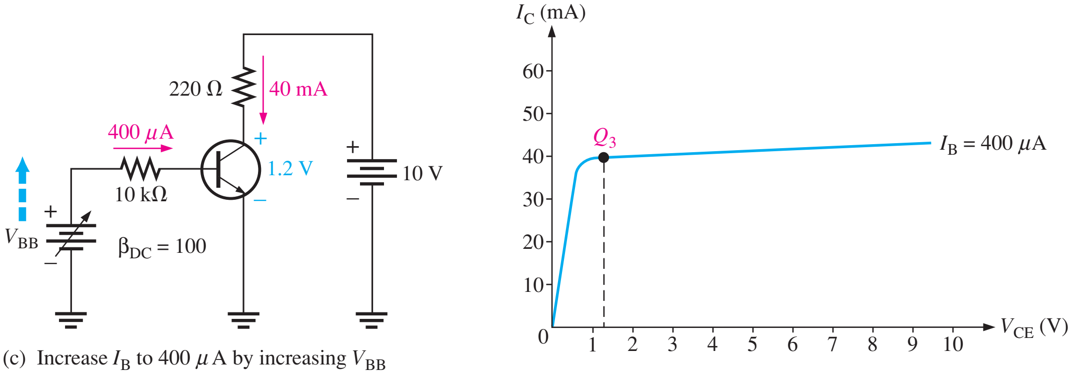
This is the equation of a straight line with a slope of $-1/R_C$, an *x* intercept of $V_{CE} = V_{CC}$, and a *y* intercept of V_{CC}/R_C, which is $I_{C(sat)}$.


220 Ω
20 mA
200 μA
+
5.6 V
−
10 kΩ
+
10 V
−
V_{BB}
$\beta_{DC} = 100$
I_C (mA)
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
Q_1
$I_B = 200\ \mu A$
V_{CE} (V)

(a) $I_B = 200\ \mu A$


220 Ω
30 mA
300 μA
+
3.4 V
−
10 kΩ
+
10 V
−
V_{BB}
$\beta_{DC} = 100$
I_C (mA)
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
Q_2
$I_B = 300\ \mu A$
V_{CE} (V)

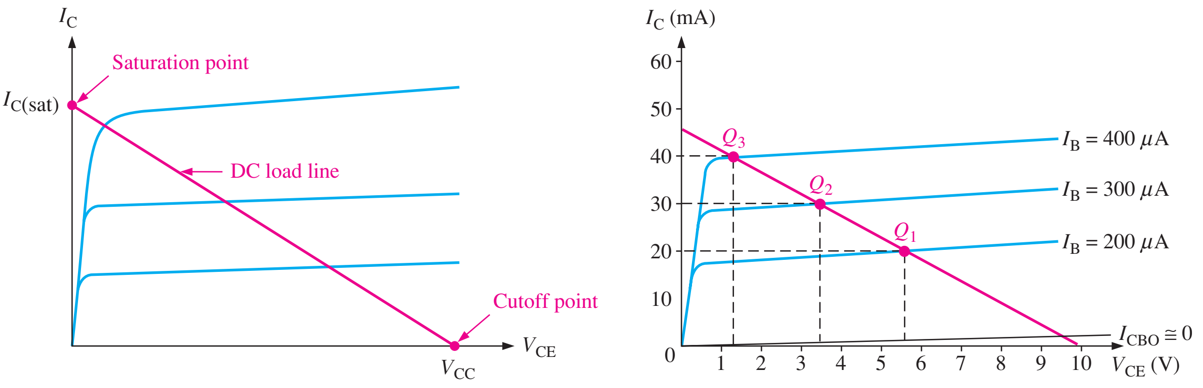
(b) Increase I_B to 300 μA by increasing V_{BB}


220 Ω
40 mA
400 μA
+
1.2 V
−
10 kΩ
+
10 V
−
V_{BB}
$\beta_{DC} = 100$
I_C (mA)
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
Q_3
$I_B = 400\ \mu A$
V_{CE} (V)

(c) Increase I_B to 400 μA by increasing V_{BB}

▲ **FIGURE 5–3**

Illustration of Q-point adjustment.



(a)

(b)

▲ **FIGURE 5–4**

The dc load line.

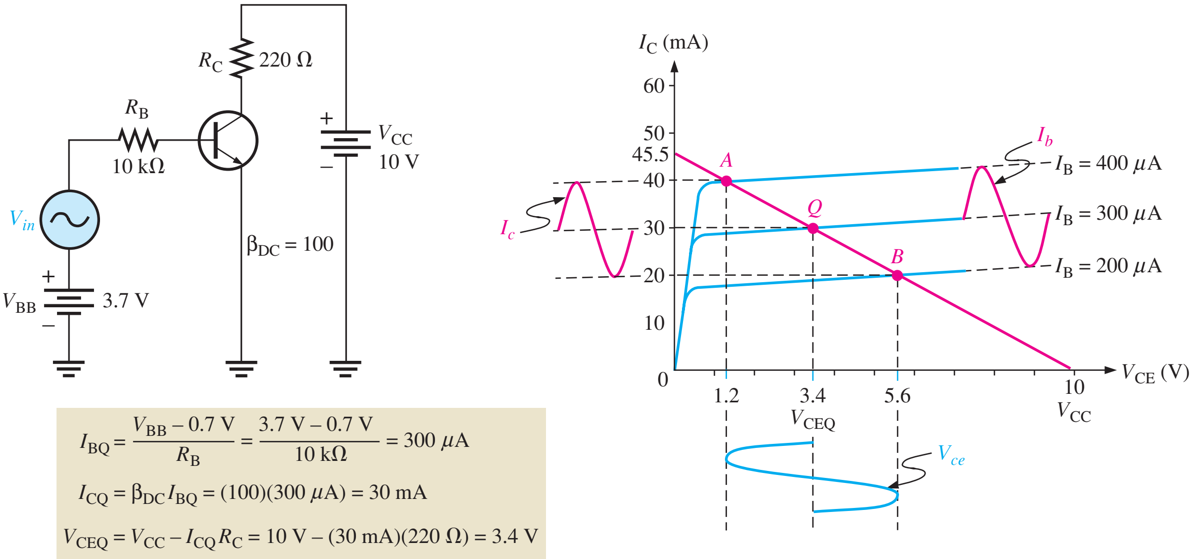
FYI

Gordon Moore, one of the founders of Intel, observed in an article in the April, 1965, issue of *Electronics* magazine that innovations in technology would allow a doubling of the number of transistors in a given space every year (in an update article in 1975, Moore adjusted the rate to every two years to account for the growing complexity of chips), and that the speed of those transistors would increase. This prediction has become widely known as Moore's law.

The point at which the load line intersects a characteristic curve represents the Q-point for that particular value of I_B. Figure 5–4(b) illustrates the Q-point on the load line for each value of I_B in Figure 5–3.

Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

Figure 5–5 shows an example of the linear operation of a transistor. AC quantities are indicated by lowercase italic subscripts. Assume a sinusoidal voltage, V_{in}, is superimposed on V_{BB}, causing the base current to vary sinusoidally 100 μA above and below its Q-point value of 300 μA. This, in turn, causes the collector current to vary 10 mA above and below its Q-point value of 30 mA. As a result of the variation in collector current, the collector-to-emitter voltage varies 2.2 V above and below its Q-point value of 3.4 V. Point *A* on the load line in Figure 5–5 corresponds to the positive peak of the sinusoidal input voltage. Point *B* corresponds to the negative peak, and point *Q* corresponds to the zero value of the sine wave, as indicated. V_{CEQ}, I_{CQ}, and I_{BQ} are dc Q-point values with no input sinusoidal voltage applied.



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

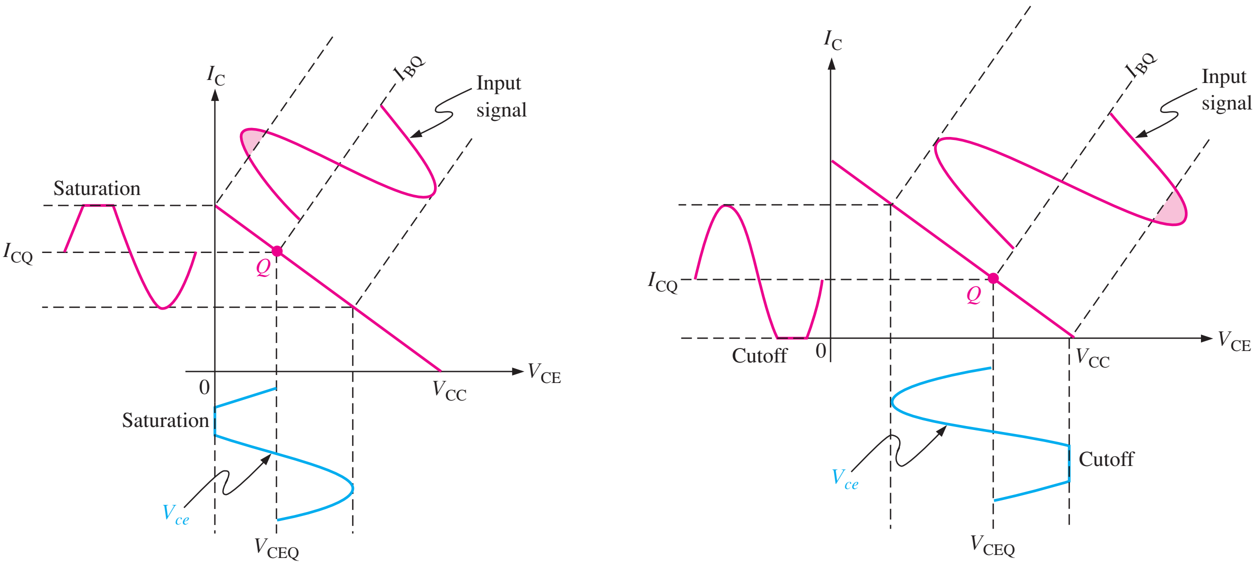
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$

▲ FIGURE 5–5

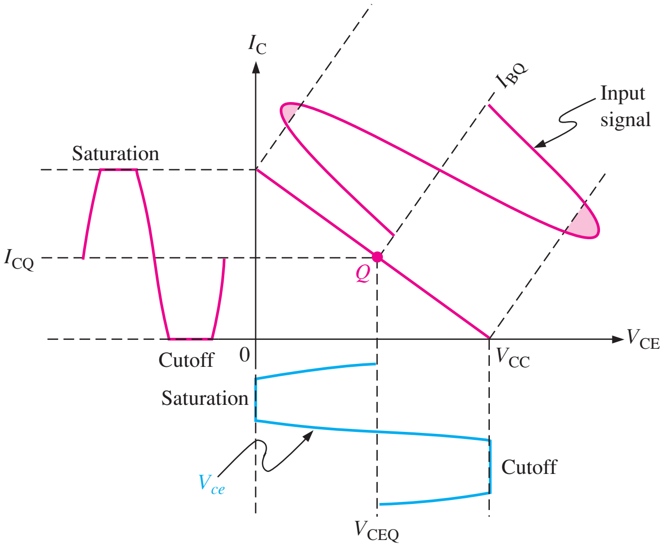
Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.

Waveform Distortion As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the V_{ce} waveform to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6. In each case the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle. When both peaks are limited as in Figure 5–6(c), the transistor is being driven into both saturation and cutoff by an excessively large input signal. When only the positive peak is limited, the transistor is being driven into cutoff but not saturation. When only the negative peak is limited, the transistor is being driven into saturation but not cutoff.


I_C
I_{BQ}
Input signal
Saturation
I_{CQ}
Q
0
V_{CE}
V_{CC}
Saturation
V_{ce}
V_{CEQ}
I_C
I_{BQ}
Input signal
I_{CQ}
Q
Cutoff
0
V_{CE}
V_{CC}
Cutoff
V_{ce}
V_{CEQ}

(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.


I_C
I_{BQ}
Input signal
Saturation
I_{CQ}
Q
Cutoff
0
V_{CE}
V_{CC}
Saturation
Cutoff
V_{ce}
V_{CEQ}

(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

▲ FIGURE 5–6

Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

EXAMPLE 5–1

Determine the Q-point for the circuit in Figure 5–7 and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

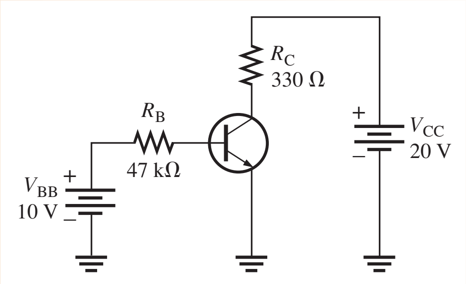
Solution The Q-point is defined by the values of I_C and V_{CE}.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = \mathbf{39.6\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\ V}$$

▶ FIGURE 5–7



The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

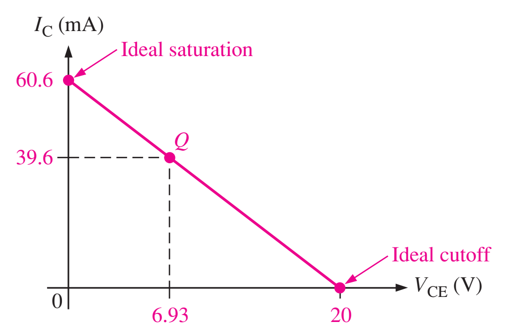
$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21.0\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff.* The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

▶ FIGURE 5–8



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$

*Related Problem** Find the Q-point for the circuit in Figure 5–7, and determine the maximum peak value of base current for linear operation for the following circuit values: $\beta_{DC} = 100$, $R_C = 1.0$ kΩ, and $V_{CC} = 24$ V.

***Answers can be found at www.pearsonhighered.com/floyd.**

Open the Multisim file E05-01 in the Examples folder on the companion website. Measure I_C and V_{CE} and compare with the calculated values.

SECTION 5–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. What are the upper and lower limits on a dc load line in terms of V_{CE} and I_C?
2. Define *Q-point.*
3. At what point on the load line does saturation occur? At what point does cutoff occur?
4. For maximum V_{ce}, where should the Q-point be placed?

5–2 VOLTAGE-DIVIDER BIAS

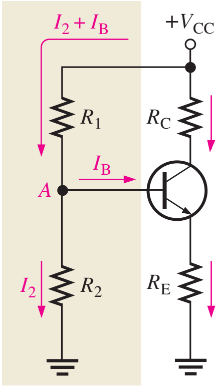
You will now study a method of biasing a transistor for linear operation using a single-source resistive voltage divider. This is the most widely used biasing method. Four other methods are covered in Section 5–3.

After completing this section, you should be able to

- ❑ **Analyze a voltage-divider biased circuit**
  - ◆ Define the term *stiff voltage-divider* ◆ Calculate currents and voltages in a voltage-divider biased circuit
- ❑ Explain the loading effects in voltage-divider bias
  - ◆ Describe how dc input resistance at the transistor base affects the bias
- ❑ Apply Thevenin's theorem to the analysis of voltage-divider bias
  - ◆ Analyze both *npn* and *pnp* circuits

Up to this point a separate dc source, V_{BB}, was used to bias the base-emitter junction because it could be varied independently of V_{CC} and it helped to illustrate transistor operation. A more practical bias method is to use V_{CC} as the single bias source, as shown in Figure 5–9. To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (V_{CC}) as shown.

A dc bias voltage at the base of the transistor can be developed by a resistive voltage-divider that consists of R_1 and R_2, as shown in Figure 5–9. V_{CC} is the dc collector supply voltage. Two current paths are between point *A* and ground: one through R_2 and the other through the base-emitter junction of the transistor and R_E.



▲ FIGURE 5–9

Voltage-divider bias.

Generally, voltage-divider bias circuits are designed so that the base current is much smaller than the current (I_2) through R_2 in Figure 5–9. In this case, the voltage-divider circuit is very straightforward to analyze because the loading effect of the base current can be ignored. A voltage divider in which the base current is small compared to the current in R_2 is said to be a **stiff voltage divider** because the base voltage is relatively independent of different transistors and temperature effects.

To analyze a voltage-divider circuit in which I_B is small compared to I_2, first calculate the voltage on the base using the unloaded voltage-divider rule:

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

Equation 5–1

Once you know the base voltage, you can find the voltages and currents in the circuit, as follows:

$$V_E = V_B - V_{BE}$$

Equation 5–2

and

$$I_C \cong I_E = \frac{V_E}{R_E}$$

Equation 5–3

Then,

$$V_C = V_{CC} - I_C R_C$$

Equation 5–4

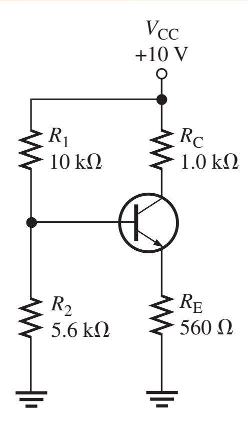
Once you know V_C and V_E, you can determine V_{CE}.

$$V_{CE} = V_C - V_E$$

EXAMPLE 5–2

Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of Figure 5–10 if $\beta_{DC} = 100$.

▶ FIGURE 5–10



Solution The base voltage is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{5.6\text{ k}\Omega}{15.6\text{ k}\Omega}\right)10\text{ V} = 3.59\text{ V}$$

So,

$$V_E = V_B - V_{BE} = 3.59\text{ V} - 0.7\text{ V} = 2.89\text{ V}$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89\text{ V}}{560\ \Omega} = 5.16\text{ mA}$$

Therefore,

$$I_C \cong I_E = \mathbf{5.16\text{ mA}}$$

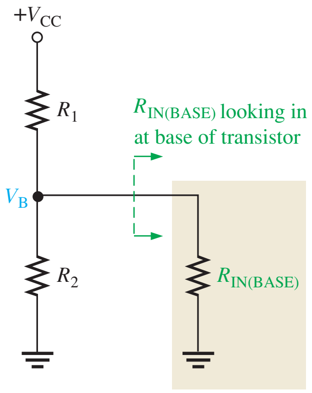
and

$$V_C = V_{CC} - I_C R_C = 10\text{ V} - (5.16\text{ mA})(1.0\text{ k}\Omega) = 4.84\text{ V}$$
$$V_{CE} = V_C - V_E = 4.84\text{ V} - 2.89\text{ V} = \mathbf{1.95\text{ V}}$$

Related Problem If the voltage divider in Figure 5–10 was not stiff, how would V_B be affected?

Open the Multisim file E05-02 in the Examples folder on the companion website. Measure I_C and V_{CE}. If these results do not agree very closely with those in the Example, what original assumption was incorrect?

The basic analysis developed in Example 5–2 is all that is needed for most voltage-divider circuits, but there may be cases where you need to analyze the circuit with more accuracy. Ideally, a voltage-divider circuit is stiff, which means that the transistor does not appear as a significant load. All circuit design involves trade-offs; and one trade-off is that stiff voltage dividers require smaller resistors, which are not always desirable because of potential loading effects on other circuits and added power requirements. If the circuit designer wanted to raise the input resistance, the divider string may not be stiff; and more detailed analysis is required to calculate circuit parameters. To determine if the divider is stiff, you need to examine the dc input resistance looking in at the base as shown in Figure 5–11.



Stiff:

$$R_{IN(BASE)} \geqq 10R_2$$

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

Not stiff:

$$R_{IN(BASE)} < 10R_2$$

$$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}}\right)V_{CC}$$

◀ **FIGURE 5–11**

Voltage divider with load.

Loading Effects of Voltage-Divider Bias

DC Input Resistance at the Transistor Base The dc input resistance of the transistor is proportional to β_{DC}, so it will change for different transistors. When a transistor is operating in its linear region, the emitter current (I_E) is $\beta_{DC}I_B$. When the emitter resistor is viewed from the base circuit, the resistor appears to be larger than its actual value because of the dc current gain in the transistor. That is, $R_{IN(BASE)} = V_B/I_B = V_B/(I_E/\beta_{DC})$.

$$\boldsymbol{R_{IN(BASE)} = \frac{\beta_{DC}V_B}{I_E}}$$

Equation 5–5

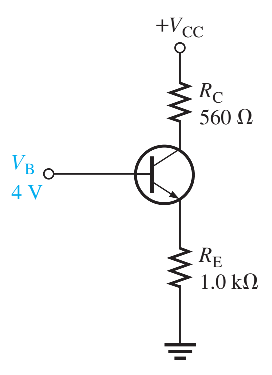
This is the effective load on the voltage divider illustrated in Figure 5–11.

You can quickly estimate the loading effect by comparing $R_{IN(BASE)}$ to the resistor R_2 in the voltage divider. As long as $R_{IN(BASE)}$ is at least ten times larger than R_2, the loading effect will be 10% or less and the voltage divider is stiff. If $R_{IN(BASE)}$ is less than ten times R_2, it should be combined in parallel with R_2.

EXAMPLE 5–3

Determine the dc input resistance looking in at the base of the transistor in Figure 5–12. $\beta_{DC} = 125$ and $V_B = 4$ V.

▶ **FIGURE 5–12**



Solution

$$I_E = \frac{V_B - 0.7\text{ V}}{R_E} = \frac{3.3\text{ V}}{1.0\text{ k}\Omega} = 3.3\text{ mA}$$

$$R_{IN(BASE)} = \frac{\beta_{DC}V_B}{I_E} = \frac{125(4\text{ V})}{3.3\text{ mA}} = \mathbf{152\text{ k}\Omega}$$

Related Problem What is $R_{IN(BASE)}$ in Figure 5–12 if $\beta_{DC} = 60$ and $V_B = 2$ V?

Thevenin's Theorem Applied to Voltage-Divider Bias

To analyze a voltage-divider biased transistor circuit for base current loading effects, we will apply Thevenin's theorem to evaluate the circuit. First, let's get an equivalent base-emitter circuit for the circuit in Figure 5–13(a) using Thevenin's theorem. Looking out from the base terminal, the bias circuit can be redrawn as shown in Figure 5–13(b). Apply Thevenin's theorem to the circuit left of point A, with V_{CC} replaced by a short to ground and the transistor disconnected from the circuit. The voltage at point A with respect to ground is

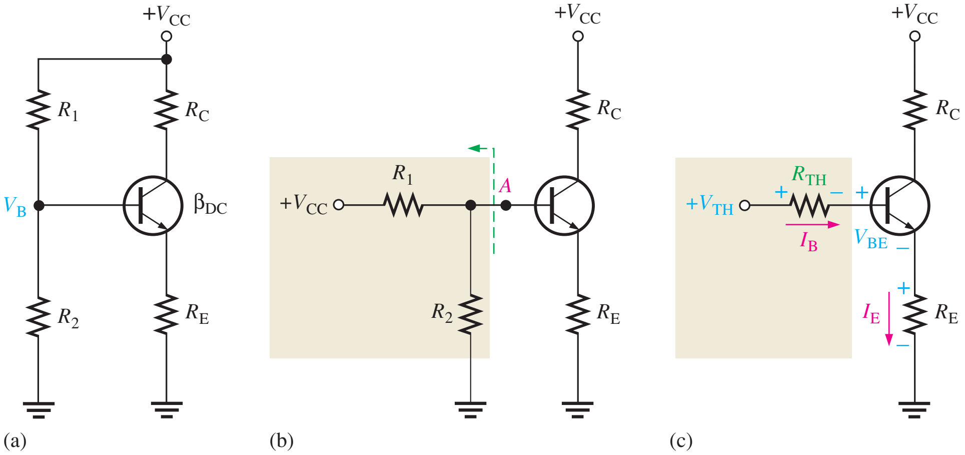
$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

and the resistance is

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

▶ **FIGURE 5–13**

Thevenizing the bias circuit.



The Thevenin equivalent of the bias circuit, connected to the transistor base, is shown in the beige box in Figure 5–13(c). Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

Substituting, using Ohm's law, and solving for V_{TH},

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting I_E/β_{DC} for I_B,

$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E,

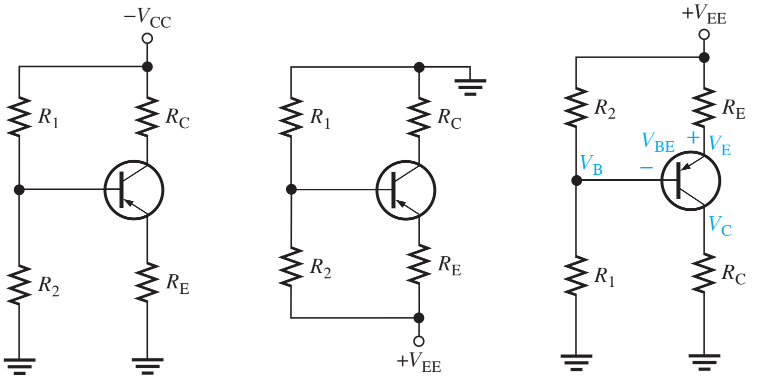
Equation 5–6

$$\boldsymbol{I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}}$$

If R_{TH}/β_{DC} is small compared to R_E, the result is the same as for an unloaded voltage divider.

Voltage-divider bias is widely used because reasonably good bias stability is achieved with a single supply voltage.

Voltage-Divider Biased PNP Transistor As you know, a *pnp* transistor requires bias polarities opposite to the *npn.* This can be accomplished with a negative collector supply voltage, as in Figure 5–14(a), or with a positive emitter supply voltage, as in Figure 5–14(b).



(a) Negative collector supply voltage, V_{CC}

(b) Positive emitter supply voltage, V_{EE}

(c) The circuit in (b) redrawn

▲ FIGURE 5–14

Voltage-divider biased *pnp* transistor.

In a schematic, the *pnp* is often drawn upside down so that the supply voltage is at the top of the schematic and ground at the bottom, as in Figure 5–14(c).

The analysis procedure is the same as for an *npn* transistor circuit using Thevenin's theorem and Kirchhoff's voltage law, as demonstrated in the following steps with reference to Figure 5–14. For Figure 5–14(a), applying Kirchhoff's voltage law around the base-emitter circuit gives

$$V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E = 0$$

By Thevenin's theorem,

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

The base current is

$$I_B = \frac{I_E}{\beta_{DC}}$$

The equation for I_E is

$$\boldsymbol{I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}}$$ Equation 5–7

For Figure 5–14(b), the analysis is as follows:

$$-V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E - V_{EE} = 0$$

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_{EE}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_B = \frac{I_E}{\beta_{DC}}$$

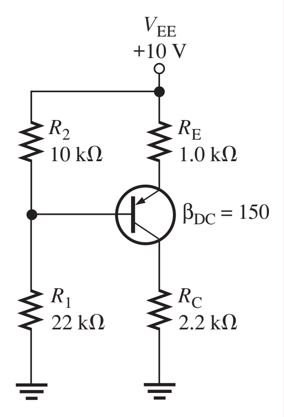
The equation for I_E is

$$\boldsymbol{I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}}$$ Equation 5–8

EXAMPLE 5–4

Find I_C and V_{EC} for the *pnp* transistor circuit in Figure 5–15.

▶ FIGURE 5–15



Solution This circuit has the configuration of Figures 5–14(b) and (c). Apply Thevenin's theorem.

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_{EE} = \left(\frac{22\text{ k}\Omega}{22\text{ k}\Omega + 10\text{ k}\Omega}\right)10\text{ V} = (0.688)10\text{ V} = 6.88\text{ V}$$

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(22\text{ k}\Omega)(10\text{ k}\Omega)}{22\text{ k}\Omega + 10\text{ k}\Omega} = 6.88\text{ k}\Omega$$

Use Equation 5–8 to determine I_E.

$$I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}} = \frac{6.88\text{ V} + 0.7\text{ V} - 10\text{ V}}{1.0\text{ k}\Omega + 45.9\ \Omega} = \frac{-2.42\text{ V}}{1.0459\text{ k}\Omega} = -2.31\text{ mA}$$

The negative sign on I_E indicates that the assumed current direction in the Kirchhoff's analysis is opposite from the actual current direction. From I_E, you can determine I_C and V_{EC} as follows:

$$I_C = I_E = \mathbf{2.31\ mA}$$

$$V_C = I_CR_C = (2.31\text{ mA})(2.2\text{ k}\Omega) = 5.08\text{ V}$$

$$V_E = V_{EE} - I_ER_E = 10\text{ V} - (2.31\text{ mA})(1.0\text{ k}\Omega) = 7.68\text{ V}$$

$$V_{EC} = V_E - V_C = 7.68\text{ V} - 5.08\text{ V} = \mathbf{2.6\ V}$$

Related Problem Determine $R_{IN(BASE)}$ for Figure 5–15.

Open the Multisim file E05-04 in the Examples folder on the companion website. Measure I_C and V_{EC}.

EXAMPLE 5–5

Find I_C and V_{CE} for a *pnp* transistor circuit with these values: $R_1 = 68\text{ k}\Omega$, $R_2 = 47\text{ k}\Omega$, $R_C = 1.8\text{ k}\Omega$, $R_E = 2.2\text{ k}\Omega$, $V_{CC} = -6\text{ V}$, and $\beta_{DC} = 75$. Refer to Figure 5–14(a), which shows the schematic with a negative supply voltage.

Solution Apply Thevenin's theorem.

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{47\text{ k}\Omega}{68\text{ k}\Omega + 47\text{ k}\Omega}\right)(-6\text{ V})$$
$$= (0.409)(-6\text{ V}) = -2.45\text{ V}$$

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(68\text{ k}\Omega)(47\text{ k}\Omega)}{(68\text{ k}\Omega + 47\text{ k}\Omega)} = 27.8\text{ k}\Omega$$

Use Equation 5–7 to determine I_E.

$$I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{2.45\text{ V} + 0.7\text{ V}}{2.2\text{ k}\Omega + 371\ \Omega}$$

$$= \frac{3.15\text{ V}}{2.57\text{ k}\Omega} = 1.23\text{ mA}$$

From I_E, you can determine I_C and V_{CE} as follows:

$$I_C \cong I_E = \mathbf{1.23\text{ mA}}$$

$$V_C = -V_{CC} + I_CR_C = -6\text{ V} + (1.23\text{ mA})(1.8\text{ k}\Omega) = -3.79\text{ V}$$

$$V_E = -I_ER_E = -(1.23\text{ mA})(2.2\text{ k}\Omega) = -2.71\text{ V}$$

$$V_{CE} = V_C - V_E = -3.79\text{ V} + 2.71\text{ V} = \mathbf{-1.08\text{ V}}$$

Related Problem What value of β_{DC} is required in this example in order to neglect $R_{IN(BASE)}$ in keeping with the basic ten-times rule for a stiff voltage divider?

SECTION 5–2 CHECKUP

1. If the voltage at the base of a transistor is 5 V and the base current is 5 μA, what is the dc input resistance at the base?
2. If a transistor has a dc beta of 190, $V_B = 2$ V, and $I_E = 2$ mA, what is the dc input resistance at the base?
3. What bias voltage is developed at the base of a transistor if both resistors in a stiff voltage divider are equal and $V_{CC} = +10$ V?
4. What are two advantages of voltage-divider bias?

5–3 OTHER BIAS METHODS

In this section, four additional methods for dc biasing a transistor circuit are discussed. Although these methods are not as common as voltage-divider bias, you should be able to recognize them when you see them and understand the basic differences.

After completing this section, you should be able to

- ❑ **Analyze four more types of bias circuits**
- ❑ Discuss emitter bias
  - ◆ Analyze an emitter-biased circuit
- ❑ Discuss base bias
  - ◆ Analyze a base-biased circuit ◆ Explain Q-point stability of base bias
- ❑ Discuss emitter-feedback bias
  - ◆ Define negative feedback ◆ Analyze an emitter-feedback biased circuit
- ❑ Discuss collector-feedback bias
  - ◆ Analyze a collector-feedback biased circuit ◆ Discuss Q-point stability over temperature

Emitter Bias

Emitter bias provides excellent bias stability in spite of changes in β or temperature. It uses both a positive and a negative supply voltage. To obtain a reasonable estimate of the key dc values in an emitter-biased circuit, analysis is quite easy. In an *npn* circuit, such as shown in Figure 5–17, the small base current causes the base voltage to be slightly below ground. The emitter voltage is one diode drop less than this. The combination of this small drop across R_B and V_{BE} forces the emitter to be at approximately -1 V. Using this approximation, you can obtain the emitter current as

$$I_E = \frac{-V_{EE} - 1\text{ V}}{R_E}$$

V_{EE} is entered as a negative value in this equation.

You can apply the approximation that $I_C \cong I_E$ to calculate the collector voltage.

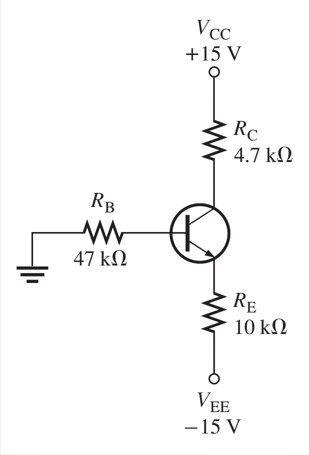
$$V_C = V_{CC} - I_C R_C$$

The approximation that $V_E \cong -1$ V is useful for troubleshooting because you won't need to perform any detailed calculations. As in the case of voltage-divider bias, there is a more rigorous calculation for cases where you need a more exact result.

EXAMPLE 5–6

Calculate I_E and V_{CE} for the circuit in Figure 5–16 using the approximations $V_E \cong -1$ V and $I_C \cong I_E$.

▶ FIGURE 5–16



Solution

$$V_E \cong -1\text{ V}$$

$$I_E = \frac{-V_{EE} - 1\text{ V}}{R_E} = \frac{-(-15\text{ V}) - 1\text{ V}}{10\text{ k}\Omega} = \frac{14\text{ V}}{10\text{ k}\Omega} = \mathbf{1.4\text{ mA}}$$

$$V_C = V_{CC} - I_C R_C = +15\text{ V} - (1.4\text{ mA})(4.7\text{ k}\Omega) = 8.4\text{ V}$$

$$V_{CE} = 8.4\text{ V} - (-1) = \mathbf{9.4\text{ V}}$$

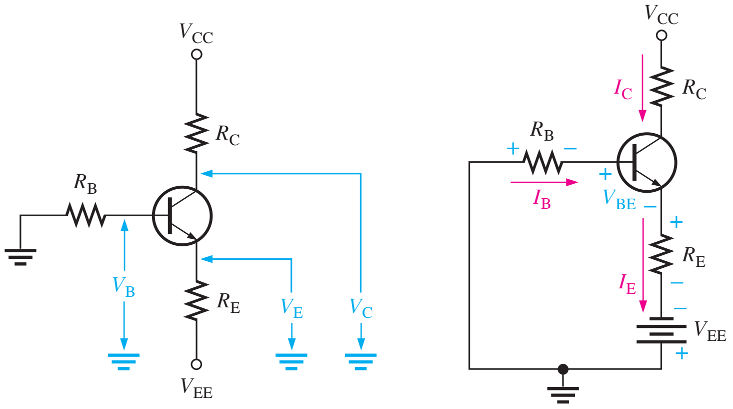
Related Problem If V_{EE} is changed to -12 V, what is the new value of V_{CE}?

The approximation that $V_E \cong -1$ V and the neglect of β_{DC} may not be accurate enough for design work or detailed analysis. In this case, Kirchhoff's voltage law can be applied as follows to develop a more detailed formula for I_E. Kirchhoff's voltage law applied around the base-emitter circuit in Figure 5–17(a), which has been redrawn in part (b) for analysis, gives the following equation:

$$V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0$$

Substituting, using Ohm's law,

$$V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0$$



(a) (b)

FIGURE 5–17

An *npn* transistor with emitter bias. Polarities are reversed for a *pnp* transistor. Single subscripts indicate voltages with respect to ground.

Substituting for $I_B \cong I_E/\beta_{DC}$ and transposing V_{EE},

$$\left(\frac{I_E}{\beta_{DC}}\right)R_B + I_E R_E + V_{BE} = -V_{EE}$$

Factoring out I_E and solving for I_E,

$$\boldsymbol{I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}}$$

Equation 5–9

Voltages with respect to ground are indicated by a single subscript. The emitter voltage with respect to ground is

$$V_E = V_{EE} + I_E R_E$$

The base voltage with respect to ground is

$$V_B = V_E + V_{BE}$$

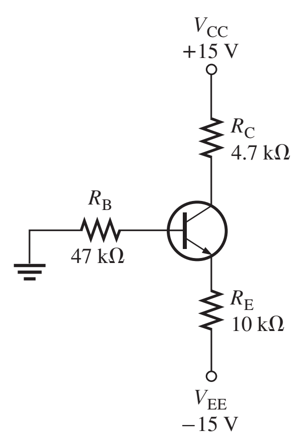
The collector voltage with respect to ground is

$$V_C = V_{CC} - I_C R_C$$

EXAMPLE 5–7

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–18 will change if β_{DC} increases from 100 to 200 when one transistor is replaced by another.

FIGURE 5–18



Solution For $\beta_{DC} = 100$,

$$I_{C(1)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/100} = 1.37\text{ mA}$$

$$V_C = V_{CC} - I_{C(1)}R_C = 15\text{ V} - (1.37\text{ mA})(4.7\text{ k}\Omega) = 8.56\text{ V}$$

$$V_E = V_{EE} + I_ER_E = -15\text{ V} + (1.37\text{ mA})(10\text{ k}\Omega) = -1.3\text{ V}$$

Therefore,

$$V_{CE(1)} = V_C - V_E = 8.56\text{ V} - (-1.3\text{ V}) = 9.83\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/200} = 1.38\text{ mA}$$

$$V_C = V_{CC} - I_{C(2)}R_C = 15\text{ V} - (1.38\text{ mA})(4.7\text{ k}\Omega) = 8.51\text{ V}$$

$$V_E = V_{EE} + I_ER_E = -15\text{ V} + (1.38\text{ mA})(10\text{ k}\Omega) = -1.2\text{ V}$$

Therefore,

$$V_{CE(2)} = V_C - V_E = 8.51\text{ V} - (-1.2\text{ V}) = 9.71\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\% = \left(\frac{1.38\text{ mA} - 1.37\text{ mA}}{1.37\text{ mA}}\right)100\% = 0.730\%$$

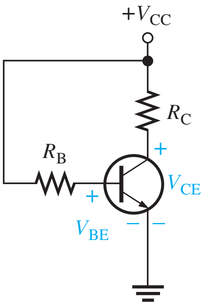
The percent change in V_{CE} is

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\% = \left(\frac{9.71\text{ V} - 9.83\text{ V}}{9.83\text{ V}}\right)100\% = \mathbf{-1.22\%}$$

Related Problem Determine the Q-point in Figure 5–18 if β_{DC} increases to 300.

Base Bias

This method of biasing is common in switching circuits. Figure 5–19 shows a base-biased transistor. The analysis of this circuit for the linear region shows that it is directly dependent on β_{DC}. Starting with Kirchhoff's voltage law around the base circuit,



▲ **FIGURE 5–19**

Base bias.

$$V_{CC} - V_{R_B} - V_{BE} = 0$$

Substituting I_BR_B for V_{R_B}, you get

$$V_{CC} - I_BR_B - V_{BE} = 0$$

Then solving for I_B,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Kirchhoff's voltage law applied around the collector circuit in Figure 5–19 gives the following equation:

$$V_{CC} - I_CR_C - V_{CE} = 0$$

Solving for V_{CE},

Equation 5–10

$$\boldsymbol{V_{CE} = V_{CC} - I_CR_C}$$

Substituting the expression for I_B into the formula $I_C = \beta_{DC}I_B$ yields

Equation 5–11

$$\boldsymbol{I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)}$$

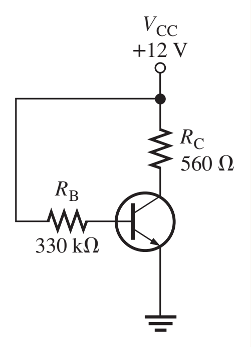
Q-Point Stability of Base Bias Notice that Equation 5–11 shows that I_C is dependent on β_{DC}. The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base bias circuit extremely beta-dependent and unpredictable.

Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of β_{DC} values from one transistor to another of the same type due to manufacturing variations. For these reasons, base bias is rarely used in linear circuits but is discussed here so you will be familiar with it.

EXAMPLE 5–8

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 100 to 200.

▶ FIGURE 5–20



Solution For $\beta_{DC} = 100$,

$$I_{C(1)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 3.42\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}R_C = 12\text{ V} - (3.42\text{ mA})(560\ \Omega) = 10.1\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 200\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 6.84\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}R_C = 12\text{ V} - (6.84\text{ mA})(560\ \Omega) = 8.17\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\%$$

$$= \left(\frac{6.84\text{ mA} - 3.42\text{ mA}}{3.42\text{ mA}}\right)100\% = \mathbf{100\%}\text{ (an increase)}$$

The percent change in V_{CE} is

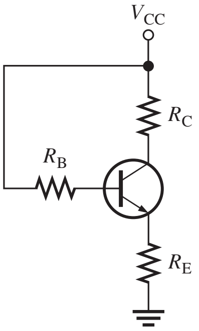
$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\%$$

$$= \left(\frac{8.17\text{ V} - 10.1\text{ V}}{10.1\text{ V}}\right)100\% = \mathbf{-19.1\%}\text{ (a decrease)}$$

As you can see, the Q-point is very dependent on β_{DC} in this circuit and therefore makes the base bias arrangement very unreliable. Consequently, base bias is not normally used if linear operation is required. However, it can be used in switching applications.

Related Problem Determine I_C if β_{DC} increases to 300.

Open the Multisim file E05-08 in the Examples folder on the companion website. Set $\beta_{DC} = 100$ and measure I_C and V_{CE}. Next, set $\beta_{DC} = 200$ and measure I_C and V_{CE}. Compare results with the calculated values.



▲ **FIGURE 5–21**

Emitter-feedback bias.

Emitter-Feedback Bias

If an emitter resistor is added to the base-bias circuit in Figure 5–20, the result is emitter-feedback bias, as shown in Figure 5–21. The idea is to help make base bias more predictable with negative **feedback**, which negates any attempted change in collector current with an opposing change in base voltage. If the collector current tries to increase, the emitter voltage increases, causing an increase in base voltage because $V_B = V_E + V_{BE}$. This increase in base voltage reduces the voltage across R_B, thus reducing the base current and keeping the collector current from increasing. A similar action occurs if the collector current tries to decrease. While this is better for linear circuits than base bias, it is still dependent on β_{DC} and is not as predictable as voltage-divider bias. To calculate I_E, you can write Kirchhoff's voltage law (KVL) around the base circuit.

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Substituting I_E/β_{DC} for I_B, you can see that I_E is still dependent on β_{DC}.

Equation 5–12

$$\mathbf{I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}}}$$

EXAMPLE 5–9

The base-bias circuit from Example 5–8 is converted to emitter-feedback bias by the addition of a 1 kΩ emitter resistor. All other values are the same, and a transistor with a $\beta_{DC} = 100$ is used. Determine how much the Q-point will change if the first transistor is replaced with one having a $\beta_{DC} = 200$. Compare the results to those of the base-bias circuit.

Solution For $\beta_{DC} = 100$,

$$I_{C(1)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/100} = 2.63\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}(R_C + R_E) = 12\text{ V} - (2.63\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 7.90\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/200} = 4.26\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}(R_C + R_E) = 12\text{ V} - (4.26\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 5.35\text{ V}$$

The percent change in I_C is

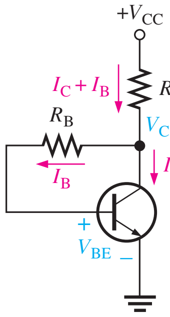
$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\% = \left(\frac{4.26\text{ mA} - 2.63\text{ mA}}{2.63\text{ mA}}\right)100\% = \mathbf{62.0\%}$$

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\% = \left(\frac{7.90\text{ V} - 5.35\text{ V}}{7.90\text{ V}}\right)100\% = \mathbf{-32.3\%}$$

Although the emitter-feedback bias significantly improved the stability of the bias for a change in β_{DC} compared to base bias, it still does not provide a reliable Q-point.

Related Problem Determine I_C if a transistor with $\beta_{DC} = 300$ is used in the circuit.

Collector-Feedback Bias



▲ FIGURE 5–22

Collector-feedback bias.

In Figure 5–22, the base resistor R_B is connected to the collector rather than to V_{CC}, as it was in the base bias arrangement discussed earlier. The collector voltage provides the bias for the base-emitter junction. The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. If I_C tries to increase, it drops more voltage across R_C, thereby causing V_C to decrease. When V_C decreases, there is a decrease in voltage across R_B, which decreases I_B. The decrease in I_B produces less I_C which, in turn, drops less voltage across R_C and thus offsets the decrease in V_C.

Analysis of a Collector-Feedback Bias Circuit By Ohm's law, the base current can be expressed as

$$I_B = \frac{V_C - V_{BE}}{R_B}$$

Let's assume that $I_C \gg I_B$. The collector voltage is

$$V_C \cong V_{CC} - I_C R_C$$

Also,

$$I_B = \frac{I_C}{\beta_{DC}}$$

Substituting for V_C in the equation $I_B = (V_C - V_{BE})/R_B$,

$$\frac{I_C}{\beta_{DC}} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B}$$

The terms can be arranged so that

$$\frac{I_C R_B}{\beta_{DC}} + I_C R_C = V_{CC} - V_{BE}$$

Then you can solve for I_C as follows:

$$I_C\left(R_C + \frac{R_B}{\beta_{DC}}\right) = V_{CC} - V_{BE}$$

$$\boldsymbol{I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}}}$$

Equation 5–13

Since the emitter is ground, $V_{CE} = V_C$.

$$\boldsymbol{V_{CE} = V_{CC} - I_C R_C}$$

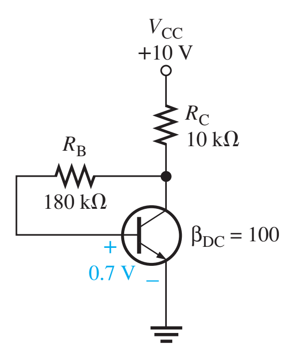
Equation 5–14

Q-Point Stability Over Temperature Equation 5–13 shows that the collector current is dependent to some extent on β_{DC} and V_{BE}. This dependency, of course, can be minimized by making $R_C \gg R_B/\beta_{DC}$ and $V_{CC} \gg V_{BE}$. An important feature of collector-feedback bias is that it essentially eliminates the β_{DC} and V_{BE} dependency even if the stated conditions are met.

As you have learned, β_{DC} varies directly with temperature, and V_{BE} varies inversely with temperature. As the temperature goes up in a collector-feedback circuit, β_{DC} goes up and V_{BE} goes down. The increase in β_{DC} acts to increase I_C. The decrease in V_{BE} acts to increase I_B which, in turn also acts to increase I_C. As I_C tries to increase, the voltage drop across R_C also tries to increase. This tends to reduce the collector voltage and therefore the voltage across R_B, thus reducing I_B and offsetting the attempted increase in I_C and the attempted decrease in V_C. The result is that the collector-feedback circuit maintains a relatively stable Q-point. The reverse action occurs when the temperature decreases.

EXAMPLE 5–10 Calculate the Q-point values (I_C and V_{CE}) for the circuit in Figure 5–23.

▶ FIGURE 5–23



Solution Using Equation 5–13, the collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}} = \frac{10\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega + 180\text{ k}\Omega/100} = \mathbf{788\ \mu A}$$

Using Equation 5–14, the collector-to-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (788\ \mu\text{A})(10\text{ k}\Omega) = \mathbf{2.12\ V}$$

Related Problem Calculate the Q-point values in Figure 5–23 for $\beta_{DC} = 200$ and determine the percent change in the Q-point from $\beta_{DC} = 100$ to $\beta_{DC} = 200$.

Open the Multisim file E05-10 in the Examples folder on the companion website. Measure I_C and V_{CE}. Compare with the calculated values.

SECTION 5–3 CHECKUP

1. Why is emitter bias more stable than base bias?
2. What is the main disadvantage of emitter bias?
3. Explain how an increase in β_{DC} causes a reduction in base current in a collector-feedback circuit.
4. What is the main disadvantage of the base bias method?
5. Explain why the base bias Q-point changes with temperature.
6. How does emitter-feedback bias improve on base bias?

5–4 TROUBLESHOOTING

In a biased transistor circuit, the transistor can fail or a resistor in the bias circuit can fail. We will examine several possibilities in this section using the voltage-divider bias arrangement. Many circuit failures result from open resistors, internally open transistor leads and junctions, or shorted junctions. Often, these failures can produce an apparent cutoff or saturation condition when voltage is measured at the collector.

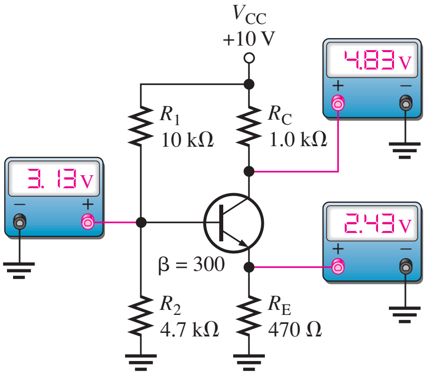
After completing this section, you should be able to

- ❑ **Troubleshoot faults in transistor bias circuits**
- ❑ Troubleshoot a voltage-divider biased transistor circuit
  - ◆ Troubleshoot the circuit for several common faults ◆ Use voltage measurement to isolate a fault

Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

Troubleshooting a Voltage-Divider Biased Transistor

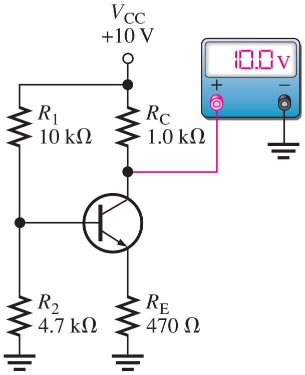
An example of a transistor with voltage-divider bias is shown in Figure 5–24. For the specific component values shown, you should get the voltage readings approximately as indicated when the circuit is operating properly.



◀ FIGURE 5–24

A voltage-divider biased transistor with correct voltages.

For this type of bias circuit, a particular group of faults will cause the transistor collector to be at V_{CC} when measured with respect to ground. Five faults are indicated for the circuit in Figure 5–25(a). The collector voltage is equal to 10 V with respect to ground for each of the faults as indicated in the table in part (b). Also, for each of the faults, the base voltage and the emitter voltage with respect to ground are given.



(a) Faulty circuit

FAULT	DESCRIPTION	V_C	V_E	V_B
1	R_1 open	10 V	0 V	0 V
2	R_E open	10 V	2.50 V	3.20 V
3	Base internally open	10 V	0 V	3.20 V
4	Emitter internally open	10 V	0 V	3.20 V
5	Collector internally open	10 V	0.41 V	1.11 V

(b) Possible faults for circuit in part (a)

▲ FIGURE 5–25

Faults for which $V_C = V_{CC}$.

Fault 1: Resistor R_1 Open This fault removes the bias voltage from the base, thus connecting the base to ground through R_2 and forcing the transistor into cutoff because $V_B = 0$ V and $I_B = 0$ A. The transistor is nonconducting so there is no I_C and, therefore, no voltage drop across R_C. This makes the collector voltage equal to V_{CC} (10 V). Since there is no base current or collector current, there is also no emitter current and $V_E = 0$ V.

Fault 2: Resistor R_E Open This fault prevents base current, emitter current, and collector current except for a very small I_{CBO} that can be neglected. Since $I_C = 0$ A, there is no voltage drop across R_C and, therefore, $V_C = V_{CC} = 10$ V. The voltage divider produces a voltage at the base with respect to ground as follows:

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{4.7\text{ k}\Omega}{14.7\text{ k}\Omega}\right)10\text{ V} = 3.20\text{ V}$$

When a voltmeter is connected to the emitter, it provides a current path through its high internal impedance, resulting in a forward-biased base-emitter junction. Therefore, the emitter voltage is $V_E = V_B - V_{BE}$. The amount of the forward voltage drop across the BE junction depends on the current. $V_{BE} = 0.7$ V is assumed for purposes of illustration, but it may be much less. The result is an emitter voltage as follows:

$$V_E = V_B - V_{BE} = 3.2\text{ V} - 0.7\text{ V} = 2.5\text{ V}$$

Fault 3: Base Internally Open An internal transistor fault is more likely to happen than an open resistor. Again, the transistor is nonconducting so $I_C = 0$ A and $V_C = V_{CC} = 10$ V. Just as for the case of the open R_E, the voltage divider produces 3.2 V at the external base connection. The voltage at the external emitter connection is 0 V because there is no emitter current through R_E and, thus, no voltage drop.

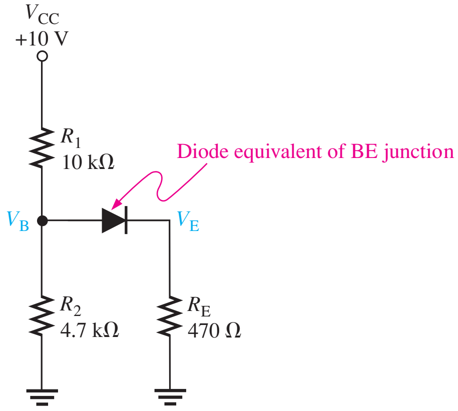
Fault 4: Emitter Internally Open Again, the transistor is nonconducting, so $I_C = 0$ A and $V_C = V_{CC} = 10$ V. Just as for the case of the open R_E and the internally open base, the voltage divider produces 3.2 V at the base. The voltage at the external emitter lead is 0 V because that point is open and connected to ground through R_E. Notice that Faults 3 and 4 produce identical symptoms.

Fault 5: Collector Internally Open Since there is an internal open in the transistor collector, there is no I_C and, therefore, $V_C = V_{CC} = 10$ V. In this situation, the voltage divider is loaded by R_E through the forward-biased BE junction, as shown by the approximate equivalent circuit in Figure 5–26. The base voltage and emitter voltage are determined as follows:

$$\begin{aligned} V_B &\cong \left(\frac{R_2 \| R_E}{R_1 + R_2 \| R_E}\right)V_{CC} + 0.7\text{ V} \\ &= \left(\frac{427\ \Omega}{10.427\text{ k}\Omega}\right)10\text{ V} + 0.7\text{ V} = 0.41\text{ V} + 0.7\text{ V} = 1.11\text{ V} \\ V_E &= V_B - V_{BE} = 1.11\text{ V} - 0.7\text{ V} = 0.41\text{ V}\end{aligned}$$

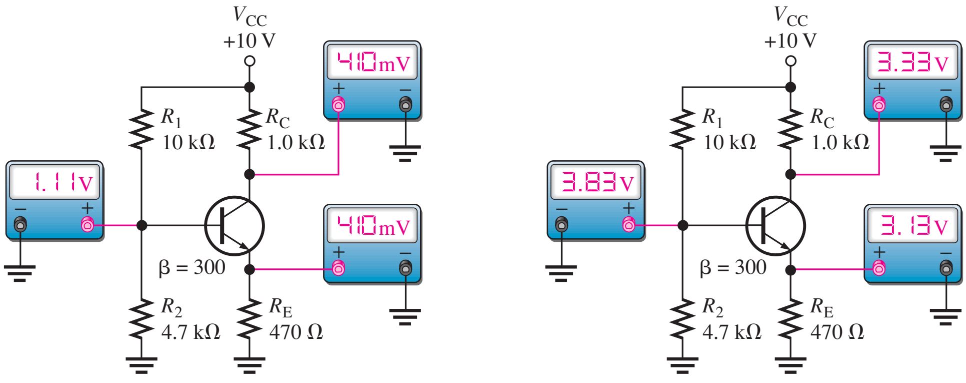
▶ FIGURE 5–26

Equivalent bias circuit for an internally open collector.



There are two possible additional faults for which the transistor is conducting or appears to be conducting, based on the collector voltage measurement. These are indicated in Figure 5–27.

Fault 6: Resistor R_C Open For this fault, which is illustrated in Figure 5–27(a), the collector voltage may lead you to think that the transistor is in saturation, but actually it is



(a) R_C open

(b) R_2 open

FIGURE 5–27

Faults for which the transistor is conducting or appears to be conducting.

nonconducting. Obviously, if R_C is open, there can be no collector current. In this situation, the equivalent bias circuit is the same as for Fault 5, as illustrated in Figure 5–26. Therefore, $V_B = 1.11$ V and since the BE junction is forward-biased,

$$V_E = V_B - V_{BE} = 1.11\text{ V} - 0.7\text{ V} = 0.41\text{ V}$$

When a voltmeter is connected to the collector to measure V_C, a current path is provided through the internal impedance of the meter and the BC junction is forward-biased by V_B. Therefore,

$$V_C = V_B - V_{BC} = 1.11\text{ V} - 0.7\text{ V} = 0.41\text{ V}$$

Again the forward drops across the internal transistor junctions depend on the current. We are using 0.7 V for illustration, but the forward drops may be much less.

Fault 7: Resistor R_2 Open When R_2 opens as shown in Figure 5–27(b), the base voltage and base current increase from their normal values because the voltage divider is now formed by R_1 and $R_{IN(BASE)}$. In this case, the base voltage is determined by the emitter voltage ($V_B = V_E + V_{BE}$).

First, verify whether the transistor is in saturation or not. The collector saturation current and the base current required to produce saturation are determined as follows (assuming $V_{CE(sat)} = 0.2$ V):

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C + R_E} = \frac{9.8\text{ V}}{1.47\text{ k}\Omega} = 6.67\text{ mA}$$

$$I_{B(sat)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{6.67\text{ mA}}{300} = 22.2\ \mu\text{A}$$

Assuming the transistor is saturated, the maximum base current is determined.

$$I_{E(sat)} \cong 6.67\text{ mA}$$
$$V_E = I_{E(sat)}R_E = 3.13\text{ V}$$
$$V_B = V_E + V_{BE} = 3.83\text{ V}$$
$$R_{IN(BASE)} = \frac{B_{DC}V_B}{I_E} = \frac{(300)(3.83\text{ V})}{6.67\text{ mA}} = 172\text{ k}\Omega$$
$$I_B = \frac{V_{CC}}{R_1 + R_{IN(BASE)}} = \frac{10\text{ V}}{182\text{ k}\Omega} = 54.9\text{ mA}$$

Since this amount of base current is more than enough to produce saturation, the transistor is definitely saturated. Therefore, V_E, V_B, and V_C are as follows:

$$V_E = 3.13\text{ V}$$
$$V_B = 3.83\text{ V}$$
$$V_C = V_{CC} - I_{C(sat)}R_C = 10\text{ V} - (6.67\text{ mA})(1.0\text{ k}\Omega) = 3.33\text{ V}$$

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

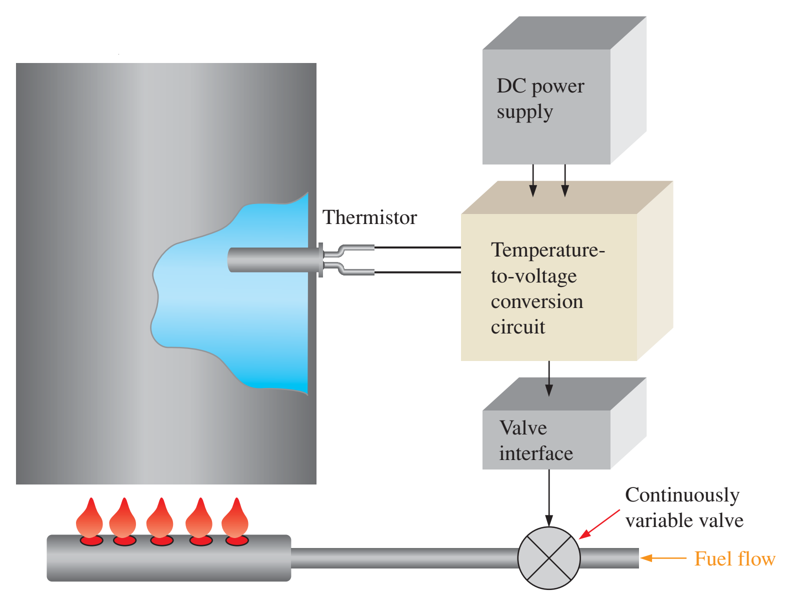
1. Multisim file TSE05-01
2. Multisim file TSE05-02
3. Multisim file TSE05-03
4. Multisim file TSE05-04
5. Multisim file TSE05-05

SECTION 5–4 CHECKUP

1. How do you determine when a transistor is saturated? When a transistor is in cutoff?
2. In a voltage-divider biased *npn* transistor circuit, you measure V_{CC} at the collector and an emitter voltage 0.7 V less than the base voltage. Is the transistor functioning in cutoff, or is R_E open?
3. What symptoms does an open R_C produce?

Application Activity: *Temperature to Voltage Conversion*

The focus of this Application Activity is a temperature-sensing circuit that converts the temperature of a liquid to a proportional voltage for the purpose of maintaining the temperature of the liquid within a specified range. Figure 5–28 illustrates the temperature-control system. The temperature sensor is a **thermistor**, which is a device whose resistance changes with temperature. The thermistor is connected to a transistor circuit that is biased for linear operation. The output voltage of the circuit is proportional to the thermistor resistance and thus to the temperature of the liquid in the tank. The output voltage goes to an interface circuit that


DC power supply
Thermistor
Temperature-to-voltage conversion circuit
Valve interface
Continuously variable valve
Fuel flow

▶ FIGURE 5–28

Temperature-control system.

controls the valve to control the flow of fuel to the burner based on the voltage. If the temperature of the liquid is below a set value, the fuel is increased and if it is above that value, the fuel is decreased. The temperature is to be maintained at 70°C ± 5°C.

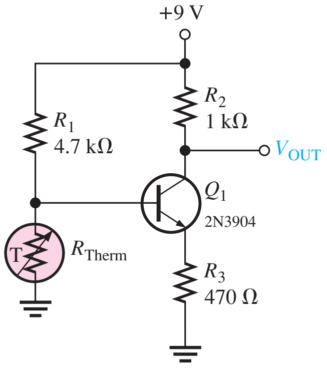
Designing the Circuit

Circuit Configuration A voltage-divider biased linear amplifier is used for the temperature-to-voltage conversion. The thermistor is used as one of the resistors in the voltage-divider bias. This thermistor has a positive temperature coefficient so, if the temperature increases, the resistance of the thermistor increases and if the temperature decreases, the resistance decreases. The base voltage changes proportionally to the change in thermistor resistance. The output voltage is inversely proportional to the base voltage, so as the temperature goes up, the output voltage decreases and reduces the fuel flow to the burner. As the temperature goes down, the output voltage increases and allows more fuel to the burner.

Components As shown in Figure 5–29(a), the circuit is implemented with a 2N3904 transistor, three resistors and a thermistor with the values shown, and a +9 V dc source. The thermistor has the temperature characteristic shown in part (b).

FIGURE 5–29

Temperature-to-voltage conversion circuit.



(a) Circuit

TEMPERATURE, °C	THERMISTOR RESISTANCE, kΩ
60	1.256
65	1.481
70	1.753
75	2.084
80	2.490

(b) Temperature characteristic of the thermistor for the specified range

1. Plot a graph of the thermistor temperature characteristic.
2. Refer to Figure 5–29 and calculate the emitter and collector currents for each temperature shown.
3. Calculate the output voltage for each temperature shown in Figure 5–29.

Simulation

The temperature-to-voltage conversion circuit is simulated to determine how the output voltage changes with temperature, as shown in Figure 5–30. The thermistor is represented by a resistor with values corresponding to each specified temperature.

4. Compare your calculations for the output voltage with the simulated values.

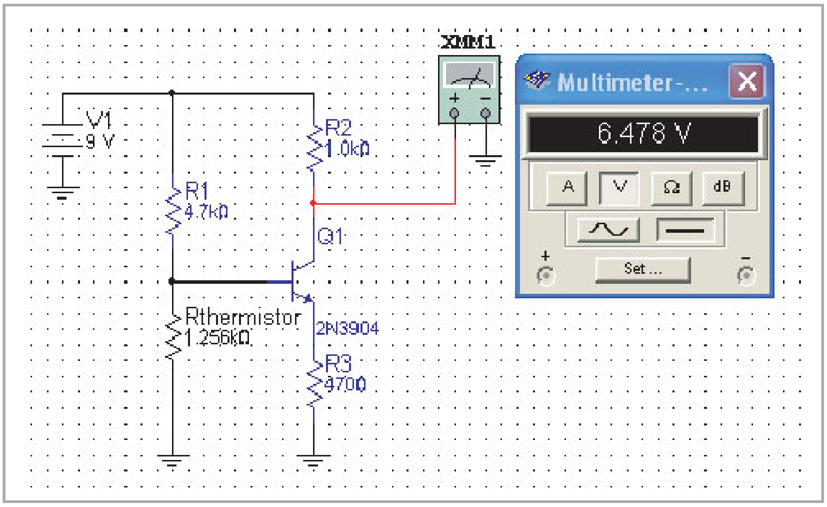
Simulate the circuit using your Multisim software. Observe the operation with the virtual multimeter.

Prototyping and Testing

Now that all the components have been selected, the prototype circuit is constructed and tested. After the circuit is successfully tested, it is ready to be finalized on a printed circuit board.

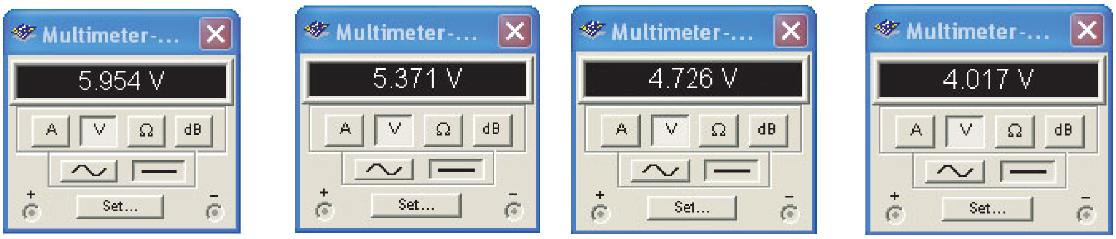
Lab Experiment

To build and test a similar circuit, go to Experiment 5 in your lab manual *(Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).


XMM1
V1
9 V
R2
1.0kΩ
R1
4.7kΩ
Q1
Rthermistor
1.256kΩ
2N3904
R3
470Ω
Multimeter-...
A
V
Ω
dB
Set ...

6.478 V

(a) Circuit output voltage at 60° C


Multimeter-...
A
V
Ω
dB
Set ...

5.954 V

5.371 V

4.726 V

4.017 V

R_{therm} = 1.481 kΩ

R_{therm} = 1.753 kΩ

R_{therm} = 2.084 kΩ

R_{therm} = 2.490 kΩ

(b) Circuit output voltages at 65°, 70°, 75°, and 80°

▲ **FIGURE 5–30**

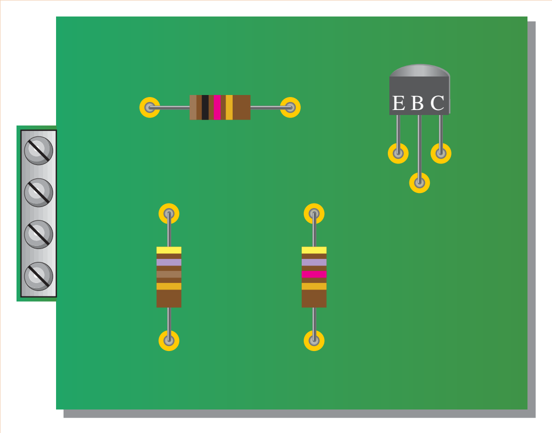
Operation of the temperature-to-voltage conversion circuit over temperature.

The Printed Circuit Board

A partially completed printed circuit board is shown in Figure 5–31. Indicate how you would add conductive traces to complete the circuit and show the input/output terminal functions.

► **FIGURE 5–31**

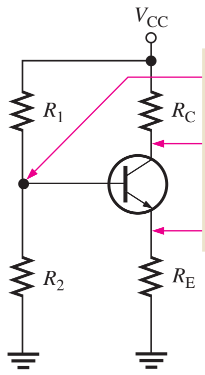
Partially complete temperature conversion circuit PC board.



SUMMARY OF TRANSISTOR BIAS CIRCUITS

npn transistors are shown. Supply voltage polarities are reversed for *pnp* transistors.

VOLTAGE-DIVIDER BIAS



$$V_B = V_E + V_{BE}$$

$$V_C = V_{CC} - I_C R_C$$

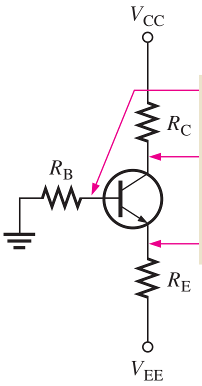
$$V_E = I_E R_E$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

$$I_C \cong I_E$$

$$I_B \cong \frac{V_B}{R_{IN(BASE)}}$$

EMITTER BIAS



$$V_B = V_E + V_{BE}$$

$$V_C = V_{CC} - I_C R_C$$

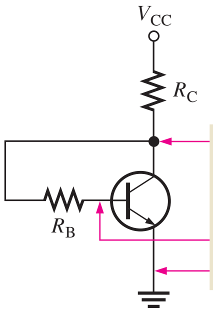
$$V_E = V_{EE} + I_E R_E$$

$$I_E \cong \frac{-V_{EE} - V_{BE}}{R_E}$$

$$I_C \cong I_E$$

$$I_B = \frac{V_B}{R_B}$$

COLLECTOR-FEEDBACK BIAS



$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{BE}$$

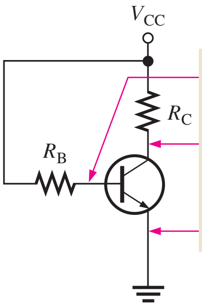
$$V_E = 0\ \text{V}$$

$$I_C \cong \frac{V_{CC} - V_{BE}}{R_C}$$

$$I_E \cong I_C$$

$$I_B = \frac{V_C - V_{BE}}{R_B}$$

BASE BIAS



$$V_B = V_{BE}$$

$$V_C = V_{CC} - I_C R_C$$

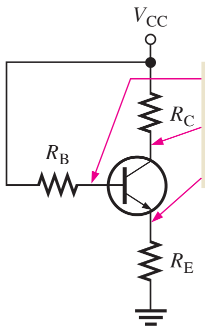
$$V_E = 0\ \text{V}$$

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BB}}{R_B}\right)$$

$$I_E \cong I_C$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

EMITTER-FEEDBACK BIAS



$$V_B = I_E R_E + V_{BE}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}}$$

$$I_C \cong I_E$$

$$I_B = \frac{V_{CC} - V_B}{R_B}$$

SUMMARY

Section 5–1

- The purpose of biasing a circuit is to establish a proper stable dc operating point (Q-point).
- The Q-point of a circuit is defined by specific values for I_C and V_{CE}. These values are called the coordinates of the Q-point.
- A dc load line passes through the Q-point on a transistor's collector curves intersecting the vertical axis at approximately $I_{C(sat)}$ and the horizontal axis at $V_{CE(off)}$.
- The linear (active) operating region of a transistor lies along the load line below saturation and above cutoff.

Section 5–2

- Loading effects are neglected for a stiff voltage divider.
- The dc input resistance at the base of a BJT is approximately $\beta_{DC}R_E$.
- Voltage-divider bias provides good Q-point stability with a single-polarity supply voltage. It is the most common bias circuit.

Section 5–3

- Emitter bias generally provides good Q-point stability but requires both positive and negative supply voltages.
- The base bias circuit arrangement has poor stability because its Q-point varies widely with β_{DC}.
- Emitter-feedback bias combines base bias with the addition of an emitter resistor.
- Collector-feedback bias provides good stability using negative feedback from collector to base.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

DC load line A straight line plot of I_C and V_{CE} for a transistor circuit.

Feedback The process of returning a portion of a circuit's output back to the input in such a way as to oppose or aid a change in the output.

Linear region The region of operation along the load line between saturation and cutoff.

Q-point The dc operating (bias) point of an amplifier specified by voltage and current values.

Stiff voltage divider A voltage divider for which loading effects can be neglected.

KEY FORMULAS

Voltage-Divider Bias

5–1 $V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$ for a stiff voltage divider

5–2 $V_E = V_B - V_{BE}$

5–3 $I_C \cong I_E = \frac{V_E}{R_E}$

5–4 $V_C = V_{CC} - I_C R_C$

5–5 $R_{IN(BASE)} = \frac{\beta_{DC}V_B}{I_E}$

5–6 $I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$

5–7 $I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}$

5–8 $I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}$

Emitter Bias

5–9 $I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$

Base Bias

5–10 $V_{CE} = V_{CC} - I_C R_C$

5–11 $I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$

Emitter-Feedback Bias

5–12 $I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}}$

Collector-Feedback Bias

5–13 $I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta_{DC}}$

5–14 $V_{CE} = V_{CC} - I_C R_C$

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. DC bias establishes the dc operating point for an amplifier.
2. Q-point is the quadratic point in a bias circuit.
3. The dc load line intersects the horizontal axis of a transistor characteristic curve at $V_{CE} = V_{CC}$.
4. The dc load line intersects the vertical axis of a transistor characteristic curve at $I_C = 0$.
5. The linear region of a transistor's operation lies between saturation and cutoff.
6. Voltage-divider bias is rarely used.
7. Input resistance at the base of the transistor can affect voltage-divider bias.
8. Stiff voltage-divider bias is essentially independent of base loading.
9. Emitter bias uses one dc supply voltage.
10. Negative feedback is employed in collector-feedback bias.
11. Base bias is less stable than voltage-divider bias.
12. A *pnp* transistor requires bias voltage polarities opposite to an *npn* transistor.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If V_{BB} in Figure 5–7 is increased, the Q-point value of collector current will
   (a) increase **(b)** decrease **(c)** not change
2. If V_{BB} in Figure 5–7 is increased, the Q-point value of V_{CE} will
   (a) increase **(b)** decrease **(c)** not change
3. If the value of R_2 in Figure 5–10 is reduced, the base voltage will
   (a) increase **(b)** decrease **(c)** not change
4. If the value of R_1 in Figure 5–10 is increased, the emitter current will
   (a) increase **(b)** decrease **(c)** not change
5. If R_E in Figure 5–15 is decreased, the collector current will
   (a) increase **(b)** decrease **(c)** not change
6. If R_B in Figure 5–18 is reduced, the base-to-emitter voltage will
   (a) increase **(b)** decrease **(c)** not change
7. If V_{CC} in Figure 5–20 is increased, the base-to-emitter voltage will
   (a) increase **(b)** decrease **(c)** not change
8. If R_1 in Figure 5–24 opens, the collector voltage will
   (a) increase **(b)** decrease **(c)** not change
9. If R_2 in Figure 5–24 opens, the collector voltage will
   (a) increase **(b)** decrease **(c)** not change
10. If R_2 in Figure 5–24 is increased, the emitter current will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 5–1

1. The maximum value of collector current in a biased transistor is

(a) $\beta_{DC}I_B$ **(b)** $I_{C(sat)}$ **(c)** greater than I_E **(d)** $I_E - I_B$

2. Ideally, a dc load line is a straight line drawn on the collector characteristic curves between

(a) the Q-point and cutoff **(b)** the Q-point and saturation

(c) $V_{CE(cutoff)}$ and $I_{C(sat)}$ **(d)** $I_B = 0$ and $I_B = I_C/\beta_{DC}$

3. If a sinusoidal voltage is applied to the base of a biased *npn* transistor and the resulting sinusoidal collector voltage is clipped near zero volts, the transistor is

(a) being driven into saturation **(b)** being driven into cutoff

(c) operating nonlinearly **(d)** answers (a) and (c)

(e) answers (b) and (c)

Section 5–2

4. The input resistance at the base of a biased transistor depends mainly on

(a) β_{DC} **(b)** R_B **(c)** R_E **(d)** β_{DC} and R_E

5. In a voltage-divider biased transistor circuit such as in Figure 5–13, $R_{IN(BASE)}$ can generally be neglected in calculations when

(a) $R_{IN(BASE)} > R_2$ **(b)** $R_2 > 10R_{IN(BASE)}$ **(c)** $R_{IN(BASE)} > 10R_2$ **(d)** $R_1 \ll R_2$

6. In a certain voltage-divider biased *npn* transistor, V_B is 2.95 V. The dc emitter voltage is approximately

(a) 2.25 V **(b)** 2.95 V **(c)** 3.65 V **(d)** 0.7 V

7. Voltage-divider bias

(a) cannot be independent of β_{DC} **(b)** can be essentially independent of β_{DC}

(c) is not widely used **(d)** requires fewer components than all the other methods

Section 5–3

8. Emitter bias is

(a) essentially independent of β_{DC} **(b)** very dependent on β_{DC}

(c) provides a stable bias point **(d)** answers (a) and (c)

9. In an emitter bias circuit, $R_E = 2.7\ k\Omega$ and $V_{EE} = 15$ V. The emitter current

(a) is 5.3 mA **(b)** is 2.7 mA

(c) is 180 mA **(d)** cannot be determined

10. The disadvantage of base bias is that

(a) it is very complex **(b)** it produces low gain

(c) it is too beta dependent **(d)** it produces high leakage current

11. Collector-feedback bias is

(a) based on the principle of positive feedback **(b)** based on beta multiplication

(c) based on the principle of negative feedback **(d)** not very stable

Section 5–4

12. In a voltage-divider biased *npn* transistor, if the upper voltage-divider resistor (the one connected to V_{CC}) opens,

(a) the transistor goes into cutoff **(b)** the transistor goes into saturation

(c) the transistor burns out **(d)** the supply voltage is too high

13. In a voltage-divider biased *npn* transistor, if the lower voltage-divider resistor (the one connected to ground) opens,

(a) the transistor is not affected **(b)** the transistor may be driven into cutoff

(c) the transistor may be driven into saturation **(d)** the collector current will decrease

14. In a voltage-divider biased *pnp* transistor, there is no base current, but the base voltage is approximately correct. The most likely problem(s) is

(a) a bias resistor is open **(b)** the collector resistor is open

(c) the base-emitter junction is open **(d)** the emitter resistor is open

(e) answers (a) and (c) **(f)** answers (c) and (d)

15. If R_1 in Figure 5–25 is open, the base voltage is

(a) +10 V **(b)** 0 V **(c)** 3.13 V **(d)** 0.7 V

16. If R_1 is open, the collector current in Figure 5–25 is

(a) 5.17 mA **(b)** 10 mA **(c)** 4.83 mA **(d)** 0 mA

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

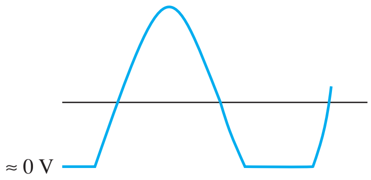
BASIC PROBLEMS

Section 5–1

The DC Operating Point

1. The output (collector voltage) of a biased transistor amplifier is shown in Figure 5–32. Is the transistor biased too close to cutoff or too close to saturation?

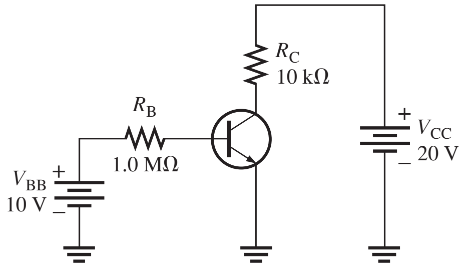
▶ FIGURE 5–32



2. What is the Q-point for a biased transistor as in Figure 5–2 with $I_B = 150\ \mu A$, $\beta_{DC} = 75$, $V_{CC} = 18$ V, and $R_C = 1.0\ k\Omega$?
3. What is the saturation value of collector current in Problem 2?
4. What is the cutoff value of V_{CE} in Problem 2?
5. Determine the intercept points of the dc load line on the vertical and horizontal axes of the collector-characteristic curves for the circuit in Figure 5–33.

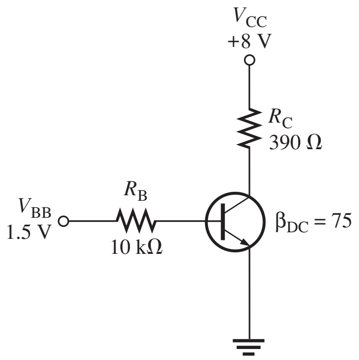
▶ FIGURE 5–33

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F05-33).

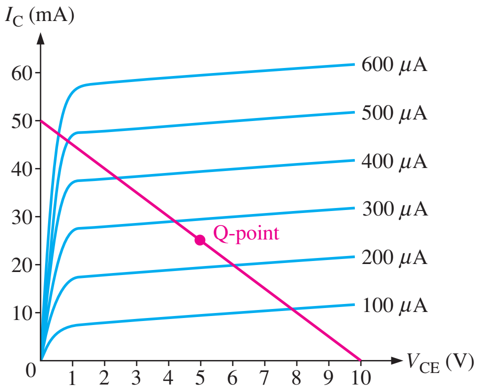


6. Assume that you wish to bias the transistor in Figure 5–33 with $I_B = 20\ \mu A$. To what voltage must you change the V_{BB} supply? What are I_C and V_{CE} at the Q-point, given that $\beta_{DC} = 50$?
7. Design a biased-transistor circuit using $V_{BB} = V_{CC} = 10$ V for a Q-point of $I_C = 5$ mA and $V_{CE} = 4$ V. Assume $\beta_{DC} = 100$. The design involves finding R_B, R_C, and the *minimum* power rating of the transistor. (The actual power rating should be greater.) Sketch the circuit.
8. Determine whether the transistor in Figure 5–34 is biased in cutoff, saturation, or the linear region. Remember that $I_C = \beta_{DC} I_B$ is valid only in the linear region.

▶ FIGURE 5–34



▶ FIGURE 5–35



9. From the collector characteristic curves and the dc load line in Figure 5–35, determine the following:

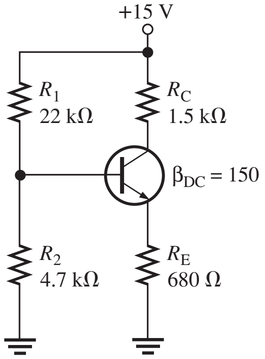
- **(a)** Collector saturation current
- **(b)** V_{CE} at cutoff
- **(c)** Q-point values of I_B, I_C, and V_{CE}

10. From Figure 5–35 determine the following:

- **(a)** Maximum collector current for linear operation
- **(b)** Base current at the maximum collector current
- **(c)** V_{CE} at maximum collector current

Section 5–2

Voltage-Divider Bias


+15 V
R_1
22 kΩ
R_C
1.5 kΩ
β_{DC} = 150
R_2
4.7 kΩ
R_E
680 Ω

▲ FIGURE 5–36

11. What is the minimum value of β_{DC} in Figure 5–36 that makes $R_{IN(BASE)} \geqq 10R_2$?

12. The bias resistor R_2 in Figure 5–36 is replaced by a 15 kΩ potentiometer. What minimum resistance setting causes saturation?

13. If the potentiometer described in Problem 12 is set at 2 kΩ, what are the values for I_C and V_{CE}?

14. Determine all transistor terminal voltages with respect to ground in Figure 5–37.

15. Show the connections required to replace the transistor in Figure 5–37 with a *pnp* device.

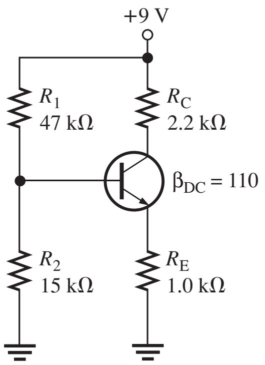
16. **(a)** Determine V_B in Figure 5–38.

(b) How is V_B affected if the transistor is replaced by one with a β_{DC} of 50?

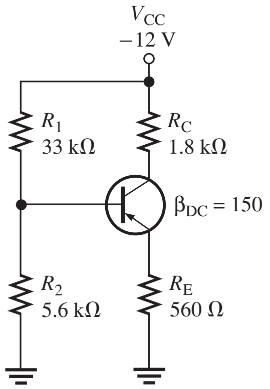
17. Determine the following in Figure 5–38:

- **(a)** Q-point values
- **(b)** The minimum power rating of the transistor

18. Determine I_1, I_2, and I_B in Figure 5–38.


+9 V
R_1
47 kΩ
R_C
2.2 kΩ
β_{DC} = 110
R_2
15 kΩ
R_E
1.0 kΩ

▲ FIGURE 5–37


V_{CC}
−12 V
R_1
33 kΩ
R_C
1.8 kΩ
β_{DC} = 150
R_2
5.6 kΩ
R_E
560 Ω

▲ FIGURE 5–38

Section 5–3 Other Bias Methods

19. Analyze the circuit in Figure 5–39 to determine the correct voltages at the transistor terminals with respect to ground. Assume $\beta_{DC} = 100$.

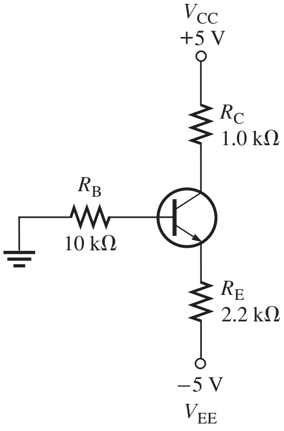
20. To what value can R_E in Figure 5–39 be reduced without the transistor going into saturation?

21. Taking V_{BE} into account in Figure 5–39, how much will I_E change with a temperature increase from 25°C to 100°C? The V_{BE} is 0.7 V at 25°C and decreases 2.5 mV per degree Celsius. Neglect any change in β_{DC}.

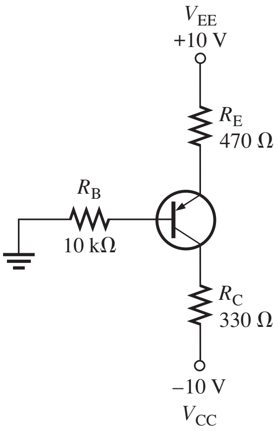
22. When can the effect of a change in β_{DC} be neglected in the emitter bias circuit?

23. Determine I_C and V_{CE} in the *pnp* emitter bias circuit of Figure 5–40. Assume $\beta_{DC} = 100$.

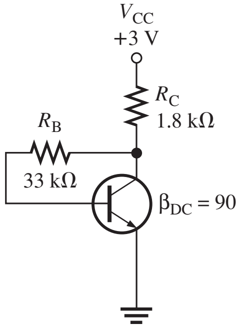
24. Determine V_B, V_C, and I_C in Figure 5–41.



▲ FIGURE 5–39



▲ FIGURE 5–40



▲ FIGURE 5–41

25. What value of R_C can be used to decrease I_C in Problem 24 by 25 percent?

26. What is the minimum power rating for the transistor in Problem 25?

27. A collector-feedback circuit uses an *npn* transistor with $V_{CC} = 12$ V, $R_C = 1.2$ kΩ, and $R_B = 47$ kΩ. Determine the collector current and the collector voltage if $\beta_{DC} = 200$.

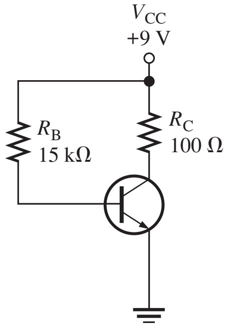
28. Determine I_B, I_C, and V_{CE} for a base-biased transistor circuit with the following values: $\beta_{DC} = 90$, $V_{CC} = 12$ V, $R_B = 22$ kΩ, and $R_C = 100$ Ω.

29. If β_{DC} in Problem 28 doubles over temperature, what are the Q-point values?

30. You have two base bias circuits connected for testing. They are identical except that one is biased with a separate V_{BB} source and the other is biased with the base resistor connected to V_{CC}. Ammeters are connected to measure collector current in each circuit. You vary the V_{CC} supply voltage and observe that the collector current varies in one circuit, but not in the other. In which circuit does the collector current change? Explain your observation.

31. The datasheet for a particular transistor specifies a minimum β_{DC} of 50 and a maximum β_{DC} of 125. What range of Q-point values can be expected if an attempt is made to mass-produce the circuit in Figure 5–42? Is this range acceptable if the Q-point must remain in the transistor's linear region?

32. The base bias circuit in Figure 5–42 is subjected to a temperature variation from 0°C to 70°C. The β_{DC} decreases by 50 percent at 0°C and increases by 75 percent at 70°C from its nominal value of 110 at 25°C. What are the changes in I_C and V_{CE} over the temperature range of 0°C to 70°C?

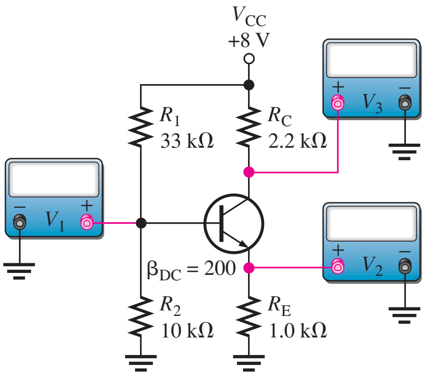


▲ FIGURE 5–42

Section 5–4 Troubleshooting

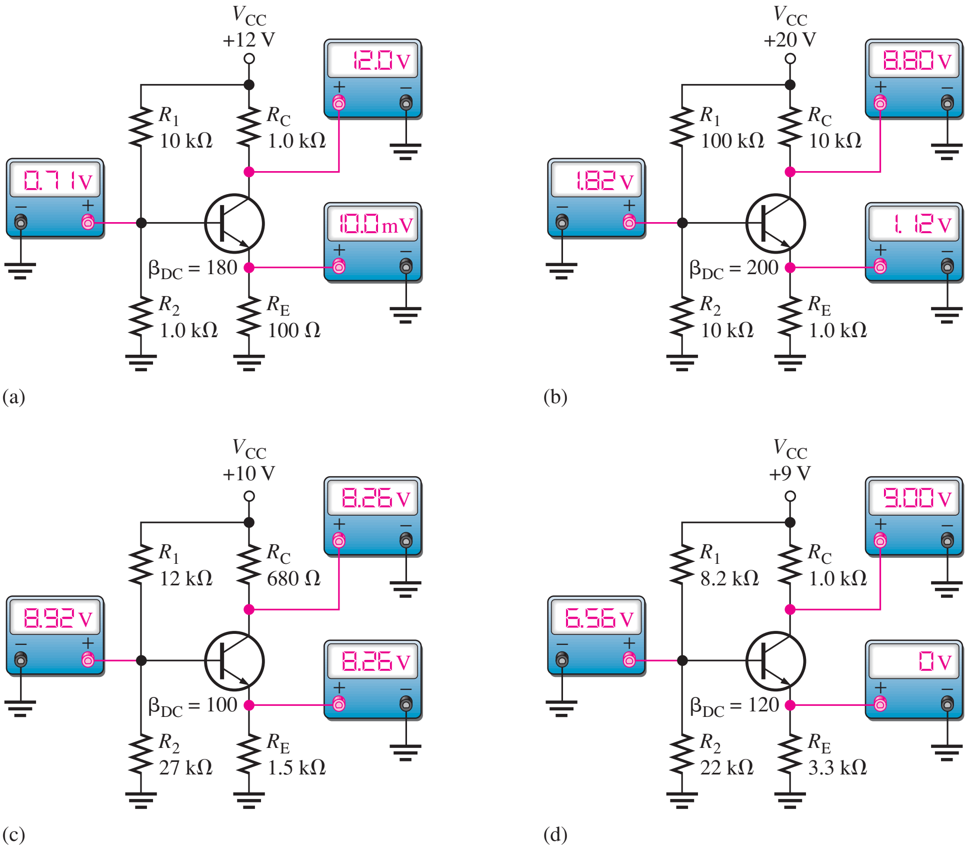
33. Determine the meter readings in Figure 5–43 if R_1 is open.

▶ FIGURE 5–43


V_{CC}
+8 V
R_1
33 kΩ
R_C
2.2 kΩ
V_3
V_1
β_{DC} = 200
V_2
R_2
10 kΩ
R_E
1.0 kΩ
+
−

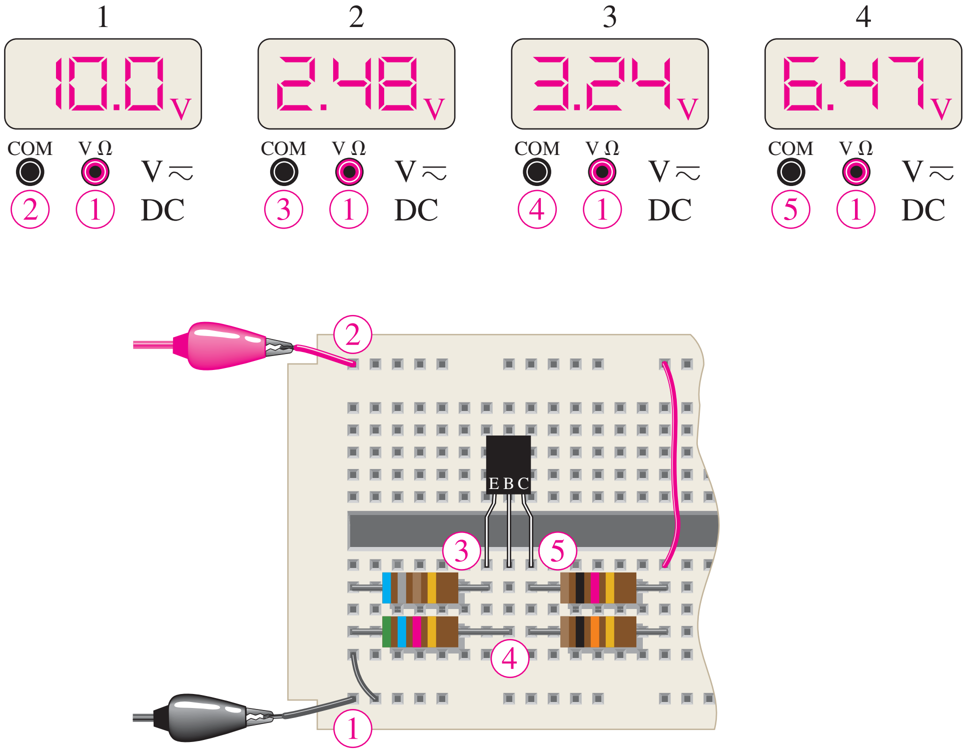
34. Assume the emitter becomes shorted to ground in Figure 5–43 by a solder splash or stray wire clipping. What do the meters read? When you correct the problem, what do the meters read?

35. Determine the most probable failures, if any, in each circuit of Figure 5–44, based on the indicated measurements.


V_{CC}
+12 V
12.0 V
R_1
10 kΩ
R_C
1.0 kΩ
0.71 V
10.0 mV
β_{DC} = 180
R_2
1.0 kΩ
R_E
100 Ω
(a)
V_{CC}
+20 V
8.80 V
R_1
100 kΩ
R_C
10 kΩ
1.82 V
1.12 V
β_{DC} = 200
R_2
10 kΩ
R_E
1.0 kΩ
(b)
V_{CC}
+10 V
8.26 V
R_1
12 kΩ
R_C
680 Ω
8.92 V
8.26 V
β_{DC} = 100
R_2
27 kΩ
R_E
1.5 kΩ
(c)
V_{CC}
+9 V
9.00 V
R_1
8.2 kΩ
R_C
1.0 kΩ
6.56 V
0 V
β_{DC} = 120
R_2
22 kΩ
R_E
3.3 kΩ
(d)
+
−

▲ FIGURE 5–44

36. Determine if the DMM readings 2 through 4 in the breadboard circuit of Figure 5–45 are correct. If they are not, isolate the problem(s). The transistor is a *pnp* device with a specified dc beta range of 35 to 100.



▲ FIGURE 5–45

37. Determine each meter reading in Figure 5–45 for each of the following faults:

(a) the 680 Ω resistor open

(b) the 5.6 kΩ resistor open

(c) the 10 kΩ resistor open

(d) the 1.0 kΩ resistor open

(e) a short from emitter to ground

(f) an open base-emitter junction

APPLICATION ACTIVITY PROBLEMS

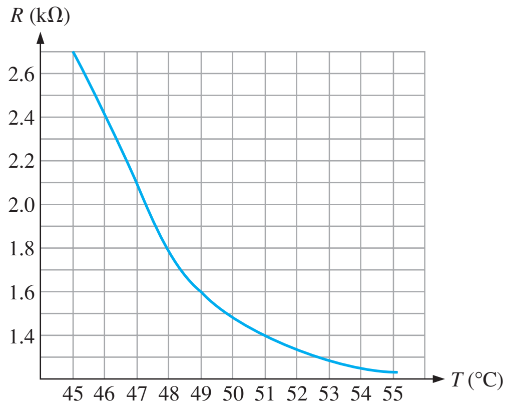
38. Determine V_B, V_E, and V_C in the temperature-to-voltage conversion circuit in Figure 5–29(a) if R_1 fails open.

39. What faults will cause the transistor in the temperature-to-voltage conversion circuit to go into cutoff?

40. A thermistor with the characteristic curve shown in Figure 5–46 is used in the circuit of Figure 5–29(a). Calculate the output voltage for temperatures of 45°C, 48°C, and 53°C. Assume a stiff voltage divider.

41. Explain how you would identify an open collector-base junction in the transistor in Figure 5–29(a).

► FIGURE 5–46

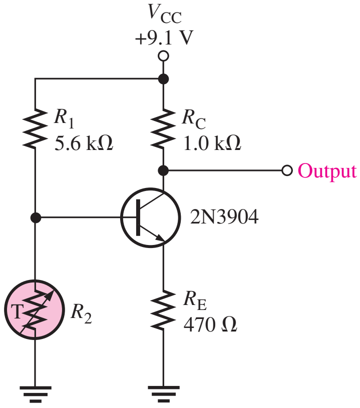


DATASHEET PROBLEMS

42. Analyze the temperature-to-voltage conversion circuit in Figure 5–47 at the temperature extremes indicated on the graph in Figure 5–46 for both minimum and maximum specified datasheet values of h_{FE}. Refer to the partial datasheet in Figure 5–48.

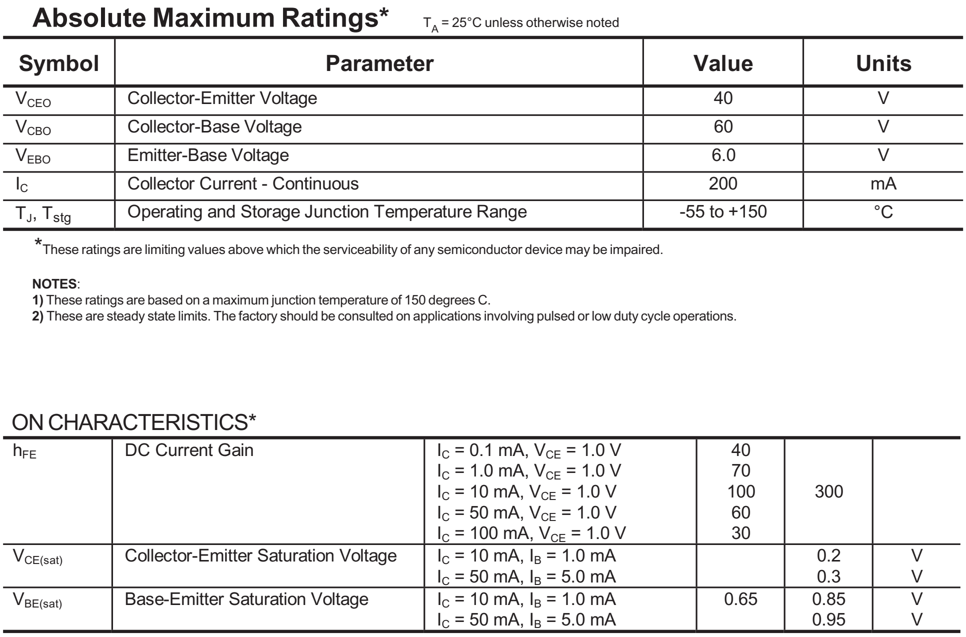
43. Verify that no maximum ratings are exceeded in the temperature-to-voltage conversion circuit in Figure 5–47. Refer to the partial datasheet in Figure 5–48.

▶ **FIGURE 5–47**



▶ **FIGURE 5–48**

Partial datasheet for the 2N3904 transistor. Copyright Fairchild Semiconductor Corporation. Used by permission.



Absolute Maximum Ratings* T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

ON CHARACTERISTICS*

h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V	40		
		I_C = 1.0 mA, V_{CE} = 1.0 V	70		
		I_C = 10 mA, V_{CE} = 1.0 V	100	300	
		I_C = 50 mA, V_{CE} = 1.0 V	60		
		I_C = 100 mA, V_{CE} = 1.0 V	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA		0.2	V
		I_C = 50 mA, I_B = 5.0 mA		0.3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA	0.65	0.85	V
		I_C = 50 mA, I_B = 5.0 mA		0.95	V

44. Refer to the partial datasheet in Figure 5–49.

(a) What is the maximum collector current for a 2N2222A?

(b) What is the maximum reverse base-emitter voltage for a 2N2218A?

45. Determine the maximum power dissipation for a 2N2222A at 100°C.

46. When you increase the collector current in a 2N2219A from 1 mA to 500 mA, how much does the minimum β_{DC} (h_{FE}) change?

ADVANCED PROBLEMS

47. Design a circuit using base bias that operates from a 15 V dc voltage and draws a maximum current from the dc source ($I_{CC(max)}$) of 10 mA. The Q-point values are to be $I_C = 5$ mA and $V_{CE} = 5$ V. The transistor is a 2N3904. Assume a midpoint value for β_{DC}.

Maximum Ratings

Rating	Symbol	2N2218 2N2219 2N2221 2N2222	2N2218A 2N2219A 2N2221A 2N2222A	2N5581 2N5582	Unit
Collector-Emitter voltage	V_{CEO}	30	40	40	V dc
Collector-Base voltage	V_{CBO}	60	75	75	V dc
Emitter-Base voltage	V_{EBO}	5.0	6.0	6.0	V dc
Collector current — continuous	I_C	800	800	800	mA dc
		2N2218,A 2N2219,A	2N2221,A 2N2222,A	2N5581 2N5582	
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.8 4.57	0.5 2.28	0.6 3.33	Watt mW/°C
Total device dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	3.0 17.1	1.2 6.85	2.0 11.43	Watt mW/°C
Operating and storage junction Temperature range	T_J, T_{stg}		−65 to +200		°C

Electrical Characteristics (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
Off Characteristics					
Collector-Emitter breakdown voltage		$V_{(BR)CEO}$			V dc
(I_C = 10 mA dc, I_B = 0)	Non-A Suffix		30	—	
	A-Suffix, 2N5581, 2N5582		40	—	
Collector-Base breakdown voltage		$V_{(BR)CBO}$			V dc
(I_C = 10 μA dc, I_E = 0)	Non-A Suffix		60	—	
	A-Suffix, 2N5581, 2N5582		75	—	
Emitter-Base breakdown voltage		$V_{(BR)EBO}$			V dc
(I_E = 10 μA dc, I_C = 0)	Non-A Suffix		5.0	—	
	A-Suffix, 2N5581, 2N5582		6.0	—	
Collector cutoff current		I_{CEX}		10	nA dc
(V_{CE} = 60 V dc, $V_{EB(off)}$ = 3.0 V dc	A-Suffix, 2N5581, 2N5582		—		
Collector cutoff current		I_{CBO}			μA dc
(V_{CB} = 50 V dc, I_E = 0)	Non-A Suffix		—	0.01	
(V_{CB} = 60 V dc, I_E = 0)	A-Suffix, 2N5581, 2N5582		—	0.01	
(V_{CB} = 50 V dc, I_E = 0, T_A = 150°C)	Non-A Suffix		—	10	
(V_{CB} = 60 V dc, I_E = 0, T_A = 150°C)	A-Suffix, 2N5581, 2N5582		—	10	
Emitter cutoff current		I_{EBO}	—	10	nA dc
(V_{EB} = 3.0 V dc, I_C = 0)	A-Suffix, 2N5581, 2N5582				
Base cutoff current		I_{BL}	—	20	nA dc
(V_{CE} = 60 V dc, $V_{EB(off)}$ = 3.0 V dc)	A-Suffix				
On Characteristics					
DC current gain		h_{FE}			—
(I_C = 0.1 mA dc, V_{CE} = 10 V dc)	2N2218,A, 2N2221,A, 2N5581(1)		20	—	
	2N2219,A, 2N2222,A, 2N5582(1)		35	—	
(I_C = 1.0 mA dc, V_{CE} = 10 V dc)	2N2218,A, 2N2221,A, 2N5581		25	—	
	2N2219,A, 2N2222,A, 2N5582		50	—	
(I_C = 10 mA dc, V_{CE} = 10 V dc)	2N2218,A, 2N2221,A, 2N5581(1)		35	—	
	2N2219,A, 2N2222,A, 2N5582(1)		75	—	
(I_C = 10 mA dc, V_{CE} = 10 V dc, T_A = – 55°C)	2N2218,A, 2N2221,A, 2N5581		15	—	
	2N2219,A, 2N2222,A, 2N5582		35	—	
(I_C = 150 mA dc, V_{CE} = 10 V dc)	2N2218,A, 2N2221,A, 2N5581		40	120	
	2N2219,A, 2N2222,A, 2N5582		100	300	
(I_C = 150 mA dc, V_{CE} = 1.0 V dc)	2N2218,A, 2N2221,A, 2N5581		20	—	
	2N2219,A, 2N2222,A, 2N5582		50	—	
(I_C = 500 mA dc, V_{CE} = 10 V dc)	2N2218, 2N2221		20	—	
	2N2219, 2N2222		30	—	
	2N2218A, 2N2221A, 2N5581		25	—	
	2N2219A, 2N2222A, 2N5582		40	—	
Collector-Emitter saturation voltage		$V_{CE(sat)}$			V dc
(I_C = 150 mA dc, I_B = 15 mA dc)	Non-A Suffix		—	0.4	
	A-Suffix, 2N5581, 2N5582		—	0.3	
(I_C = 500 mA dc, I_B = 50 mA dc)	Non-A Suffix		—	1.6	
	A-Suffix, 2N5581, 2N5582		—	1.0	
Base-Emitter saturation voltage		$V_{BE(sat)}$			V dc
(I_C = 150 mA dc, I_B = 15 mA dc)	Non-A Suffix		0.6	1.3	
	A-Suffix, 2N5581, 2N5582		0.6	1.2	
(I_C = 500 mA dc, I_B = 50 mA dc)	Non-A Suffix		—	2.6	
	A-Suffix, 2N5581, 2N5582		—	2.0	

▲ FIGURE 5–49

Partial datasheet for 2N2218A–2N2222A.

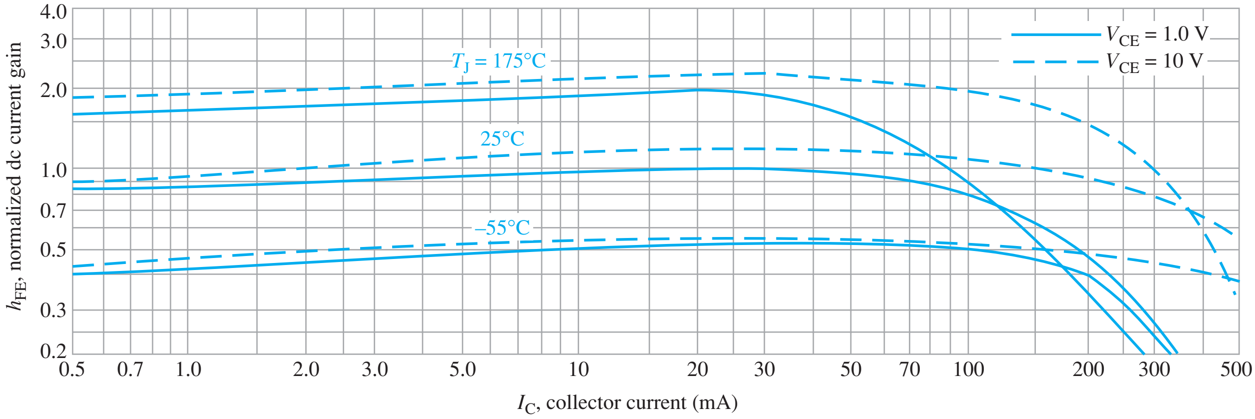
48. Design a circuit using emitter bias that operates from dc voltages of +12 V and −12 V. The maximum I_{CC} is to be 20 mA and the Q-point is at 10 mA and 4 V. The transistor is a 2N3904.

49. Design a circuit using voltage-divider bias for the following specifications: $V_{CC} = 9$ V, $I_{CC(max)} = 5$ mA, $I_C = 1.5$ mA, and $V_{CE} = 3$ V. The transistor is a 2N3904.

50. Design a collector-feedback circuit using a 2N2222A with $V_{CC} = 5$ V, $I_C = 10$ mA, and $V_{CE} = 1.5$ V.

51. Can you replace the 2N3904 in Figure 5–47 with a 2N2222A and maintain the same range of output voltage over a temperature range from 45°C to 55°C?

52. Refer to the datasheet graph in Figure 5–50 and the partial datasheet in Figure 5–49. Determine the minimum dc current gain for a 2N2222A at −55°C, 25°C, and 175°C for $V_{CE} = 1$ V.



▲ FIGURE 5–50

53. A design change is required in the valve interface circuit of the temperature-control system shown in Figure 5–28. The new design will have a valve interface input resistance of 10 kΩ. Determine the effect this change has on the temperature-to-voltage conversion circuit.

54. Investigate the feasibility of redesigning the temperature-to-voltage conversion circuit in Figure 5–29 to operate from a dc supply voltage of 5.1 V and produce the same range of output voltages determined in the Application Activity over the required thermistor temperature range from 60°C to 80°C.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

55. Open file TSP05-55 and determine the fault.

56. Open file TSP05-56 and determine the fault.

57. Open file TSP05-57 and determine the fault.

58. Open file TSP05-58 and determine the fault.

59. Open file TSP05-59 and determine the fault.

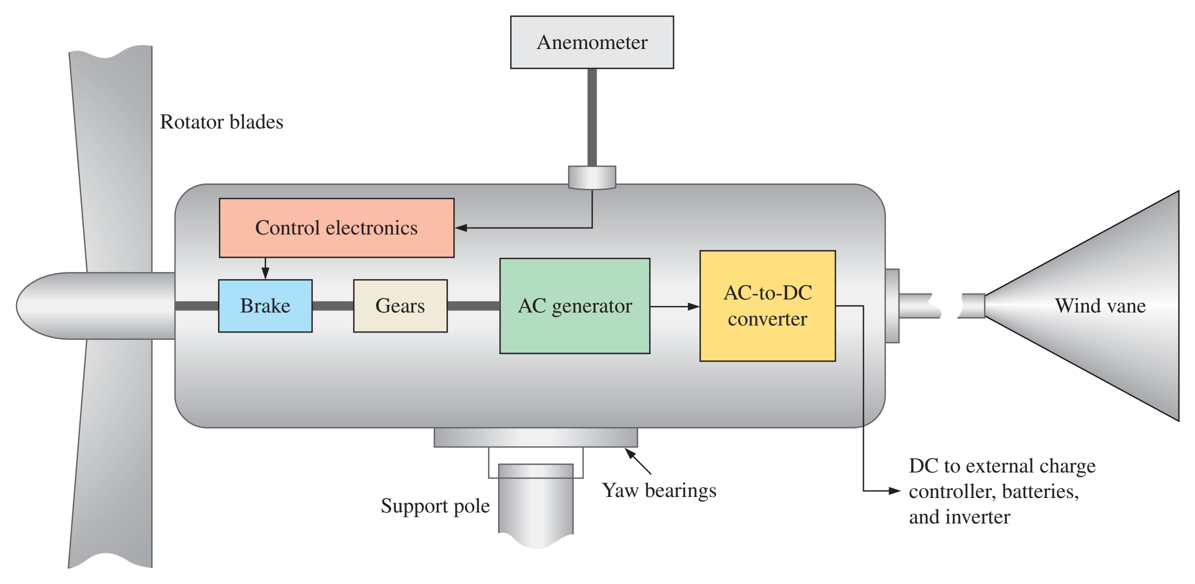
60. Open file TSP05-60 and determine the fault.

GreenTech Application 5: *Wind Power*

Wind energy, like solar energy, is a major renewable resource. Wind is actually a product of solar energy because differences in earth temperatures result in the movement of air. Wind turbines harvest energy from the wind and may be used as small single units to supply an individual home or wind farms where tens to hundreds of large units harvest wind energy and convert it to electricity.

Two key elements in a wind turbine are the blades and the ac generator. In many wind turbines, electronic circuits sense the wind direction and speed and adjust the orientation and pitch of the blades to maximize the energy collected from the wind. The generator produces a varying ac voltage that depends on the rotational speed of the blades due to the wind. Since the frequency and amplitude of a generator output varies with wind speed, the ac output is converted to dc and then back to 60 Hz ac with an inverter. Like a solar power system, the energy can be stored in batteries using a charge controller for smaller applications, or the energy can be connected directly to the grid for large-scale applications.

Figure GA5–1 shows a basic diagram of a horizontal-axis wind turbine (HAWT) for small power applications, such as home use. A typical wind turbine has three blades and is mounted on a very high support tower. Wind energy is converted to mechanical energy by the rotating blades. As shown in Figure GA5–1, the blade rotation is applied to a shaft, which is geared up to turn the ac generator shaft at a higher rate than the blades are rotating. The generator rotation produces an ac voltage output with a frequency that depends on the rate of rotation. Since it is a variable frequency and amplitude output, as previously mentioned, the ac is converted to dc by the ac-to-dc converter. The dc is sent to a charge controller that charges the storage batteries. The battery output is applied to an inverter where it is converted to a 120 V, 60 Hz ac voltage for individual consumer use. The wind vane and yaw bearing assembly are used on small turbines to keep the blades pointed into the wind. An anemometer senses the wind speed in order to brake the blades when the wind reaches a specified speed. This prevents mechanical damage if the wind speed is too high.

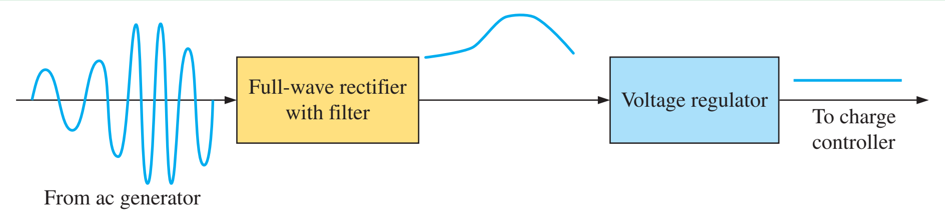


▲ FIGURE GA5–1

Basic small HAWT system operation.

The AC-to-DC Converter

Because of the variable frequency of the ac from the generator, it must first be converted to dc for the charge controller. A rectifier and regulator are used for the conversion, as illustrated in Figure GA5–2. The ac voltage from the generator varies in amplitude and frequency as a function of wind speed. The ac-to-dc converter changes the varying ac to a varying dc voltage, which is then applied to a voltage regulator to produce a specified constant dc voltage, as shown.

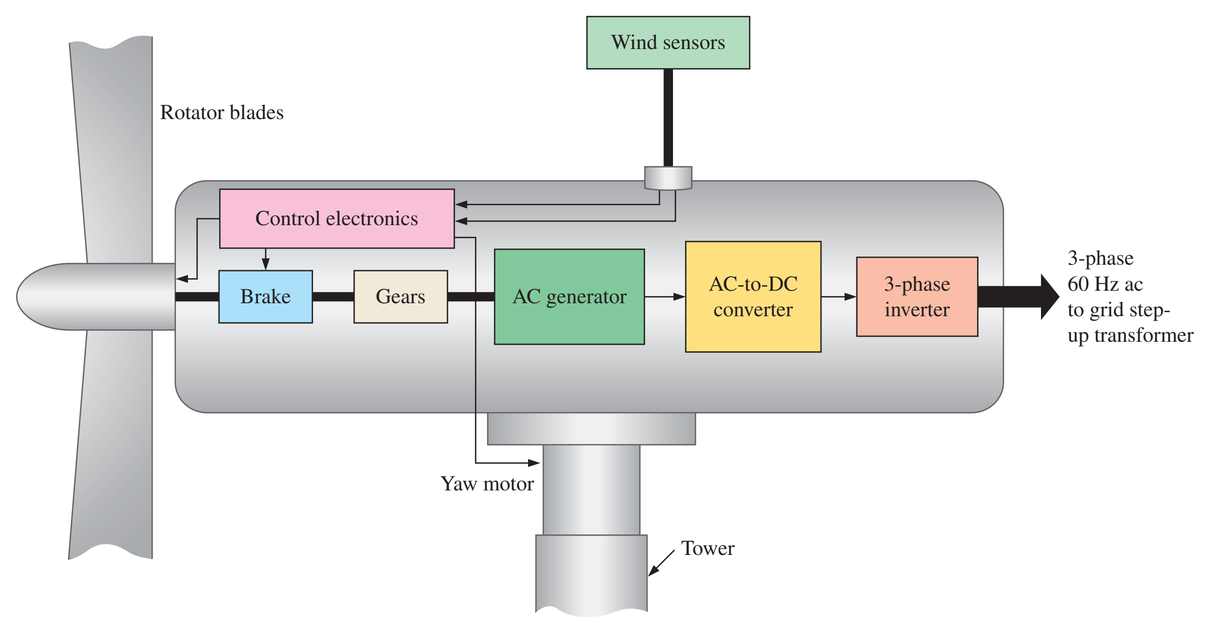

Full-wave rectifier with filter
Voltage regulator
To charge controller
From ac generator

▲ FIGURE GA5–2

AC-to-DC converter block diagram.

Large-Scale Wind Turbines

Figure GA5–3 is a horizontal axis grid-tie turbine, which is the most common configuration for commercial wind farm applications. The wind direction sensor sends a signal to the control electronics so the yaw motor can keep the turbine pointing into the wind. The wind speed sensor sends a signal to the control electronics so the pitch of the blades can be adjusted for maximum efficiency. Also, when the wind exceeds a specified speed, the control electronics activates the brakes to reduce or stop rotation of the blades, preventing damage to the unit.


Wind sensors
Rotator blades
Control electronics
Brake
Gears
AC generator
AC-to-DC converter
3-phase inverter
3-phase 60 Hz ac to grid step-up transformer
Yaw motor
Tower

▲ FIGURE GA5–3

Large horizontal-axis wind turbine (HAWT).

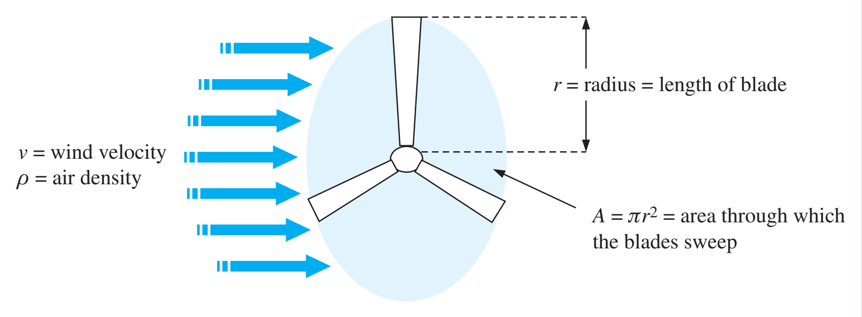
For large wind turbines (above 100 kW–150 kW) the voltage generated is usually 690 V three-phase ac. The output goes to a transformer usually located in the tower or near its base and is stepped up to thousands of volts depending on the requirements of the local electrical grid.

Power in the Wind

The amount of power available in the wind can be calculated using the following formula:

$$P = \frac{\rho A v^3}{2}$$

In the formula, ρ is the density of the air, A is the area swept by the blades, and v is the velocity (speed) of the wind. Note that the power is dependent on the length of the blades, r, and the cube of the wind speed, v^3. Since $A = \pi r^2$, if the length of the blades is doubled, the available power in the wind will be increased by four times ($2^2 = 4$). If the wind velocity doubles, the available power in the wind is increased by eight times ($2^3 = 8$). Of course, a turbine cannot convert all of the available wind power into mechanical power to turn the generator. In fact, most practical turbines can convert less than 50% of the wind power. Figure GA5–4 illustrates the factors that affect the amount of power that can be extracted from the wind.


r = radius = length of blade
v = wind velocity
ρ = air density
$A = \pi r^2$ = area through which the blades sweep

▲ FIGURE GA5–4

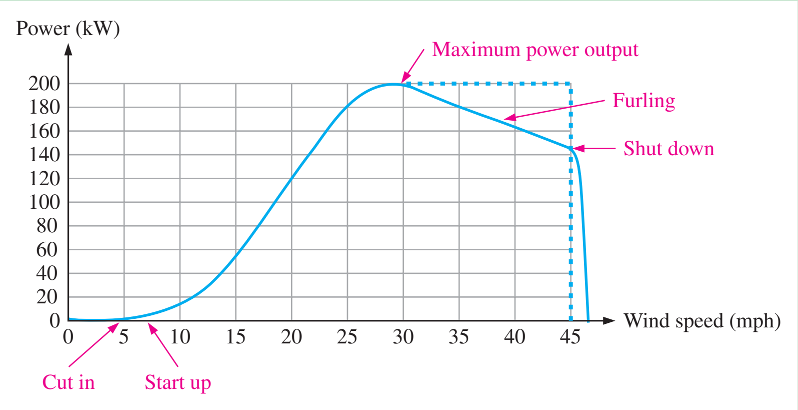
Factor determining the available power in the wind.

Betz Law This law states that the theoretical limit of the amount of power that can be extracted from the wind is 59% if all conditions are perfect. This limiting factor was developed by Albert Betz in 1926. In practice, 20% to 40% can normally be expected.

Wind Power Curve

A wind power curve shows the amount of power that can be extracted over a range of wind speeds (velocities) for specific turbines. Wind power curves will vary from one type of turbine to another. Figure GA5–5 shows a typical curve. The *cut-in speed* is the wind speed at which the blades begin to turn. The *start-up speed* is the wind speed at which the blades are moving fast enough to cause the generator to produce electricity. The start-up speed is slightly higher than the cut-in speed. The *maximum power output* is the peak power that the turbine can produce. For this example curve, the maximum power output is approximately 200 kW at a wind speed of approximately 28 mph.

To limit the rotational speed of the blades above the maximum power output (MPO) point in order to prevent damage to the machine, a process called *furling* is used. Ideally, the curve is kept as level as possible as shown by the dashed portion of the curve in Figure GA5–5. However, in practice, the power decreases above that point, once the furling process is activated. Furling can be accomplished by changing the pitch of the blades or turning the entire turbine away from the wind direction slightly under direction of the control electronics. Also, when the wind reaches a predetermined maximum, the turbine can be completely shut down. For example, the curve shows this turbine being shut down at 45 mph.



▲ **FIGURE GA5–5**

Example of a wind power curve for a wind turbine.

Questions

Some questions may require research beyond the content of this coverage. Answers are at the end of the book.

1. What does HAWT stand for?
2. Why does the input voltage to the ac-to-dc converter vary in amplitude and frequency?
3. What are the physical factors that determine the amount of power available in the wind that strikes the blades of a turbine?
4. What is the Betz limit?
5. In wind farms, how close together should the turbines generally be placed?

The following websites are recommended for viewing HAWTs in action. Many other websites are also available.

http://www.youtube.com/watch?v=eXejxcW-XGo
http://www.youtube.com/watch?v=RFPj9frhKuo
http://www.youtube.com/watch?v=7PLvr-lpADM&NR=1
http://www.youtube.com/watch?v=7rlVMJgPRc4
http://www.youtube.com/watch?v=NeVClBaQI_Q
http://www.youtube.com/watch?v=PEEAl9laoUg
http://www.youtube.com/watch?v=N9_FKGxD27g
http://www.youtube.com/watch?v=v05MuBseBQE
http://www.youtube.com/watch?v=hBRfboAscww

BJT Amplifiers

6

CHAPTER OUTLINE

6–1 Amplifier Operation
6–2 Transistor AC Models
6–3 The Common-Emitter Amplifier
6–4 The Common-Collector Amplifier
6–5 The Common-Base Amplifier
6–6 Multistage Amplifiers
6–7 The Differential Amplifier
6–8 Troubleshooting
Application Activity
GreenTech Application 6: *Wind Power*

CHAPTER OBJECTIVES

- Describe amplifier operation
- Discuss transistor models
- Describe and analyze the operation of common-emitter amplifiers
- Describe and analyze the operation of common-collector amplifiers
- Describe and analyze the operation of common-base amplifiers
- Describe and analyze the operation of multistage amplifiers
- Discuss the differential amplifier and its operation
- Troubleshoot amplifier circuits

KEY TERMS

- *r* parameter
- Common-emitter
- ac ground
- Input resistance
- Output resistance
- Attenuation
- Bypass capacitor
- Common-collector
- Emitter-follower
- Common-base
- Decibel
- Differential amplifier
- Common mode
- CMRR (Common-mode rejection ratio)

APPLICATION ACTIVITY PREVIEW

The Application Activity in this chapter involves a preamplifier circuit for a public address system. The complete system includes the preamplifier, a power amplifier, and a dc power supply. You will focus on the preamplifier in this chapter and then on the power amplifier in Chapter 7.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

The things you learned about biasing a transistor in Chapter 5 are now applied in this chapter where bipolar junction transistor (BJT) circuits are used as small-signal amplifiers. The term *small-signal* refers to the use of signals that take up a relatively small percentage of an amplifier's operational range. Additionally, you will learn how to reduce an amplifier to an equivalent dc and ac circuit for easier analysis, and you will learn about multistage amplifiers. The differential amplifier is also covered.

6–1 AMPLIFIER OPERATION

The biasing of a transistor is purely a dc operation. The purpose of biasing is to establish a Q-point about which variations in current and voltage can occur in response to an ac input signal. In applications where small signal voltages must be amplified—such as from an antenna or a microphone—variations about the Q-point are relatively small. Amplifiers designed to handle these small ac signals are often referred to as *small-signal amplifiers.*

After completing this section, you should be able to

- ❑ **Describe amplifier operation**
- ❑ Identify ac quantities
  - ◆ Distinguish ac quantities from dc quantities
- ❑ Discuss the operation of a linear amplifier
  - ◆ Define *phase inversion* ◆ Graphically illustrate amplifier operation
  - ◆ Analyze ac load line operation

HISTORY NOTE

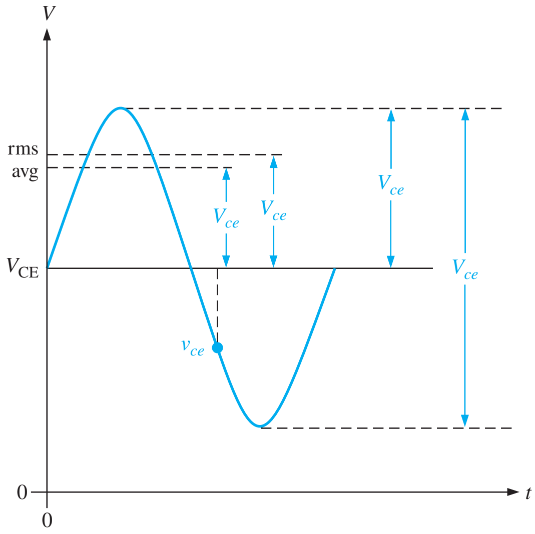
The American inventor Lee De Forest (1873–1961) is one of several pioneers of radio development. De Forest experimented with receiving long-distance radio signals and in 1907 patented an electronic device named the *audion,* which was the first amplifier. De Forest's new three-electrode (triode) vacuum tube boosted radio waves as they were received and made possible what was then called "wireless telephony," which allowed the human voice, music, or any broadcast signal to be heard.

AC Quantities

In the previous chapters, dc quantities were identified by nonitalic uppercase (capital) subscripts such as I_C, I_E, V_C, and V_{CE}. Lowercase italic subscripts are used to indicate ac quantities of rms, peak, and peak-to-peak currents and voltages: for example, I_c, I_e, I_b, V_c, and V_{ce} (rms values are assumed unless otherwise stated). Instantaneous quantities are represented by both lowercase letters and subscripts such as i_c, i_e, i_b, and v_{ce}. Figure 6–1 illustrates these quantities for a specific voltage waveform.

▶ FIGURE 6–1

V_{ce} can represent rms, average, peak, or peak-to-peak, but rms will be assumed unless stated otherwise. v_{ce} can be any instantaneous value on the curve.



In addition to currents and voltages, resistances often have different values when a circuit is analyzed from an ac viewpoint as opposed to a dc viewpoint. Lowercase subscripts are used to identify ac resistance values. For example, R_c is the ac collector resistance, and R_C is the dc collector resistance. You will see the need for this distinction later. Resistance values *internal* to the transistor use a lowercase r' to show it is an ac resistance. An example is the internal ac emitter resistance, r'_e.

The Linear Amplifier

A linear amplifier provides amplification of a signal without any distortion so that the output signal is an exact amplified replica of the input signal. A voltage-divider biased transistor with a sinusoidal ac source capacitively coupled to the base through C_1 and a load capacitively coupled to the collector through C_2 is shown in Figure 6–2. The coupling capacitors block dc and thus prevent the internal source resistance, R_s, and the load resistance, R_L, from changing the dc bias voltages at the base and collector. The capacitors ideally appear as shorts to the signal voltage. The sinusoidal source voltage causes the base voltage to vary sinusoidally above and below its dc bias level, V_{BQ}. The resulting variation in base current produces a larger variation in collector current because of the current gain of the transistor.

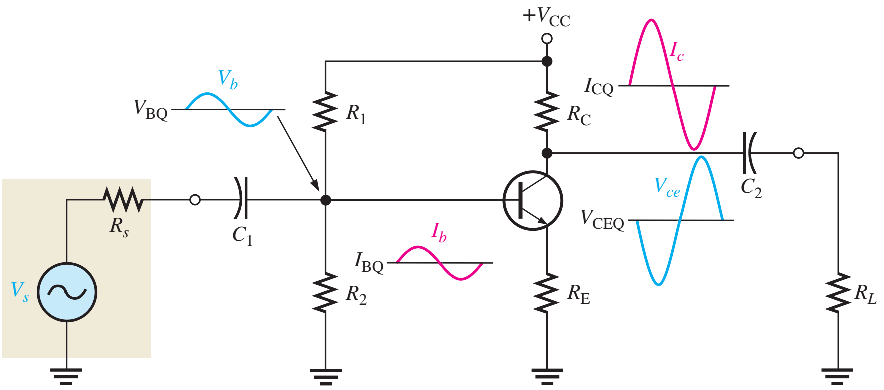


FIGURE 6–2

An amplifier with voltage-divider bias driven by an ac voltage source with an internal resistance, R_s.

As the sinusoidal collector current increases, the collector voltage decreases. The collector current varies above and below its Q-point value, I_{CQ}, in phase with the base current. The sinusoidal collector-to-emitter voltage varies above and below its Q-point value, V_{CEQ}, 180° out of phase with the base voltage, as illustrated in Figure 6–2. A transistor always produces a **phase inversion** between the base voltage and the collector voltage.

A Graphical Picture The operation just described can be illustrated graphically on the ac load line, as shown in Figure 6–3. The sinusoidal voltage at the base produces a base current that varies above and below the Q-point on the ac load line, as shown by the arrows.

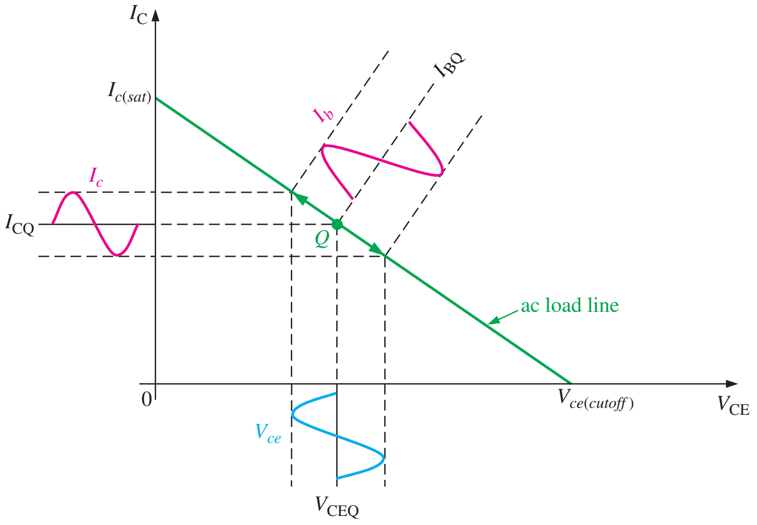


FIGURE 6–3

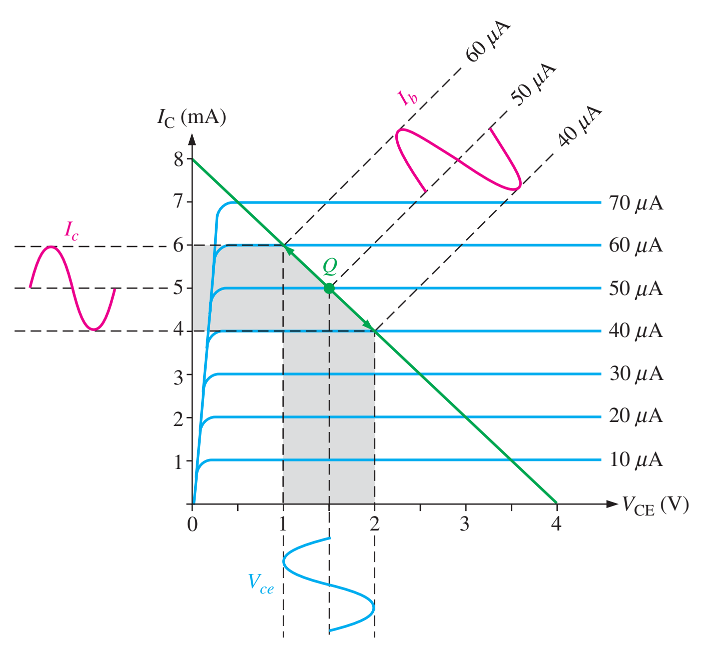
Graphical ac load line operation of the amplifier showing the variation of the base current, collector current, and collector-to-emitter voltage about their dc Q-point values. I_b and I_c are on different scales.

Lines projected from the peaks of the base current, across to the I_C axis, and down to the V_{CE} axis, indicate the peak-to-peak variations of the collector current and collector-to-emitter voltage, as shown. The ac load line differs from the dc load line because the effective ac collector resistance is R_L in parallel with R_C and is less than the dc collector resistance R_C alone. This difference between the dc and the ac load lines is covered in Chapter 7 in relation to power amplifiers.

EXAMPLE 6–1

The ac load line operation of a certain amplifier extends 10 μA above and below the Q-point base current value of 50 μA, as shown in Figure 6–4. Determine the resulting peak-to-peak values of collector current and collector-to-emitter voltage from the graph.

▶ FIGURE 6–4



Solution Projections on the graph of Figure 6–4 show the collector current varying from 6 mA to 4 mA for a peak-to-peak value of **2 mA** and the collector-to-emitter voltage varying from 1 V to 2 V for a peak-to-peak value of **1 V**.

Related Problem[*] What are the Q-point values of I_C and V_{CE} in Figure 6–4?

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

SECTION 6–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. When I_b is at its positive peak, I_c is at its _____ peak, and V_{ce} is at its _____ peak.
2. What is the difference between V_{CE} and V_{ce}?
3. What is the difference between R_e and r'_e?

6–2 TRANSISTOR AC MODELS

To visualize the operation of a transistor in an amplifier circuit, it is often useful to represent the device by a model circuit. A transistor model circuit uses various internal transistor parameters to represent its operation. Transistor models are described in this section based on resistance or *r* parameters. Another system of parameters, called *h* parameters, is briefly described.

After completing this section, you should be able to

- **Discuss transistor models**
- List and define the *r* parameters
- Describe the *r*-parameter transistor model
- Determine r'_e using a formula
- Compare ac beta and dc beta
- List and define the *h* parameters

r Parameters

The five *r* parameters commonly used for BJTs are given in Table 6–1. The italic lowercase letter *r* with a prime denotes resistances internal to the transistor.

▼ TABLE 6–1

r parameters.

r PARAMETER	DESCRIPTION
α_{ac}	ac alpha (I_c/I_e)
β_{ac}	ac beta (I_c/I_b)
r'_e	ac emitter resistance
r'_b	ac base resistance
r'_c	ac collector resistance

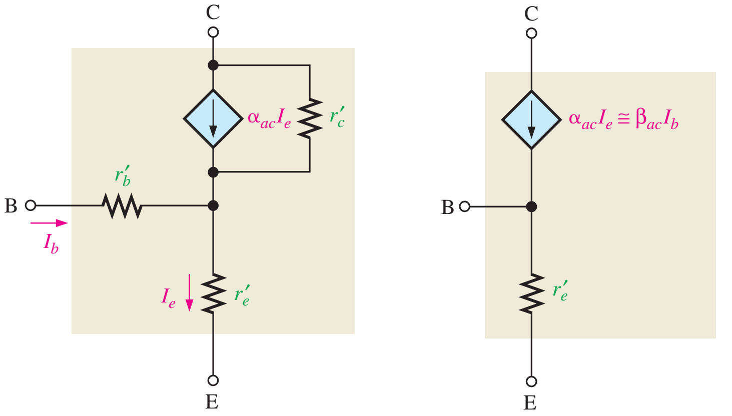
r-Parameter Transistor Model

An ***r*-parameter** model for a BJT is shown in Figure 6–5(a). For most general analysis work, it can be simplified as follows: The effect of the ac base resistance (r'_b) is usually small enough to neglect, so it can be replaced by a short. The ac collector resistance (r'_c) is usually several hundred kilohms and can be replaced by an open. The resulting simplified *r*-parameter equivalent circuit is shown in Figure 6–5(b).

The interpretation of this model circuit in terms of a transistor's ac operation is as follows: A resistance (r'_e) appears between the emitter and base terminals. This is the resistance "seen" looking into the emitter of a forward-biased transistor. The collector effectively acts as a dependent current source of $\alpha_{ac}I_e$ or, equivalently, $\beta_{ac}I_b$, represented by the diamond-shaped symbol. These factors are shown with a transistor symbol in Figure 6–6.

Determining r'_e by a Formula

For amplifier analysis, the ac emitter resistance, r'_e, is the most important of the *r* parameters. To calculate the approximate value of r'_e, you can use Equation 6–1, which is derived



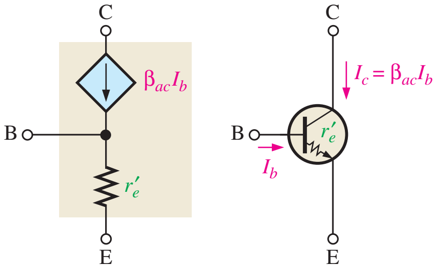
(a) Generalized *r*-parameter model for a BJT (b) Simplified *r*-parameter model for a BJT

▲ **FIGURE 6–5**

r-parameter transistor model.

▶ **FIGURE 6–6**

Relation of transistor symbol to *r*-parameter model.



assuming an abrupt junction between the *n* and *p* regions. It is also temperature dependent and is based on an ambient temperature of 20°C.

Equation 6–1

$$r'_e \cong \frac{25\text{ mV}}{I_E}$$

The numerator will be slightly larger for higher temperatures or transistors with a gradual (instead of an abrupt) junction. Although these cases will yield slightly different results, most designs are not critically dependent on the value of r'_e, and you will generally obtain excellent agreement with actual circuits using the equation as given. The derivation for Equation 6–1 can be found in “Derivations of Selected Equations” at www.pearsonhighered.com/floyd.

EXAMPLE 6–2

Determine the r'_e of a transistor that is operating with a dc emitter current of 2 mA.

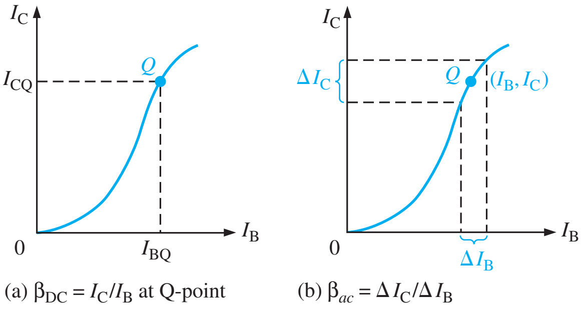
Solution

$$r'_e \cong \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{2\text{ mA}} = \mathbf{12.5\ \Omega}$$

Related Problem What is I_E if $r'_e = 8\ \Omega$?

Comparison of the AC Beta (β_{ac}) to the DC Beta (β_{DC})

For a typical transistor, a graph of I_C versus I_B is nonlinear, as shown in Figure 6–7(a). If you pick a Q-point on the curve and cause the base current to vary an amount ΔI_B, then the collector current will vary an amount ΔI_C as shown in part (b). At different points on the nonlinear curve, the ratio $\Delta I_C/\Delta I_B$ will be different, and it may also differ from the I_C/I_B ratio at the Q-point. Since $\beta_{DC} = I_C/I_B$ and $\beta_{ac} = \Delta I_C/\Delta I_B$, the values of these two quantities can differ slightly.



(a) $\beta_{DC} = I_C/I_B$ at Q-point (b) $\beta_{ac} = \Delta I_C/\Delta I_B$

◀ **FIGURE 6–7**

I_C-versus-I_B curve illustrates the difference between $\beta_{DC} = I_C/I_B$ and $\beta_{ac} = \Delta I_C/\Delta I_B$.

h Parameters

A manufacturer's datasheet typically specifies *h* (hybrid) parameters (h_i, h_r, h_f, and h_o) because they are relatively easy to measure.

The four basic ac *h* parameters and their descriptions are given in Table 6–2. Each of the four *h* parameters carries a second subscript letter to designate the common-emitter (*e*), common-base (*b*), or common-collector (*c*) amplifier configuration, as listed in Table 6–3. The term *common* refers to one of the three terminals (E, B, or C) that is referenced to ac ground for both input and output signals. The characteristics of each of these three BJT amplifier configurations are covered later in this chapter.

h PARAMETER	DESCRIPTION	CONDITION
h_i	Input impedance (resistance)	Output shorted
h_r	Voltage feedback ratio	Input open
h_f	Forward current gain	Output shorted
h_o	Output admittance (conductance)	Input open

◀ **TABLE 6–2**

Basic ac *h* parameters.

CONFIGURATION	*h* PARAMETERS
Common-Emitter	$h_{ie}, h_{re}, h_{fe}, h_{oe}$
Common-Base	$h_{ib}, h_{rb}, h_{fb}, h_{ob}$
Common-Collector	$h_{ic}, h_{rc}, h_{fc}, h_{oc}$

◀ **TABLE 6–3**

Subscripts of *h* parameters for each of the three amplifier configurations.

Relationships of *h* Parameters and *r* Parameters

The ac current ratios, α_{ac} and β_{ac}, convert directly from *h* parameters as follows:

$$\alpha_{ac} = h_{fb}$$
$$\beta_{ac} = h_{fe}$$

Because datasheets often provide only common-emitter h parameters, the following formulas show how to convert them to r parameters. We will use r parameters throughout the text because they are easier to apply and more practical.

$$r'_e = \frac{h_{re}}{h_{oe}}$$

$$r'_c = \frac{h_{re} + 1}{h_{oe}}$$

$$r'_b = h_{ie} - \frac{h_{re}}{h_{oe}}(1 + h_{fe})$$

SECTION 6–2
CHECKUP

1. Define each of the parameters: α_{ac}, β_{ac}, r'_e, r'_b, and r'_c.
2. Which h parameter is equivalent to β_{ac}?
3. If $I_E = 15$ mA, what is the approximate value of r'_e?

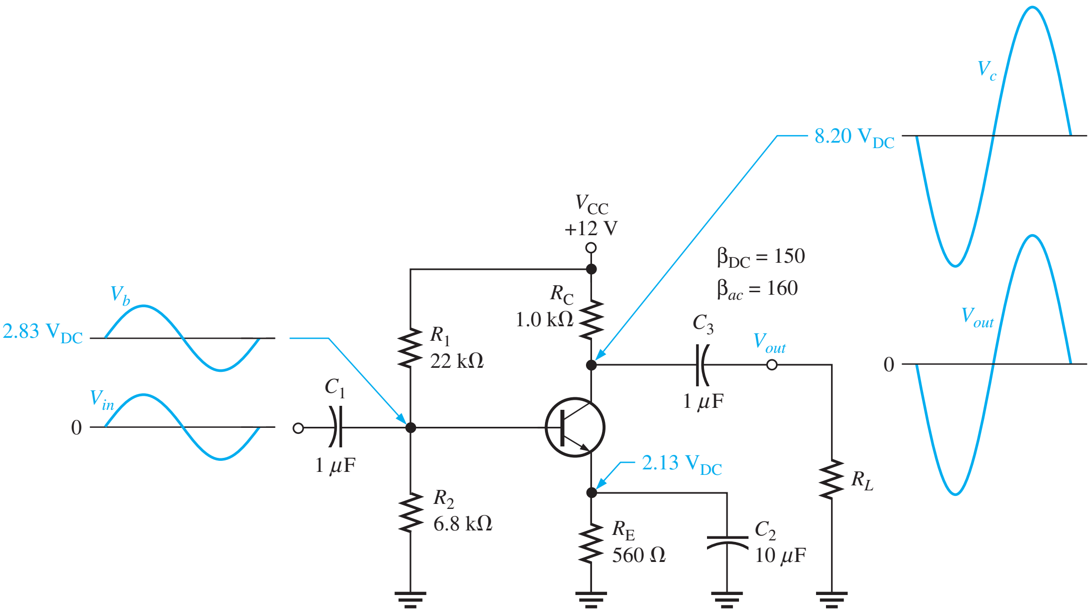
6–3 THE COMMON-EMITTER AMPLIFIER

As you have learned, a BJT can be represented in an ac model circuit. Three amplifier configurations are the common-emitter, the common-base, and the common-collector. The common-emitter (CE) configuration has the emitter as the common terminal, or ground, to an ac signal. CE amplifiers exhibit high voltage gain and high current gain. The common-collector and common-base configurations are covered in the sections 6–4 and 6–5.

After completing this section, you should be able to

- ❑ **Describe and analyze the operation of common-emitter amplifiers**
- ❑ Discuss a common-emitter amplifier with voltage-divider bias
  - ◆ Show input and output signals ◆ Discuss phase inversion
- ❑ Perform a dc analysis
  - ◆ Represent the amplifier by its dc equivalent circuit
- ❑ Perform an ac analysis
  - ◆ Represent the amplifier by its ac equivalent circuit ◆ Define *ac ground* ◆ Discuss the voltage at the base ◆ Discuss the input resistance at the base and the output resistance
- ❑ Analyze the amplifier for voltage gain
  - ◆ Define *attenuation* ◆ Define *bypass capacitor* ◆ Describe the effect of an emitter bypass capacitor on voltage gain ◆ Discuss voltage gain without a bypass capacitor ◆ Explain the effect of a load on voltage gain
- ❑ Discuss the stability of the voltage gain
  - ◆ Define *stability* ◆ Explain the purpose of swamping r'_e and the effect on input resistance
- ❑ Determine current gain and power gain

Figure 6–8 shows a **common-emitter** amplifier with voltage-divider bias and coupling capacitors C_1 and C_3 on the input and output and a bypass capacitor, C_2, from emitter to ground. The input signal, V_{in}, is capacitively coupled to the base terminal, the output signal, V_{out}, is capacitively coupled from the collector to the load. The amplified output is 180° out of phase with the input. Because the ac signal is applied to the base terminal as



▲ FIGURE 6–8

A common-emitter amplifier.

the input and taken from the collector terminal as the output, the emitter is common to both the input and output signals. There is no signal at the emitter because the bypass capacitor effectively shorts the emitter to ground at the signal frequency. All amplifiers have a combination of both ac and dc operation, which must be considered, but keep in mind that the common-emitter designation refers to the ac operation.

Phase Inversion The output signal is 180° out of phase with the input signal. As the input signal voltage changes, it causes the ac base current to change, resulting in a change in the collector current from its Q-point value. If the base current increases, the collector current increases above its Q-point value, causing an increase in the voltage drop across R_C. This increase in the voltage across R_C means that the voltage at the collector decreases from its Q-point. So, any change in input signal voltage results in an opposite change in collector signal voltage, which is a phase inversion.

DC Analysis

To analyze the amplifier in Figure 6–8, the dc bias values must first be determined. To do this, a dc equivalent circuit is developed by removing the coupling and bypass capacitors because they appear open as far as the dc bias is concerned. This also removes the load resistor and signal source. The dc equivalent circuit is shown in Figure 6–9.

Theveninizing the bias circuit and applying Kirchhoff's voltage law to the base-emitter circuit,

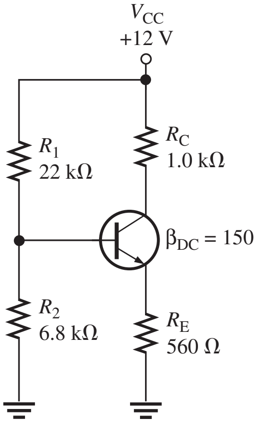
$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(6.8\text{ k}\Omega)(22\text{ k}\Omega)}{6.8\text{ k}\Omega + 22\text{ k}\Omega} = 5.19\text{ k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{6.8\text{ k}\Omega}{6.8\text{ k}\Omega + 22\text{ k}\Omega}\right)12\text{ V} = 2.83\text{ V}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{2.83\text{ V} - 0.7\text{ V}}{560\ \Omega + 34.6\ \Omega} = 3.58\text{ mA}$$

$$I_C \cong I_E = 3.58\text{ mA}$$

$$V_E = I_ER_E = (3.58\text{ mA})(560\ \Omega) = 2\text{ V}$$



▲ FIGURE 6–9

DC equivalent circuit for the amplifier in Figure 6–8.

$$V_B = V_E + 0.7\text{ V} = 2.7\text{ V}$$
$$V_C = V_{CC} - I_C R_C = 12\text{ V} - (3.58\text{ mA})(1.0\text{ k}\Omega) = 8.42\text{ V}$$
$$V_{CE} = V_C - V_E = 8.42\text{ V} - 2\text{ V} = 6.42\text{ V}$$

AC Analysis

To analyze the ac signal operation of an amplifier, an ac equivalent circuit is developed as follows:

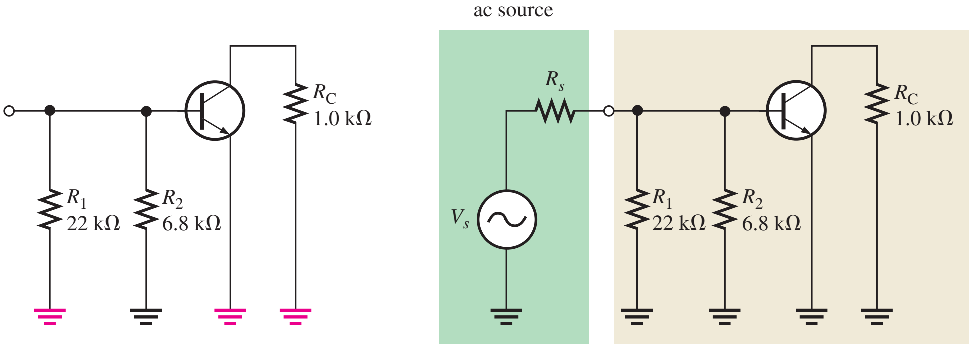
1. The capacitors C_1, C_2, and C_3 are replaced by effective shorts because their values are selected so that X_C is negligible at the signal frequency and can be considered to be 0 Ω.
2. The dc source is replaced by ground.

A dc voltage source has an internal resistance of near 0 Ω because it holds a constant voltage independent of the load (within limits); no ac voltage can be developed across it so it appears as an ac short. This is why a dc source is called an **ac ground**.

The ac equivalent circuit for the common-emitter amplifier in Figure 6–8 is shown in Figure 6–10(a). Notice that both R_C and R_1 have one end connected to ac ground (red) because, in the actual circuit, they are connected to V_{CC} which is, in effect, ac ground.

▶ **FIGURE 6–10**

AC equivalent circuit for the amplifier in Figure 6–8.



(a) Without an input signal voltage (AC ground is shown in red.)

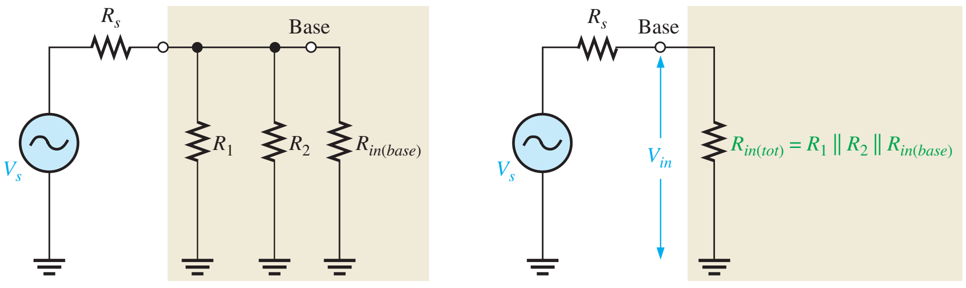
(b) With an input signal voltage

In ac analysis, the ac ground and the actual ground are treated as the same point electrically. The amplifier in Figure 6–8 is called a common-emitter amplifier because the bypass capacitor C_2 keeps the emitter at ac ground. Ground is the common point in the circuit.

Signal (AC) Voltage at the Base An ac voltage source, V_s, is shown connected to the input in Figure 6–10(b). If the internal resistance of the ac source is 0 Ω, then all of the source voltage appears at the base terminal. If, however, the ac source has a nonzero internal resistance, then three factors must be taken into account in determining the actual signal voltage at the base. These are the *source resistance* (R_s), the *bias resistance* ($R_1 \| R_2$), and the *ac input resistance* at the base of the transistor ($R_{in(base)}$). This is illustrated in Figure 6–11(a) and is simplified by combining R_1, R_2, and $R_{in(base)}$ in parallel to get the total **input resistance**, $R_{in(tot)}$, which is the resistance "seen" by an ac source connected to the input, as shown in Figure 6–11(b). A high value of input resistance is desirable so that the amplifier will not excessively load the signal source. This is opposite to the requirement for a stable Q-point, which requires smaller resistors. The conflicting requirement for high input resistance and stable biasing is but one of the many trade-offs that must be considered when choosing components for a circuit. The total input resistance is expressed by the following formula:

Equation 6–2

$$R_{in(tot)} = R_1 \| R_2 \| R_{in(base)}$$



(a)

(b)

◀ **FIGURE 6–11**

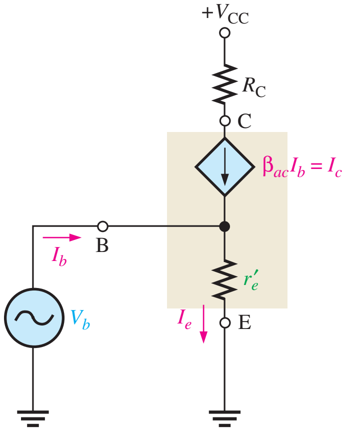
AC equivalent of the base circuit.

As you can see in the figure, the source voltage, V_s, is divided down by R_s (source resistance) and $R_{in(tot)}$ so that the signal voltage at the base of the transistor is found by the voltage-divider formula as follows:

$$V_b = \left(\frac{R_{in(tot)}}{R_s + R_{in(tot)}}\right)V_s$$

If $R_s \ll R_{in(tot)}$, then $V_b \cong V_s$ where V_b is the input voltage, V_{in}, to the amplifier.

Input Resistance at the Base To develop an expression for the ac input resistance looking in at the base, use the simplified r-parameter model of the transistor. Figure 6–12 shows the transistor model connected to the external collector resistor, R_C. The input resistance looking in at the base is



▲ **FIGURE 6–12**

r-parameter transistor model (inside shaded block) connected to external circuit.

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b}$$

The base voltage is

$$V_b = I_e r'_e$$

and since $I_e \cong I_c$,

$$I_b \cong \frac{I_e}{\beta_{ac}}$$

Substituting for V_b and I_b,

$$R_{in(base)} = \frac{V_b}{I_b} = \frac{I_e r'_e}{I_e/\beta_{ac}}$$

Cancelling I_e,

$$\boldsymbol{R_{in(base)} = \beta_{ac} r'_e}$$

Equation 6–3

Output Resistance The **output resistance** of the common-emitter amplifier is the resistance looking in at the collector and is approximately equal to the collector resistor.

$$\boldsymbol{R_{out} \cong R_C}$$

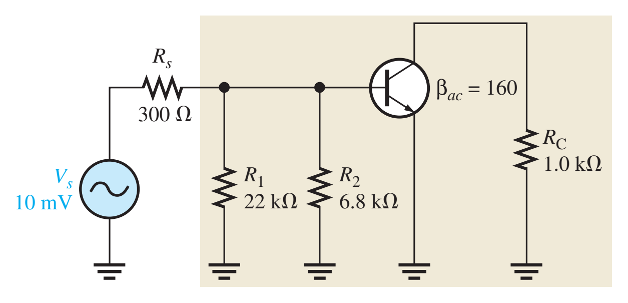
Equation 6–4

Actually, $R_{out} = R_C \parallel r'_c$, but since the internal ac collector resistance of the transistor, r'_c, is typically much larger than R_C, the approximation is usually valid.

EXAMPLE 6–3

Determine the signal voltage at the base of the transistor in Figure 6–13. This circuit is the ac equivalent of the amplifier in Figure 6–8 with a 10 mV rms, 300 Ω signal source. I_E was previously found to be 3.80 mA.

▶ FIGURE 6–13



Solution First, determine the ac emitter resistance.

$$r'_e \cong \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{3.80\text{ mA}} = 6.58\ \Omega$$

Then,

$$R_{in(base)} = \beta_{ac} r'_e = 160(6.58\ \Omega) = 1.05\text{ k}\Omega$$

Next, determine the total input resistance viewed from the source.

$$R_{in(tot)} = R_1 \| R_2 \| R_{in(base)} = \frac{1}{\dfrac{1}{22\text{ k}\Omega} + \dfrac{1}{6.8\text{ k}\Omega} + \dfrac{1}{1.05\text{ k}\Omega}} = 873\ \Omega$$

The source voltage is divided down by R_s and $R_{in(tot)}$, so the signal voltage at the base is the voltage across $R_{in(tot)}$.

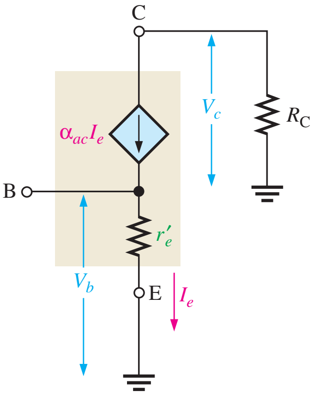
$$V_b = \left(\frac{R_{in(tot)}}{R_s + R_{in(tot)}}\right)V_s = \left(\frac{873\ \Omega}{1173\ \Omega}\right)10\text{ mV} = \mathbf{7.44\ mV}$$

As you can see, there is significant attenuation (reduction) of the source voltage due to the source resistance and amplifier's input resistance combining to act as a voltage divider.

Related Problem Determine the signal voltage at the base of Figure 6–13 if the source resistance is 75 Ω and another transistor with an ac beta of 200 is used.

Voltage Gain

The ac voltage gain expression for the common-emitter amplifier is developed using the model circuit in Figure 6–14. The gain is the ratio of ac output voltage at the collector (V_c) to ac input voltage at the base (V_b).



▲ FIGURE 6–14

Model circuit for obtaining ac voltage gain.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_b}$$

Notice in the figure that $V_c = \alpha_{ac} I_e R_C \cong I_e R_C$ and $V_b = I_e r'_e$. Therefore,

$$A_v = \frac{I_e R_C}{I_e r'_e}$$

The I_e terms cancel, so

Equation 6–5

$$\boldsymbol{A_v = \frac{R_C}{r'_e}}$$

Equation 6–5 is the voltage gain from base to collector. To get the overall gain of the amplifier from the source voltage to collector, the attenuation of the input circuit must be included.

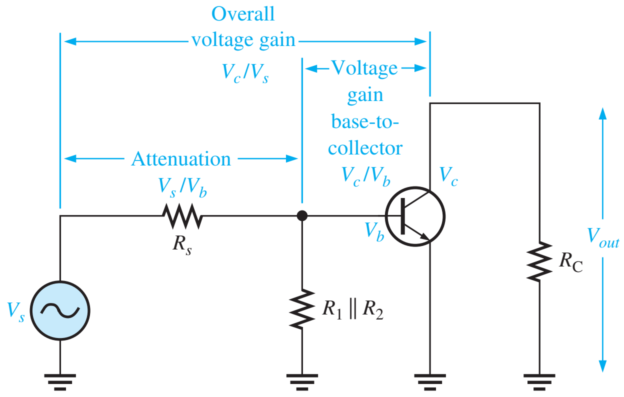
Attenuation is the reduction in signal voltage as it passes through a circuit and corresponds to a gain of less than 1. For example, if the signal amplitude is reduced by half, the attenuation is 2, which can be expressed as a gain of 0.5 because gain is the reciprocal of attenuation. Suppose a source produces a 10 mV input signal and the source resistance combined with the load resistance results in a 2 mV output signal. In this case, the attenuation is 10 mV/2 mV = 5. That is, the input signal is reduced by a factor of 5. This can be expressed in terms of gain as 1/5 = 0.2.

Assume that the amplifier in Figure 6–15 has a voltage gain from base to collector of A_v and the attenuation from the source to the base is V_s/V_b. This attenuation is produced by the source resistance and total input resistance of the amplifier acting as a voltage divider and can be expressed as

$$\text{Attenuation} = \frac{V_s}{V_b} = \frac{R_s + R_{in(tot)}}{R_{in(tot)}}$$

The overall voltage gain of the amplifier, A'_v, is the voltage gain from base to collector, V_c/V_b, times the reciprocal of the attenuation, V_b/V_s.

$$A'_v = \left(\frac{V_c}{V_b}\right)\left(\frac{V_b}{V_s}\right) = \frac{V_c}{V_s}$$



▲ **FIGURE 6–15**

Base circuit attenuation and overall voltage gain.

Effect of the Emitter Bypass Capacitor on Voltage Gain The emitter **bypass capacitor**, which is C_2 in Figure 6–8, provides an effective short to the ac signal around the emitter resistor, thus keeping the emitter at ac ground, as you have seen. With the bypass capacitor, the gain of a given amplifier is maximum and equal to R_C/r'_e.

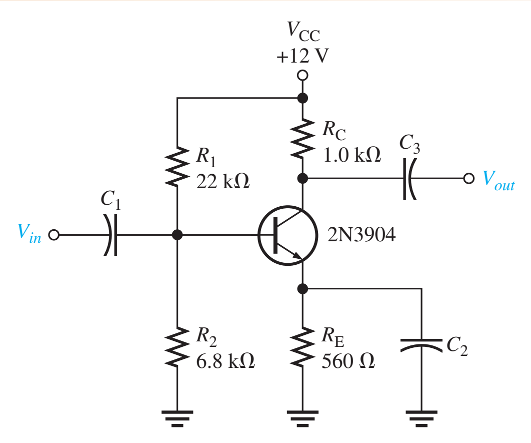
The value of the bypass capacitor must be large enough so that its reactance over the frequency range of the amplifier is very small (ideally 0 Ω) compared to R_E. A good rule-of-thumb is that the capacitive reactance, X_C, of the bypass capacitor should be at least 10 times smaller than R_E at the minimum frequency for which the amplifier must operate.

$$10X_C \leq R_E$$

EXAMPLE 6–4

Select a minimum value for the emitter bypass capacitor, C_2, in Figure 6–16 if the amplifier must operate over a frequency range from 200 Hz to 10 kHz.

▶ **FIGURE 6–16**



Solution The X_C of the bypass capacitor, C_2, should be at least ten times less than R_E.

$$X_{C2} = \frac{R_E}{10} = \frac{560\ \Omega}{10} = 56\ \Omega$$

Determine the capacitance value at the minimum frequency of 200 Hz as follows:

$$C_2 = \frac{1}{2\pi f X_{C2}} = \frac{1}{2\pi(200\text{ Hz})(56\ \Omega)} = \mathbf{14.2\ \mu F}$$

This is the minimum value for the bypass capacitor for this circuit. You can always use a larger value, although cost and physical size may impose limitations.

Related Problem If the minimum frequency is reduced to 100 Hz, what value of bypass capacitor must you use?

Voltage Gain Without the Bypass Capacitor To see how the bypass capacitor affects ac voltage gain, let's remove it from the circuit in Figure 6–16 and compare voltage gains.

Without the bypass capacitor, the emitter is no longer at ac ground. Instead, R_E is seen by the ac signal between the emitter and ground and effectively adds to r'_e in the voltage gain formula.

Equation 6–6

$$\boldsymbol{A_v = \frac{R_C}{r'_e + R_E}}$$

The effect of R_E is to decrease the ac voltage gain.

EXAMPLE 6–5

Calculate the base-to-collector voltage gain of the amplifier in Figure 6–16 both without and with an emitter bypass capacitor if there is no load resistor.

Solution From Example 6–3, $r'_e = 6.58\ \Omega$ for this same amplifier. Without C_2, the gain is

$$A_v = \frac{R_C}{r'_e + R_E} = \frac{1.0\text{ k}\Omega}{567\ \Omega} = \mathbf{1.76}$$

With C_2, the gain is

$$A_v = \frac{R_C}{r'_e} = \frac{1.0\,\text{k}\Omega}{6.58\,\Omega} = \mathbf{152}$$

As you can see, the bypass capacitor makes quite a difference.

Related Problem Determine the base-to-collector voltage gain in Figure 6–16 with R_E bypassed, for the following circuit values: $R_C = 1.8\,\text{k}\Omega$, $R_E = 1.0\,\text{k}\Omega$, $R_1 = 33\,\text{k}\Omega$, and $R_2 = 6.8\,\text{k}\Omega$.

Effect of a Load on the Voltage Gain A **load** is the amount of current drawn from the output of an amplifier or other circuit through a load resistance. When a resistor, R_L, is connected to the output through the coupling capacitor C_3, as shown in Figure 6–17(a), it creates a load on the circuit. The collector resistance at the signal frequency is effectively R_C in parallel with R_L. Remember, the upper end of R_C is effectively at ac ground. The ac equivalent circuit is shown in Figure 6–17(b). The total ac collector resistance is

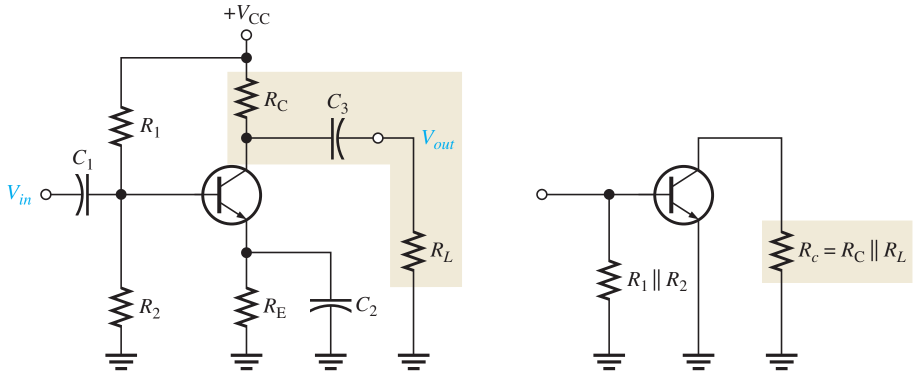
$$R_c = \frac{R_C R_L}{R_C + R_L}$$

Replacing R_C with R_c in the voltage gain expression gives

$$\boldsymbol{A_v = \frac{R_c}{r'_e}}$$

Equation 6–7

When $R_c < R_C$ because of R_L, the voltage gain is reduced. However, if $R_L \gg R_C$, then $R_c \cong R_C$ and the load has very little effect on the gain.



(a) Complete amplifier

(b) AC equivalent ($X_{C1} = X_{C2} = X_{C3} = 0$)

▲ FIGURE 6–17

A common-emitter amplifier with an ac (capacitively) coupled load.

EXAMPLE 6–6

Calculate the base-to-collector voltage gain of the amplifier in Figure 6–16 when a load resistance of 5 kΩ is connected to the output. The emitter is effectively bypassed and $r'_e = 6.58\,\Omega$.

Solution The ac collector resistance is

$$R_c = \frac{R_C R_L}{R_C + R_L} = \frac{(1.0\,\text{k}\Omega)(5\,\text{k}\Omega)}{6\,\text{k}\Omega} = 833\,\Omega$$

Therefore,

$$A_v = \frac{R_c}{r'_e} = \frac{833\ \Omega}{6.58\ \Omega} = \mathbf{127}$$

The unloaded gain was found to be 152 in Example 6–5.

Related Problem Determine the base-to-collector voltage gain in Figure 6–16 when a 10 kΩ load resistance is connected from collector to ground. Change the resistance values as follows: $R_C = 1.8\text{ k}\Omega$, $R_E = 1.0\text{ k}\Omega$, $R_1 = 33\text{ k}\Omega$, and $R_2 = 6.8\text{ k}\Omega$. The emitter resistor is effectively bypassed and $r'_e = 18.5\ \Omega$.

Stability of the Voltage Gain

Stability is a measure of how well an amplifier maintains its design values over changes in temperature or for a transistor with a different β. Although bypassing R_E does produce the maximum voltage gain, there is a stability problem because the ac voltage gain is dependent on r'_e since $A_v = R_C/r'_e$. Also, r'_e depends on I_E and on temperature. This causes the gain to be unstable over changes in temperature because when r'_e increases, the gain decreases and vice versa.

With no bypass capacitor, the gain is decreased because R_E is now in the ac circuit ($A_v = R_C/(r'_e + R_E)$). However, with R_E unbypassed, the gain is much less dependent on r'_e. If $R_E \gg r'_e$, the gain is essentially independent of r'_e because

$$A_v \cong \frac{R_C}{R_E}$$

Swamping r'_e to Stabilize the Voltage Gain

Swamping is a method used to minimize the effect of r'_e without reducing the voltage gain to its minimum value. This method "swamps" out the effect of r'_e on the voltage gain. Swamping is, in effect, a compromise between having a bypass capacitor across R_E and having no bypass capacitor at all.

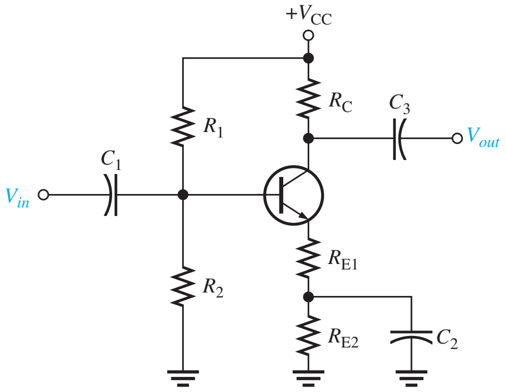
In a swamped amplifier, R_E is partially bypassed so that a reasonable gain can be achieved, and the effect of r'_e on the gain is greatly reduced or eliminated. The total external emitter resistance, R_E, is formed with two separate emitter resistors, R_{E1} and R_{E2}, as indicated in Figure 6–18. One of the resistors, R_{E2}, is bypassed and the other is not.

Both resistors ($R_{E1} + R_{E2}$) affect the dc bias while only R_{E1} affects the ac voltage gain.

$$A_v = \frac{R_C}{r'_e + R_{E1}}$$

▶ FIGURE 6–18

A swamped amplifier uses a partially bypassed emitter resistance to minimize the effect of r'_e on the gain in order to achieve gain stability.



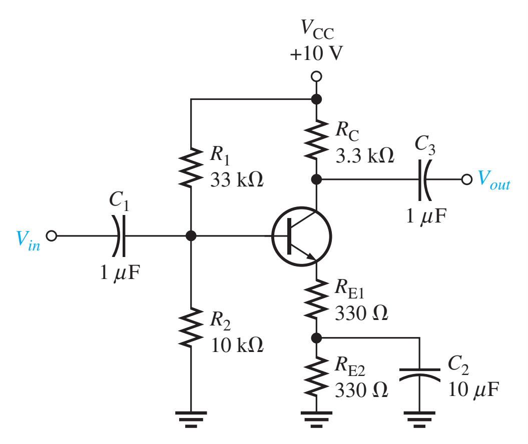
If R_{E1} is at least ten times larger than r'_e, then the effect of r'_e is minimized and the approximate voltage gain for the swamped amplifier is

$$\mathbf{A_v \cong \frac{R_C}{R_{E1}}}$$ Equation 6–8

EXAMPLE 6–7

Determine the voltage gain of the swamped amplifier in Figure 6–19. Assume that the bypass capacitor has a negligible reactance for the frequency at which the amplifier is operated. Assume $r'_e = 20\ \Omega$.

▶ FIGURE 6–19



Solution R_{E2} is bypassed by C_2. R_{E1} is more than ten times r'_e so the approximate voltage gain is

$$A_v \cong \frac{R_C}{R_{E1}} = \frac{3.3\text{ k}\Omega}{330\ \Omega} = \mathbf{10}$$

Related Problem What would be the voltage gain without C_2? What would be the voltage gain with C_2 bypassing both R_{E1} and R_{E2}?

The Effect of Swamping on the Amplifier's Input Resistance The ac input resistance, looking in at the base of a common-emitter amplifier with R_E completely bypassed, is $R_{in} = \beta_{ac}r'_e$. When the emitter resistance is partially bypassed, the portion of the resistance that is unbypassed is seen by the ac signal and results in an increase in the ac input resistance by appearing in series with r'_e. The formula is

$$\mathbf{R_{in(base)} = \beta_{ac}(r'_e + R_{E1})}$$ Equation 6–9

EXAMPLE 6–8

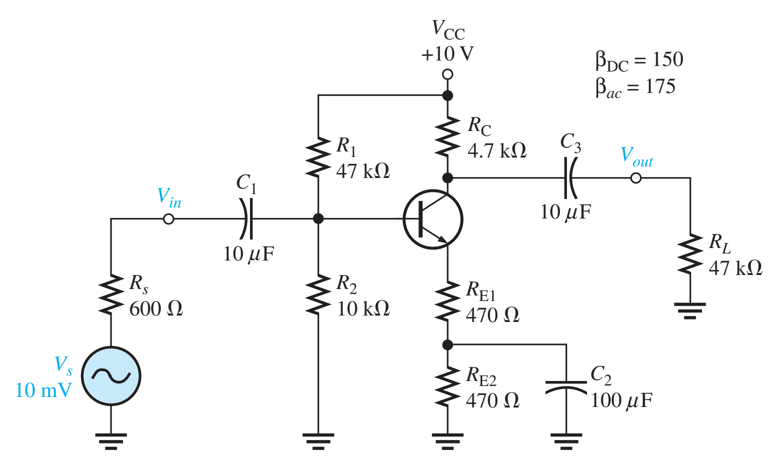
For the amplifier in Figure 6–20,

(a) Determine the dc collector voltage.

(b) Determine the ac collector voltage.

(c) Draw the total collector voltage waveform and the total output voltage waveform.

▶ FIGURE 6–20

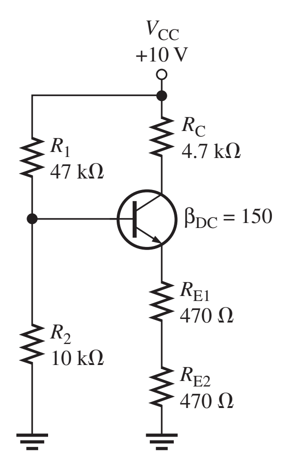


V_{CC}
+10 V
β_{DC} = 150
β_{ac} = 175
R_C
4.7 kΩ
R_1
47 kΩ
C_3
V_{out}
10 μF
C_1
V_{in}
10 μF
R_L
47 kΩ
R_s
600 Ω
R_2
10 kΩ
R_{E1}
470 Ω
V_s
10 mV
R_{E2}
470 Ω
C_2
100 μF

Solution **(a)** Determine the dc bias values using the dc equivalent circuit in Figure 6–21.

▶ FIGURE 6–21

DC equivalent for the circuit in Figure 6–20.



V_{CC}
+10 V
R_1
47 kΩ
R_C
4.7 kΩ
β_{DC} = 150
R_{E1}
470 Ω
R_2
10 kΩ
R_{E2}
470 Ω

Apply Thevenin's theorem and Kirchhoff's voltage law to the base-emitter circuit in Figure 6–21.

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(47\text{ k}\Omega)(10\text{ k}\Omega)}{47\text{ k}\Omega + 10\text{ k}\Omega} = 8.25\text{ k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\text{ k}\Omega}{47\text{ k}\Omega + 10\text{ k}\Omega}\right)10\text{ V} = 1.75\text{ V}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{1.75\text{ V} - 0.7\text{ V}}{940\ \Omega + 55\ \Omega} = 1.06\text{ mA}$$

$$I_C \cong I_E = 1.06\text{ mA}$$

$$V_E = I_E(R_{E1} + R_{E2}) = (1.06\text{ mA})(940\ \Omega) = 1\text{ V}$$

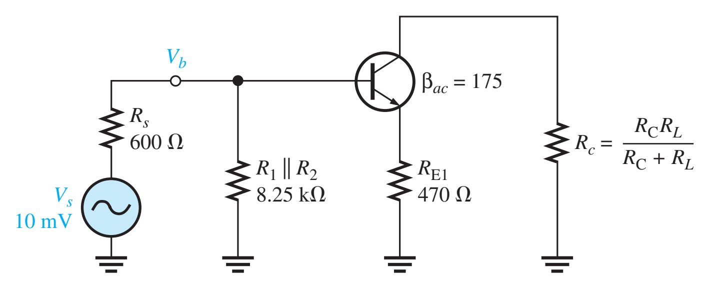
$$V_B = V_E + 0.7\text{ V} = 1\text{ V} - 0.7\text{ V} = 0.3\text{ V}$$

$$V_C = V_{CC} - I_CR_C = 10\text{ V} - (1.06\text{ mA})(4.7\text{ k}\Omega) = \mathbf{5.02\text{ V}}$$

(b) The ac analysis is based on the ac equivalent circuit in Figure 6–22.

FIGURE 6–22

AC equivalent for the circuit in Figure 6–20.



The first thing to do in the ac analysis is calculate r'_e.

$$r'_e \cong \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1.06\text{ mA}} = 23.6\ \Omega$$

Next, determine the attenuation in the base circuit. Looking from the 600 Ω source, the total R_{in} is

$$R_{in(tot)} = R_1 \| R_2 \| R_{in(base)}$$
$$R_{in(base)} = \beta_{ac}(r'_e + R_{E1}) = 175(494\ \Omega) = 86.5\text{ k}\Omega$$

Therefore,

$$R_{in(tot)} = 47\text{ k}\Omega \| 10\text{ k}\Omega \| 86.5\text{ k}\Omega = 7.53\text{ k}\Omega$$

The attenuation from source to base is

$$\text{Attenuation} = \frac{V_s}{V_b} = \frac{R_s + R_{in(tot)}}{R_{in(tot)}} = \frac{600\ \Omega + 7.53\text{ k}\Omega}{7.53\text{ k}\Omega} = 1.08$$

Before A_v can be determined, you must know the ac collector resistance R_c.

$$R_c = \frac{R_C R_L}{R_C + R_L} = \frac{(4.7\text{ k}\Omega)(47\text{ k}\Omega)}{4.7\text{ k}\Omega + 47\text{ k}\Omega} = 4.27\text{ k}\Omega$$

The voltage gain from base to collector is

$$A_v \cong \frac{R_c}{R_{E1}} = \frac{4.27\text{ k}\Omega}{470\ \Omega} = 9.09$$

The overall voltage gain is the reciprocal of the attenuation times the amplifier voltage gain.

$$A'_v = \left(\frac{V_b}{V_s}\right)A_v = (0.93)(9.09) = 8.45$$

The source produces 10 mV rms, so the rms voltage at the collector is

$$V_c = A'_v V_s = (8.45)(10\text{ mV}) = \mathbf{84.5\ mV}$$

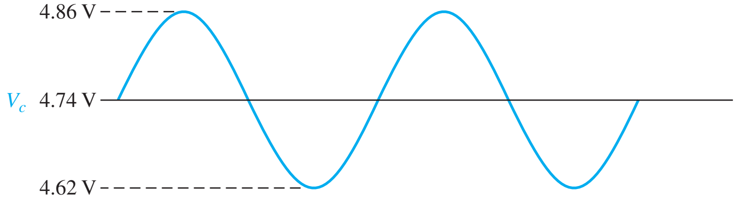
(c) The total collector voltage is the signal voltage of 84.5 mV rms riding on a dc level of 4.74 V, as shown in Figure 6–23(a), where approximate peak values are determined as follows:

$$\text{Max } V_{c(p)} = V_C + 1.414\,V_c = 4.74\text{ V} + (84.5\text{ mV})(1.414) = 4.86\text{ V}$$
$$\text{Min } V_{c(p)} = V_C - 1.414\,V_c = 4.74\text{ V} - (84.5\text{ mV})(1.414) = 4.62\text{ V}$$

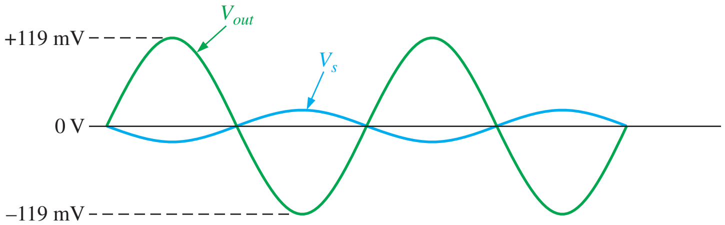
The coupling capacitor, C_3, keeps the dc level from getting to the output. So, V_{out} is equal to the ac component of the collector voltage ($V_{out(p)} = (84.5\text{ mV})(1.414) = 119\text{ mV}$),

FIGURE 6–23

Voltages for Figure 6–20.



(a) Total collector voltage



(b) Source and output ac voltages

as indicated in Figure 6–23(b). The source voltage, V_s, is shown to emphasize the phase inversion.

Related Problem What is A_v in Figure 6–20 with R_L removed?

Open the Multisim file E06-08 in the Examples folder on the companion website. Measure the dc and the ac values of the collector voltage and compare with the calculated values.

Current Gain

The current gain from base to collector is I_c/I_b or β_{ac}. However, the overall current gain of the common-emitter amplifier is

Equation 6–10

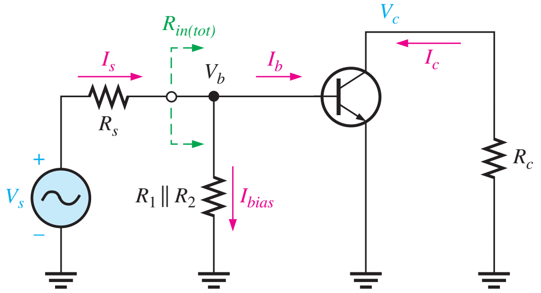
$$\boldsymbol{A_i = \frac{I_c}{I_s}}$$

I_s is the total signal input current produced by the source, part of which (I_b) is base current and part of which (I_{bias}) goes through the bias circuit ($R_1 \parallel R_2$), as shown in Figure 6–24. The source "sees" a total resistance of $R_s + R_{in(tot)}$. The total current produced by the source is

$$I_s = \frac{V_s}{R_s + R_{in(tot)}}$$

FIGURE 6–24

Signal currents (directions shown are for the positive half-cycle of V_s).



Power Gain

The overall power gain is the product of the overall voltage gain (A'_v) and the overall current gain (A_i).

$$A_p = A'_v A_i$$ Equation 6–11

where $A'_v = V_c/V_s$.

SECTION 6–3 CHECKUP

1. In the dc equivalent circuit of an amplifier, how are the capacitors treated?
2. When the emitter resistor is bypassed with a capacitor, how is the gain of the amplifier affected?
3. Explain swamping.
4. List the elements included in the total input resistance of a common-emitter amplifier.
5. What elements determine the overall voltage gain of a common-emitter amplifier?
6. When a load resistor is capacitively coupled to the collector of a CE amplifier, is the voltage gain increased or decreased?
7. What is the phase relationship of the input and output voltages of a CE amplifier?

6–4 THE COMMON-COLLECTOR AMPLIFIER

The **common-collector** (CC) amplifier is usually referred to as an emitter-follower (EF). The input is applied to the base through a coupling capacitor, and the output is at the emitter. The voltage gain of a CC amplifier is approximately 1, and its main advantages are its high input resistance and current gain.

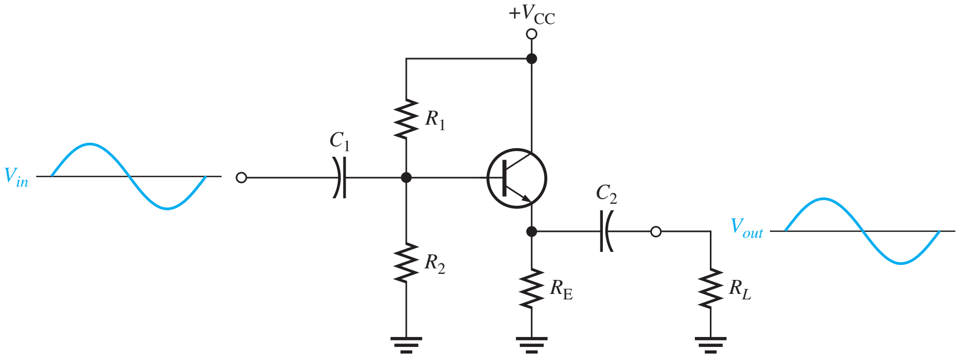
After completing this section, you should be able to

- **Describe and analyze the operation of common-collector amplifiers**
- Discuss the emitter-follower amplifier with voltage-divider bias
- Analyze the amplifier for voltage gain
    - Explain the term *emitter-follower*
- Discuss and calculate input resistance
- Determine output resistance
- Determine current gain
- Determine power gain
- Describe the Darlington pair
    - Discuss an application
- Discuss the Sziklai pair

An **emitter-follower** circuit with voltage-divider bias is shown in Figure 6–25. Notice that the input signal is capacitively coupled to the base, the output signal is capacitively coupled from the emitter, and the collector is at ac ground. There is no phase inversion, and the output is approximately the same amplitude as the input.

▶ FIGURE 6–25

Emitter-follower with voltage-divider bias.



Voltage Gain

As in all amplifiers, the voltage gain is $A_v = V_{out}/V_{in}$. The capacitive reactances are assumed to be negligible at the frequency of operation. For the emitter-follower, as shown in the ac model in Figure 6–26,

$$V_{out} = I_eR_e$$

and

$$V_{in} = I_e(r'_e + R_e)$$

Therefore, the voltage gain is

$$A_v = \frac{I_eR_e}{I_e(r'_e + R_e)}$$

The I_e current terms cancel, and the base-to-emitter voltage gain expression simplifies to

$$A_v = \frac{R_e}{r'_e + R_e}$$

where R_e is the parallel combination of R_E and R_L. If there is no load, then $R_e = R_E$. Notice that the gain is always less than 1. If $R_e \gg r'_e$, then a good approximation is

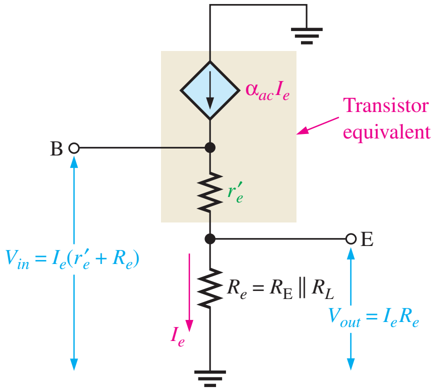
Equation 6–12

$$\mathbf{A_v \cong 1}$$

Since the output voltage is at the emitter, it is in phase with the base voltage, so there is no inversion from input to output. Because there is no inversion and because the voltage gain is approximately 1, the output voltage closely follows the input voltage in both phase and amplitude; thus the term *emitter-follower.*

▶ FIGURE 6–26

Emitter-follower model for voltage gain derivation.



Input Resistance

The emitter-follower is characterized by a high input resistance; this is what makes it a useful circuit. Because of the high input resistance, it can be used as a buffer to minimize loading effects when a circuit is driving a low-resistance load. The derivation of the input resistance, looking in at the base of the common-collector amplifier, is similar to that for the common-emitter amplifier. In a common-collector circuit, however, the emitter resistor is *never* bypassed because the output is taken across R_e, which is R_E in parallel with R_L.

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b} = \frac{I_e(r'_e + R_e)}{I_b}$$

Since $I_e \cong I_c = \beta_{ac}I_b$,

$$R_{in(base)} \cong \frac{\beta_{ac}I_b(r'_e + R_e)}{I_b}$$

The I_b terms cancel; therefore,

$$R_{in(base)} \cong \beta_{ac}(r'_e + R_e)$$

If $R_e \gg r'_e$, then the input resistance at the base is simplified to

$$\boldsymbol{R_{in(base)} \cong \beta_{ac}R_e}$$

Equation 6–13

The bias resistors in Figure 6–25 appear in parallel with $R_{in(base)}$, looking from the input source; and just as in the common-emitter circuit, the total input resistance is

$$R_{in(tot)} = R_1 \parallel R_2 \parallel R_{in(base)}$$

Output Resistance

With the load removed, the output resistance, looking into the emitter of the emitter-follower, is approximated as follows:

$$\boldsymbol{R_{out} \cong \left(\frac{R_s}{\beta_{ac}}\right) \parallel R_E}$$

Equation 6–14

R_s is the resistance of the input source. The derivation of Equation 6–14, found in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd, is relatively involved and several assumptions have been made. The output resistance is very low, making the emitter-follower useful for driving low-resistance loads.

Current Gain

The current gain for the emitter-follower in Figure 6–25 is

$$\boldsymbol{A_i = \frac{I_e}{I_{in}}}$$

Equation 6–15

where $I_{in} = V_{in}/R_{in(tot)}$.

Power Gain

The common-collector power gain is the product of the voltage gain and the current gain. For the emitter-follower, the power gain is approximately equal to the current gain because the voltage gain is approximately 1.

$$A_p = A_v A_i$$

Since $A_v \cong 1$, the power gain is

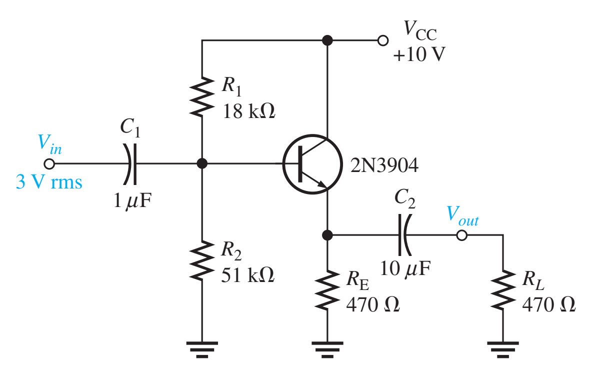
$$\boldsymbol{A_p \cong A_i}$$

Equation 6–16

EXAMPLE 6–9

Determine the total input resistance of the emitter-follower in Figure 6–27. Also find the voltage gain, current gain, and power gain in terms of power delivered to the load, R_L. Assume $\beta_{ac} = 175$ and that the capacitive reactances are negligible at the frequency of operation.

▶ FIGURE 6–27



Solution The ac emitter resistance external to the transistor is

$$R_e = R_E \parallel R_L = 470\ \Omega \parallel 470\ \Omega = 235\ \Omega$$

The approximate resistance, looking in at the base, is

$$R_{in(base)} \cong \beta_{ac}R_e = (175)(235\ \Omega) = 41.1\ \text{k}\Omega$$

The total input resistance is

$$R_{in(tot)} = R_1 \parallel R_2 \parallel R_{in(base)} = 18\ \text{k}\Omega \parallel 51\ \text{k}\Omega \parallel 41.1\ \text{k}\Omega = \mathbf{10.1\ k\Omega}$$

The voltage gain is $A_v \cong 1$. By using r'_e, you can determine a more precise value of A_v if necessary.

$$V_E = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} - V_{BE} = \left(\frac{51\ \text{k}\Omega}{18\ \text{k}\Omega + 51\ \text{k}\Omega}\right)10\ \text{V} - 0.7\ \text{V}$$
$$= (0.739)(10\ \text{V}) - 0.7\ \text{V} = 6.69\ \text{V}$$

Therefore,

$$I_E = \frac{V_E}{R_E} = \frac{6.69\ \text{V}}{470\ \Omega} = 14.2\ \text{mA}$$

and

$$r'_e \cong \frac{25\ \text{mV}}{I_E} = \frac{25\ \text{mV}}{14.2\ \text{mA}} = 1.76\ \Omega$$

So,

$$A_v = \frac{R_e}{r'_e + R_e} = \frac{235\ \Omega}{237\ \Omega} = \mathbf{0.992}$$

The small difference in A_v as a result of considering r'_e is insignificant in most cases.

The current gain is $A_i = I_e/I_{in}$. The calculations are as follows:

$$I_e = \frac{V_e}{R_e} = \frac{A_vV_b}{R_e} \cong \frac{(0.992)(3\ \text{V})}{235\ \Omega} = \frac{2.98\ \text{V}}{235\ \Omega} = 12.7\ \text{mA}$$

$$I_{in} = \frac{V_{in}}{R_{in(tot)}} = \frac{3\ \text{V}}{10.1\ \text{k}\Omega} = 297\ \mu\text{A}$$

$$A_i = \frac{I_e}{I_{in}} = \frac{12.7\ \text{mA}}{297\ \mu\text{A}} = \mathbf{42.8}$$

The power gain is

$$A_p \cong A_i = 42.8$$

Since $R_L = R_E$, one-half of the power is dissipated in R_E and one-half in R_L. Therefore, in terms of power to the load, the power gain is

$$A_{p(load)} = \frac{A_p}{2} = \frac{42.8}{2} = \mathbf{21.4}$$

Related Problem If R_L in Figure 6–27 is decreased in value, does power gain to the load increase or decrease?

Open the Multisim file E06-09 in the Examples folder on the companion website. Measure the voltage gain and compare with the calculated value.

The Darlington Pair

As you have seen, β_{ac} is a major factor in determining the input resistance of an amplifier. The β_{ac} of the transistor limits the maximum achievable input resistance you can get from a given emitter-follower circuit.

One way to boost input resistance is to use a **Darlington pair,** as shown in Figure 6–28. The collectors of two transistors are connected, and the emitter of the first drives the base of the second. This configuration achieves β_{ac} multiplication as shown in the following steps. The emitter current of the first transistor is

$$I_{e1} \cong \beta_{ac1} I_{b1}$$

This emitter current becomes the base current for the second transistor, producing a second emitter current of

$$I_{e2} \cong \beta_{ac2} I_{e1} = \beta_{ac1}\beta_{ac2} I_{b1}$$

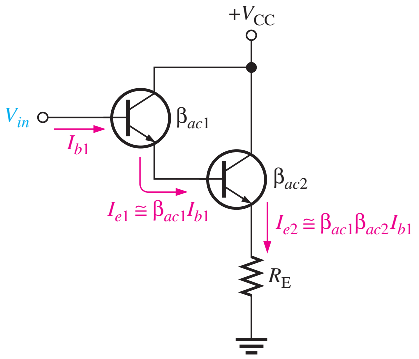
Therefore, the effective current gain of the Darlington pair is

$$\beta_{ac} = \beta_{ac1}\beta_{ac2}$$

Neglecting r'_e by assuming that it is much smaller than R_E, the input resistance is

$$\boldsymbol{R_{in} = \beta_{ac1}\beta_{ac2}R_E}$$

Equation 6–17


$+V_{CC}$
V_{in}
I_{b1}
β_{ac1}
β_{ac2}
$I_{e1} \cong \beta_{ac1} I_{b1}$
$I_{e2} \cong \beta_{ac1}\beta_{ac2} I_{b1}$
R_E

◀ FIGURE 6–28

A Darlington pair multiplies β_{ac}.

An Application The emitter-follower is often used as an interface between a circuit with a high output resistance and a low-resistance load. In such an application, the emitter-follower is called a *buffer.*

HISTORY NOTE

Sidney Darlington (1906–1997) was a renowned electrical engineer, whose name lives on through the transistor configuration he patented in 1953. He also had inventions in chirp radar, bombsights, and gun and rocket guidance. In 1945, he was awarded the Presidential Medal of Freedom and in 1975, he received IEEE's Edison Medal "for basic contributions to network theory and for important inventions in radar systems and electronic circuits" and the IEEE Medal of Honor in 1981 "for fundamental contributions to filtering and signal processing leading to chirp radar."

Suppose a common-emitter amplifier with a 1.0 kΩ collector resistance must drive a low-resistance load such as an 8 Ω low-power speaker. If the speaker is capacitively coupled to the output of the amplifier, the 8 Ω load appears—to the ac signal—in parallel with the 1.0 kΩ collector resistor. This results in an ac collector resistance of

$$R_c = R_C \| R_L = 1.0\,\text{k}\Omega \,\|\, 8\,\Omega = 7.94\,\Omega$$

Obviously, this is not acceptable because most of the voltage gain is lost ($A_v = R_c/r'_e$). For example, if $r'_e = 5\,\Omega$, the voltage gain is reduced from

$$A_v = \frac{R_C}{r'_e} = \frac{1.0\,\text{k}\Omega}{5\,\Omega} = 200$$

with no load to

$$A_v = \frac{R_c}{r'_e} = \frac{7.94\,\Omega}{5\,\Omega} = 1.59$$

with an 8 Ω speaker load.

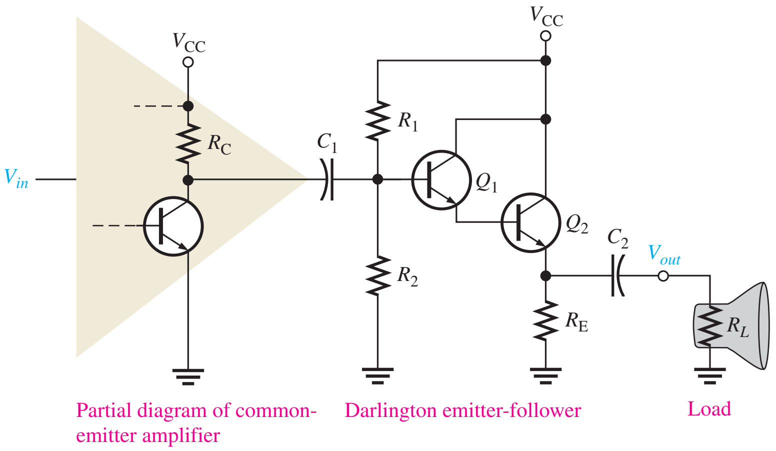
An emitter-follower using a Darlington pair can be used to interface the amplifier and the speaker, as shown in Figure 6–29.

F Y I

The circuit arrangement in Figure 6–29 is useful for low-power applications (<1 W load power) but is inefficient and wasteful for higher power requirements.

▶ **FIGURE 6–29**

A Darlington emitter-follower used as a buffer between a common-emitter amplifier and a low-resistance load such as a speaker.



EXAMPLE 6–10

In Figure 6–29 for the common-emitter amplifier, $V_{CC} = 12\text{ V}$, $R_C = 1.0\,\text{k}\Omega$ and $r'_e = 5\,\Omega$. For the Darlington emitter-follower, $R_1 = 10\,\text{k}\Omega$, $R_2 = 22\,\text{k}\Omega$, $R_E = 22\,\Omega$, $R_L = 8\,\Omega$, $V_{CC} = 12\text{ V}$, and $\beta_{DC} = \beta_{ac} = 100$ for each transistor. Neglect $R_{IN(BASE)}$ of the Darlington.

(a) Determine the voltage gain of the common-emitter amplifier.

(b) Determine the voltage gain of the Darlington emitter-follower.

(c) Determine the overall voltage gain and compare to the gain of the common-emitter amplifier driving the speaker directly without the Darlington emitter-follower.

Solution **(a)** To determine A_v for the common-emitter amplifier, first find r'_e for the Darlington emitter-follower.

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{22\,\text{k}\Omega}{32\,\text{k}\Omega}\right)12\text{ V} = 8.25\text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{V_B - 2V_{BE}}{R_E} = \frac{8.25\text{ V} - 1.4\text{ V}}{22\,\Omega} = \frac{6.85\text{ V}}{22\,\Omega} = 311\text{ mA}$$

$$r'_e = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{311\text{ mA}} = 80\text{ m}\Omega$$

Note that R_E must dissipate a power of

$$P_{R_E} = I_E^2 R_E = (311\text{ mA})^2(22\ \Omega) = 2.13\text{ W}$$

and transistor Q_2 must dissipate

$$P_{Q2} = (V_{CC} - V_E)I_E = (5.4\text{ V})(311\text{ mA}) = 1.68\text{ W}$$

Next, the ac emitter resistance of the Darlington emitter-follower is

$$R_e = R_E \parallel R_L = 22\ \Omega \parallel 8\ \Omega = 5.87\ \Omega$$

The total input resistance of the Darlington emitter-follower is

$$\begin{aligned} R_{in(tot)} &= R_1 \parallel R_2 \parallel \beta_{ac}^2(r'_e + R_e) \\ &= 10\text{ k}\Omega \parallel 22\text{ k}\Omega \parallel 100^2(80\text{ m}\Omega + 5.87\ \Omega) = 6.16\text{ k}\Omega \end{aligned}$$

The effective ac collector resistance of the common-emitter amplifier is

$$R_c = R_C \parallel R_{in(tot)} = 1.0\text{ k}\Omega \parallel 6.16\text{ k}\Omega = 860\ \Omega$$

The voltage gain of the common-emitter amplifier is

$$A_v = \frac{R_c}{r'_e} = \frac{860\ \Omega}{5\ \Omega} = \mathbf{172}$$

(b) The effective ac emitter resistance was found in part (a) to be 5.87 Ω. The voltage gain for the Darlington emitter-follower is

$$A_v = \frac{R_e}{r'_e + R_e} = \frac{5.87\ \Omega}{80\text{ m}\Omega + 5.87\ \Omega} = \mathbf{0.99}$$

(c) The overall voltage gain is

$$A'_v = A_{v(\text{EF})}A_{v(\text{CE})} = (0.99)(172) = \mathbf{170}$$

If the common-emitter amplifier drives the speaker directly, the gain is 1.59 as we previously calculated.

Related Problem Using the same circuit values, determine the voltage gain of the common-emitter amplifier in Figure 6–29 if a single transistor is used in the emitter-follower in place of the Darlington pair. Assume $\beta_{DC} = \beta_{ac} = 100$. Explain the difference in the voltage gain without the Darlington pair.

The Sziklai Pair

The **Sziklai pair,** shown in Figure 6–30, is similar to the Darlington pair except that it consists of two types of transistors, an *npn* and a *pnp*. This configuration is sometimes

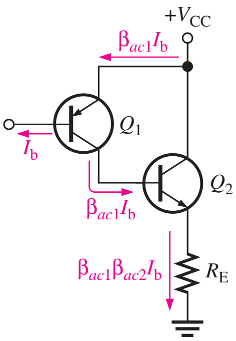


FIGURE 6–30

The Sziklai pair.

HISTORY NOTE

George Clifford Sziklai, born in Hungary in 1909, was an electronics engineer, who emigrated to New York in 1930. Among many other contributions to radio and TV, he invented the transistor configuration named after him, the *Sziklai pair,* also known as the complementary Darlington. Sziklai is also credited with constructing the first image orthicon television camera and inventing a high-speed elevator in addition to some 200 other patents.

known as a *complementary Darlington* or a *compound transistor.* The current gain is about the same as in the Darlington pair, as illustrated. The difference is that the Q_2 base current is the Q_1 collector current instead of emitter current, as in the Darlington arrangement.

An advantage of the Sziklai pair, compared to the Darlington, is that it takes less voltage to turn it on because only one barrier potential has to be overcome. A Sziklai pair is sometimes used in conjunction with a Darlington pair as the output stage of power amplifiers. In this case, the output power transistors are both the same type (two *npn* or two *pnp* transistors). This makes it easier to obtain exact matches of the output transistors, resulting in improved thermal stability and better sound quality in audio applications.

SECTION 6–4 CHECKUP

1. What is a common-collector amplifier called?
2. What is the ideal maximum voltage gain of a common-collector amplifier?
3. What characteristic of the common-collector amplifier makes it a useful circuit?

6–5 THE COMMON-BASE AMPLIFIER

The common-base (CB) amplifier provides high voltage gain with a maximum current gain of 1. Since it has a low input resistance, the CB amplifier is the most appropriate type for certain applications where sources tend to have very low-resistance outputs.

After completing this section, you should be able to

- **Describe and analyze the operation of common-base amplifiers**
- Determine the voltage gain
  - Explain why there is no phase inversion
- Discuss and calculate input resistance
- Determine output resistance
- Determine current gain
- Determine power gain

A typical **common-base** amplifier is shown in Figure 6–31. The base is the common terminal and is at ac ground because of capacitor C_2. The input signal is capacitively coupled to the emitter. The output is capacitively coupled from the collector to a load resistor.

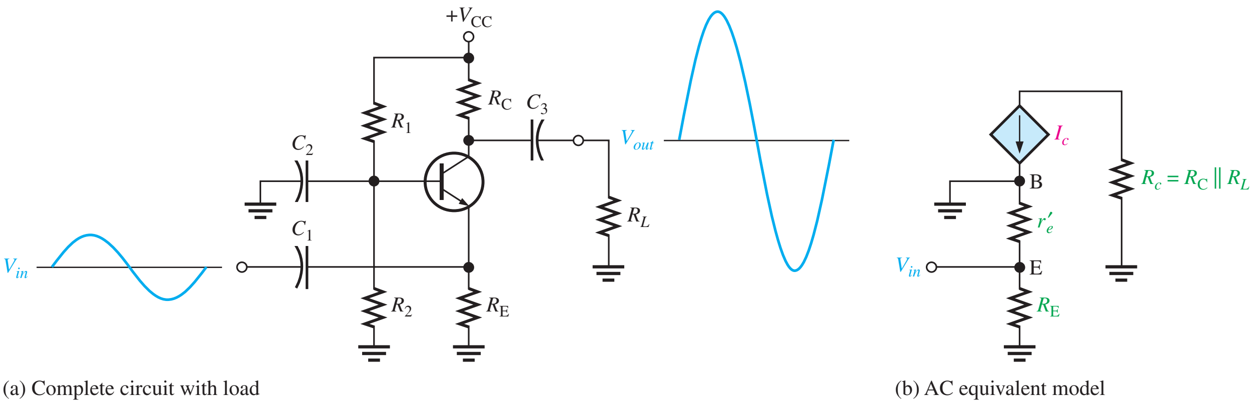
FYI

The CB amplifier is useful at high frequencies when impedance matching is required because input impedance can be controlled and because noninverting amps have better frequency response.

Voltage Gain

The voltage gain from emitter to collector is developed as follows ($V_{in} = V_e, V_{out} = V_c$).

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_e} = \frac{I_c R_c}{I_e(r'_e \parallel R_E)} \cong \frac{I_e R_c}{I_e(r'_e \parallel R_E)}$$



(a) Complete circuit with load

(b) AC equivalent model

FIGURE 6–31

Common-base amplifier with voltage-divider bias.

If $R_E \gg r'_e$, then

$$\mathbf{A_v \cong \frac{R_c}{r'_e}}$$ **Equation 6–18**

where $R_c = R_C \parallel R_L$. Notice that the gain expression is the same as for the common-emitter amplifier. However, there is no phase inversion from emitter to collector.

Input Resistance

The resistance, looking in at the emitter, is

$$R_{in(emitter)} = \frac{V_{in}}{I_{in}} = \frac{V_e}{I_e} = \frac{I_e(r'_e \parallel R_E)}{I_e}$$

If $R_E \gg r'_e$, then

$$\mathbf{R_{in(emitter)} \cong r'_e}$$ **Equation 6–19**

R_E is typically much greater than r'_e, so the assumption that $r'_e \parallel R_E \cong r'_e$ is usually valid. The input resistance can be set to a desired value by using a swamping resistor.

Output Resistance

Looking into the collector, the ac collector resistance, r'_c, appears in parallel with R_C. As you have previously seen in connection with the CE amplifier, r'_c is typically much larger than R_C, so a good approximation for the output resistance is

$$\mathbf{R_{out} \cong R_C}$$ **Equation 6–20**

Current Gain

The current gain is the output current divided by the input current. I_c is the ac output current, and I_e is the ac input current. Since $I_c \cong I_e$, the current gain is approximately 1.

$$\mathbf{A_i \cong 1}$$ **Equation 6–21**

Power Gain

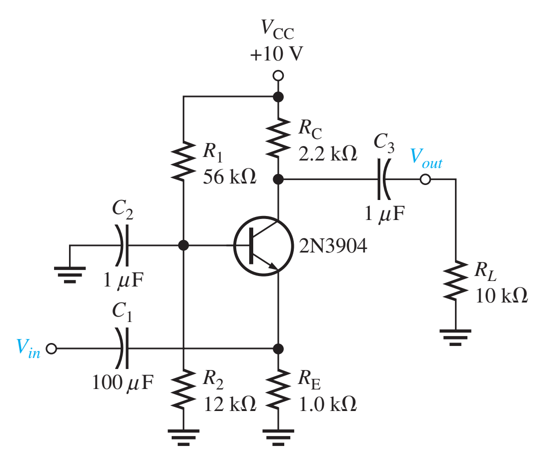
Since the current gain is approximately 1 for the common-base amplifier and $A_p = A_v A_i$, the power gain is approximately equal to the voltage gain.

$$\mathbf{A_p \cong A_v}$$ **Equation 6–22**

EXAMPLE 6–11

Find the input resistance, voltage gain, current gain, and power gain for the amplifier in Figure 6–32. $\beta_{DC} = 250$.

▶ FIGURE 6–32



Solution First, find I_E so that you can determine r'_e. Then $R_{in} \cong r'_e$.

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(56\,\text{k}\Omega)(12\,\text{k}\Omega)}{56\,\text{k}\Omega + 12\,\text{k}\Omega} = 9.88\,\text{k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{12\,\text{k}\Omega}{56\,\text{k}\Omega + 12\,\text{k}\Omega}\right)10\text{ V} = 1.76\text{ V}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{1.76\text{ V} - 0.7\text{ V}}{1.0\,\text{k}\Omega + 39.5\,\Omega} = 1.02\text{ mA}$$

Therefore,

$$R_{in} \cong r'_e = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1.02\text{ mA}} = \mathbf{24.5\,\Omega}$$

Calculate the voltage gain as follows:

$$R_c = R_C \parallel R_L = 2.2\,\text{k}\Omega \parallel 10\,\text{k}\Omega = 1.8\,\text{k}\Omega$$

$$A_v = \frac{R_c}{r'_e} = \frac{1.8\,\text{k}\Omega}{24.5\,\Omega} = \mathbf{73.5}$$

Also, $A_i \cong$ **1** and $A_p \cong A_v =$ **76.3.**

Related Problem Find A_v in Figure 6–32 if $\beta_{DC} = 50$.

Open the Multisim file E06-11 in the Examples folder on the companion website. Measure the voltage gain and compare with the calculated value.

SECTION 6–5 CHECKUP

1. Can the same voltage gain be achieved with a common-base as with a common-emitter amplifier?
2. Does the common-base amplifier have a low or a high input resistance?
3. What is the maximum current gain in a common-base amplifier?

6–6 MULTISTAGE AMPLIFIERS

Two or more amplifiers can be connected in a **cascaded** arrangement with the output of one amplifier driving the input of the next. Each amplifier in a cascaded arrangement is known as a **stage.** The basic purpose of a multistage arrangement is to increase the overall voltage gain. Although discrete multistage amplifiers are not as common as they once were, a familiarization with this area provides insight into how circuits affect each other when they are connected together.

After completing this section, you should be able to

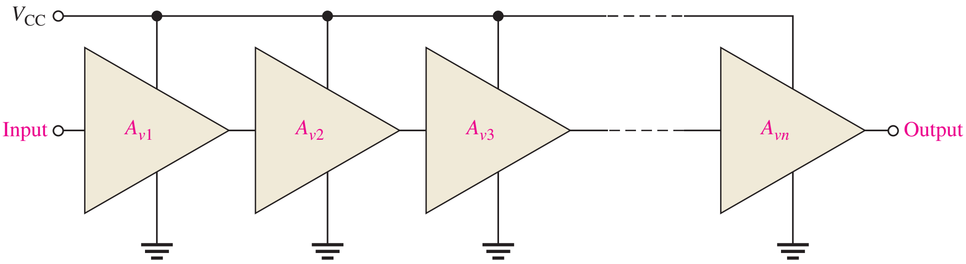
- ❑ **Describe and analyze the operation of multistage amplifiers**
- ❑ Determine the overall voltage gain of multistage amplifiers
  - ◆ Express the voltage gain in decibels (dB)
- ❑ Discuss and analyze capacitively-coupled multistage amplifiers
  - ◆ Describe loading effects ◆ Determine the voltage gain of each stage in a two-stage amplifier ◆ Determine the overall voltage gain ◆ Determine the dc voltages
- ❑ Describe direct-coupled multistage amplifiers

Multistage Voltage Gain

The overall voltage gain, A'_v, of cascaded amplifiers, as shown in Figure 6–33, is the product of the individual voltage gains.

$$A'_v = A_{v1}A_{v2}A_{v3}\ldots A_{vn}$$ **Equation 6–23**

where n is the number of stages.



▲ FIGURE 6–33

Cascaded amplifiers. Each triangular symbol represents a separate amplifier.

Amplifier voltage gain is often expressed in **decibels** (dB) as follows:

$$A_{v(\text{dB})} = 20 \log A_v$$ **Equation 6–24**

This is particularly useful in **multistage** systems because the overall voltage gain in dB is the *sum* of the individual voltage gains in dB.

$$A'_{v(\text{dB})} = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \cdots + A_{vn(\text{dB})}$$

EXAMPLE 6–12

A certain cascaded amplifier arrangement has the following voltage gains: $A_{v1} = 10$, $A_{v2} = 15$, and $A_{v3} = 20$. What is the overall voltage gain? Also express each gain in decibels (dB) and determine the total voltage gain in dB.

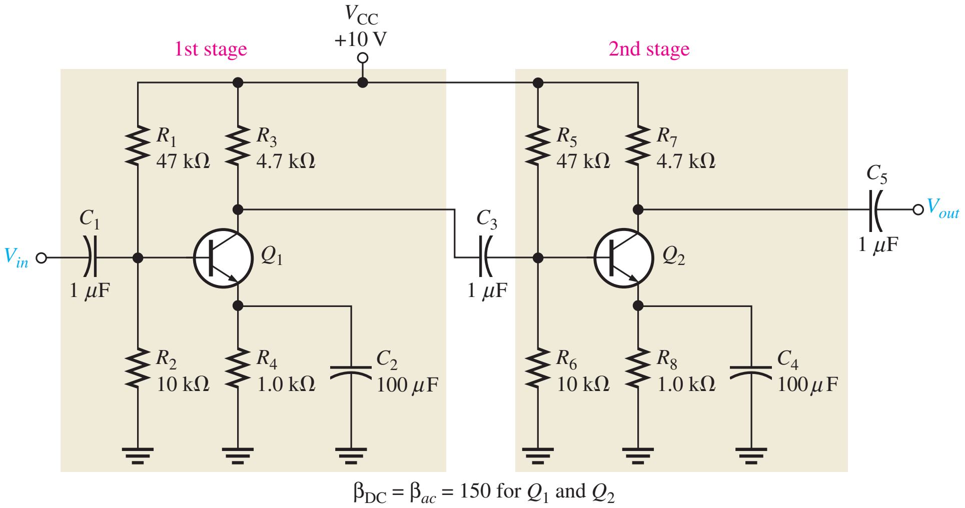
Solution

$$\begin{aligned}
A'_v &= A_{v1}A_{v2}A_{v3} = (10)(15)(20) = \mathbf{3000} \\
A_{v1(\text{dB})} &= 20 \log 10 = \mathbf{20.0\ dB} \\
A_{v2(\text{dB})} &= 20 \log 15 = \mathbf{23.5\ dB} \\
A_{v3(\text{dB})} &= 20 \log 20 = \mathbf{26.0\ dB} \\
A'_{v(\text{dB})} &= 20.0\text{ dB} + 23.5\text{ dB} + 26.0\text{ dB} = \mathbf{69.5\ dB}
\end{aligned}$$

Related Problem In a certain multistage amplifier, the individual stages have the following voltage gains: $A_{v1} = 25$, $A_{v2} = 5$, and $A_{v3} = 12$. What is the overall gain? Express each gain in dB and determine the total voltage gain in dB.

Capacitively-Coupled Multistage Amplifier

For purposes of illustration, we will use the two-stage capacitively coupled amplifier in Figure 6–34. Notice that both stages are identical common-emitter amplifiers with the output of the first stage capacitively coupled to the input of the second stage. Capacitive coupling prevents the dc bias of one stage from affecting that of the other but allows the ac signal to pass without attenuation because $X_C \cong 0\ \Omega$ at the frequency of operation. Notice, also, that the transistors are labeled Q_1 and Q_2.



▲ **FIGURE 6–34**

A two-stage common-emitter amplifier.

Loading Effects In determining the voltage gain of the first stage, you must consider the loading effect of the second stage. Because the coupling capacitor C_3 effectively appears as a short at the signal frequency, the total input resistance of the second stage presents an ac load to the first stage.

Looking from the collector of Q_1, the two biasing resistors in the second stage, R_5 and R_6, appear in parallel with the input resistance at the base of Q_2. In other words, the signal at the collector of Q_1 "sees" R_3, R_5, R_6, and $R_{in(base2)}$ of the second stage all in parallel to ac ground. Thus, the effective ac collector resistance of Q_1 is the total of all these resistances in parallel, as Figure 6–35 illustrates. The voltage gain of the first stage is reduced by the loading of the second stage because the effective ac collector resistance of the first stage is less than the actual value of its collector resistor, R_3. Remember that $A_v = R_c/r'_e$.

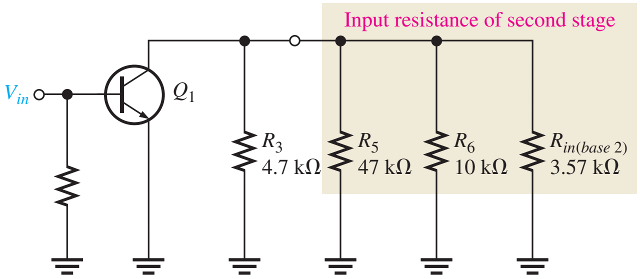


FIGURE 6–35

AC equivalent of first stage in Figure 6–34, showing loading from second stage input resistance.

Voltage Gain of the First Stage The ac collector resistance of the first stage is

$$R_{c1} = R_3 \| R_5 \| R_6 \| R_{in(base2)}$$

Remember that lowercase italic subscripts denote ac quantities such as for R_c.

You can verify that $I_E = 1.05$ mA, $r'_e = 23.8\Omega$, and $R_{in(base2)} = 3.57\text{ k}\Omega$. The effective ac collector resistance of the first stage is as follows:

$$R_{c1} = 4.7\text{ k}\Omega \| 47\text{ k}\Omega \| 10\text{ k}\Omega \| 3.57\text{ k}\Omega = 1.63\text{ k}\Omega$$

Therefore, the base-to-collector voltage gain of the first stage is

$$A_{v1} = \frac{R_{c1}}{r'_e} = \frac{1.63\text{ k}\Omega}{23.8\ \Omega} = 68.5$$

Voltage Gain of the Second Stage The second stage has no load resistor, so the ac collector resistance is R_7, and the gain is

$$A_{v2} = \frac{R_7}{r'_e} = \frac{4.7\text{ k}\Omega}{23.8\ \Omega} = 197$$

Compare this to the gain of the first stage, and notice how much the loading from the second stage reduced the gain.

Overall Voltage Gain The overall amplifier gain with no load on the output is

$$A'_v = A_{v1}A_{v2} = (68.5)(197) \cong 13{,}495$$

If an input signal of 100 μV, for example, is applied to the first stage and if there is no attenuation in the input base circuit due to the source resistance, an output from the second stage of $(100\ \mu\text{V})(13{,}495) \cong 1.35$ V will result. The overall voltage gain can be expressed in dB as follows:

$$A'_{v(\text{dB})} = 20 \log(13{,}495) = 82.6\text{ dB}$$

DC Voltages in the Capacitively Coupled Multistage Amplifier Since both stages in Figure 6–34 are identical, the dc voltages for Q_1 and Q_2 are the same. Since $\beta_{DC}R_4 \gg R_2$ and $\beta_{DC}R_8 \gg R_6$, the dc base voltage for Q_1 and Q_2 is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\text{ k}\Omega}{57\text{ k}\Omega}\right)10\text{ V} = 1.75\text{ V}$$

The dc emitter and collector voltages are as follows:

$$V_E = V_B - 0.7\text{ V} = 1.05\text{ V}$$

$$I_E = \frac{V_E}{R_4} = \frac{1.05\text{ V}}{1.0\text{ k}\Omega} = 1.05\text{ mA}$$

$$I_C \cong I_E = 1.05\text{ mA}$$

$$V_C = V_{CC} - I_C R_3 = 10\text{ V} - (1.05\text{ mA})(4.7\text{ k}\Omega) = 5.07\text{ V}$$

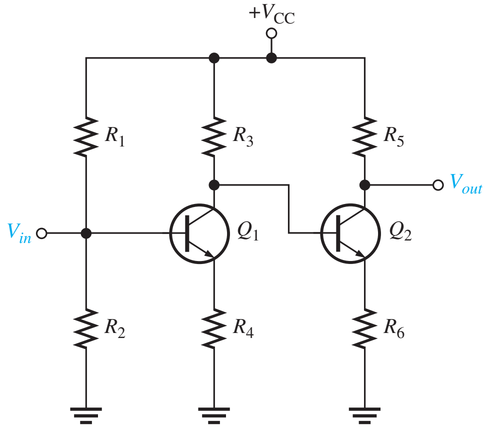
Direct-Coupled Multistage Amplifiers

A basic two-stage, direct-coupled amplifier is shown in Figure 6–36. Notice that there are no coupling or bypass capacitors in this circuit. The dc collector voltage of the first stage provides the base-bias voltage for the second stage. Because of the direct coupling, this type of amplifier has a better low-frequency response than the capacitively coupled type in which the reactance of coupling and bypass capacitors at very low frequencies may become excessive. The increased reactance of capacitors at lower frequencies produces gain reduction in capacitively coupled amplifiers.

Direct-coupled amplifiers can be used to amplify low frequencies all the way down to dc (0 Hz) without loss of voltage gain because there are no capacitive reactances in the circuit. The disadvantage of direct-coupled amplifiers, on the other hand, is that small changes in the dc bias voltages from temperature effects or power-supply variation are amplified by the succeeding stages, which can result in a significant drift in the dc levels throughout the circuit.

▶ FIGURE 6–36

A basic two-stage direct-coupled amplifier.



SECTION 6–6 CHECKUP

1. What does the term *stage* mean?
2. How is the overall voltage gain of a multistage amplifier determined?
3. Express a voltage gain of 500 in dB.
4. Discuss a disadvantage of a capacitively coupled amplifier.

6–7 THE DIFFERENTIAL AMPLIFIER

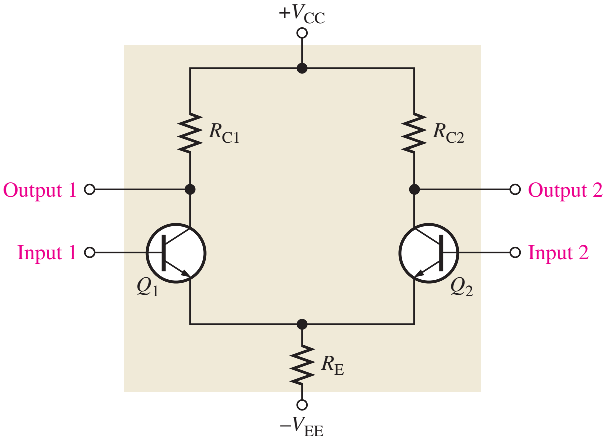
A **differential amplifier** is an amplifier that produces outputs that are a function of the difference between two input voltages. The differential amplifier has two basic modes of operation: differential (in which the two inputs are different) and common mode (in which the two inputs are the same). The differential amplifier is important in operational amplifiers, which are covered beginning in Chapter 12.

After completing this section, you should be able to

- ❑ **Describe the differential amplifier and its operation**
- ❑ Discuss the basic operation
  - ◆ Calculate dc currents and voltages
- ❑ Discuss the modes of signal operation
  - ◆ Describe single-ended differential input operation ◆ Describe double-ended differential input operation ◆ Determine common-mode operation
- ❑ Define and determine the common-mode rejection ratio (CMRR)

Basic Operation

A basic differential amplifier (diff-amp) circuit is shown in Figure 6–37. Notice that the differential amplifier has two inputs and two outputs.



◄ FIGURE 6–37

Basic differential amplifier.

The following discussion is in relation to Figure 6–38 and consists of a basic dc analysis of the diff-amp's operation. First, when both inputs are grounded (0 V), the emitters are at −0.7 V, as indicated in Figure 6–38(a). It is assumed that the transistors are identically matched by careful process control during manufacturing so that their dc emitter currents are the same when there is no input signal. Thus,

$$I_{E1} = I_{E2}$$

Since both emitter currents combine through R_E,

$$I_{E1} = I_{E2} = \frac{I_{R_E}}{2}$$

where

$$I_{R_E} = \frac{V_E - V_{EE}}{R_E}$$

Based on the approximation that $I_C \cong I_E$,

$$I_{C1} = I_{C2} \cong \frac{I_{R_E}}{2}$$

Since both collector currents and both collector resistors are equal (when the input voltage is zero),

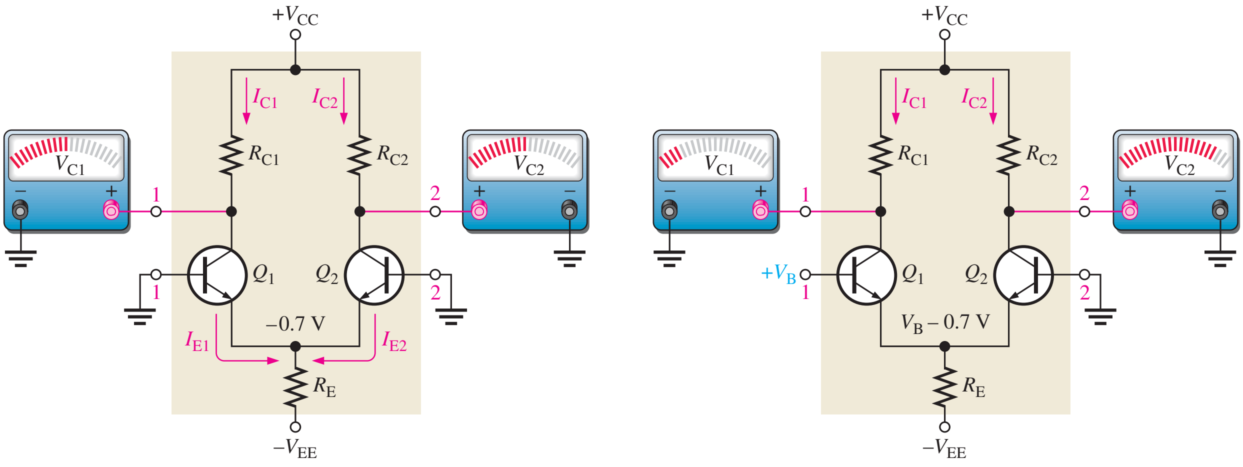
$$V_{C1} = V_{C2} = V_{CC} - I_{C1}R_{C1}$$

This condition is illustrated in Figure 6–38(a).

Next, input 2 is left grounded, and a positive bias voltage is applied to input 1, as shown in Figure 6–38(b). The positive voltage on the base of Q_1 increases I_{C1} and raises the emitter voltage to

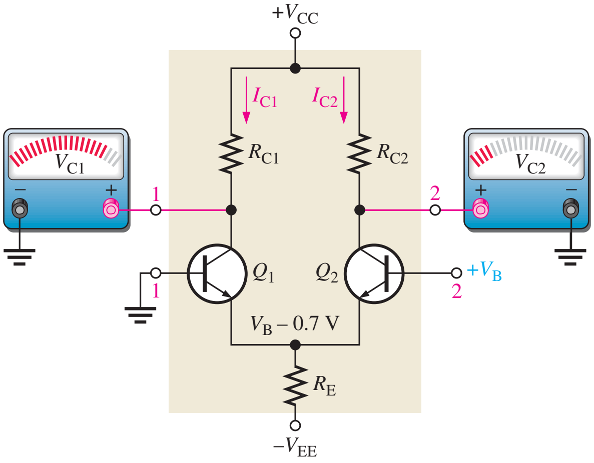
$$V_E = V_B - 0.7\text{ V}$$

This action reduces the forward bias (V_{BE}) of Q_2 because its base is held at 0 V (ground), thus causing I_{C2} to decrease. The net result is that the increase in I_{C1} causes a decrease in V_{C1}, and the decrease in I_{C2} causes an increase in V_{C2}, as shown.



(a) Both inputs grounded

(b) Bias voltage on input 1 with input 2 grounded



(c) Bias voltage on input 2 with input 1 grounded

▲ **FIGURE 6–38**

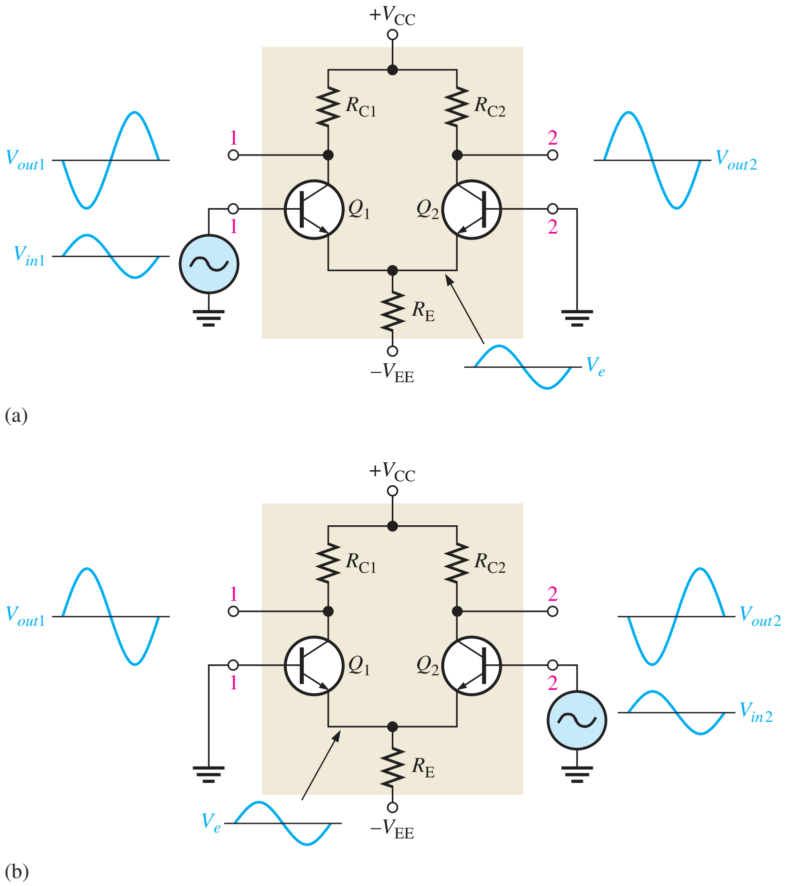
Basic operation of a differential amplifier (ground is zero volts) showing relative changes in voltages.

Finally, input 1 is grounded and a positive bias voltage is applied to input 2, as shown in Figure 6–38(c). The positive bias voltage causes Q_2 to conduct more, thus increasing I_{C2}. Also, the emitter voltage is raised. This reduces the forward bias of Q_1, since its base is held at ground, and causes I_{C1} to decrease. The result is that the increase in I_{C2} produces a decrease in V_{C2}, and the decrease in I_{C1} causes V_{C1} to increase, as shown.

Modes of Signal Operation

Single-Ended Differential Input When a diff-amp is operated with this input configuration, one input is grounded and the signal voltage is applied only to the other input, as shown in Figure 6–39. In the case where the signal voltage is applied to input 1 as in part (a), an inverted, amplified signal voltage appears at output 1 as shown. Also, a signal voltage appears in phase at the emitter of Q_1. Since the emitters of Q_1 and Q_2 are common, the emitter signal becomes an input to Q_2, which functions as a common-base amplifier. The signal is amplified by Q_2 and appears, noninverted, at output 2. This action is illustrated in part (a).

In the case where the signal is applied to input 2 with input 1 grounded, as in Figure 6–39(b), an inverted, amplified signal voltage appears at output 2. In this situation, Q_1 acts as a common-base amplifier, and a noninverted, amplified signal appears at output 1.



(a)

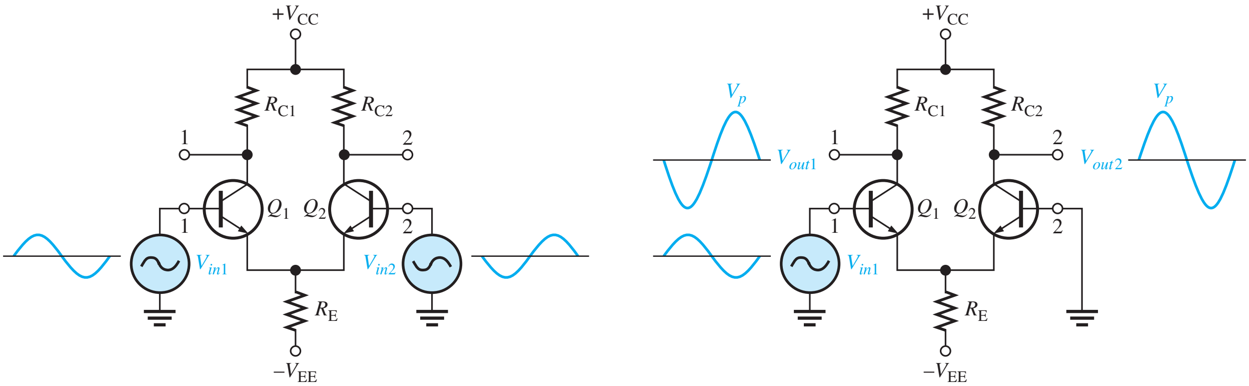
(b)

FIGURE 6–39

Single-ended differential input operation.

Double-Ended Differential Inputs In this input configuration, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 6–40(a). Each input affects the outputs, as you will see in the following discussion.

Figure 6–40(b) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Figure 6–40(c) on page 308 shows the output signals due to the signal on input 2 acting alone as a single-ended input. Notice in parts (b) and (c) that the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, you get the total output signals, as shown in Figure 6–40(d).

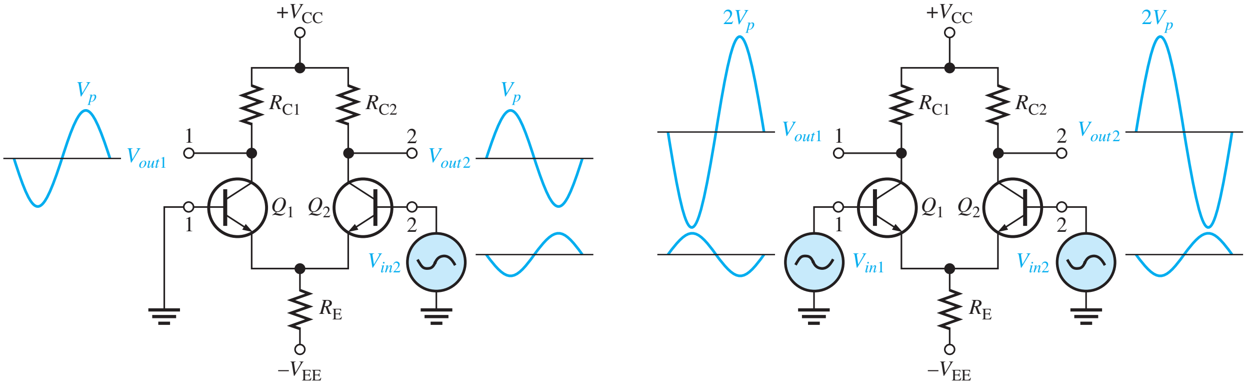


(a) Differential inputs (180° out of phase)

(b) Outputs due to V_{in1}

FIGURE 6–40

Double-ended differential operation. (*continued on next page*)


+V_{CC}
R_{C1}
R_{C2}
V_p
$2V_p$
V_{out1}
V_{out2}
Q_1
Q_2
V_{in1}
V_{in2}
R_E
$-V_{EE}$
1
2

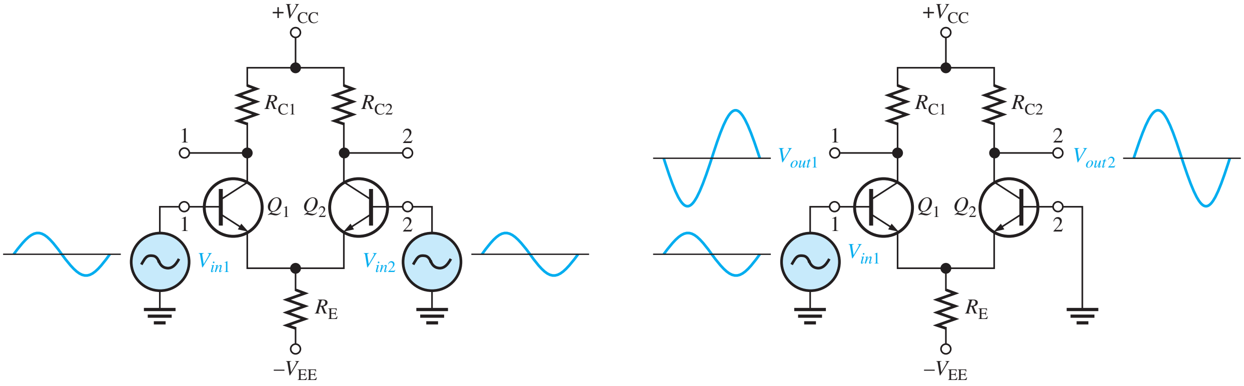
(c) Outputs due to V_{in2}

(d) Total outputs

▲ FIGURE 6–40

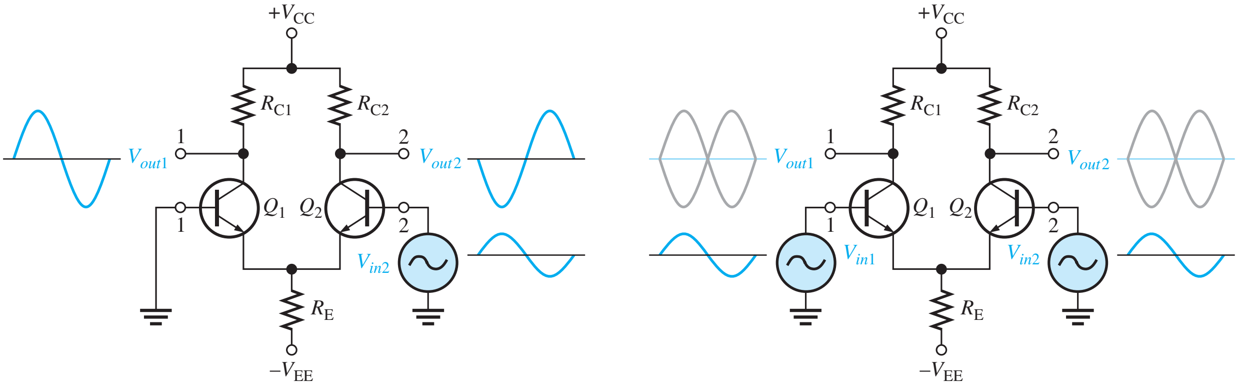
(continued)

Common-Mode Inputs One of the most important aspects of the operation of a diff-amp can be seen by considering the **common-mode** condition where two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 6–41(a). Again, by considering each input signal as acting alone, you can understand the basic operation.


+V_{CC}
R_{C1}
R_{C2}
V_{out1}
V_{out2}
Q_1
Q_2
V_{in1}
V_{in2}
R_E
$-V_{EE}$
1
2

(a) Common-mode inputs (in phase)

(b) Outputs due to V_{in1}


+V_{CC}
R_{C1}
R_{C2}
V_{out1}
V_{out2}
Q_1
Q_2
V_{in1}
V_{in2}
R_E
$-V_{EE}$
1
2

(c) Outputs due to V_{in2}

(d) Outputs due to V_{in1} and V_{in2} cancel because they are equal in amplitude but opposite in phase. The resulting outputs are 0 V ac.

▲ FIGURE 6–41

Common-mode operation of a differential amplifier.

Figure 6–41(b) shows the output signals due to the signal on only input 1, and Figure 6–41(c) shows the output signals due to the signal on only input 2. Notice that the corresponding signals on output 1 are of the opposite polarity, and so are the ones on output 2. When the input signals are applied to both inputs, the outputs are superimposed and they cancel, resulting in a zero output voltage, as shown in Figure 6–41(d).

This action is called *common-mode rejection.* Its importance lies in the situation where an unwanted signal appears commonly on both diff-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the outputs and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines from adjacent lines, the 60 Hz power line, or other sources.

Common-Mode Rejection Ratio

Desired signals appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the outputs as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the diff-amp and do not appear on the outputs. The measure of an amplifier's ability to reject common-mode signals is a parameter called the **CMRR (common-mode rejection ratio)**.

Ideally, a diff-amp provides a very high gain for desired signals (single-ended or differential) and zero gain for common-mode signals. Practical diff-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high differential voltage gain (usually several thousand). The higher the differential gain with respect to the common-mode gain, the better the performance of the diff-amp in terms of rejection of common-mode signals. This suggests that a good measure of the diff-amp's performance in rejecting unwanted common-mode signals is the ratio of the differential voltage gain $A_{v(d)}$ to the common-mode gain, A_{cm}. This ratio is the common-mode rejection ratio, CMRR.

$$\mathbf{CMRR} = \frac{A_{v(d)}}{A_{cm}}$$

Equation 6–25

The higher the CMRR, the better. A very high value of CMRR means that the differential gain $A_{v(d)}$ is high and the common-mode gain A_{cm} is low.

The CMRR is often expressed in decibels (dB) as

$$\mathbf{CMRR} = 20\log\left(\frac{A_{v(d)}}{A_{cm}}\right)$$

Equation 6–26

EXAMPLE 6–13

A certain diff-amp has a differential voltage gain of 2000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibels.

Solution $A_{v(d)} = 2000$, and $A_{cm} = 0.2$. Therefore,

$$\text{CMRR} = \frac{A_{v(d)}}{A_{cm}} = \frac{2000}{0.2} = \mathbf{10{,}000}$$

Expressed in decibels,

$$\text{CMRR} = 20\log(10{,}000) = \mathbf{80\ dB}$$

Related Problem Determine the CMRR and express it in decibels for an amplifier with a differential voltage gain of 8500 and a common-mode gain of 0.25.

A CMRR of 10,000 means that the desired input signal (differential) is amplified 10,000 times more than the unwanted noise (common-mode). For example, if the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the output 10,000 times greater in amplitude than the noise. Thus, the noise or interference has been essentially eliminated.

SECTION 6–7 CHECKUP

1. Distinguish between double-ended and single-ended differential inputs.
2. Define *common-mode rejection.*
3. For a given value of differential gain, does a higher CMRR result in a higher or lower common-mode gain?

6–8 TROUBLESHOOTING

In working with any circuit, you must first know how it is supposed to work before you can troubleshoot it for a failure. The two-stage capacitively coupled amplifier discussed in Section 6–6 is used to illustrate a typical troubleshooting procedure.

After completing this section, you should be able to

- ❑ **Troubleshoot amplifier circuits**
- ❑ Discuss a troubleshooting procedure
  ◆ Describe the analysis phase ◆ Describe the planning phase ◆ Describe the measurement phase

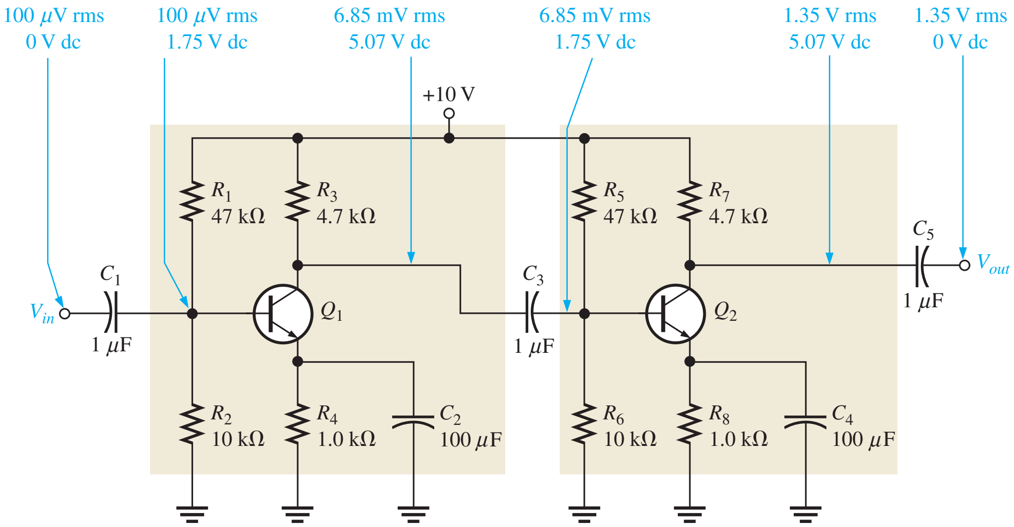
Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

When you are faced with having to troubleshoot a circuit, the first thing you need is a schematic with the proper dc and signal voltages labeled. You must know what the correct voltages in the circuit should be before you can identify an incorrect voltage. Schematics of some circuits are available with voltages indicated at certain points. If this is not the case, you must use your knowledge of the circuit operation to determine the correct voltages. Figure 6–42 is the schematic for the two-stage amplifier that was analyzed in Section 6–6. The correct voltages are indicated at each point.

Troubleshooting Procedure

The analysis, planning, and measurement approach to troubleshooting, discussed in Chapter 2, will be used.

Analysis It has been found that there is no output voltage, V_{out}. You have also determined that the circuit did work properly and then failed. A visual check of the circuit board or assembly for obvious problems such as broken or poor connections, solder splashes,


100 μV rms
0 V dc
100 μV rms
1.75 V dc
6.85 mV rms
5.07 V dc
6.85 mV rms
1.75 V dc
1.35 V rms
5.07 V dc
1.35 V rms
0 V dc
+10 V
R1
47 kΩ
R3
4.7 kΩ
R5
47 kΩ
R7
4.7 kΩ
C5
Vout
1 μF
C1
Vin
1 μF
Q1
C3
1 μF
Q2
R2
10 kΩ
R4
1.0 kΩ
C2
100 μF
R6
10 kΩ
R8
1.0 kΩ
C4
100 μF

▶ FIGURE 6–42

A two-stage common-emitter amplifier with correct voltages indicated. Both transistors have dc and ac betas of 150. Different values of β will produce slightly different results.

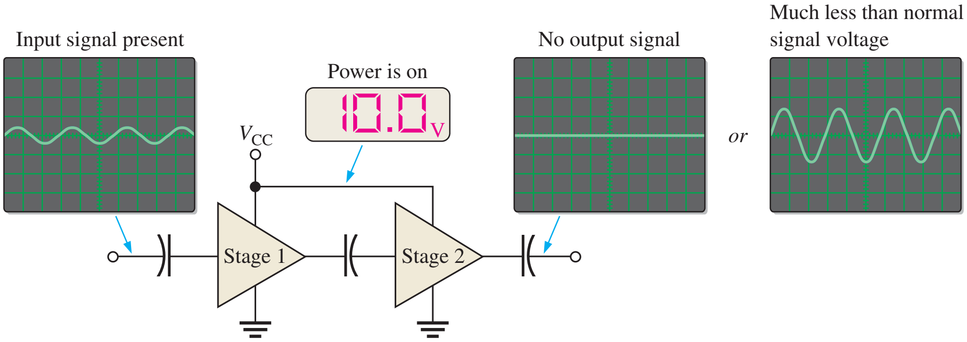
wire clippings, or burned components turns up nothing. You conclude that the problem is most likely a faulty component in the amplifier circuit or an open connection. Also, the dc supply voltage may not be correct or may be missing.

Planning You decide to use an oscilloscope to check the dc levels and the ac signals (you prefer to use a DMM to measure the dc voltages) at certain test points. Also, you decide to apply the half-splitting method to trace the voltages in the circuit and use an in-circuit transistor tester if a transistor is suspected of being faulty.

Measurement To determine the faulty component in a multistage amplifier, use the general five-step troubleshooting procedure which is illustrated as follows.

Step 1: *Perform a power check.* Assume the dc supply voltage is correct as indicated in Figure 6–43.

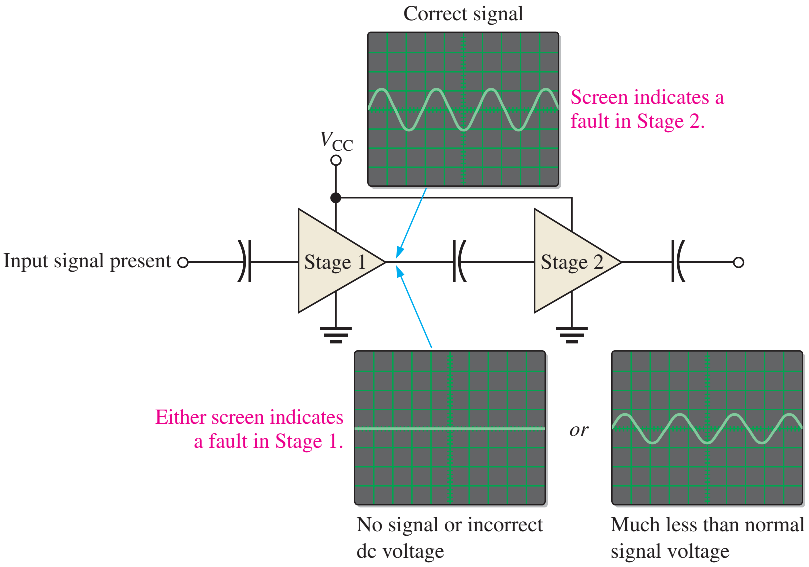
Step 2: *Check the input and output voltages.* Assume the measurements indicate that the input signal voltage is correct. However, there is no output signal voltage or the output signal voltage is much less than it should be, as shown by the diagram in Figure 6–43.


Input signal present
Power is on
10.0V
No output signal
Much less than normal
signal voltage
VCC
or
Stage 1
Stage 2

▲ FIGURE 6–43

Initial check of a faulty two-stage amplifier.

Step 3: *Apply the half-splitting method of signal tracing.* Check the voltages at the output of the first stage. No signal voltage or a much less than normal signal voltage indicates that the problem is in the first stage. An incorrect dc voltage also indicates a first-stage problem. If the signal voltage and the dc voltage are correct at the output of the first stage, the problem is in the second stage. After this check, you have narrowed the problem to one of the two stages. This step is illustrated in Figure 6–44.


Correct signal
Screen indicates a fault in Stage 2.
V_{CC}
Input signal present
Stage 1
Stage 2
Either screen indicates a fault in Stage 1.
or
No signal or incorrect dc voltage
Much less than normal signal voltage

▲ FIGURE 6–44

Half-splitting signal tracing isolates the faulty stage.

Step 4: *Apply fault analysis.* Focus on the faulty stage and determine the component failure that can produce the incorrect output.

Symptom: DC voltages incorrect.

Likely faults: A failure of any resistor or the transistor will produce an incorrect dc bias voltage. A leaky bypass or coupling capacitor will also affect the dc bias voltages. Further measurements in the stage are necessary to isolate the faulty component.

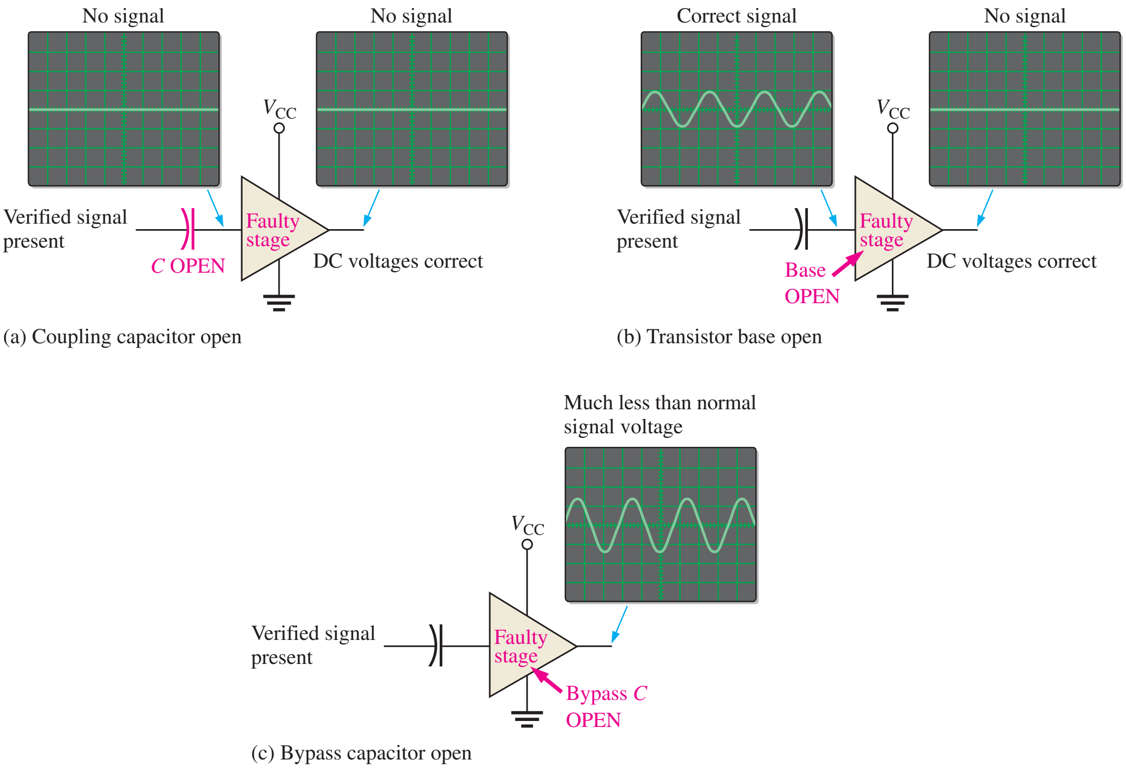
Incorrect ac voltages and the most likely fault(s) are illustrated in Figure 6–45 as follows:

(a) *Symptom 1:* Signal voltage at output missing; dc voltage correct.
Symptom 2: Signal voltage at base missing; dc voltage correct.
Likely fault: Input coupling capacitor open. This prevents the signal from getting to the base.

(b) *Symptom:* Correct signal at base but no output signal.
Likely fault: Transistor base open.

(c) *Symptom:* Signal voltage at output much less than normal; dc voltage correct.
Likely fault: Bypass capacitor open.

Step 5: *Replace or repair.* With the power turned off, replace the defective component or repair the defective connection. Turn on the power, and check for proper operation.


No signal
No signal
V_{CC}
Verified signal present
C OPEN
Faulty stage
DC voltages correct
Correct signal
No signal
V_{CC}
Verified signal present
Base OPEN
Faulty stage
DC voltages correct
Much less than normal signal voltage
V_{CC}
Verified signal present
Faulty stage
Bypass C OPEN

(a) Coupling capacitor open

(b) Transistor base open

(c) Bypass capacitor open

▲ **FIGURE 6–45**

Troubleshooting a faulty stage.

EXAMPLE 6–14

The two-stage amplifier in Figure 6–42 has malfunctioned. Specify the step-by-step troubleshooting procedure for an assumed fault.

Solution Assume there are no visual or other indications of a problem such as a charred resistor, solder splash, wire clipping, broken connection, or extremely hot component. The troubleshooting procedure for a certain fault scenario is as follows:

Step 1: There is power to the circuit as indicated by a correct V_{CC} measurement.

Step 2: There is a verified input signal voltage, but no output signal voltage is measured.

Step 3: The signal voltage and the dc voltage at the collector of Q_1 are correct. This means that the problem is in the second stage or the coupling capacitor C_3 between the stages.

Step 4: The correct signal voltage and dc bias voltage are measured at the base of Q_2. This eliminates the possibility of a fault in C_3 or the second stage bias circuit.

The collector of Q_2 is at 10 V and there is no signal voltage. This measurement, made directly on the transistor collector, indicates that either the collector is shorted to V_{CC} or the transistor is internally open. It is unlikely that the collector resistor R_7 is shorted but to verify, turn off the power and use an ohmmeter to check.

The possibility of a short is eliminated by the ohmmeter check. The other possible faults are (a) transistor Q_2 internally open or (b) emitter resistor or connection open. Use a transistor tester and/or ohmmeter to check each of these possible faults with power off.

Step 5: Replace the faulty component or repair open connection and retest the circuit for proper operation.

Related Problem Determine the possible fault(s) if, in Step 4, you find no signal voltage at the base of Q_2 but the dc voltage is correct.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE06-01
2. Multisim file TSE06-02
3. Multisim file TSE06-03
4. Multisim file TSE06-04
5. Multisim file TSE06-05

SECTION 6–8 CHECKUP

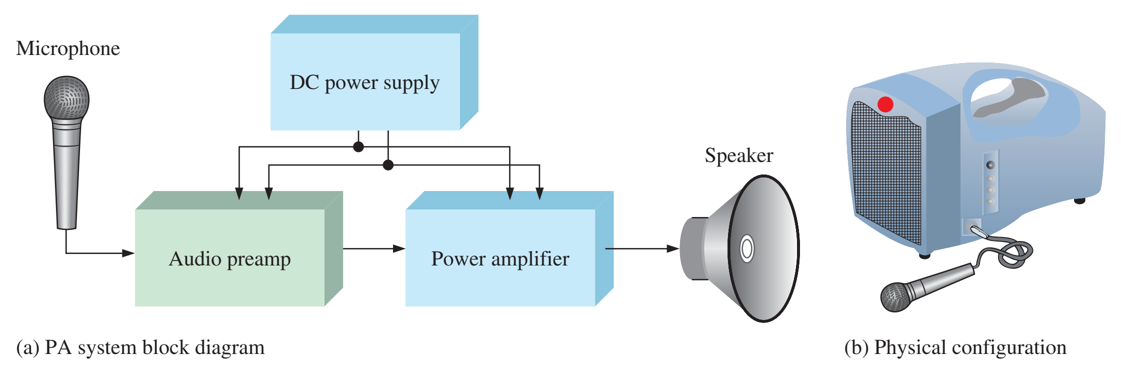
1. If C_4 in Figure 6–42 were open, how would the output signal be affected? How would the dc level at the collector of Q_2 be affected?
2. If R_5 in Figure 6–42 were open, how would the output signal be affected?
3. If the coupling capacitor C_3 in Figure 6–42 shorted out, would any of the dc voltages in the amplifier be changed? If so, which ones?

Application Activity: *Audio Preamplifier for PA System*

An audio preamplifier is to be developed for use in a small portable public address (PA) system. The preamplifier will have a microphone input, and its output will drive a power amplifier to be developed in Chapter 7. A block diagram of the complete PA system is shown in Figure 6–46(a), and its physical configuration is shown in part (b). The dc supply voltages are provided by a battery pack or by an electronic power supply.

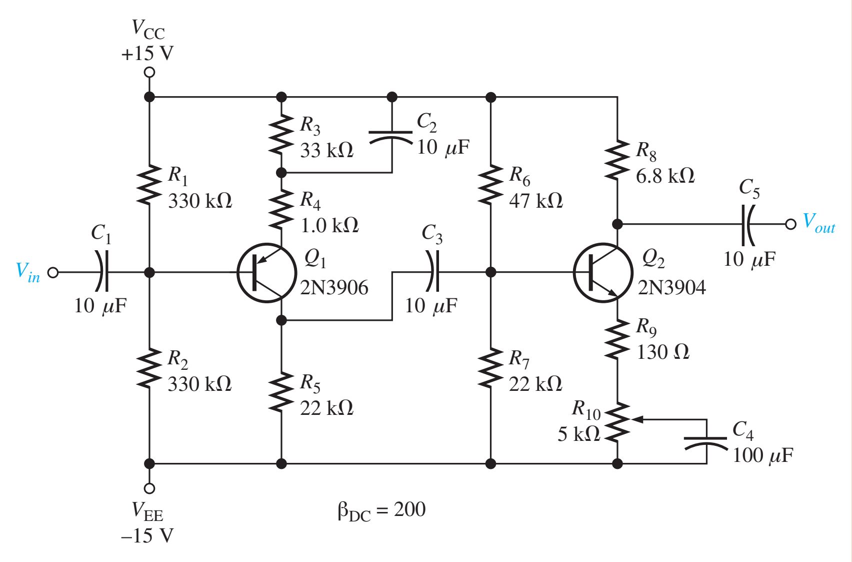
The Circuit

A 2-stage audio voltage preamplifier is shown in Figure 6–47. The first stage is a common-emitter *pnp* with voltage-divider bias, and the second stage is a common-emitter *npn* with voltage-divider bias. It has been decided that the amplifier should operate from 30 V dc to get a large enough signal voltage swing to provide a maximum of 6 W to the speaker. Because small IC regulators such as the 78xx and 79xx series are not available above 24 V,


Microphone
DC power supply
Speaker
Audio preamp
Power amplifier
(a) PA system block diagram
(b) Physical configuration

▲ FIGURE 6–46

The public address system.


V_{CC}
+15 V
R_1
330 kΩ
R_2
330 kΩ
R_3
33 kΩ
C_2
10 μF
R_4
1.0 kΩ
Q_1
2N3906
R_5
22 kΩ
C_1
10 μF
V_{in}
C_3
10 μF
R_6
47 kΩ
R_7
22 kΩ
R_8
6.8 kΩ
Q_2
2N3904
R_9
130 Ω
R_{10}
5 kΩ
C_4
100 μF
C_5
10 μF
V_{out}
V_{EE}
–15 V
$\beta_{DC} = 200$

▲ FIGURE 6–47

Two-stage voltage preamplifier.

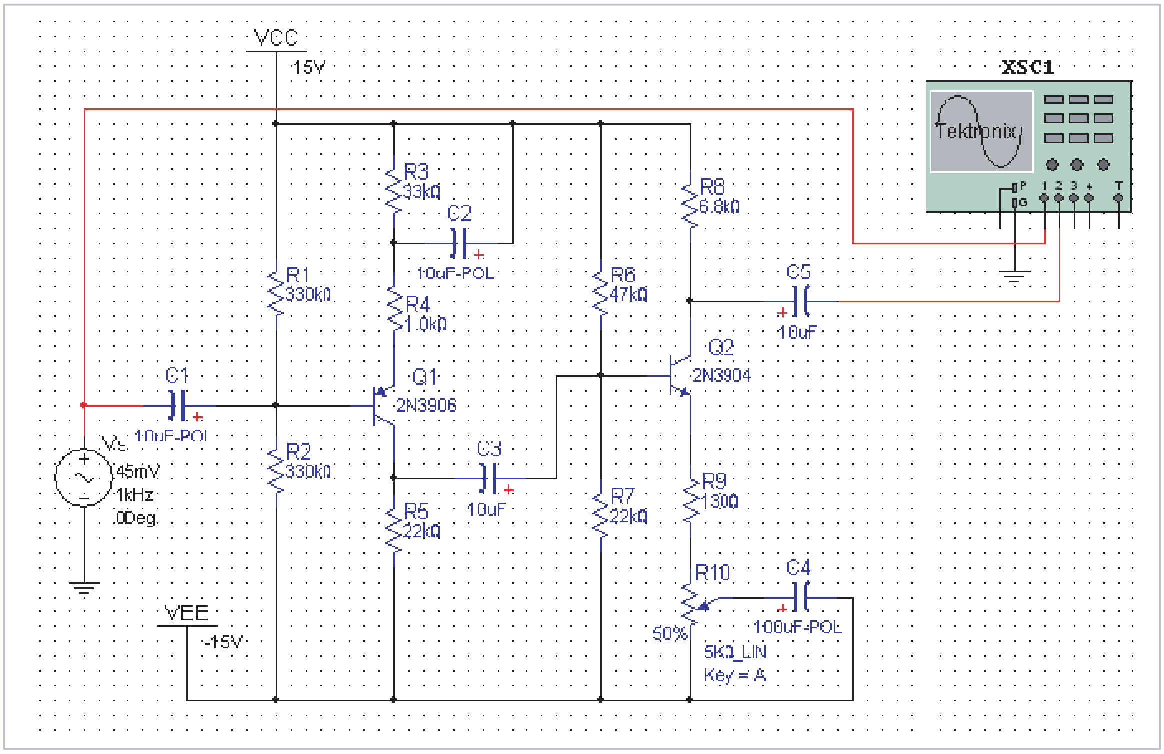
dual ±15 V dc supplies are used in this particular system instead of a single supply. The operation is essentially the same as if a single +30 V dc source had been used. The potentiometer at the output provides gain adjustment for volume control. The input to the first stage is from the microphone, and the output of the second stage will drive a power amplifier to be developed in Chapter 7. The power amplifier will drive the speaker. The preamp is to operate with a peak input signal range of from 25 mV to 50 mV. The minimum range of voltage gain adjustment is from 90 to 170.

1. Calculate the theoretical voltage gain of the first stage when the second stage is set for maximum gain.
2. Calculate the theoretical maximum voltage gain of the second stage.
3. Determine the overall theoretical voltage gain.
4. Calculate the circuit power dissipation with no signal (quiescent).

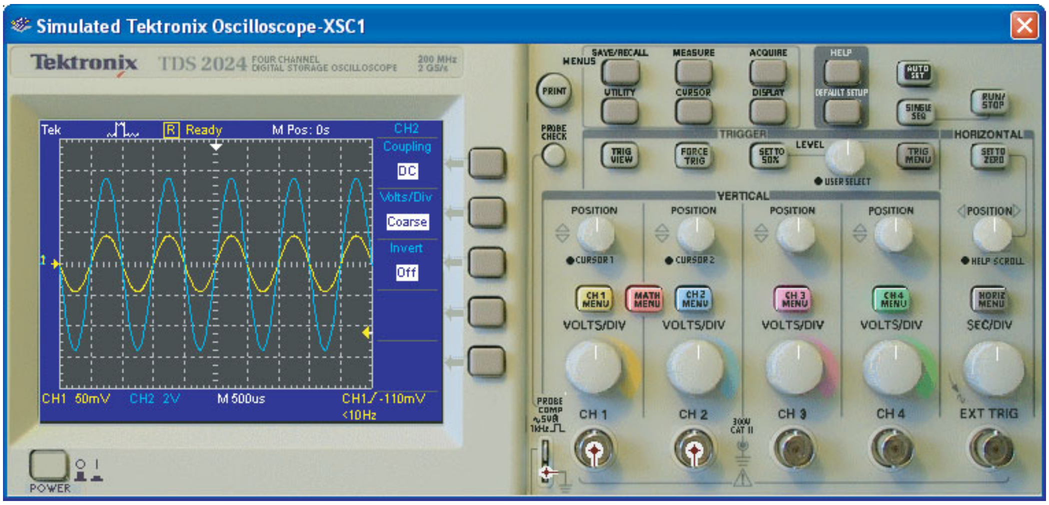
Simulation

The preamp is simulated with a peak input signal of 45 mV using Multisim. The results are shown in Figure 6–48.

5. Determine the voltage gain of the simulated circuit based on the voltage measurements.
6. Compare the measured voltage gain with the calculated voltage gain.


VCC
15V
XSC1
Tektronix
P G 1 2 3 4 T
R3
33kΩ
C2
10uF-POL
R8
6.8kΩ
R1
330kΩ
R4
1.0kΩ
R6
47kΩ
C5
10uF
Q1
2N3906
Q2
2N3904
C1
10uF-POL
Vs
45mV
1kHz
0Deg
R2
330kΩ
C3
10uF
R5
22kΩ
R7
22kΩ
R9
130Ω
R10
C4
100uF-POL
50%
5KΩ_LIN
Key = A
VEE
-15V

(a) Circuit screen


Simulated Tektronix Oscilloscope-XSC1
Tektronix TDS 2024 FOUR CHANNEL DIGITAL STORAGE OSCILLOSCOPE 200 MHz 2 GS/s
Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
CH1 50mV
CH2 2V
M 500us
CH1 ∕ -110mV
<10Hz
POWER
MENUS
SAVE/RECALL
MEASURE
ACQUIRE
HELP
AUTO SET
PRINT
UTILITY
CURSOR
DISPLAY
DEFAULT SETUP
SINGLE SEQ
RUN/STOP
PROBE CHECK
TRIGGER
LEVEL
TRIG VIEW
FORCE TRIG
SET TO 50%
TRIG MENU
HORIZONTAL
SET TO ZERO
USER SELECT
VERTICAL
POSITION
CURSOR 1
CURSOR 2
HELP SCROLL
CH 1 MENU
MATH MENU
CH 2 MENU
CH 3 MENU
CH 4 MENU
HORIZ MENU
VOLTS/DIV
SEC/DIV
PROBE COMP ~5V@ 1kHz
CH 1
CH 2
CH 3
CH 4
EXT TRIG
300V CAT II

(b) Input signal (yellow) and output signal (blue)

▲ FIGURE 6–48

Preamp input and output signals.

Simulate the preamp circuit using your Multisim software. Observe the operation with the virtual oscilloscope.

Prototyping and Testing*

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

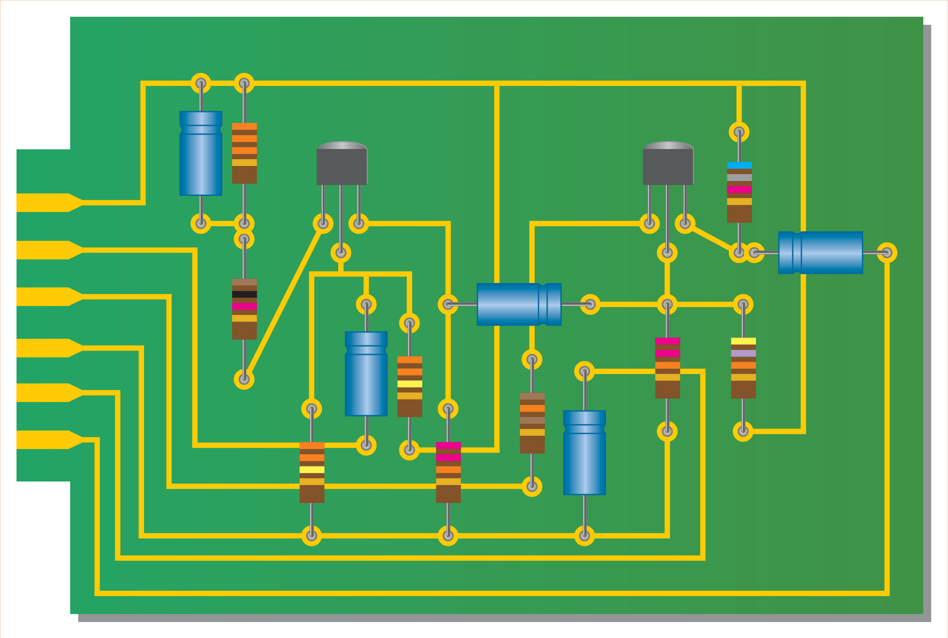
Lab Experiment

To build and test a similar circuit, go to Experiment 6 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The preamp is implemented on a printed circuit board as shown in Figure 6–49.

7. Check the printed circuit board and verify that it agrees with the schematic in Figure 6–47. The volume control potentiometer is mounted off the PC board for easy access.
8. Label each input and output pin according to function.



▲ FIGURE 6–49

Preamp circuit board.

Troubleshooting

Two preamp circuit boards have failed the production test. You will troubleshoot the boards based on the scope measurements shown in Figure 6–50.

9. List possible faults for board 1.
10. List possible faults for board 2.

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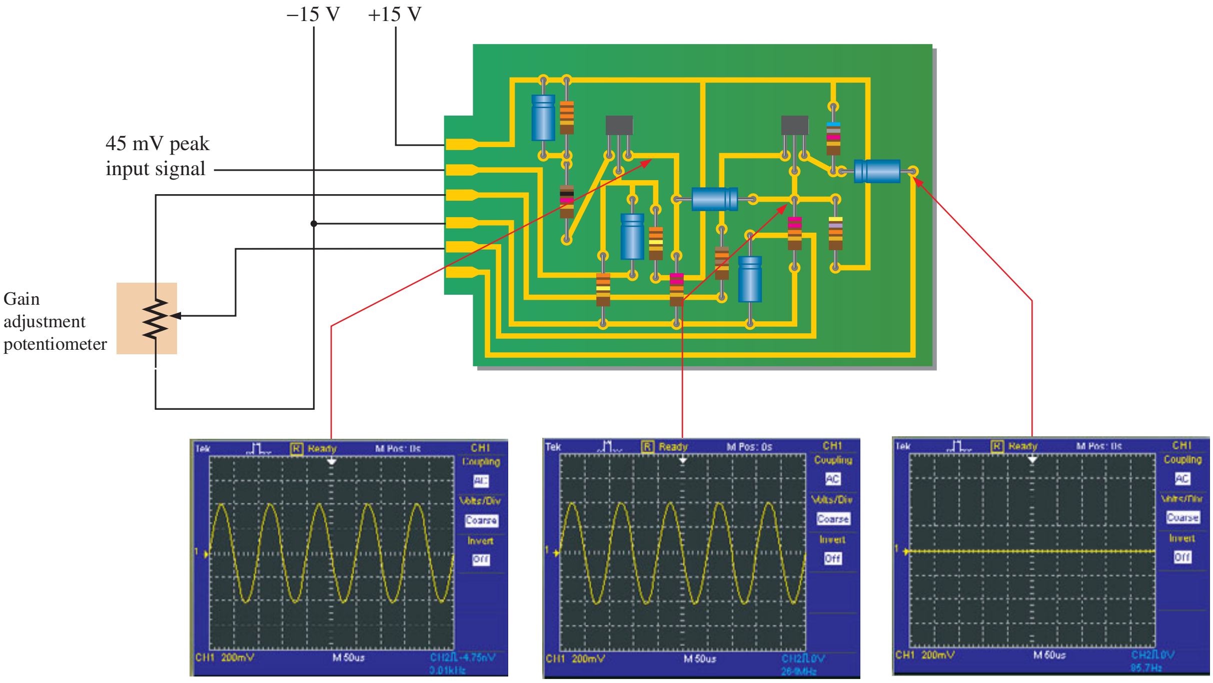
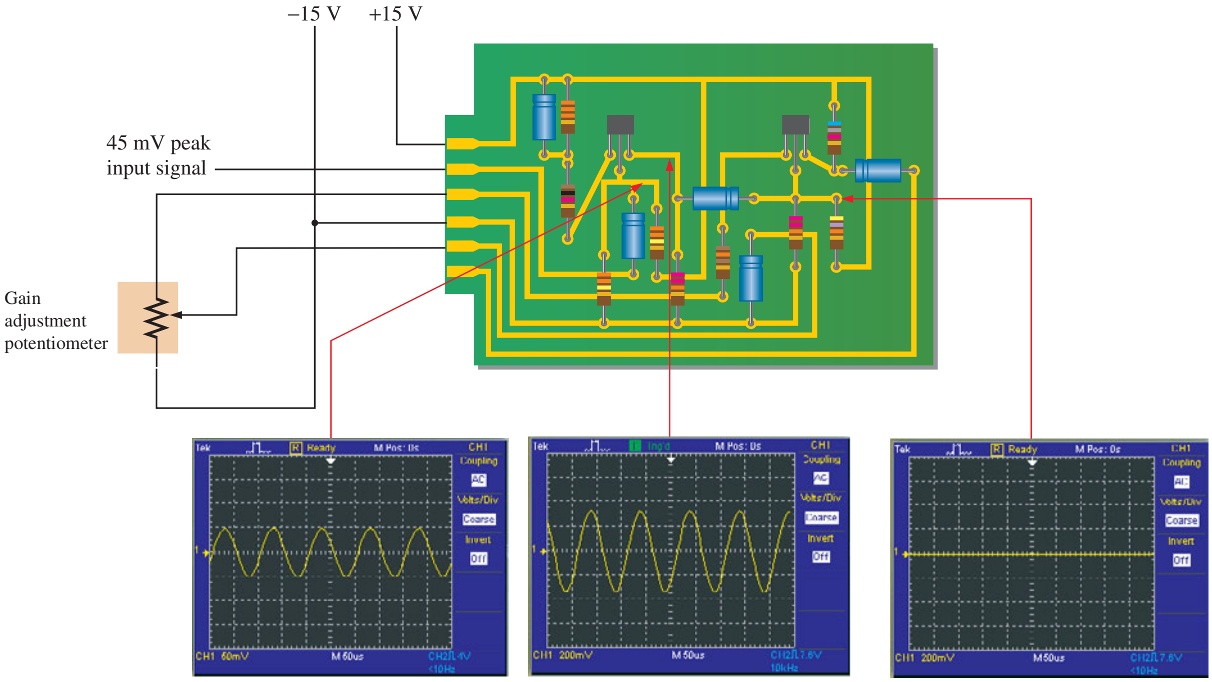
*An example of a combined software/hardware approach to simulating and prototyping a circuit is NI ELVIS (National Instrument Educational Laboratory Virtual Instrumentation Suite), which combines Multisim software with actual prototyping hardware.


−15 V
+15 V
45 mV peak input signal
Gain adjustment potentiometer
CH1 200mV
M 50us
CH1 200mV
M 50us
CH1 200mV
M 50us

(a) Test result for board 1


−15 V
+15 V
45 mV peak input signal
Gain adjustment potentiometer
CH1 50mV
M 50us
CH1 200mV
M 50us
CH1 200mV
M 50us

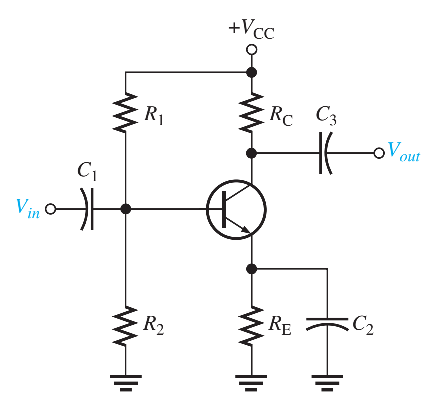
(b) Test result for board 2

▲ FIGURE 6–50

Test of two faulty preamp boards.

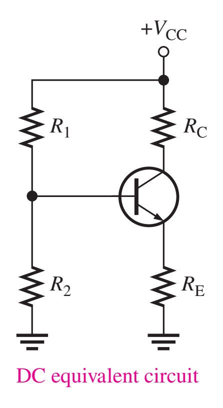
SUMMARY OF THE COMMON-EMITTER AMPLIFIER

CIRCUIT WITH VOLTAGE-DIVIDER BIAS



- Input is at the base. Output is at the collector.
- There is a phase inversion from input to output.
- C_1 and C_3 are coupling capacitors for the input and output signals.
- C_2 is the emitter-bypass capacitor.
- All capacitors must have a negligible reactance at the frequency of operation, so they appear as shorts.
- Emitter is at ac ground due to the bypass capacitor.

EQUIVALENT CIRCUITS AND FORMULAS



DC equivalent circuit

- DC formulas:

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2}$$

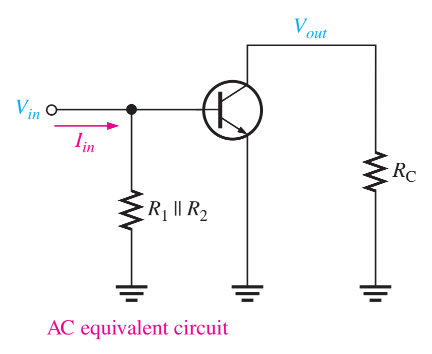
$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

$$V_E = I_ER_E$$

$$V_B = V_E + V_{BE}$$

$$V_C = V_{CC} - I_CR_C$$



AC equivalent circuit

- AC formulas:

$$r'_e = \frac{25\text{ mV}}{I_E}$$

$$R_{in(base)} = \beta_{ac}r'_e$$

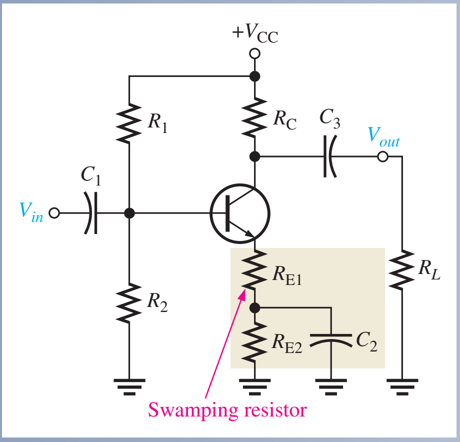
$$R_{out} \cong R_C$$

$$A_v = \frac{R_C}{r'_e}$$

$$A_i = \frac{I_c}{I_{in}}$$

$$A_p = A'_vA_i$$

SWAMPED AMPLIFIER WITH RESISTIVE LOAD



$+V_{CC}$
R_1
R_C
C_3
V_{out}
C_1
V_{in}
R_{E1}
R_L
R_2
R_{E2}
C_2
Swamping resistor

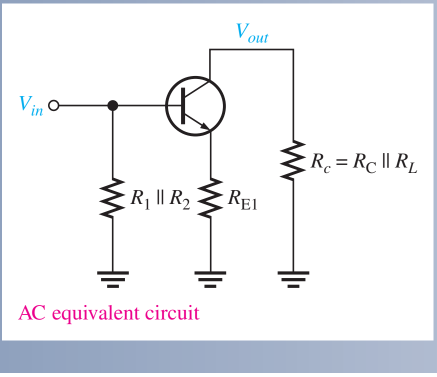
- AC formulas:

$$A_v \cong \frac{R_c}{R_{E1}}$$

where $R_c = R_C \| R_L$

$$R_{in(base)} = \beta_{ac}(r'_e + R_{E1})$$

- Swamping stabilizes gain by minimizing the effect of r'_e.
- Swamping reduces the voltage gain from its unswamped value.
- Swamping increases input resistance.
- The load resistance reduces the voltage gain. The smaller the load resistance, the less the gain.

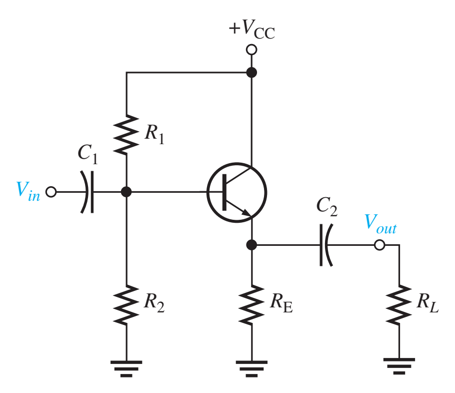


V_{out}
V_{in}
$R_c = R_C \| R_L$
$R_1 \| R_2$
R_{E1}

AC equivalent circuit

SUMMARY OF THE COMMON-COLLECTOR AMPLIFIER

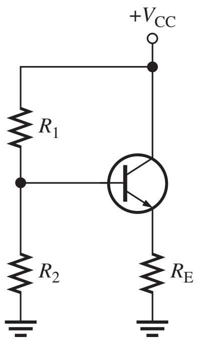
CIRCUIT WITH VOLTAGE-DIVIDER BIAS



$+V_{CC}$
R_1
C_1
V_{in}
C_2
V_{out}
R_2
R_E
R_L

- Input is at the base. Output is at the emitter.
- There is no phase inversion from input to output.
- Input resistance is high. Output resistance is low.
- Maximum voltage gain is 1.
- Collector is at ac ground.
- Coupling capacitors must have a negligible reactance at the frequency of operation.

EQUIVALENT CIRCUITS AND FORMULAS



DC equivalent circuit

- DC formulas:

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2}$$

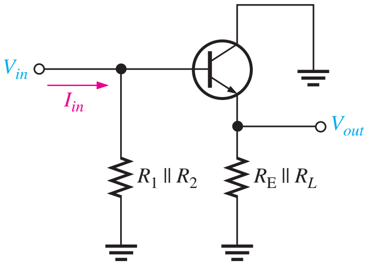
$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

$$V_E = I_ER_E$$

$$V_B = V_E + V_{BE}$$

$$V_C = V_{CC}$$


V_{in}
I_{in}
V_{out}
$R_1 \parallel R_2$
$R_E \parallel R_L$

AC equivalent circuit

- AC formulas:

$$r'_e = \frac{25\text{ mV}}{I_E}$$

$$R_{in(base)} = \beta_{ac}(r'_e + R_e) \cong \beta_{ac}R_e$$

$$R_{out} = \left(\frac{R_s}{\beta_{ac}}\right) \parallel R_E$$

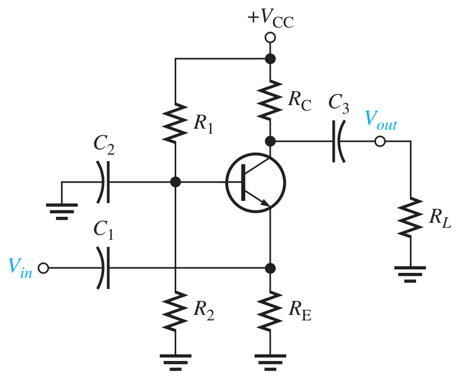
$$A_v = \frac{R_e}{r'_e + R_e} \cong 1$$

$$A_i = \frac{I_e}{I_{in}}$$

$$A_p \cong A_i$$

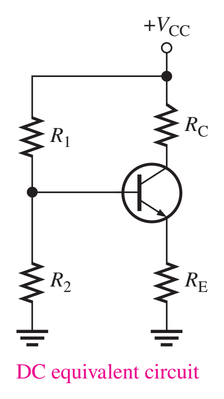
SUMMARY OF COMMON-BASE AMPLIFIER

CIRCUIT WITH VOLTAGE-DIVIDER BIAS


$+V_{CC}$
R_C
C_3
V_{out}
R_1
C_2
C_1
V_{in}
R_L
R_2
R_E

- Input is at the emitter. Output is at the collector.
- There is no phase inversion from input to output.
- Input resistance is low. Output resistance is high.
- Maximum current gain is 1.
- Base is at ac ground.

EQUIVALENT CIRCUITS AND FORMULAS


$+V_{CC}$
R_1
R_C
R_2
R_E

DC equivalent circuit

- DC formulas:

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2}$$

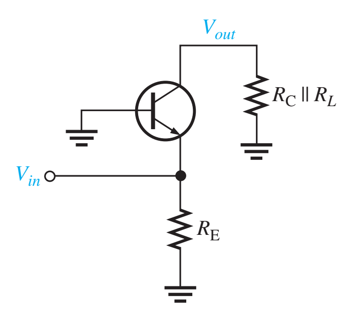
$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

$$V_E = I_ER_E$$

$$V_B = V_E + V_{BE}$$

$$V_C = V_{CC} - I_CR_C$$


V_{out}
$R_C \parallel R_L$
V_{in}
R_E

AC equivalent circuit

- AC formulas:

$$r'_e = \frac{25\text{ mV}}{I_E}$$

$$R_{in(emitter)} \cong r'_e$$

$$R_{out} \cong R_C$$

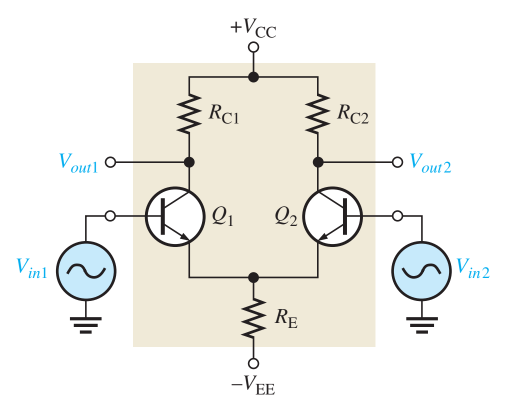
$$A_v \cong \frac{R_c}{r'_e}$$

$$A_i \cong 1$$

$$A_p \cong A_v$$

SUMMARY OF DIFFERENTIAL AMPLIFIER

CIRCUIT WITH DIFFERENTIAL INPUTS


$+V_{CC}$
R_{C1}
R_{C2}
V_{out1}
V_{out2}
Q_1
Q_2
V_{in1}
V_{in2}
R_E
$-V_{EE}$

- Double-ended differential inputs (shown)

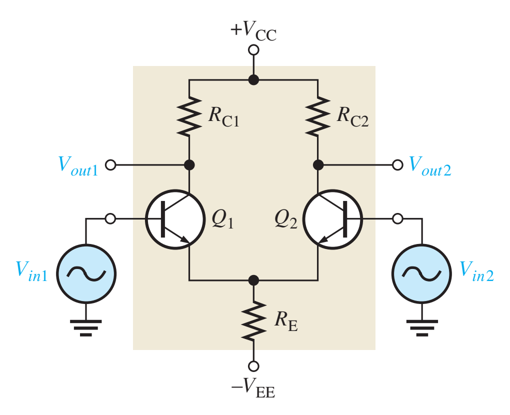
  Signal on both inputs

  Input signals are out of phase
- Single-ended differential inputs (not shown)

  Signal on one input only

  One input connected to ground

CIRCUIT WITH COMMON-MODE INPUTS



- Both input signals are the same phase, frequency, and amplitude.
- Common-mode rejection ratio:

$$\text{CMRR} = \frac{A_{v(d)}}{A_{cm}}$$

$$\text{CMRR} = 20\log\left(\frac{A_{v(d)}}{A_{cm}}\right)$$

SUMMARY

Section 6–1

- A small-signal amplifier uses only a small portion of its load line under signal conditions.
- The ac load line differs from the dc load line because the effective ac collector resistance is less than the dc collector resistance.

Section 6–2

- *r* parameters are easily identifiable and applicable with a transistor's circuit operation.
- *h* parameters are important because manufacturers' datasheets specify transistors using *h* parameters.

Section 6–3

- A common-emitter amplifier has high voltage, current, and power gains, but a relatively low input resistance.
- Swamping is a method of stabilizing the voltage gain.

Section 6–4

- A common-collector amplifier has high input resistance and high current gain, but its voltage gain is approximately 1.
- A Darlington pair provides beta multiplication for increased input resistance.
- A common-collector amplifier is known as an emitter-follower.

Section 6–5

- The common-base amplifier has a high voltage gain, but it has a very low input resistance and its current gain is approximately 1.
- Common-emitter, common-collector, and common-base amplifier configurations are summarized in Table 6–4.

TABLE 6–4

Relative comparison of amplifier configurations. The current gains and the input and output resistances are the approximate maximum achievable values, with the bias resistors neglected.

	CE	CC	CB
Voltage gain, A_v	High R_C/r'_e	Low $\cong 1$	High R_C/r'_e
Current gain, $A_{i(max)}$	High β_{ac}	High β_{ac}	Low $\cong 1$
Power gain, A_p	Very high A_iA_v	High $\cong A_i$	High $\cong A_v$
Input resistance, $R_{in(max)}$	Low $\beta_{ac}r'_e$	High $\beta_{ac}R_E$	Very low r'_e
Output resistance, R_{out}	High R_C	Very low $(R_s/\beta_{ac}) \parallel R_E$	High R_C

Section 6–6

- The total gain of a multistage amplifier is the product of the individual gains (sum of dB gains).
- Single-stage amplifiers can be connected in sequence with capacitively-coupling and direct coupling methods to form multistage amplifiers.

Section 6–7

- A differential input voltage appears between the inverting and noninverting inputs of a differential amplifier.
- In the differential mode, a diff-amp can be operated with single-ended or double-ended inputs.
- In single-ended operation, there is a signal on one input and the other input is grounded.
- In double-ended operation, two signals that are 180° out of phase are on the inputs.
- Common-mode occurs when equal in-phase voltages are applied to both input terminals.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

ac ground A point in a circuit that appears as ground to ac signals only.

Attenuation The reduction in the level of power, current, or voltage.

Bypass capacitor A capacitor placed across the emitter resistor of an amplifier.

CMRR (common-mode rejection ratio) A measure of a differential amplifier's ability to reject common-mode signals.

Common-base (CB) A BJT amplifier configuration in which the base is the common terminal to an ac signal or ground.

Common-collector (CC) A BJT amplifier configuration in which the collector is the common terminal to an ac signal or ground.

Common-emitter (CE) A BJT amplifier configuration in which the emitter is the common terminal to an ac signal or ground.

Common mode A condition where two signals applied to differential inputs are of the same phase, frequency, and amplitude.

Decibel A logarithmic measure of the ratio of one voltage to another or one power to another.

Differential amplifier An amplifier in which the output is a function of the difference between two input voltages.

Emitter-follower A popular term for a common-collector amplifier.

Input resistance The resistance seen by an ac source connected to the input of an amplifier.

Output resistance The ac resistance looking in at the output of an amplifier.

***r* parameter** One of a set of BJT characteristic parameters that include α_{ac}, β_{ac}, r'_e, r'_b, and r'_c.

KEY FORMULAS

6–1	$r'_e \cong \dfrac{25\text{ mV}}{I_E}$	Internal ac emitter resistance

Common-Emitter

6–2	$R_{in(base)} = R_1 \parallel R_2 \parallel R_{in(base)}$	Total amplifier input resistance, voltage-divider bias
6–3	$R_{in(base)} = \beta_{ac} r'_e$	Input resistance at base
6–4	$R_{out} \cong R_C$	Output resistance
6–5	$A_v = \dfrac{R_C}{r'_e}$	Voltage gain, base-to-collector, unloaded
6–6	$A_v = \dfrac{R_C}{r'_e + R_E}$	Voltage gain without bypass capacitor
6–7	$A_v = \dfrac{R_c}{r'_e}$	Voltage gain, base-to-collector, loaded, bypassed R_E

6–8	$A_v \cong \dfrac{R_C}{R_{E1}}$	Voltage gain, swamped amplifier
6–9	$R_{in(base)} = \beta_{ac}(r'_e + R_{E1})$	Input resistance at base, swamped amplifier
6–10	$A_i = \dfrac{I_c}{I_s}$	Current gain, input source to collector
6–11	$A_p = A'_v A_i$	Power gain

Common-Collector (Emitter-Follower)

6–12	$A_v \cong 1$	Voltage gain, base-to-emitter
6–13	$R_{in(base)} \cong \beta_{ac} R_e$	Input resistance at base, loaded
6–14	$R_{out} \cong \left(\dfrac{R_s}{\beta_{ac}}\right) \parallel R_E$	Output resistance
6–15	$A_i = \dfrac{I_e}{I_{in}}$	Current gain
6–16	$A_p \cong A_i$	Power gain
6–17	$R_{in} = \beta_{ac1}\beta_{ac2}R_E$	Input resistance, Darlington pair

Common-Base

6–18	$A_v \cong \dfrac{R_c}{r'_e}$	Voltage gain, emitter-to-collector
6–19	$R_{in(emitter)} \cong r'_e$	Input resistance at emitter
6–20	$R_{out} \cong R_C$	Output resistance
6–21	$A_i \cong 1$	Current gain
6–22	$A_p \cong A_v$	Power gain

Multistage Amplifier

6–23	$A'_v = A_{v1}A_{v2}A_{v3} \ldots A_{vn}$	Overall voltage gain
6–24	$A_{v(\mathrm{dB})} = 20 \log A_v$	Voltage gain expressed in dB

Differential Amplifier

6–25	$\mathrm{CMRR} = \dfrac{A_{v(d)}}{A_{cm}}$	Common-mode rejection ratio
6–26	$\mathrm{CMRR} = 20 \log\left(\dfrac{A_{v(d)}}{A_{cm}}\right)$	Common mode rejection ratio in dB

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. In an amplifier, a coupling capacitor should appear ideally as a short to the signal.
2. r parameters include β_{ac} and r'_e.
3. h parameters are never specified on a datasheet.
4. The r parameter β_{ac} is the same as the h parameter h_{fe}.
5. A bypass capacitor in a CE amplifier decreases the voltage gain.
6. If R_C in a CE amplifier is increased, the voltage gain is reduced.
7. The load is the amount of current drawn from the output of an amplifier.
8. In a CE amplifier, the gain can be stabilized by using a swamping resistor.

9. An emitter-follower is a CC amplifier.
10. A CC amplifier has high voltage gain.
11. A Darlington pair consists essentially of two CC amplifiers.
12. A CB amplifier has high current gain.
13. The overall voltage gain of a multistage amplifier is the product of the gains of each stage.
14. A differential amplifier amplifies the difference of two input signals.
15. CMRR is the common-mode resistance ratio.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the transistor in Figure 6–8 is exchanged for one with higher betas, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
2. If C_2 is removed from the circuit in Figure 6–8, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
3. If the value of R_C in Figure 6–8 is increased, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
4. If the amplitude of V_{in} in Figure 6–8 is decreased, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
5. If C_2 in Figure 6–27 is shorted, the average value of the output voltage will
   (a) increase **(b)** decrease **(c)** not change
6. If the value of R_E in Figure 6–27 is increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
7. If the value of C_1 in Figure 6–27 is increased, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
8. If the value of R_C in Figure 6–32 is increased, the current gain will
   (a) increase **(b)** decrease **(c)** not change
9. If C_2 and C_4 in Figure 6–34 are increased in value, V_{out} will
   (a) increase **(b)** decrease **(c)** not change
10. If the value of R_4 in Figure 6–34 is reduced, the overall voltage gain will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 6–1

1. A small-signal amplifier
   (a) uses only a small portion of its load line
   (b) always has an output signal in the mV range
   (c) goes into saturation once on each input cycle
   (d) is always a common-emitter amplifier

Section 6–2

2. The parameter h_{fe} corresponds to
   (a) β_{DC} **(b)** β_{ac} **(c)** r'_e **(d)** r'_c
3. If the dc emitter current in a certain transistor amplifier is 3 mA, the approximate value of r'_e is
   (a) 3 kΩ **(b)** 3 Ω **(c)** 8.33 Ω **(d)** 0.33 kΩ

Section 6–3

4. A certain common-emitter amplifier has a voltage gain of 100. If the emitter bypass capacitor is removed,
   (a) the circuit will become unstable **(b)** the voltage gain will decrease
   (c) the voltage gain will increase **(d)** the Q-point will shift

5. For a common-emitter amplifier, $R_C = 1.0\ \text{k}\Omega$, $R_E = 390\ \Omega$, $r'_e = 15\ \Omega$, and $\beta_{ac} = 75$. Assuming that R_E is completely bypassed at the operating frequency, the voltage gain is

(a) 66.7 **(b)** 2.56 **(c)** 2.47 **(d)** 75

6. In the circuit of Question 5, if the frequency is reduced to the point where $X_{C(bypass)} = R_E$, the voltage gain

(a) remains the same **(b)** is less **(c)** is greater

7. In a common-emitter amplifier with voltage-divider bias, $R_{in(base)} = 68\ \text{k}\Omega$, $R_1 = 33\ \text{k}\Omega$, and $R_2 = 15\ \text{k}\Omega$. The total ac input resistance is

(a) 68 kΩ **(b)** 8.95 kΩ **(c)** 22.2 kΩ **(d)** 12.3 kΩ

8. A CE amplifier is driving a 10 kΩ load. If $R_C = 2.2\ \text{k}\Omega$ and $r'_e = 10\ \Omega$, the voltage gain is approximately

(a) 220 **(b)** 1000 **(c)** 10 **(d)** 180

Section 6–4

9. For a common-collector amplifier, $R_E = 100\ \Omega$, $r'_e = 10\ \Omega$, and $\beta_{ac} = 150$. The ac input resistance at the base is

(a) 1500 Ω **(b)** 15 kΩ **(c)** 110 Ω **(d)** 16.5 kΩ

10. If a 10 mV signal is applied to the base of the emitter-follower circuit in Question 9, the output signal is approximately

(a) 100 mV **(b)** 150 mV **(c)** 1.5 V **(d)** 10 mV

11. In a certain emitter-follower circuit, the current gain is 50. The power gain is approximately

(a) $50A_v$ **(b)** 50 **(c)** 1 **(d)** answers (a) and (b)

12. In a Darlington pair configuration, each transistor has an ac beta of 125. If R_E is 560 Ω, the input resistance is

(a) 560 Ω **(b)** 70 kΩ **(c)** 8.75 MΩ **(d)** 140 kΩ

Section 6–5

13. The input resistance of a common-base amplifier is

(a) very low **(b)** very high

(c) the same as a CE **(d)** the same as a CC

Section 6–6

14. Each stage of a four-stage amplifier has a voltage gain of 15. The overall voltage gain is

(a) 60 **(b)** 15 **(c)** 50,625 **(d)** 3078

15. The overall gain found in Question 14 can be expressed in decibels as

(a) 94.1 dB **(b)** 47.0 dB **(c)** 35.6 dB **(d)** 69.8 dB

Section 6–7

16. A differential amplifier

(a) is used in op-amps **(b)** has one input and one output

(c) has two outputs **(d)** answers (a) and (c)

17. When a differential amplifier is operated single-ended,

(a) the output is grounded

(b) one input is grounded and a signal is applied to the other

(c) both inputs are connected together

(d) the output is not inverted

18. In the double-ended differential mode,

(a) opposite polarity signals are applied to the inputs

(b) the gain is 1

(c) the outputs are different amplitudes

(d) only one supply voltage is used

19. In the common mode,

(a) both inputs are grounded

(b) the outputs are connected together

(c) an identical signal appears on both inputs

(d) the output signals are in-phase

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 6–1 Amplifier Operation

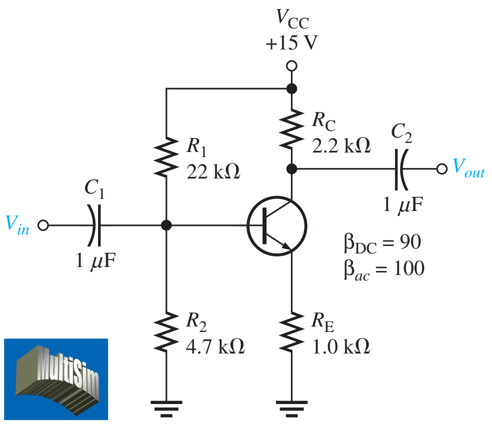
1. What is the lowest value of dc collector current to which a transistor having the characteristic curves in Figure 6–4 can be biased and still retain linear operation with a peak-to-peak base current swing of 20 μA?
2. What is the highest value of I_C under the conditions described in Problem 1?

Section 6–2 Transistor AC Models

3. If the dc emitter current in a transistor is 3 mA, what is the value of r'_e?
4. If the h_{fe} of a transistor is specified as 200, determine β_{ac}.
5. A certain transistor has a dc beta (h_{FE}) of 130. If the dc base current is 10 μA, determine r'_e. $\alpha_{DC} = 0.99$.
6. At the dc bias point of a certain transistor circuit, $I_B = 15\ \mu$A and $I_C = 2$ mA. Also, a variation in I_B of 3 μA about the Q-point produces a variation in I_C of 0.35 mA about the Q-point. Determine β_{DC} and β_{ac}.

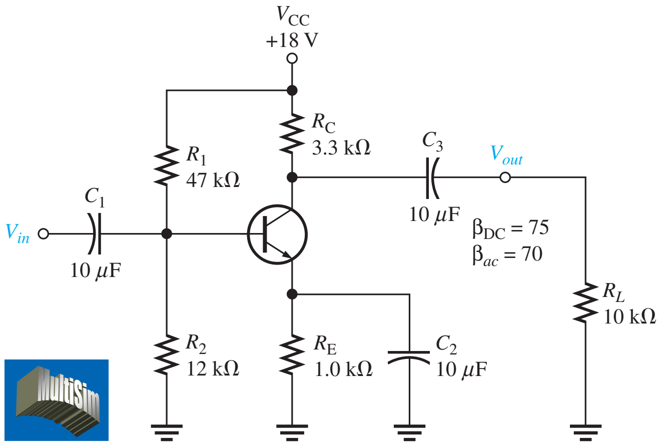
Section 6–3 The Common-Emitter Amplifier

7. Draw the dc equivalent circuit and the ac equivalent circuit for the unloaded amplifier in Figure 6–51.
8. Determine the following dc values for the amplifier in Figure 6–51.
   (a) V_B **(b)** V_E **(c)** I_E **(d)** I_C **(e)** V_C
9. Calculate the quiescent power dissipation in Figure 6–51.
10. Determine the following values for the amplifier in Figure 6–51.
    (a) $R_{in(base)}$ **(b)** $R_{in(tot)}$ **(c)** A_v
11. Connect a bypass capacitor across R_E in Figure 6–51, and repeat Problem 10.
12. Connect a 10 kΩ load resistor to the output in Figure 6–51, and repeat Problem 11.
13. Determine the following dc values for the amplifier in Figure 6–52.
    (a) I_E **(b)** V_E **(c)** V_B **(d)** I_C **(e)** V_C **(f)** V_{CE}



▲ FIGURE 6–51

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F06-51).



▲ FIGURE 6–52

14. Determine the following ac values for the amplifier in Figure 6–52.

(a) $R_{in(base)}$ **(b)** R_{in} **(c)** A_v **(d)** A_i **(e)** A_p

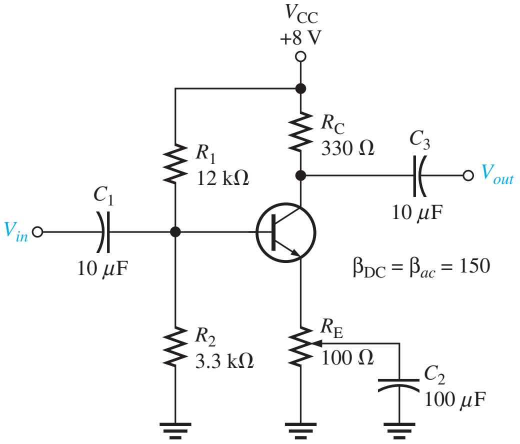
15. Assume that a 600 Ω, 12 μV rms voltage source is driving the amplifier in Figure 6–52. Determine the overall voltage gain by taking into account the attenuation in the base circuit, and find the *total* output voltage (ac and dc). What is the phase relationship of the collector signal voltage to the base signal voltage?

16. The amplifier in Figure 6–53 has a variable gain control, using a 100 Ω potentiometer for R_E with the wiper ac-grounded. As the potentiometer is adjusted, more or less of R_E is bypassed to ground, thus varying the gain. The total R_E remains constant to dc, keeping the bias fixed. Determine the maximum and minimum gains for this unloaded amplifier.

17. If a load resistance of 600 Ω is placed on the output of the amplifier in Figure 6–53, what are the maximum and minimum gains?

18. Find the overall maximum voltage gain for the amplifier in Figure 6–53 with a 1.0 kΩ load if it is being driven by a 300 kΩ source.

▶ FIGURE 6–53



19. Modify the schematic to show how you would "swamp out" the temperature effects of r'_e in Figure 6–52 by making R_e at least ten times larger than r'_e. Keep the same total R_E. How does this affect the voltage gain?

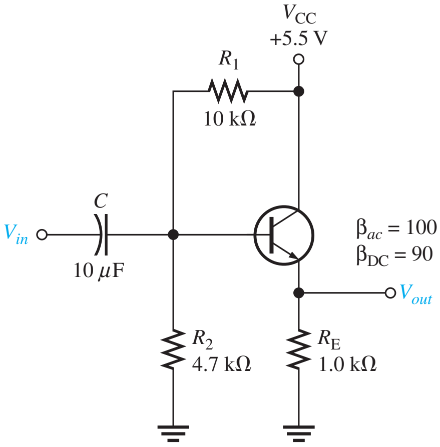
Section 6–4 The Common-Collector Amplifier

20. Determine the *exact* voltage gain for the unloaded emitter-follower in Figure 6–54.

21. What is the total input resistance in Figure 6–54? What is the dc output voltage?

22. A load resistance is capacitively coupled to the emitter in Figure 6–54. In terms of signal operation, the load appears in parallel with R_E and reduces the effective emitter resistance. How does this affect the voltage gain?

▶ FIGURE 6–54



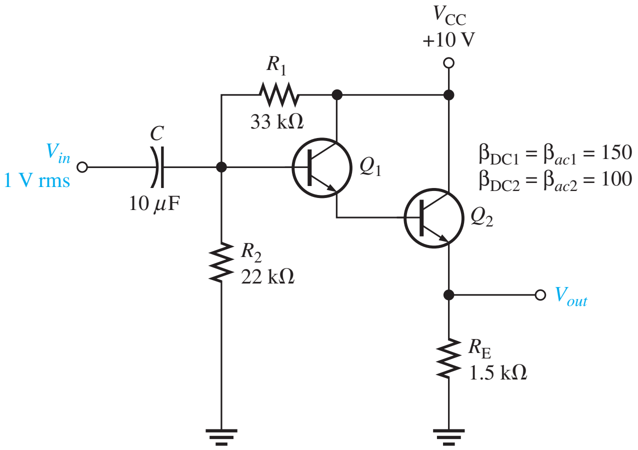
23. In Problem 22, what value of R_L will cause the voltage gain to drop to 0.9?

24. For the circuit in Figure 6–55, determine the following:

- **(a)** Q_1 and Q_2 dc terminal voltages
- **(b)** overall β_{ac}
- **(c)** r'_e for each transistor
- **(d)** total input resistance

25. Find the overall current gain A_i in Figure 6–55.

▶ **FIGURE 6–55**


V_{CC}
+10 V
R_1
33 kΩ
C
10 μF
V_{in}
1 V rms
Q_1
Q_2
$\beta_{DC1} = \beta_{ac1} = 150$
$\beta_{DC2} = \beta_{ac2} = 100$
R_2
22 kΩ
V_{out}
R_E
1.5 kΩ

Section 6–5 The Common-Base Amplifier

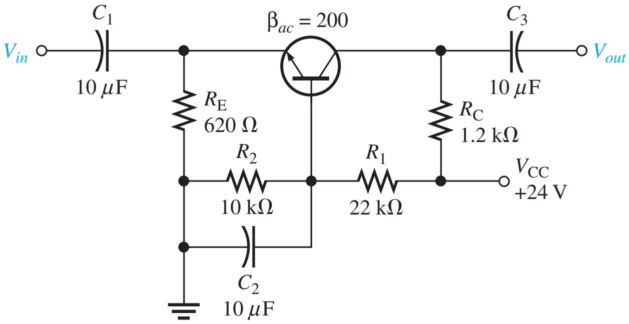
26. What is the main disadvantage of the common-base amplifier compared to the common-emitter and the emitter-follower amplifiers?

27. Find $R_{in(emitter)}$, A_v, A_i, and A_p for the unloaded amplifier in Figure 6–56.

28. Match the following generalized characteristics with the appropriate amplifier configuration.

- **(a)** Unity current gain, high voltage gain, very low input resistance
- **(b)** High current gain, high voltage gain, low input resistance
- **(c)** High current gain, unity voltage gain, high input resistance

▶ **FIGURE 6–56**


C_1
V_{in}
10 μF
$\beta_{ac} = 200$
C_3
V_{out}
10 μF
R_E
620 Ω
R_C
1.2 kΩ
R_2
10 kΩ
R_1
22 kΩ
V_{CC}
+24 V
C_2
10 μF

Section 6–6 Multistage Amplifiers

29. Each of two cascaded amplifier stages has an $A_v = 20$. What is the overall gain?

30. Each of three cascaded amplifier stages has a dB voltage gain of 10 dB. What is the overall voltage gain in dB? What is the actual overall voltage gain?

31. For the two-stage, capacitively coupled amplifier in Figure 6–57, find the following values:

(a) voltage gain of each stage

(b) overall voltage gain

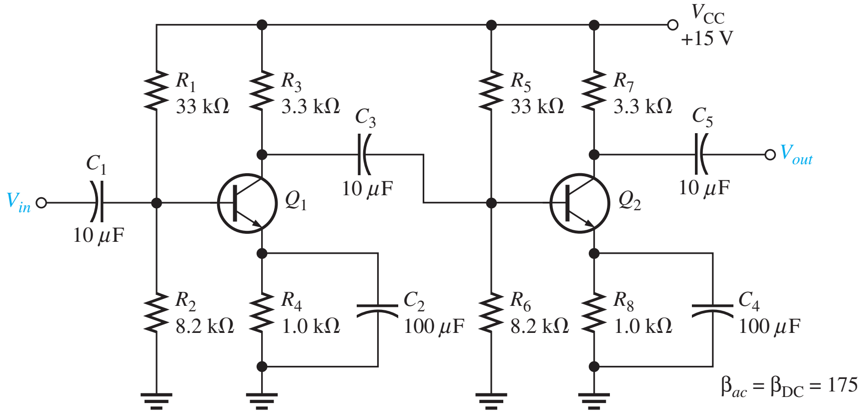
(c) Express the gains found in (a) and (b) in dB.

32. If the multistage amplifier in Figure 6–57 is driven by a 75 Ω, 50 μV source and the second stage is loaded with an $R_L = 18\ \text{k}\Omega$, determine

(a) voltage gain of each stage

(b) overall voltage gain

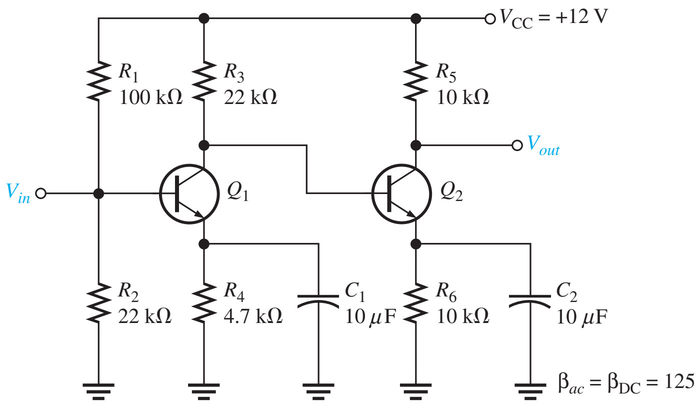
(c) Express the gains found in (a) and (b) in dB.



V_{CC}
+15 V
R_1 33 kΩ
R_3 3.3 kΩ
C_3 10 μF
R_5 33 kΩ
R_7 3.3 kΩ
C_5 10 μF
V_{out}
C_1 10 μF
V_{in}
Q_1
Q_2
R_2 8.2 kΩ
R_4 1.0 kΩ
C_2 100 μF
R_6 8.2 kΩ
R_8 1.0 kΩ
C_4 100 μF
$\beta_{ac} = \beta_{DC} = 175$

▲ FIGURE 6–57

33. Figure 6–58 shows a direct-coupled (that is, with no coupling capacitors between stages) two-stage amplifier. The dc bias of the first stage sets the dc bias of the second. Determine all dc voltages for both stages and the overall ac voltage gain.



$V_{CC} = +12$ V
R_1 100 kΩ
R_3 22 kΩ
R_5 10 kΩ
V_{out}
V_{in}
Q_1
Q_2
R_2 22 kΩ
R_4 4.7 kΩ
C_1 10 μF
R_6 10 kΩ
C_2 10 μF
$\beta_{ac} = \beta_{DC} = 125$

▲ FIGURE 6–58

34. Express the following voltage gains in dB:

(a) 12 **(b)** 50 **(c)** 100 **(d)** 2500

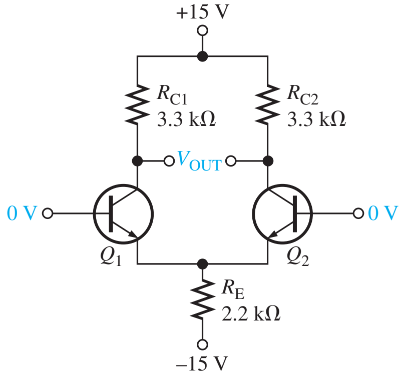
35. Express the following voltage gains in dB as standard voltage gains:

(a) 3 dB **(b)** 6 dB **(c)** 10 dB **(d)** 20 dB **(e)** 40 dB

Section 6–7 The Differential Amplifier

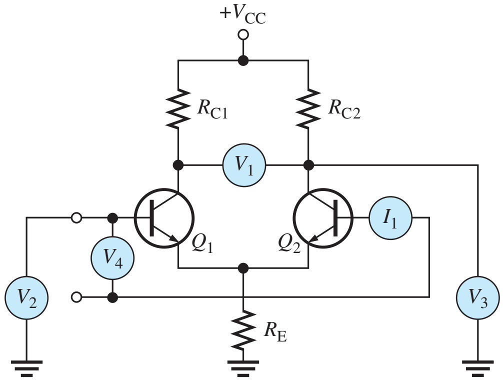
36. The dc base voltages in Figure 6–59 are zero. Using your knowledge of transistor analysis, determine the dc differential output voltage. Assume that Q_1 has an $\alpha = 0.980$ and Q_2 has an $\alpha = 0.975$.

▶ FIGURE 6–59


+15 V
R_{C1} 3.3 kΩ
R_{C2} 3.3 kΩ
V_{OUT}
0 V
0 V
Q_1
Q_2
R_E 2.2 kΩ
–15 V

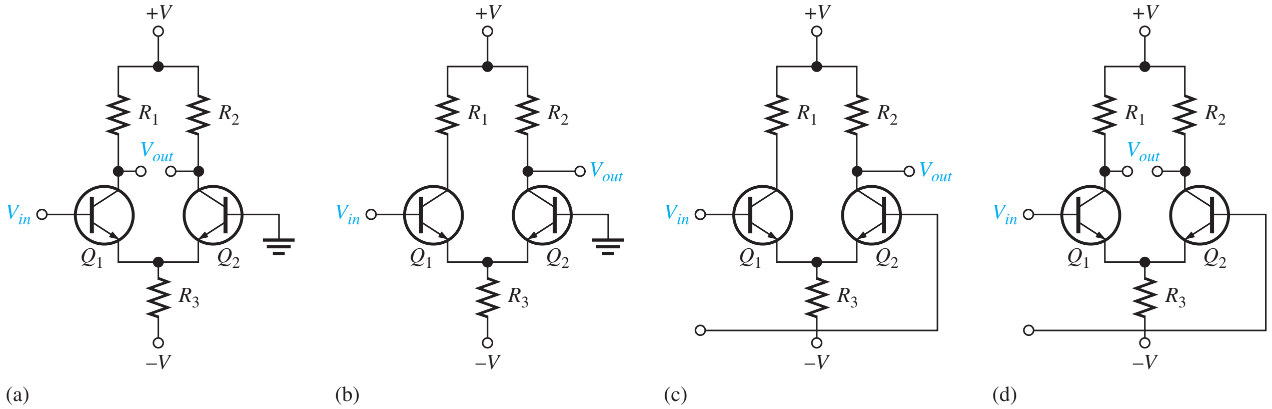
37. Identify the quantity being measured by each meter in Figure 6–60.

▶ FIGURE 6–60


$+V_{CC}$
R_{C1}
R_{C2}
V_1
I_1
Q_1
Q_2
V_4
V_2
V_3
R_E

38. A differential amplifier stage has collector resistors of 5.1 kΩ each. If $I_{C1} = 1.35$ mA and $I_{C2} = 1.29$ mA, what is the differential output voltage?

39. Identify the type of input and output configuration for each basic differential amplifier in Figure 6–61.


+V
R_1
R_2
V_{out}
V_{in}
Q_1
Q_2
R_3
–V
(a)
(b)
(c)
(d)

▲ FIGURE 6–61

Section 6–8 Troubleshooting

40. Assume that the coupling capacitor C_3 is shorted in Figure 6–34. What dc voltage will appear at the collector of Q_1?

41. Assume that R_5 opens in Figure 6–34. Will Q_2 be in cutoff or in conduction? What dc voltage will you observe at the Q_2 collector?

42. Refer to Figure 6–57 and determine the general effect of each of the following failures:

(a) C_2 open

(b) C_3 open

(c) C_4 open

(d) C_2 shorted

(e) base-collector junction of Q_1 open

(f) base-emitter junction of Q_2 open

43. Assume that you must troubleshoot the amplifier in Figure 6–57. Set up a table of test point values, input, output, and all transistor terminals that include both dc and rms values that you expect to observe when a 300 Ω test signal source with a 25 μV rms output is used.

APPLICATION ACTIVITY PROBLEMS

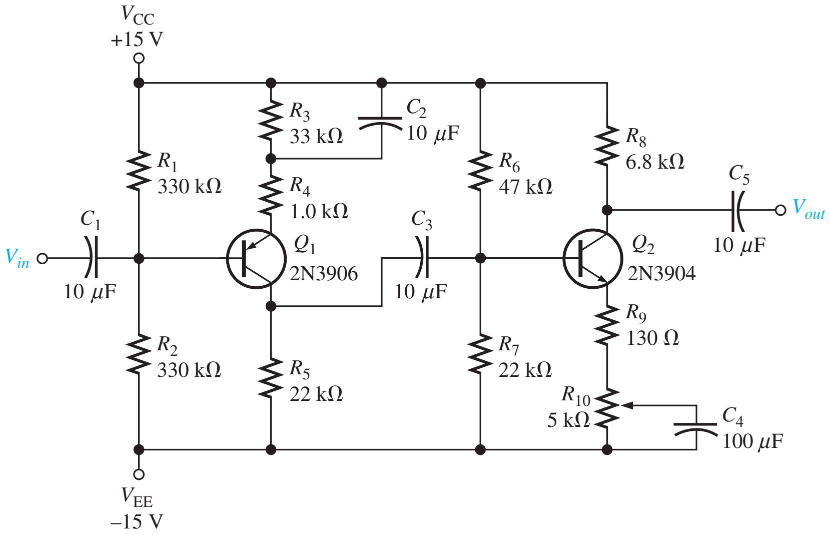
44. Refer to the public address system block diagram in Figure 6–46. You are asked to repair a system that is not working. After a preliminary check, you find that there is no output signal from the power amplifier or from the preamplifier. Based on this check and assuming that only one of the blocks is faulty, which block can you eliminate as the faulty one? What would you check next?

45. What effect would each of the following faults in the amplifier of Figure 6–62 have on the output signal?

(a) Open C_1 **(b)** Open C_2 **(c)** Open C_3 **(d)** Open C_4

(e) Q_1 collector internally open **(f)** Q_2 emitter shorted to ground

▶ FIGURE 6–62



46. Suppose a 220 Ω resistor is incorrectly installed in the R_7 position of the amplifier in Figure 6–62. What effect does this have on the circuit?

47. The connection from R_1 to the supply voltage V_1 in Figure 6–62 has opened.

(a) What happens to Q_1?

(b) What is the dc voltage at the Q_1 collector?

(c) What is the dc voltage at the Q_2 collector?

DATASHEET PROBLEMS

48. Refer to the 2N3946/2N3947 partial datasheet in Figure 6–63 on page 334. Determine the minimum value for each of the following r parameters:

(a) β_{ac} **(b)** r'_e **(c)** r'_c

49. Repeat Problem 48 for maximum values.

50. Should you use a 2N3946 or a 2N3947 transistor in a certain application if the criteria is maximum current gain?

Electrical Characteristics ($T_A = 25°\text{C}$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
Input capacitance ($V_{EB} = 1.0$ V dc, $I_C = 0$, $f = 1.0$ MHz)		C_{ibo}	–	8.0	pF
Input impedance ($I_C = 1.0$ mA, $V_{CE} = 10$ V, $f = 1.0$ kHz)	2N3946	h_{ie}	0.5	6.0	kohms
	2N3947		2.0	12	
Voltage feedback ratio ($I_C = 1.0$ mA, $V_{CE} = 10$ V, $f = 1.0$ kHz)	2N3946	h_{re}	–	10	$\times 10^{-4}$
	2N3947		–	20	
Small-signal current gain ($I_C = 1.0$ mA, $V_{CE} = 10$ V, $f = 1.0$ kHz)	2N3946	h_{fe}	50	250	–
	2N3947		100	700	
Output admittance ($I_C = 1.0$ mA, $V_{CE} = 10$ V, $f = 1.0$ kHz)	2N3946	h_{oe}	1.0	30	μmhos
	2N3947		5.0	50	
Collector base time constant ($I_C = 10$ mA, $V_{CE} = 20$ V, $f = 31.8$ MHz)		$rb'C_c$	–	200	ps
Noise figure ($I_C = 100$ μA, $V_{CE} = 5.0$ V, $R_G = 1.0$ kΩ, $f = 1.0$ kHz)		NF	–	5.0	dB

Switching Characteristics

Delay time	$V_{CC} = 3.0$ V dc, $V_{OB} = 0.5$ V dc,		t_d	–	35	ns
Rise time	$I_C = 10$ mA dc, $I_{B1} = 1.0$ mA		t_r	–	35	ns
Storage time	$V_{CC} = 3.0$ V, $I_C = 10$ mA,	2N3946	t_s	–	300	ns
		2N3947		–	375	
Fall time	$I_{B1} = I_{B2} = 1.0$ mA dc		t_f	–	75	ns

(1) Pulse test: $PW \leq 300$ μs, Duty Cycle ≤ 2%.

▲ FIGURE 6–63

Partial datasheet for the 2N3946/2N3947.

ADVANCED PROBLEMS

51. In an amplifier such as the one in Figure 6–62, explain the general effect that a leaky coupling capacitor would have on circuit performance.

52. Draw the dc and ac equivalent circuits for the amplifier in Figure 6–62.

53. Modify the 2-stage amplifier in Figure 6–62 to drive a load of 10 kΩ and maintain the same voltage gain.

54. Design a single-stage common-emitter amplifier with a voltage gain of 40 dB that operates from a dc supply voltage of +12 V. Use a 2N2222 transistor, voltage-divider bias, and a 330 Ω swamping resistor. The maximum input signal is 25 mV rms.

55. Design an emitter-follower with a minimum input resistance of 50 kΩ using a 2N3904 *npn* transistor with a $\beta_{ac} = 100$.

56. Repeat Problem 55 using a 2N3906 with a $\beta_{ac} = 100$.

57. Design a single-stage common-base amplifier for a voltage gain of 75. Use a 2N3904 with emitter bias. The dc supply voltages are to be ±6 V.

58. Refer to the amplifier in Figure 6–62 and determine the minimum value of coupling capacitors necessary for the amplifier to produce the same output voltage at 100 Hz that it does at 5000 Hz.

59. Prove that for any unloaded common-emitter amplifier with a collector resistor R_C and R_E bypassed, the voltage gain is $A_v \cong 40\ V_{R_C}$.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

60. Open file TSP06-60 and determine the fault.

61. Open file TSP06-61 and determine the fault.

62. Open file TSP06-62 and determine the fault.

63. Open file TSP06-63 and determine the fault.

64. Open file TSP06-64 and determine the fault.

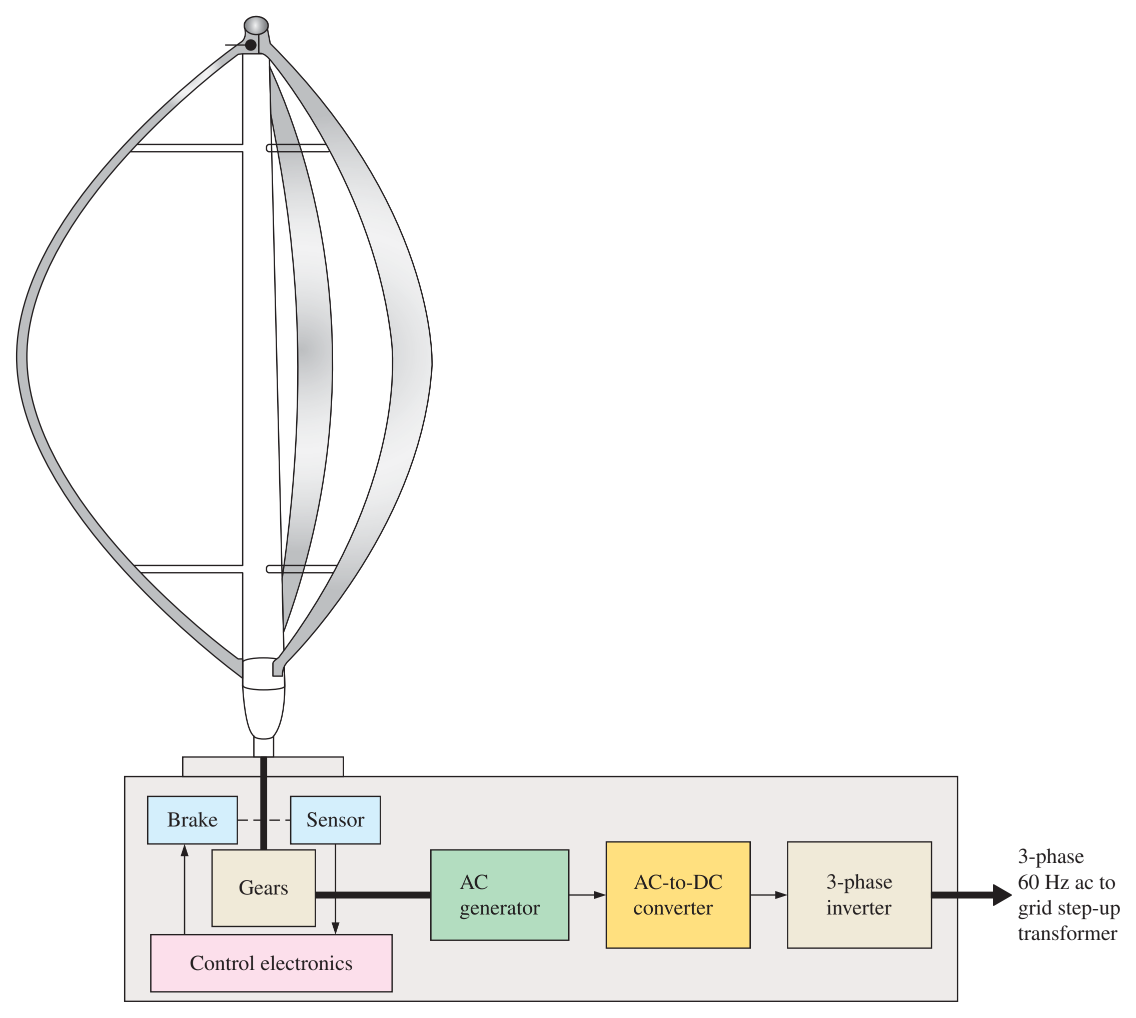
65. Open file TSP06-65 and determine the fault.

GreenTech Application 6: *Wind Power*

Vertical-Axis Turbines

In GreenTech Application 5, you learned about the horizontal-axis wind turbine (HAWT). Now, a second major type, the *vertical-axis wind turbine* (VAWT) is introduced. In a VAWT, the main rotor shaft is vertical instead of horizontal. An advantage of the VAWT is that the generator, gears, and electronics can be placed near or at ground level instead of high on top of the support tower as in a HAWT. This makes servicing much easier. Another advantage is that a VAWT does not have to be pointed toward the wind, eliminating the need for yaw mechanisms and circuits. It can capture wind from any direction. Also, VAWTs can be placed closer together in wind farms than HAWTs because HAWTs exhibit a slowing effect on the wind and VAWTs do not. Therefore, there is a limit on how close HAWTs can be to each other. At this time, the horizontal turbine is much more widely used than the vertical turbine. However, as improvements are made, the VAWT may become more competitive.

Darrieus or Eggbeater Turbine Figure GA6–1 shows one type of VAWT called a Darrieus, named after its inventer, but is more commonly known as an "eggbeater" turbine.



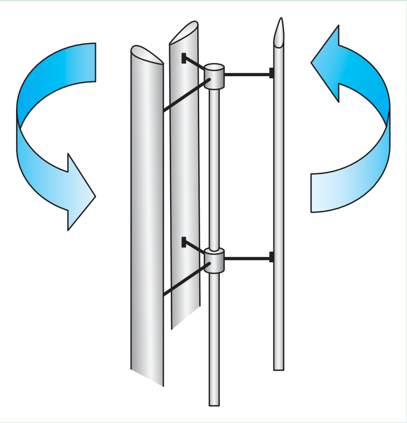
▲ FIGURE GA6–1

Diagram of a Darrieus or "eggbeater" VAWT. The size of the blade assembly is disproportionately small compared to the base, for the purpose of showing the block diagram.

VAWTs are difficult to mount on tall towers, so they are usually closer to the ground, thus requiring less support structure than HAWTs. Since the wind speed tends to be less at lower altitudes, the wind energy available is less than for a comparable-sized HAWT. Also, air flow near the ground is usually more turbulent causing more stress on the turbine. Notice that the block diagram is similar to that of the HAWT but is usually a bit simpler in terms of the control electronics. Since there is no requirement for yawing the turbine to move it into the wind, the electronics may simply detect the rotational speed of the shaft and slow or stop the blades when the wind speed reaches a specified level.

In practice, the Darrieus VAWT is typically less efficient than the propeller-driven HAWT because it does not handle variations in wind speed as effectively. Also, it is more difficult to protect the Darrieus from excessive wind speeds without completely shutting it down. It also has a lower starting torque and does not self-start very well, so an auxiliary starting motor may be required.

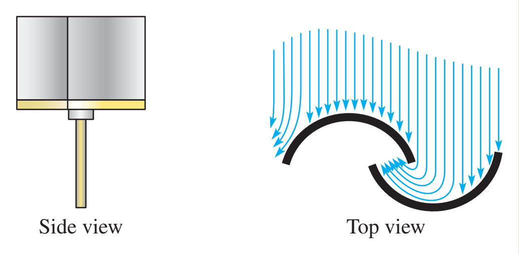
Giromill Turbine This turbine is a subtype of the Darrieus. Instead of curved blades, the giromill uses two or more straight airfoils (blades). A three-blade unit is shown in Figure GA6–2. Although it is cheaper and easier to build than a standard Darrieus turbine, it is less efficient, requires strong winds or a motor to start, and often cannot maintain a steady rate of rotation. A variation of this type of turbine has variable pitch airfoils for improvement of starting torque and reduction in torque pulsation due to uneven rotation rate.



◀ FIGURE GA6–2

A giromill turbine.

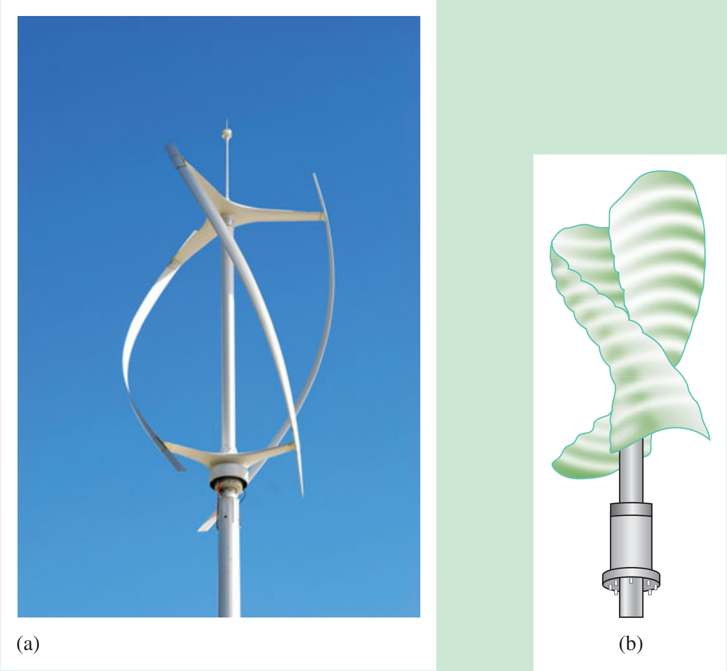
Savonius Turbines This is one of the simplest turbines but the least efficient. Aerodynamically, Savonius turbines are drag-type turbines because, as they rotate, the scoops have to move air out of the way whereas blade-type turbines work on the principle of aerodynamic lift. One form of a two-scoop turbine is shown in Figure GA6–3; sometimes three or more scoops are used. The Savonius turbine is generally limited to small power applications. In the figure, the rotation is clockwise with the wind direction as shown.



▲ FIGURE GA6–3

A form of Savonius VAWT.

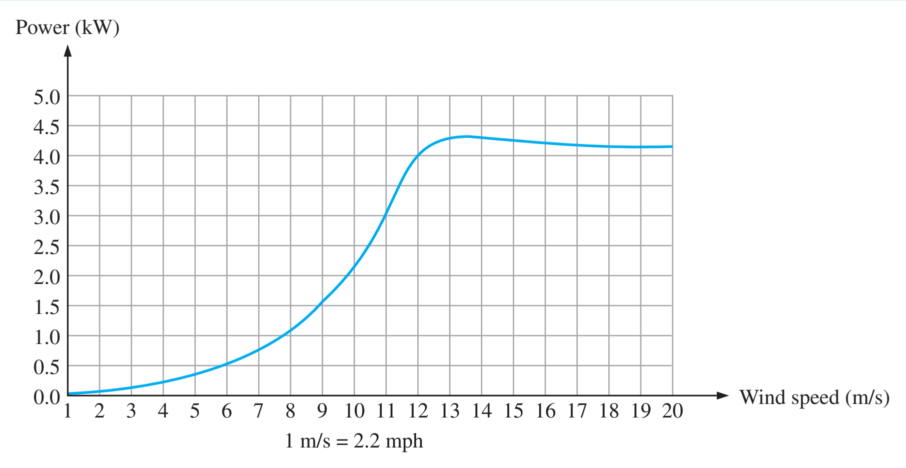
Helical Wind Turbines Another variation of the Darrieus, the helical VAWT, has blades that are shaped in a twisted helical pattern. Some advantages are that the helical turbine tends to rotate more quietly that other types of blade turbines. Also, the helical turbine can withstand much higher wind speeds than other turbines and can begin rotation at much lower wind speeds than other types of VAWTs. A photo of one type of helical configuration is shown in Figure GA6–4(a). Other forms of helix turbines are also used, as shown in part (b).



▲ **FIGURE GA6–4**

Two types of helical turbine.

A typical power curve for a typical helical turbine is shown in Figure GA6–5. Most wind turbines exhibit a similar-shaped power curve. Notice that the shape in the figure is very similar to that for the HAWT although the variable values are different for the lower power VAWT.



▲ **FIGURE GA6–5**

Power curve for helical wind turbine.

Questions

Some questions may require research beyond the content of this coverage. Answers can be found at www.pearsonhighered.com/floyd.

1. What does VAWT stand for?
2. What are the basic types of VAWT?
3. What are some advantages and disadvantages when comparing HAWTs and VAWTs?
4. What type of wind turbine would you select to power a small home? Why?

The following websites are recommended for viewing VAWTs in action. Many other websites are also available.

DARRIEUS

http://www.youtube.com/watch?v=NxMh18SGhyA

http://www.youtube.com/watch?v=Op2LtTK0x74

GIROMILL

http://www.youtube.com/watch?v=PSdU050dHdY

http://www.youtube.com/watch?v=TsCyzSxI3fc&NR=1

http://www.youtube.com/watch?v=-rQUdRMTnyM&feature=related

SAVONIUS

http://www.youtube.com/watch?v=HylhATL_Sek&feature=related

http://www.youtube.com/watch?v=-IWgXmgQlAg

http://www.youtube.com/watch?v=NMnZn6p1VLs

HELICAL

http://myefficientplanet.com/681/vertical-axis-wind-turbine-helix-lift-type-vawt/

http://www.gstriatum.com/solarenergy/2009/01/helix-wind-turbine-another-for-your-home/

http://www.youtube.com/watch?v=UruwjajWmXw

http://www.youtube.com/watch?v=sOagiPQ79Go&feature=related

7

Power Amplifiers

CHAPTER OUTLINE

7–1 The Class A Power Amplifier
7–2 The Class B and Class AB Push-Pull Amplifiers
7–3 The Class C Amplifier
7–4 Troubleshooting
Application Activity

CHAPTER OBJECTIVES

- Explain and analyze the operation of class A amplifiers
- Explain and analyze the operation of class B and class AB amplifiers
- Explain and analyze the operation of class C amplifiers
- Troubleshoot power amplifiers

KEY TERMS

- Class A
- Power gain
- Efficiency
- Class B
- Push-pull
- Class AB
- Class C

APPLICATION ACTIVITY PREVIEW

The Application Activity in this chapter continues with the public address system started in Chapter 6. Recall that the complete system includes the preamplifier, a power amplifier, and a dc power supply. You will focus on the power amplifier in this chapter and complete the total system by combining the three component parts.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

Power amplifiers are large-signal amplifiers. This generally means that a much larger portion of the load line is used during signal operation than in a small-signal amplifier. In this chapter, we will cover four classes of power amplifiers: class A, class B, class AB, and class C. These amplifier classifications are based on the percentage of the input cycle for which the amplifier operates in its linear region. Each class has a unique circuit configuration because of the way it must be operated. The emphasis is on power amplification.

Power amplifiers are normally used as the final stage of a communications receiver or transmitter to provide signal power to speakers or to a transmitting antenna. BJTs are used to illustrate power amplifier principles.

7–1 THE CLASS A POWER AMPLIFIER

When an amplifier is biased such that it always operates in the linear region where the output signal is an amplified replica of the input signal, it is a **class A** amplifier. The discussion of amplifiers in the previous chapters apply to class A operation. Power amplifiers are those amplifiers that have the objective of delivering power to a load. This means that components must be considered in terms of their ability to dissipate heat.

After completing this section, you should be able to

- **Explain and analyze the operation of class A amplifiers**
- Discuss transistor heat dissipation
    - Describe the purpose of a heat sink
- Discuss the importance of a centered Q-point
    - Describe the relationship of the dc and ac load lines with the Q-point
    - Describe the effects of a noncentered Q-point on the output waveform
- Determine power gain
- Define *dc quiescent power*
- Discuss and determine output signal power
- Define and determine the *efficiency* of a power amplifier

In a small-signal amplifier, the ac signal moves over a small percentage of the total ac load line. When the output signal is larger and approaches the limits of the ac load line, the amplifier is a **large-signal** type. Both large-signal and small-signal amplifiers are considered to be class A if they operate in the linear region at all times, as illustrated in Figure 7–1. Class A power amplifiers are large-signal amplifiers with the objective of providing power (rather than voltage) to a load. As a rule of thumb, an amplifier may be considered to be a power amplifier if it is rated for more than 1 W and it is necessary to consider the problem of heat dissipation in components.

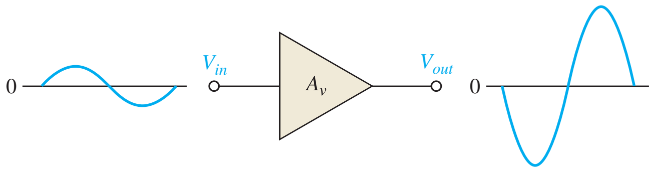


FIGURE 7–1

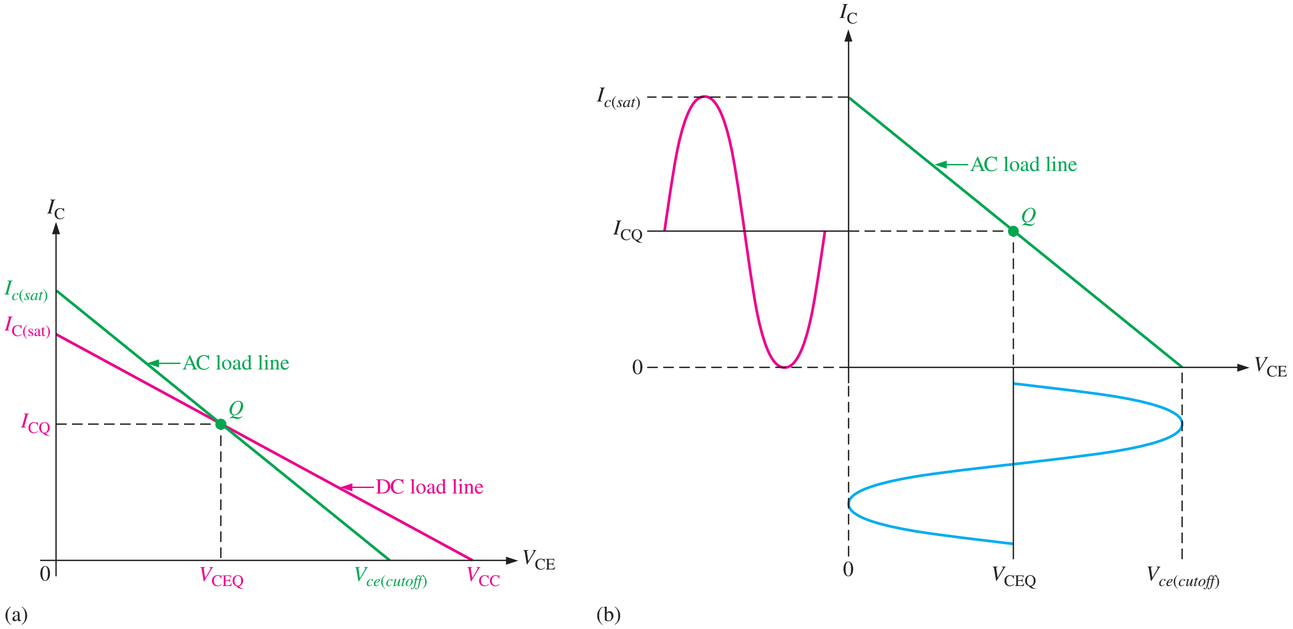
Basic class A amplifier operation. Output is shown 180° out of phase with the input (inverted).

Heat Dissipation

Power transistors (and other power devices) must dissipate a large amount of internally generated heat. For BJT power transistors, the collector terminal is the critical junction; for this reason, the transistor's case is always connected to the collector terminal. The case of all power transistors is designed to provide a large contact area between it and an external heat sink. Heat from the transistor flows through the case to the heat sink and then dissipates in the surrounding air. Heat sinks vary in size, number of fins, and type of material. Their size depends on the heat dissipation requirement and the maximum ambient temperature in which the transistor is to operate. In high-power applications (a few hundred watts), a cooling fan may be necessary.

Centered Q-Point

Recall that the dc and ac load lines intersect at the Q-point. When the Q-point is at the center of the ac load line, a maximum class A signal can be obtained. You can see this concept by examining the graph of the load line for a given amplifier in Figure 7–2(a). This graph shows the ac load line with the Q-point at its center. The collector current can vary from its



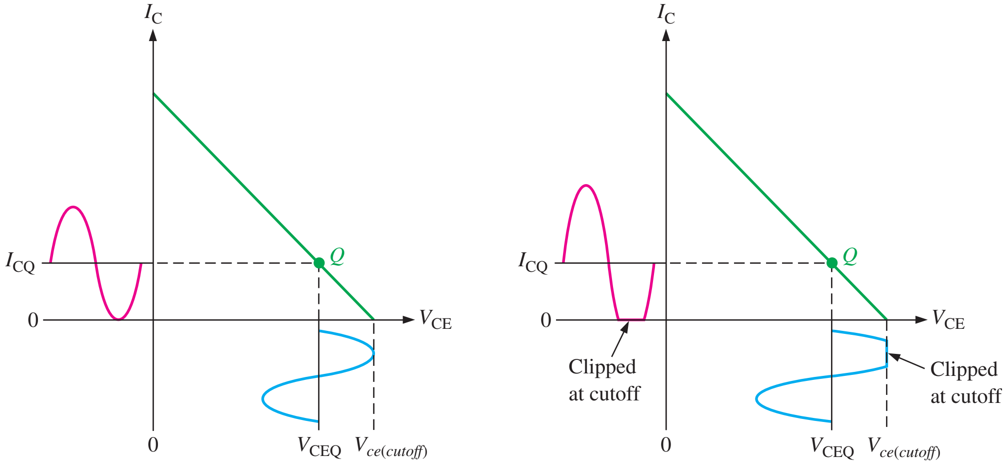
I_C
$I_{c(sat)}$
$I_{C(sat)}$
AC load line
I_{CQ}
Q
DC load line
0
V_{CEQ}
$V_{ce(cutoff)}$
V_{CC}
V_{CE}
(a)
I_C
$I_{c(sat)}$
AC load line
I_{CQ}
Q
0
V_{CE}
0
V_{CEQ}
$V_{ce(cutoff)}$
(b)

▲ FIGURE 7–2

Maximum class A output occurs when the Q-point is centered on the ac load line.

Q-point value, I_{CQ}, up to its saturation value, $I_{c(sat)}$, and down to its cutoff value of zero. Likewise, the collector-to-emitter voltage can swing from its Q-point value, V_{CEQ}, up to its cutoff value, $V_{ce(cutoff)}$, and down to its saturation value of near zero. This operation is indicated in Figure 7–2(b). The peak value of the collector current equals I_{CQ}, and the peak value of the collector-to-emitter voltage equals V_{CEQ} in this case. This signal is the maximum that can be obtained from the class A amplifier. Actually, the output cannot quite reach saturation or cutoff, so the practical maximum is slightly less.

If the Q-point is not centered on the ac load line, the output signal is limited. Figure 7–3 shows an ac load line with the Q-point moved away from center toward cutoff. The output variation is limited by cutoff in this case. The collector current can only swing down to near zero and an equal amount above I_{CQ}. The collector-to-emitter voltage can only swing up to its



I_C
I_{CQ}
Q
0
V_{CE}
0
V_{CEQ}
$V_{ce(cutoff)}$
I_C
I_{CQ}
Q
0
V_{CE}
Clipped at cutoff
Clipped at cutoff
0
V_{CEQ}
$V_{ce(cutoff)}$

(a) Amplitude of V_{ce} and I_c limited by cutoff

(b) Transistor driven into cutoff by a further increase in input amplitude

▲ FIGURE 7–3

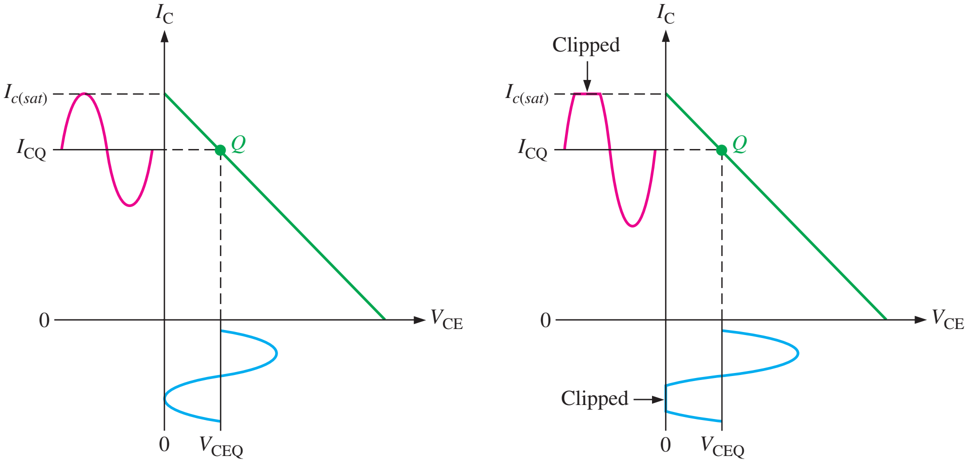
Q-point closer to cutoff.

cutoff value and an equal amount below V_{CEQ}. This situation is illustrated in Figure 7–3(a). If the amplifier is driven any further than this, it will "clip" at cutoff, as shown in Figure 7–3(b).

Figure 7–4 shows an ac load line with the Q-point moved away from center toward saturation. In this case, the output variation is limited by saturation. The collector current can only swing up to near saturation and an equal amount below I_{CQ}. The collector-to-emitter voltage can only swing down to its saturation value and an equal amount above V_{CEQ}. This situation is illustrated in Figure 7–4(a). If the amplifier is driven any further, it will "clip" at saturation, as shown in Figure 7–4(b).

FIGURE 7–4

Q-point closer to saturation.



(a) Amplitude of V_{ce} and I_c limited by saturation

(b) Transistor driven into saturation by a further increase in input amplitude

Power Gain

A power amplifier delivers power to a load. The **power gain** of an amplifier is the ratio of the output power (power delivered to the load) to the input power. In general, power gain is

Equation 7–1

$$\boldsymbol{A_p = \frac{P_L}{P_{in}}}$$

where A_p is the power gain, P_L is signal power delivered to the load, and P_{in} is signal power delivered to the amplifier.

The power gain can be computed by any of several formulas, depending on what is known. Frequently, the easiest way to obtain power gain is from input resistance, load resistance, and voltage gain. To see how this is done, recall that power can be expressed in terms of voltage and resistance as

$$P = \frac{V^2}{R}$$

For ac power, the voltage is expressed as rms. The output power delivered to the load is

$$P_L = \frac{V_L^2}{R_L}$$

The input power delivered to the amplifier is

$$P_{in} = \frac{V_{in}^2}{R_{in}}$$

By substituting into Equation 7–1, the following useful relationship is produced:

$$A_p = \frac{V_L^2}{V_{in}^2}\left(\frac{R_{in}}{R_L}\right)$$

Since $V_L/V_{in} = A_v$,

$$\boldsymbol{A_p = A_v^2\left(\frac{R_{in}}{R_L}\right)}$$

Equation 7–2

Recall from Chapter 6 that for a voltage-divider biased amplifier,

$$R_{in(tot)} = R_1 \parallel R_2 \parallel R_{in(base)}$$

and that for a CE or CC amplifier,

$$R_{in(base)} = \beta_{ac}R_e$$

Equation 7–2 shows that the power gain of an amplifier is the voltage gain squared times the ratio of the input resistance to the output load resistance. The formula can be applied to any amplifier. For example, assume a common-collector (CC) amplifier has an input resistance of 5 kΩ and a load resistance of 100 Ω. Since a CC amplifier has a voltage gain of approximately 1, the power gain is

$$A_p = A_v^2\left(\frac{R_{in}}{R_L}\right) = 1^2\left(\frac{5\text{ k}\Omega}{100\ \Omega}\right) = 50$$

For a CC amplifier, A_p is just the ratio of the input resistance to the output load resistance.

DC Quiescent Power

The power dissipation of a transistor with no signal input is the product of its Q-point current and voltage.

$$\boldsymbol{P_{\mathrm{DQ}} = I_{\mathrm{CQ}}V_{\mathrm{CEQ}}}$$

Equation 7–3

The only way a class A power amplifier can supply power to a load is to maintain a quiescent current that is at least as large as the peak current requirement for the load current. A signal will not increase the power dissipated by the transistor but actually causes less total power to be dissipated. The **dc quiescent power**, given in Equation 7–3, is the maximum power that a class A amplifier must handle. The transistor's power rating must exceed this value.

Output Power

In general, the output signal power is the product of the rms load current and the rms load voltage. The maximum unclipped ac signal occurs when the Q-point is centered on the ac load line. For a CE amplifier with a centered Q-point, the maximum peak voltage swing is

$$V_{c(max)} = I_{\mathrm{CQ}}R_c$$

The rms value is $0.707V_{c(max)}$.

The maximum peak current swing is

$$I_{c(max)} = \frac{V_{\mathrm{CEQ}}}{R_c}$$

The rms value is $0.707I_{c(max)}$.

To find the maximum signal power output, use the rms values of maximum current and voltage. The maximum power out from a class A amplifier is

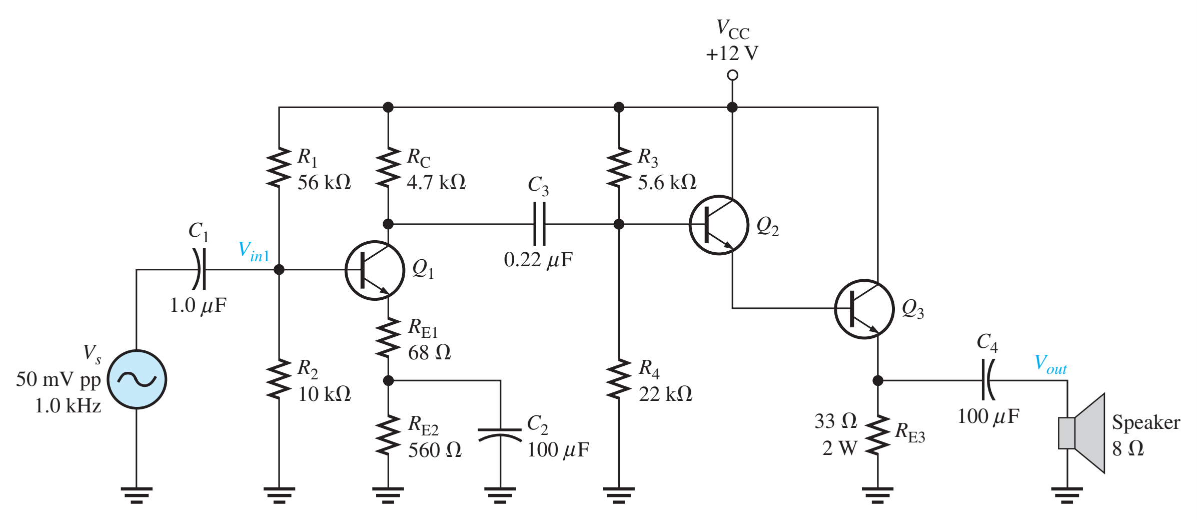
$$P_{out(max)} = (0.707I_c)(0.707V_c)$$

$$\boldsymbol{P_{out(max)} = 0.5I_{\mathrm{CQ}}V_{\mathrm{CEQ}}}$$

Equation 7–4

EXAMPLE 7–1

Determine the voltage gain and the power gain of the class A power amplifier in Figure 7–5. Assume $\beta_{ac} = 200$ for all transistors.



▲ FIGURE 7–5

Solution Notice that the first stage (Q_1) is a voltage-divider biased common-emitter with a swamping resistor (R_{E1}). The second stage (Q_2 and Q_3) is a Darlington voltage-follower configuration. The speaker is the load.

First stage: The ac collector resistance of the first stage is R_C in parallel with the input resistance to the second stage.

$$R_{c1} \cong R_C \| (R_3 \| R_4) = 4.7\text{ k}\Omega \| 5.6\text{ k}\Omega \| 22\text{ k}\Omega = 2.29\text{ k}\Omega$$

The voltage gain of the first stage is the ac collector resistance, R_{c1}, divided by the ac emitter resistance, which is the sum of $R_{E1} + r'_{e(Q1)}$. The approximate value of $r'_{e(Q1)}$ is determined by first finding I_E.

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\text{ k}\Omega}{66\text{ k}\Omega}\right)12\text{ V} = 1.82\text{ V}$$

$$I_E = \frac{V_B - 0.7\text{ V}}{R_{E1} + R_{E2}} = \frac{1.82\text{ V} - 0.7\text{ V}}{628\ \Omega} = 1.78\text{ mA}$$

$$r'_{e(Q1)} = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1.78\text{ mA}} = 14\ \Omega$$

Using the value of r'_e, determine the voltage gain of the first stage with the loading of the second stage taken into account.

$$A_{v1} = -\frac{R_{c1}}{R_{E1} + r'_{e(Q1)}} = -\frac{2.29\text{ k}\Omega}{68\ \Omega + 14\ \Omega} = -27.9$$

The negative sign is for inversion.

The total input resistance of the first stage is equal to the bias resistors in parallel with the ac input resistance at the base of Q_1.

$$R_{in(tot)1} = R_1 \| R_2 \| \beta_{ac(Q1)}(R_{E1} + r'_{e(Q1)})$$
$$= 56\text{ k}\Omega \| 10\text{ k}\Omega \| 200(68\ \Omega + 14\ \Omega) = 8.4\text{ k}\Omega$$

Second stage: The voltage gain of the darlington emitter-follower is approximately equal to 1.

$$A_{v2} \cong 1$$

Overall amplifier: The overall voltage gain is the product of the first and second stage voltage gains. Since the second stage has a gain of approximately 1, the overall gain is approximately equal to the gain of the first stage.

$$A_{v(tot)} = A_{v1}A_{v2} = (-27.9)(1) = -27.9$$

Power gain: The power gain of the amplifier can be calculated using Equation 7–2.

$$A_p = A^2_{v(tot)}\left(\frac{R_{in(tot)1}}{R_L}\right) = (-27.9)^2\left(\frac{8.4\text{ k}\Omega}{8\ \Omega}\right) = \mathbf{817{,}330}$$

Related Problem[*] What happens to the power gain if a second 8 Ω speaker is connected in parallel with the first one?

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Efficiency

The **efficiency** of any amplifier is the ratio of the output signal power supplied to a load to the total power from the dc supply. The maximum output signal power that can be obtained is given by Equation 7–4. The average power supply current, I_{CC}, is equal to I_{CQ} and the supply voltage is at least $2V_{CEQ}$. Therefore, the total dc power is

$$P_{DC} = I_{CC}V_{CC} = 2I_{CQ}V_{CEQ}$$

The maximum efficiency, η_{max}, of a capacitively coupled class A amplifier is

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.5I_{CQ}V_{CEQ}}{2I_{CQ}V_{CEQ}} = 0.25$$

The maximum efficiency of a capacitively coupled class A amplifier cannot be higher than 0.25, or 25%, and, in practice, is usually considerably less (about 10%). Although the efficiency can be made higher by transformer coupling the signal to the load, there are drawbacks to transformer coupling. These drawbacks include the size and cost of transformers as well as potential distortion problems when the transformer core begins to saturate. In general, the low efficiency of class A amplifiers limits their usefulness to small power applications that require usually less than 1 W.

EXAMPLE 7–2 Determine the efficiency of the power amplifier in Figure 7–5 (Example 7–1).

Solution The efficiency is the ratio of the signal power in the load to the power supplied by the dc source. The input voltage is 50 mV peak-to-peak which is 35.4 mV rms. The input power is, therefore,

$$P_{in} = \frac{V^2_{in}}{R_{in}} = \frac{(35.4\text{ mV})^2}{8.4\text{ k}\Omega} = 149\text{ nW}$$

The output power is

$$P_{out} = P_{in}A_p = (149\text{ nW})(817{,}330) = 122\text{ mW}$$

Most of the power from the dc source is supplied to the output stage. The current in the output stage can be computed from the dc emitter voltage of Q_3.

$$V_{E(Q3)} \cong \left(\frac{22\text{ k}\Omega}{27.6\text{ k}\Omega}\right)12\text{ V} - 1.4\text{ V} = 8.2\text{ V}$$

$$I_{E(Q3)} = \frac{V_{E(Q3)}}{R_E} = \frac{8.2\text{ V}}{33\ \Omega} = 0.25\text{ A}$$

Neglecting the other transistor and bias currents, which are very small, the total dc supply current is about 0.25 A. The power from the dc source is

$$P_{DC} = I_{CC}V_{CC} = (0.25\text{ A})(12\text{ V}) = 3\text{ W}$$

Therefore, the efficiency of the amplifier for this input is

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{122\text{ mW}}{3\text{ W}} \cong \mathbf{0.04}$$

This represents an efficiency of 4% and illustrates why class A is not a good choice for a power amplifier.

Related Problem Explain what happens to the efficiency if R_{E3} were replaced with the speaker. What problem does this have?

SECTION 7–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What is the purpose of a heat sink?
2. Which lead of a BJT is connected to the case?
3. What are the two types of clipping with a class A power amplifier?
4. What is the maximum efficiency for a class A amplifier?
5. How can the power gain of a CC amplifier be expressed in terms of a ratio of resistances?

7–2 THE CLASS B AND CLASS AB PUSH-PULL AMPLIFIERS

When an amplifier is biased at cutoff so that it operates in the linear region for 180° of the input cycle and is in cutoff for 180°, it is a **class B** amplifier. Class AB amplifiers are biased to conduct for slightly more than 180°. The primary advantage of a class B or class AB amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B or class AB is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform. The term *push-pull* refers to a common type of class B or class AB amplifier circuit in which two transistors are used on alternating half-cycles to reproduce the input waveform at the output.

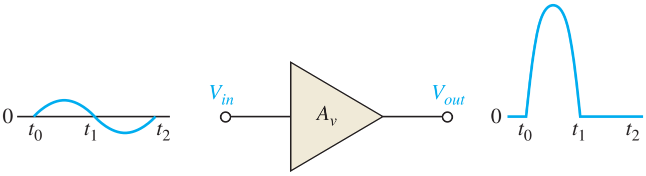
After completing this section, you should be able to

- ❑ **Explain and analyze the operation of class B and class AB amplifiers**
- ❑ Describe class B operation
  - ◆ Discuss Q-point location
- ❑ Describe class B push-pull operation
  - ◆ Discuss transformer coupling
  - ◆ Explain *complementary symmetry transistors*
  - ◆ Explain crossover distortion

- Bias a push-pull amplifier for class AB operation
  - Define *class AB*
  - Explain class AB ac signal operation
- Describe a single-supply push-pull amplifier
- Discuss class B/AB power
  - Calculate maximum output power
  - Calculate dc input power
  - Determine efficiency
- Determine the ac input resistance of a push-pull amplifier
- Discuss the Darlington class AB amplifier
  - Determine ac input resistance
- Describe the Darlington/complementary Darlington class AB amplifier

Class B Operation

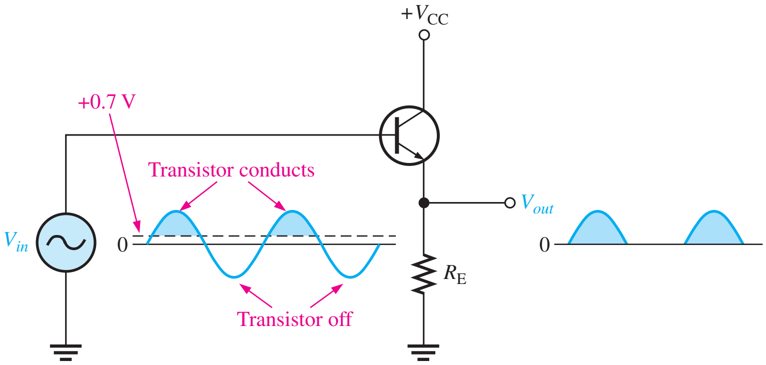
The class B operation is illustrated in Figure 7–6, where the output waveform is shown relative to the input in terms of time (t).



▲ FIGURE 7–6

Basic class B amplifier operation (noninverting).

The Q-Point Is at Cutoff The class B amplifier is biased at the cutoff point so that $I_{CQ} = 0$ and $V_{CEQ} = V_{CE(cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in Figure 7–7 with an emitter-follower circuit where the output is not a replica of the input.



▲ FIGURE 7–7

Common-collector class B amplifier.

Class B Push-Pull Operation

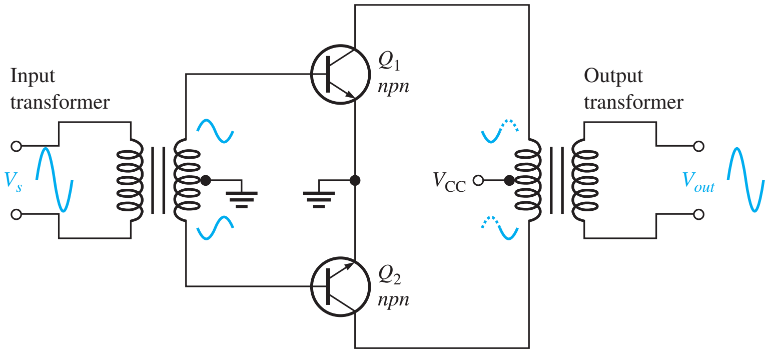
As you can see, the circuit in Figure 7–7 only conducts for the positive half of the cycle. To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle. The combination of two class B amplifiers working together is called **push-pull** operation.

There are two common approaches for using push-pull amplifiers to reproduce the entire waveform. The first approach uses transformer coupling. The second uses two **complementary symmetry transistors;** these are a matching pair of *npn*/*pnp* BJTs.

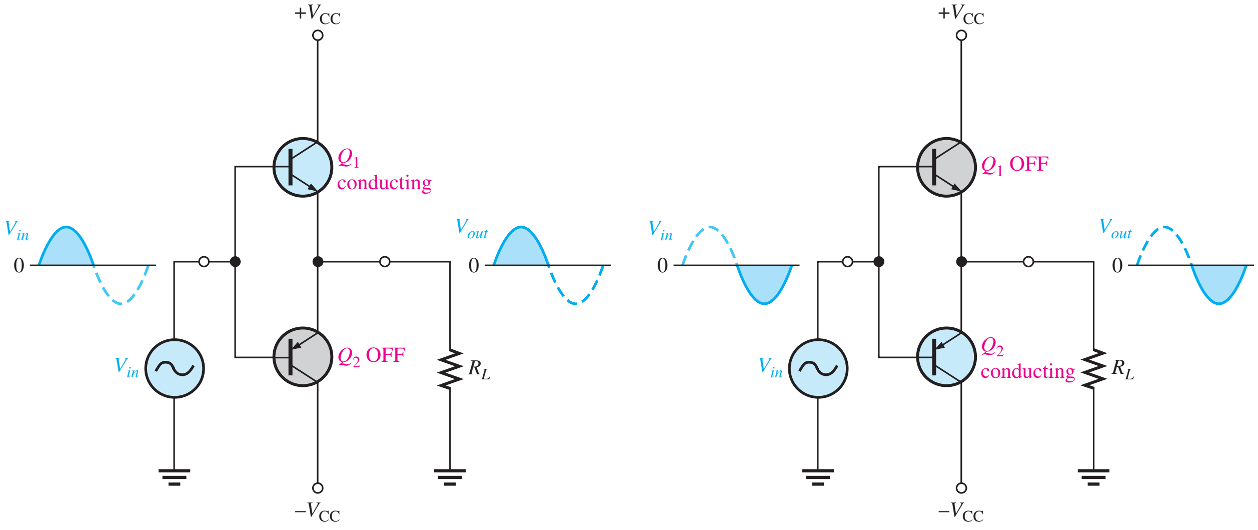
Transformer Coupling Transformer coupling is illustrated in Figure 7–8. The input transformer has a center-tapped secondary that is connected to ground, producing phase inversion of one side with respect to the other. The input transformer thus converts the input signal to two out-of-phase signals for the transistors. Notice that both transistors are *npn* types. Because of the signal inversion, Q_1 will conduct on the positive part of the cycle and Q_2 will conduct on the negative part. The output transformer combines the signals by permitting current in both directions, even though one transistor is always cut off. The positive power supply signal is connected to the center tap of the output transformer.

▶ FIGURE 7–8

Transformer-coupled push-pull amplifiers. Q_1 conducts during the positive half-cycle; Q_2 conducts during the negative half-cycle. The two halves are combined by the output transformer.



Complementary Symmetry Transistors Figure 7–9 shows one of the most popular types of push-pull class B amplifiers using two emitter-followers and both positive and negative power supplies. This is a complementary amplifier because one emitter-follower uses an *npn* transistor and the other a *pnp,* which conduct on opposite alternations of the input cycle. Notice that there is no dc base bias voltage ($V_B = 0$). Thus, only the signal voltage drives the transistors into conduction. Transistor Q_1 conducts during the positive half of the input cycle, and Q_2 conducts during the negative half.



(a) During a positive half-cycle

(b) During a negative half-cycle

▲ FIGURE 7–9

Class B push-pull ac operation.

Crossover Distortion When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting, as shown in Figure 7–10. The resulting distortion in the output waveform is called **crossover distortion.**

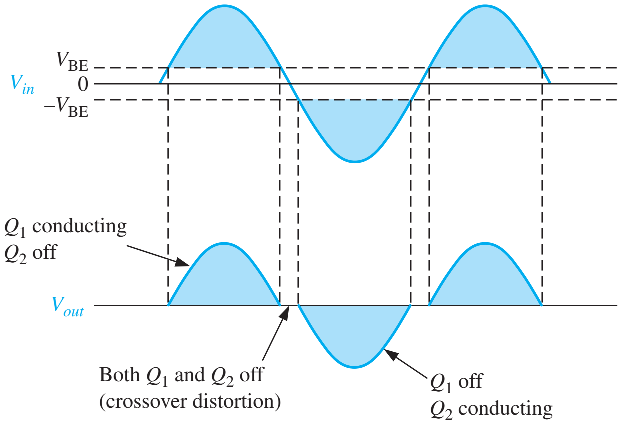


FIGURE 7–10

Illustration of crossover distortion in a class B push-pull amplifier. The transistors conduct only during portions of the input indicated by the shaded areas.

Biasing the Push-Pull Amplifier for Class AB Operation

To overcome crossover distortion, the biasing is adjusted to just overcome the V_{BE} of the transistors; this results in a modified form of operation called **class AB**. In class AB operation, the push-pull stages are biased into slight conduction, even when no input signal is present. This can be done with a voltage-divider and diode arrangement, as shown in Figure 7–11. When the diode characteristics of D_1 and D_2 are closely matched to the characteristics of the transistor base-emitter junctions, the current in the diodes and the current in the transistors are the same; this is called a **current mirror.** This current mirror produces the desired class AB operation and eliminates crossover distortion.

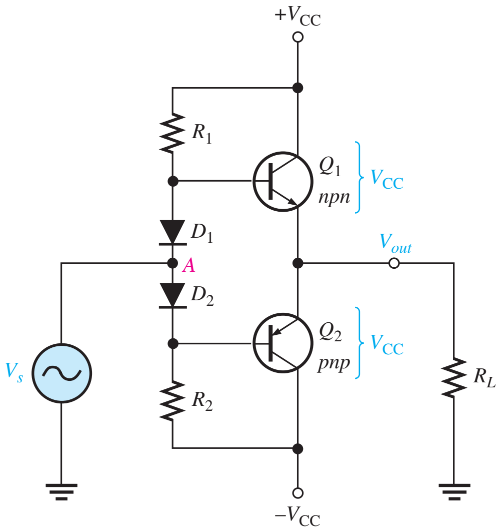


FIGURE 7–11

Biasing the push-pull amplifier with current-mirror diode bias to eliminate crossover distortion. The transistors form a complementary pair (one *npn* and one *pnp*).

In the bias path of the circuit in Figure 7–11, R_1 and R_2 are of equal value, as are the positive and negative supply voltages. This forces the voltage at point A (between the diodes) to equal 0 V and eliminates the need for an input coupling capacitor. The dc voltage on the output is also 0 V. Assuming that both diodes and both complementary transistors are identical, the drop across D_1 equals the V_{BE} of Q_1, and the drop across D_2 equals the V_{BE} of Q_2. Since they are matched, the diode current will be the same as I_{CQ}. The diode current and I_{CQ} can be found by applying Ohm's law to either R_1 or R_2 as follows:

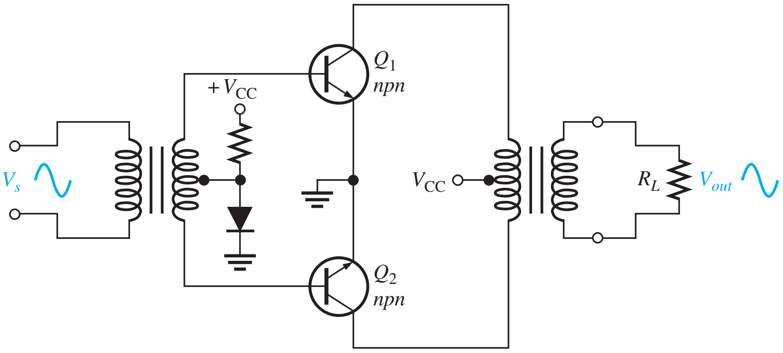
$$I_{CQ} = \frac{V_{CC} - 0.7\text{ V}}{R_1}$$

This small current required of class AB operation eliminates the crossover distortion but has the potential for thermal instability if the transistor's V_{BE} drops are not matched to the diode drops or if the diodes are not in thermal equilibrium with the transistors. Heat in the power transistors decreases the base-emitter voltage and tends to increase current. If the diodes are warmed the same amount, the current is stabilized; but if the diodes are in a cooler environment, they cause I_{CQ} to increase even more. More heat is produced in an unrestrained cycle known as *thermal runaway*. To keep this from happening, the diodes should have the same thermal environment as the transistors. In some cases, a small resistor in the emitter of each transistor can alleviate thermal runaway.

Crossover distortion also occurs in transformer-coupled amplifiers like the one shown in Figure 7–8. To eliminate it in this case, 0.7 V is applied to the input transformer's secondary that just biases both transistors into conduction. The bias voltage to produce this drop can be derived from the power supply using a single diode as shown in Figure 7–12.

FIGURE 7–12

Eliminating crossover distortion in a transformer-coupled push-pull amplifier. The biased diode compensates for the base-emitter drop of the transistors and produces class AB operation.



AC Operation Consider the ac load line for Q_1 of the class AB amplifier in Figure 7–11. The Q-point is slightly above cutoff. (In a true class B amplifier, the Q-point is at cutoff.) The ac cutoff voltage for a two-supply operation is at V_{CC} with an I_{CQ} as given earlier. The ac saturation current for a two-supply operation with a push-pull amplifier is

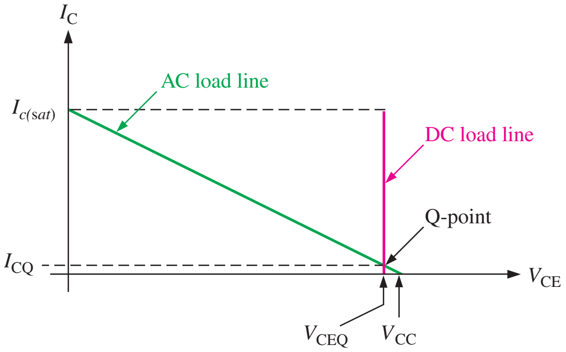
Equation 7–5

$$I_{c(sat)} = \frac{V_{CC}}{R_L}$$

The ac load line for the *npn* transistor is as shown in Figure 7–13. The dc load line can be found by drawing a line that passes through V_{CEQ} and the dc saturation current, $I_{C(sat)}$. However, the saturation current for dc is the current if the collector to emitter is shorted on

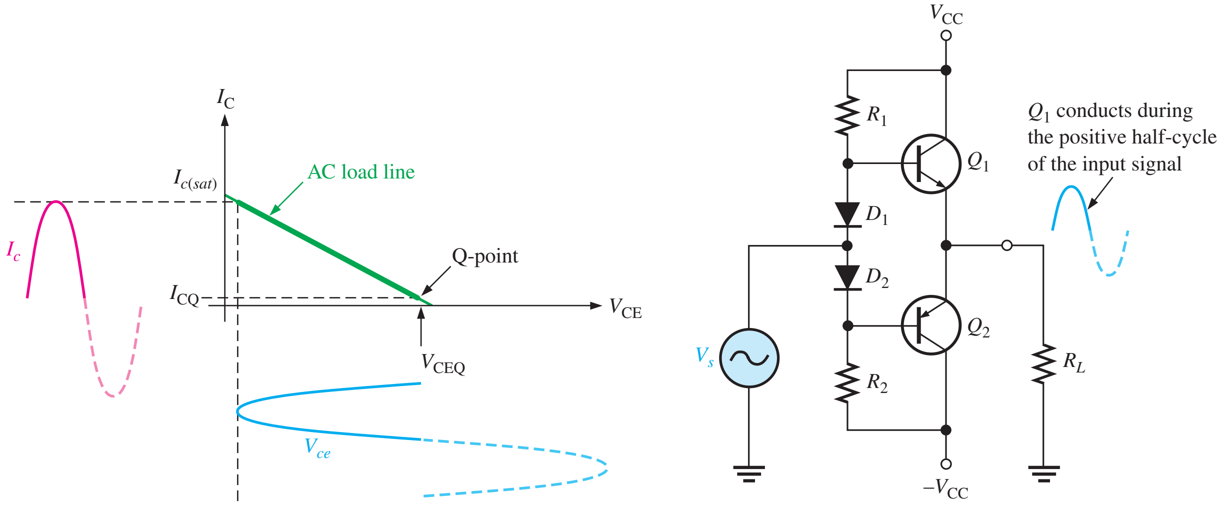
FIGURE 7–13

Load lines for a complementary symmetry push-pull amplifier. Only the load lines for the *npn* transistor are shown.



both transistors! This assumed short across the power supplies obviously would cause maximum current from the supplies and implies the dc load line passes almost vertically through the cutoff as shown. Operation along the dc load line, such as caused by thermal runaway, could produce such a high current that the transistors are destroyed.

Figure 7–14(a) illustrates the ac load line for Q_1 of the class AB amplifier in Figure 7–14(b). In the case illustrated, a signal is applied that swings over the region of the ac load line shown in bold. At the upper end of the ac load line, the voltage across the transistor (V_{ce}) is a minimum, and the output voltage is maximum.



(a) AC load line for Q_1

(b) Circuit

▲ FIGURE 7–14

Under maximum conditions, transistors Q_1 and Q_2 are alternately driven from near cutoff to near saturation. During the positive alternation of the input signal, the Q_1 emitter is driven from its Q-point value of 0 to nearly V_{CC}, producing a positive peak voltage a little less than V_{CC}. Likewise, during the negative alternation of the input signal, the Q_2 emitter is driven from its Q-point value of 0 V, to near $-V_{CC}$, producing a negative peak voltage almost equal to $-V_{CC}$. Although it is possible to operate close to the saturation current, this type of operation results in increased distortion of the signal.

The ac saturation current (Equation 7–5) is also the peak output current. Each transistor can essentially operate over its entire load line. Recall that in class A operation, the transistor can also operate over the entire load line but with a significant difference. In class A operation, the Q-point is near the middle and there is significant current in the transistors even with no signal. In class B operation, when there is no signal, the transistors have only a very small current and therefore dissipate very little power. Thus, the efficiency of a class B amplifier can be much higher than a class A amplifier. It will be shown later that the maximum efficiency of a class B amplifier is 79%.

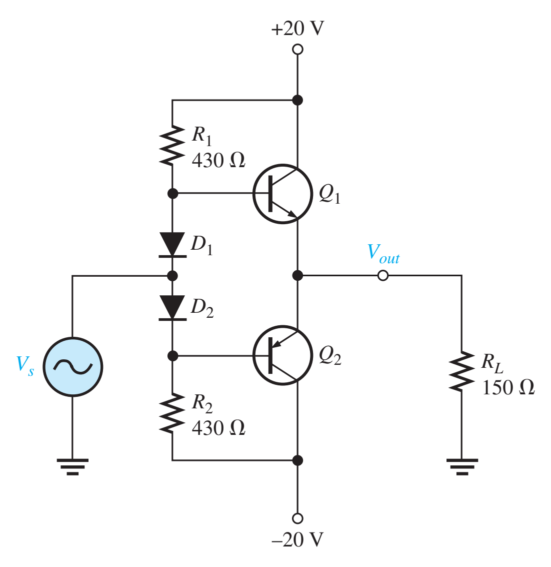
EXAMPLE 7–3

Determine the ideal maximum peak output voltage and current for the circuit shown in Figure 7–15.

Solution The ideal maximum peak output voltage is

$$V_{out(peak)} \cong V_{CEQ} \cong V_{CC} = \mathbf{20\ V}$$

FIGURE 7–15



The ideal maximum peak current is

$$I_{out(peak)} \cong I_{c(sat)} \cong \frac{V_{CC}}{R_L} = \frac{20\text{ V}}{150\ \Omega} = \mathbf{133\ mA}$$

The actual maximum values of voltage and current are slightly smaller.

Related Problem What is the maximum peak output voltage and current if the supply voltages are changed to +15 V and −15 V?

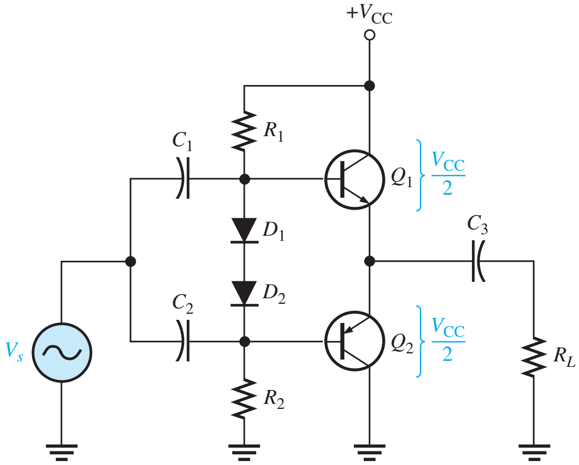
Open the Multisim file E07-03 in the Examples folder on the companion website. Measure the maximum peak-to-peak output voltage.

Single-Supply Push-Pull Amplifier

Push-pull amplifiers using complementary symmetry transistors can be operated from a single voltage source as shown in Figure 7–16. The circuit operation is the same as that described previously, except the bias is set to force the output emitter voltage to be $V_{CC}/2$ instead of zero volts used with two supplies. Because the output is not biased at zero volts,

FIGURE 7–16

Single-ended push-pull amplifier.

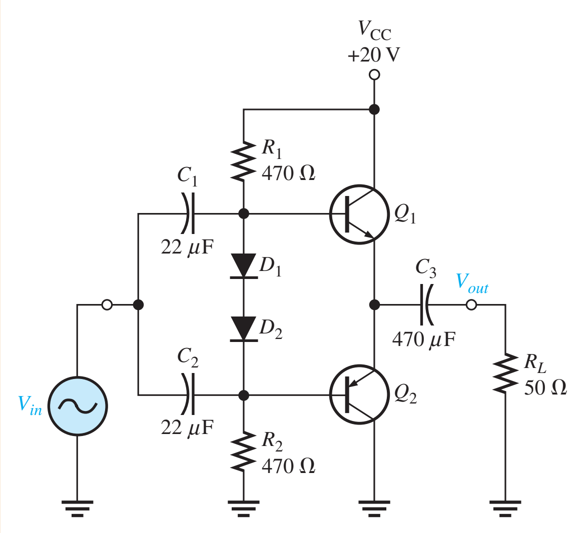


capacitive coupling for the input and output is necessary to block the bias voltage from the source and the load resistor. Ideally, the output voltage can swing from zero to V_{CC}, but in practice it does not quite reach these ideal values.

EXAMPLE 7–4

Determine the maximum ideal peak values for the output voltage and current in Figure 7–17.

▶ FIGURE 7–17



Solution The maximum peak output voltage is

$$V_{out(peak)} \cong V_{CEQ} = \frac{V_{CC}}{2} = \frac{20\text{ V}}{2} = \mathbf{10\text{ V}}$$

The maximum peak output current is

$$I_{out(peak)} \cong I_{c(sat)} = \frac{V_{CEQ}}{R_L} = \frac{10\text{ V}}{50\ \Omega} = \mathbf{200\text{ mA}}$$

Related Problem Find the maximum peak values for the output voltage and current in Figure 7–17 if V_{CC} is lowered to 15 V and the load resistance is changed to 30 Ω.

Open the Multisim file E07-04 in the Examples folder on the companion website. Measure the maximum peak-to-peak output voltage.

Class B/AB Power

Maximum Output Power You have seen that the ideal maximum peak output current for both dual-supply and single-supply push-pull amplifiers is approximately $I_{c(sat)}$, and the maximum peak output voltage is approximately V_{CEQ}. Ideally, the maximum *average* output power is, therefore,

$$P_{out} = I_{out(rms)}V_{out(rms)}$$

Since

$$I_{out(rms)} = 0.707I_{out(peak)} = 0.707I_{c(sat)}$$

and

$$V_{out(rms)} = 0.707V_{out(peak)} = 0.707V_{\text{CEQ}}$$

then

$$P_{out} = 0.5I_{c(sat)}V_{\text{CEQ}}$$

Substituting $V_{\text{CC}}/2$ for V_{CEQ}, the maximum average output power is

Equation 7–6

$$\boldsymbol{P_{out} = 0.25I_{c(sat)}V_{\text{CC}}}$$

DC Input Power The dc input power comes from the V_{CC} supply and is

$$P_{\text{DC}} = I_{\text{CC}}V_{\text{CC}}$$

Since each transistor draws current for a half-cycle, the current is a half-wave signal with an average value of

$$I_{\text{CC}} = \frac{I_{c(sat)}}{\pi}$$

So,

$$P_{\text{DC}} = \frac{I_{c(sat)}V_{\text{CC}}}{\pi}$$

Efficiency An advantage of push-pull class B and class AB amplifiers over class A is a much higher efficiency. This advantage usually overrides the difficulty of biasing the class AB push-pull amplifier to eliminate crossover distortion. Recall that efficiency, η is defined as the ratio of ac output power to dc input power.

$$\eta = \frac{P_{out}}{P_{\text{DC}}}$$

The maximum efficiency, $\eta_{\max}$, for a class B amplifier (class AB is slightly less) is developed as follows, starting with Equation 7–6.

$$P_{out} = 0.25I_{c(sat)}V_{\text{CC}}$$

$$\eta_{\max} = \frac{P_{out}}{P_{\text{DC}}} = \frac{0.25I_{c(sat)}V_{\text{CC}}}{I_{c(sat)}V_{\text{CC}}/\pi} = 0.25\pi$$

Equation 7–7

$$\boldsymbol{\eta_{\max} = 0.79}$$

or, as a percentage,

$$\eta_{\max} = 79\%$$

Recall that the maximum efficiency for class A is 0.25 (25 percent).

EXAMPLE 7–5 Find the maximum ac output power and the dc input power of the amplifier in Figure 7–18.

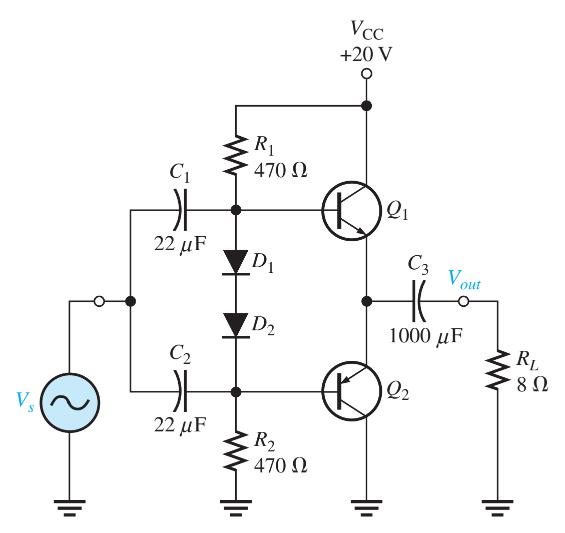
Solution The ideal maximum peak output voltage is

$$V_{out(peak)} \cong V_{\text{CEQ}} = \frac{V_{\text{CC}}}{2} = \frac{20\text{ V}}{2} = 10\text{ V}$$

The maximum peak output current is

$$I_{out(peak)} \cong I_{c(sat)} = \frac{V_{\text{CEQ}}}{R_L} = \frac{10\text{ V}}{8\ \Omega} = 1.25\text{ A}$$

▶ FIGURE 7–18



The ac output power and the dc input power are

$$P_{out} = 0.25I_{c(sat)}V_{CC} = 0.25(1.25\text{ A})(20\text{ V}) = \mathbf{6.25\ W}$$

$$P_{DC} = \frac{I_{c(sat)}V_{CC}}{\pi} = \frac{(1.25\text{ A})(20\text{ V})}{\pi} = \mathbf{7.96\ W}$$

Related Problem Determine the maximum ac output power and the dc input power in Figure 7–18 for $V_{CC} = 15\text{ V}$ and $R_L = 16\ \Omega$.

Input Resistance

The complementary push-pull configuration used in class B/class AB amplifiers is, in effect, two emitter-followers. The input resistance for the emitter-follower, where R_1 and R_2 are the bias resistors, is

$$R_{in} = \beta_{ac}(r'_e + R_E) \parallel R_1 \parallel R_2$$

Since $R_E = R_L$, the formula is

$$\boldsymbol{R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2}$$

Equation 7–8

EXAMPLE 7–6 Assume that a preamplifier stage with an output signal voltage of 3 V rms and an output resistance of 50 Ω is driving the push-pull power amplifier in Figure 7–18 (Example 7–5). Q_1 and Q_2 in the power amplifier have a β_{ac} of 100 and an r'_e of 1.6 Ω. Determine the loading effect that the power amplifier has on the preamp stage.

Solution Looking from the input signal source, the bias resistors appear in parallel because both go to ac ground and the ac resistance of the forward-biased diodes is very small and can be ignored. The input resistance at the emitter of either transistor is $\beta_{ac}(r'_e + R_L)$. So, the signal source sees R_1, R_2, and $\beta_{ac}(r'_e + R_L)$ all in parallel.

The ac input resistance of the power amplifier is

$$R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2 = 100(9.6\ \Omega) \parallel 470\ \Omega \parallel 470\ \Omega = 188\ \Omega$$

Obviously, this will have an effect on the preamp driver stage. The output resistance of the preamp stage and the input resistance of the power amp effectively form a voltage divider that reduces the output signal from the preamp. The actual signal at the power amp is

$$V_{in} = \left(\frac{R_{in}}{R_s + R_{in}}\right)V_s = \left(\frac{188\ \Omega}{238\ \Omega}\right)3\text{ V} = 2.37\text{ V}$$

Related Problem What would be the effect of raising the bias resistors in the circuit?

Darlington Class AB Amplifier

In many applications where the push-pull configuration is used, the load resistance is relatively small. For example, an 8 Ω speaker is a common load for a class AB push-pull amplifier.

As you saw in the previous example, push-pull amplifiers can present a quite low input resistance to the preceding amplifier that drives it. Depending on the output resistance of the preceding amplifier, the low push-pull input resistance can load it severely and significantly reduce the voltage gain. As an example, if each bias resistor is 1 kΩ and if the complementary transistors in a push-pull amplifier exhibit an ac beta of 50 and the load resistance is 8 Ω, the input resistance (assuming $r'_e = 1\ \Omega$) is

$$R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2 = 50(1\ \Omega + 8\ \Omega) \parallel 1\text{ k}\Omega \parallel 1\text{ k}\Omega = 236\ \Omega$$

If the collector resistance of the driving amplifier is, for example, 1.0 kΩ, the input resistance of the push-pull amplifier reduces the effective collector resistance of the driving amplifier (assuming a common-emitter) to $R_c = R_C \parallel R_{in} = 1.0\text{ k}\Omega \parallel 236\ \Omega = 190\ \Omega$. This drastically reduces the voltage gain of the driving amplifier because its gain is R_c/r'_e.

In certain applications with low-resistance loads, a push-pull amplifier using Darlington transistors can be used to increase the input resistance presented to the driving amplifier and avoid severely reducing the voltage gain. The overall ac beta of a Darlington pair is generally in excess of a thousand. Also, the bias resistors can be greater because less base current is required.

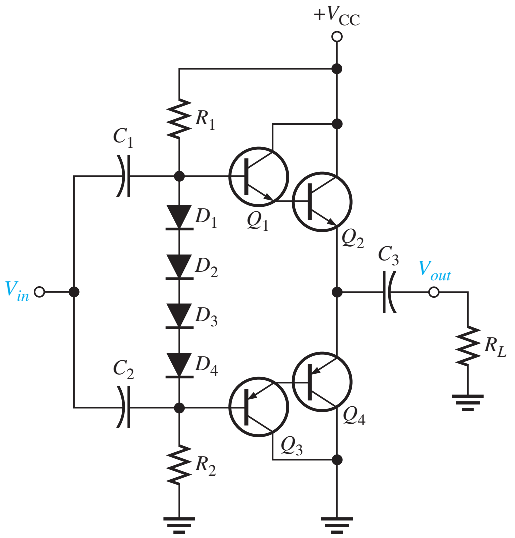
In the previous case, for example, if $\beta_{ac} = 50$ for each transistor in a Darlington pair, the overall ac beta is $\beta_{ac} = (50)(50) = 2500$. If the bias resistors are 10 kΩ, the input resistance is greatly increased, as the following calculation shows.

$$R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2 = 2500(1\ \Omega + 8\ \Omega) \parallel 10\text{ k}\Omega \parallel 10\text{ k}\Omega = 4.09\text{ k}\Omega$$

A Darlington class AB push-pull amplifier is shown in Figure 7–19. Four diodes are required in the bias circuit to match the four base-emitter junctions of the two Darlington pairs.

▶ FIGURE 7–19

A Darlington class AB push-pull amplifier.



Darlington/Complementary Darlington Class AB Amplifier

The complementary Darlington, also known as the Sziklai pair, was introduced in Chapter 6. Recall that it is similar to the traditional Darlington pair except it uses complementary transistors (one *npn* and one *pnp*). The complementary Darlington is used when it is determined that output power transistors of the same type should be used (both *npn* or both *pnp*). Figure 7–20 shows a class AB push-pull amplifier with two *npn* output power transistors (Q_2 and Q_4). The upper part of the push-pull configuration is a traditional Darlington, and the lower part is a complementary Darlington.

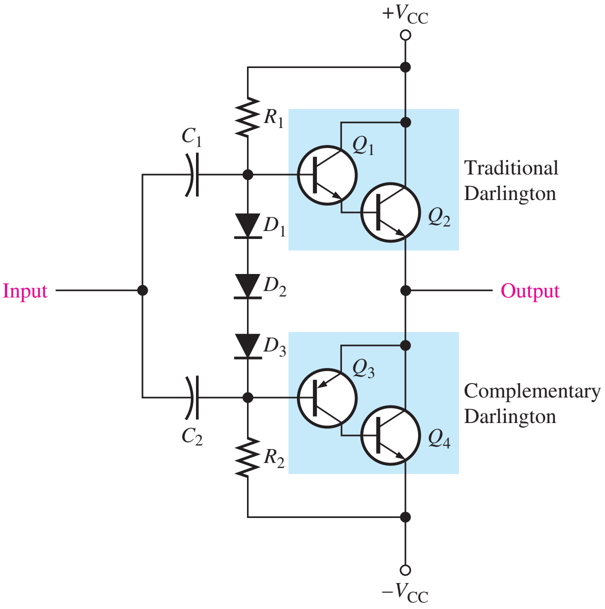


FIGURE 7–20

A Darlington/complementary Darlington class AB push-pull amplifier.

SECTION 7–2 CHECKUP

1. Where is the Q-point for a class B amplifier?
2. What causes crossover distortion?
3. What is the maximum efficiency of a push-pull class B amplifier?
4. Explain the purpose of the push-pull configuration for class B.
5. How does a class AB differ from a class B amplifier?

7–3 THE CLASS C AMPLIFIER

Class C amplifiers are biased so that conduction occurs for much less than 180°. Class C amplifiers are more efficient than either class A or push-pull class B and class AB, which means that more output power can be obtained from class C operation. The output amplitude is a nonlinear function of the input, so class C amplifiers are not used for linear amplification. They are generally used in radio frequency (RF) applications, including circuits, such as oscillators, that have a constant output amplitude, and modulators, where a high-frequency signal is controlled by a low-frequency signal.

After completing this section, you should be able to

- **Explain and analyze the operation of class C amplifiers**
- Describe basic class C operation
  - Discuss the bias of the transistor

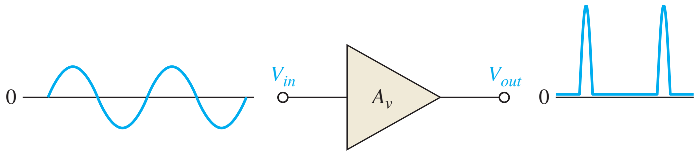
- Discuss class C power dissipation
- Explain tuned operation
- Determine maximum output power
- Explain clamper bias for a class C amplifier

Basic Class C Operation

The basic concept of class C operation is illustrated in Figure 7–21. A common-emitter class C amplifier with a resistive load is shown in Figure 7–22(a). A class C amplifier is normally operated with a resonant circuit load, so the resistive load is used only for the purpose of illustrating the concept. It is biased below cutoff with the negative V_{BB} supply. The ac source voltage has a peak value that is slightly greater than $|V_{BB}| + V_{BE}$ so that the base voltage exceeds the barrier potential of the base-emitter junction for a short time near the positive peak of each cycle, as illustrated in Figure 7–22(b). During this short interval, the transistor is turned on. When the entire ac load line is used, as shown in Figure 7–22(c), the ideal maximum collector current is $I_{c(sat)}$, and the ideal minimum collector voltage is $V_{ce(sat)}$.

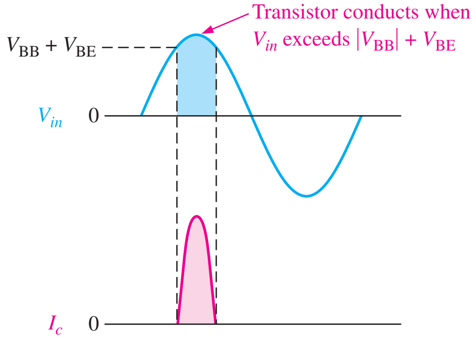
▶ FIGURE 7–21

Basic class C amplifier operation (noninverting).

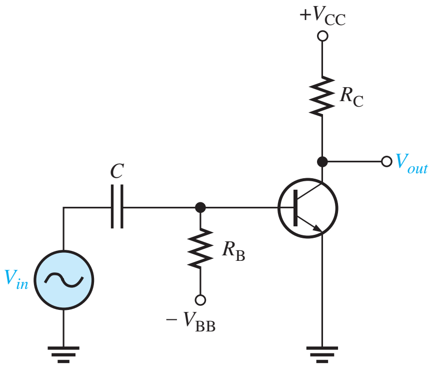


▶ FIGURE 7–22

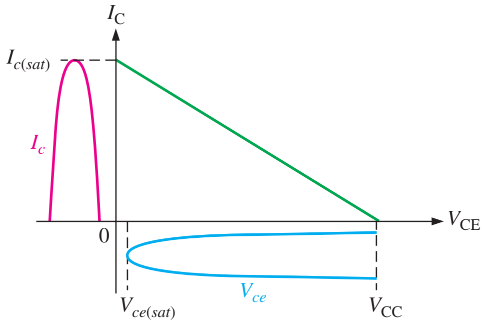
Basic class C operation.


Transistor conducts when V_{in} exceeds $|V_{BB}| + V_{BE}$
$V_{BB} + V_{BE}$
V_{in}
0
I_c
0

(b) Input voltage and output current waveforms



(a) Basic class C amplifier circuit



(c) Load line operation

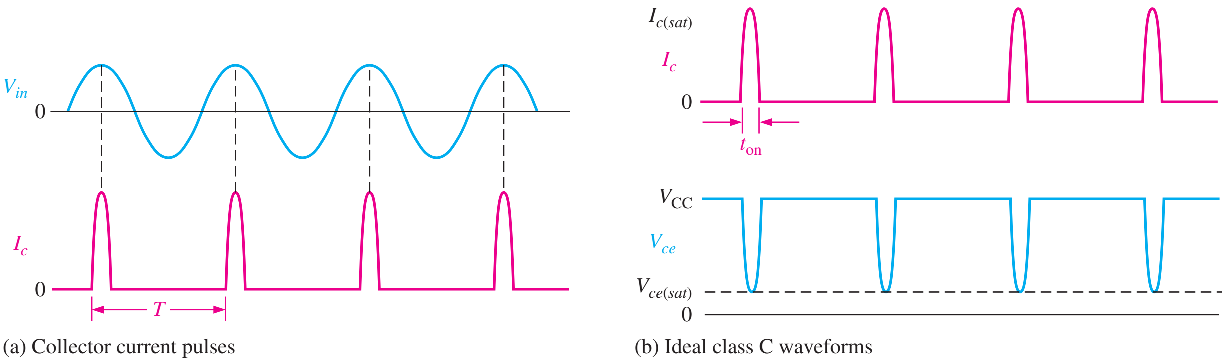
Power Dissipation

The power dissipation of the transistor in a class C amplifier is low because it is on for only a small percentage of the input cycle. Figure 7–23(a) shows the collector current pulses. The time between the pulses is the period (T) of the ac input voltage. The collector current and the collector voltage during the *on* time of the transistor are shown in Figure 7–23(b). To avoid complex mathematics, we will assume ideal pulse approximations. Using this simplification, if the output swings over the entire load, the maximum current amplitude is $I_{c(sat)}$ and the minimum voltage amplitude is $V_{ce(sat)}$ during the time the transistor is on. The power dissipation during the *on* time is, therefore,

$$P_{\mathrm{D(on)}} = I_{c\,(sat)}V_{ce\,(sat)}$$

The transistor is on for a short time, t_{on}, and off for the rest of the input cycle. Therefore, assuming the entire load line is used, the power dissipation averaged over the entire cycle is

$$P_{\mathrm{D(avg)}} = \left(\frac{t_{\mathrm{on}}}{T}\right)P_{\mathrm{D(on)}} = \left(\frac{t_{\mathrm{on}}}{T}\right)I_{c\,(sat)}V_{ce\,(sat)}$$



(a) Collector current pulses

(b) Ideal class C waveforms

▲ **FIGURE 7–23**

Class C waveforms.

EXAMPLE 7–7

A class C amplifier is driven by a 200 kHz signal. The transistor is on for 1 μs, and the amplifier is operating over 100 percent of its load line. If $I_{c(sat)} = 100$ mA and $V_{ce\,(sat)} = 0.2$ V, what is the average power dissipation of the transistor?

Solution The period is

$$T = \frac{1}{200\ \mathrm{kHz}} = 5\ \mu\mathrm{s}$$

Therefore,

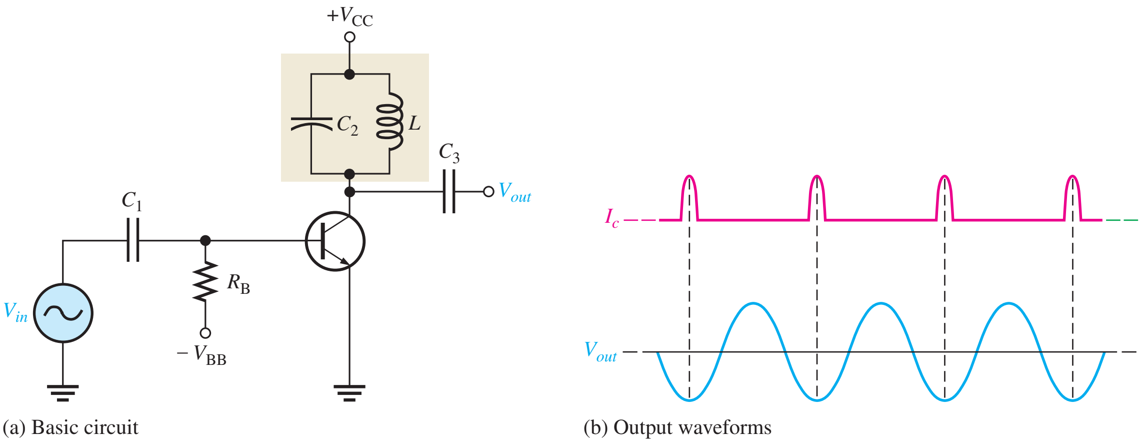
$$P_{\mathrm{D(avg)}} = \left(\frac{t_{\mathrm{on}}}{T}\right)I_{c(sat)}V_{ce(sat)} = (0.2)(100\ \mathrm{mA})(0.2\ \mathrm{V}) = \mathbf{4\ mW}$$

The low power dissipation of the transistor operated in class C is important because, as you will see later, it leads to a very high efficiency when it is operated as a tuned class C amplifier in which relatively high power is achieved in the resonant circuit.

Related Problem If the frequency is reduced from 200 kHz to 150 kHz with the same *on* time, what is the average power dissipation of the transistor?

Tuned Operation

Because the collector voltage (output) is not a replica of the input, the resistively loaded class C amplifier alone is of no value in linear applications. It is therefore necessary to use a class C amplifier with a parallel resonant circuit (tank), as shown in Figure 7–24(a). The resonant frequency of the tank circuit is determined by the formula $f_r = 1/(2\pi\sqrt{LC})$. The short pulse of collector current on each cycle of the input initiates and sustains the oscillation of the tank circuit so that an output sinusoidal voltage is produced, as illustrated in Figure 7–24(b). The tank circuit has high impedance only near the resonant frequency, so the gain is large only at this frequency.



(a) Basic circuit

(b) Output waveforms

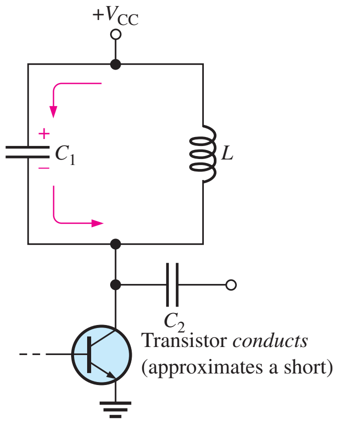
▲ FIGURE 7–24

Tuned class C amplifier.

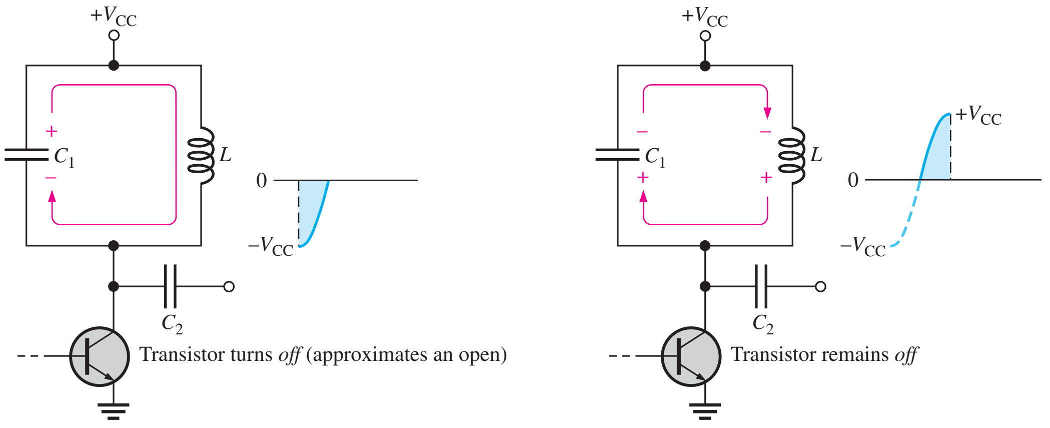
The current pulse charges the capacitor to approximately $+V_{CC}$, as shown in Figure 7–25(a). After the pulse, the capacitor quickly discharges, thus charging the inductor. Then, after the capacitor completely discharges, the inductor's magnetic field collapses and then quickly recharges C to near V_{CC} in a direction opposite to the previous charge. This completes one half-cycle of the oscillation, as shown in parts (b) and (c) of Figure 7–25. Next, the capacitor discharges again, increasing the inductor's magnetic field. The inductor then quickly recharges the capacitor back to a positive peak slightly less than the previous one, due to energy loss in the winding resistance. This completes one full cycle, as shown in parts (d) and (e) of Figure 7–25. The peak-to-peak output voltage is therefore approximately equal to $2V_{CC}$.

The amplitude of each successive cycle of the oscillation will be less than that of the previous cycle because of energy loss in the resistance of the tank circuit, as shown in Figure 7–26(a), and the oscillation will eventually die out. However, the regular recurrences of the collector current pulse re-energizes the resonant circuit and sustains the oscillations at a constant amplitude.

When the tank circuit is tuned to the frequency of the input signal (fundamental), re-energizing occurs on each cycle of the tank voltage, V_r, as shown in Figure 7–26(b). When the tank circuit is tuned to the second harmonic of the input signal, re-energizing occurs on alternate cycles as shown in Figure 7–26(c). In this case, a class C amplifier operates as a frequency multiplier (×2). By tuning the resonant tank circuit to higher harmonics, further frequency multiplication factors are achieved.

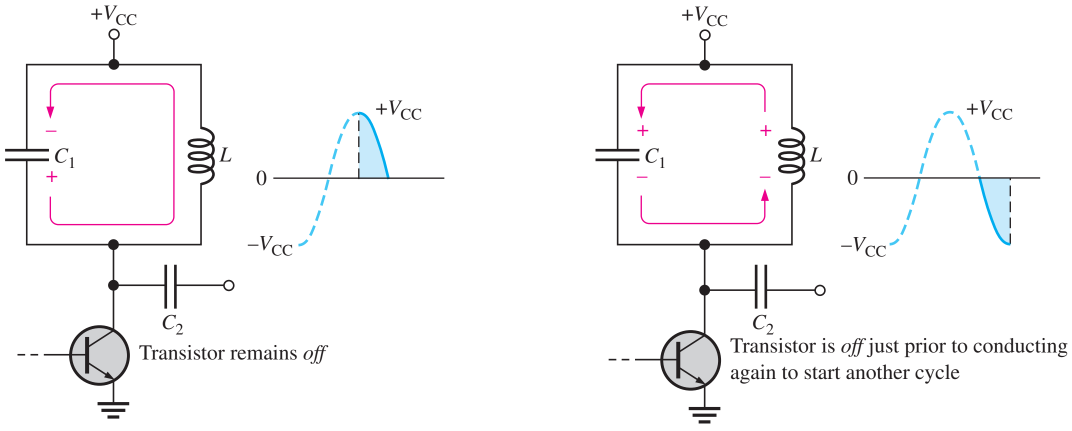

$+V_{CC}$
+
C_1
−
L
C_2
Transistor *conducts*
(approximates a short)

(a) C_1 charges to $+V_{CC}$ at the input peak when transistor is conducting.


$+V_{CC}$
+
C_1
−
L
0
$-V_{CC}$
C_2
Transistor turns *off* (approximates an open)
$+V_{CC}$
−
C_1
+
−
+
L
$+V_{CC}$
0
$-V_{CC}$
C_2
Transistor remains *off*

(b) C_1 discharges to 0 volts.

(c) L recharges C_1 in opposite direction.


$+V_{CC}$
−
C_1
+
L
$+V_{CC}$
0
$-V_{CC}$
C_2
Transistor remains *off*
$+V_{CC}$
+
C_1
−
+
−
L
$+V_{CC}$
0
$-V_{CC}$
C_2
Transistor is *off* just prior to conducting
again to start another cycle

(d) C_1 discharges to 0 volts.

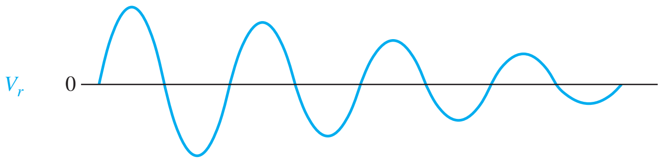
(e) L recharges C_1.

▲ **FIGURE 7–25**

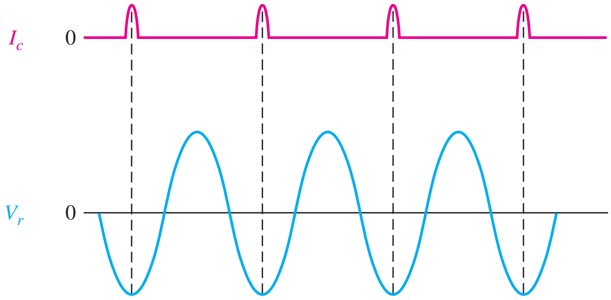
Resonant circuit action.

▶ FIGURE 7–26

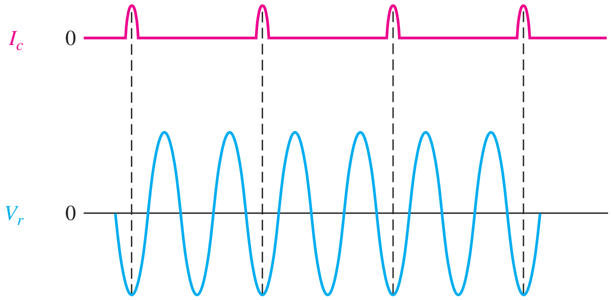
Tank circuit oscillations. V_r is the voltage across the tank circuit.



(a) An oscillation will gradually die out (decay) due to energy loss. The rate of decay depends on the efficiency of the tank circuit.



(b) Oscillation at the fundamental frequency can be sustained by short pulses of collector current.



(c) Oscillation at the second harmonic frequency

Maximum Output Power

Since the voltage developed across the tank circuit has a peak-to-peak value of approximately $2V_{CC}$, the maximum output power can be expressed as

$$P_{out} = \frac{V^2_{rms}}{R_c} = \frac{(0.707V_{CC})^2}{R_c}$$

Equation 7–9

$$\boldsymbol{P_{out} = \frac{0.5V^2_{CC}}{R_c}}$$

R_c is the equivalent parallel resistance of the collector tank circuit at resonance and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier is

$$P_T = P_{out} + P_{D(avg)}$$

Therefore, the efficiency is

Equation 7–10

$$\boldsymbol{\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}}$$

When $P_{out} >> P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).

EXAMPLE 7–8 Suppose the class C amplifier described in Example 7–7 has a V_{CC} equal to 24 V and the R_c is 100 Ω. Determine the efficiency.

Solution From Example 7–7, $P_{D(avg)} = 4$ mW.

$$P_{out} = \frac{0.5V_{CC}^2}{R_c} = \frac{0.5(24\text{ V})^2}{100\ \Omega} = 2.88\text{ W}$$

Therefore,

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}} = \frac{2.88\text{ W}}{2.88\text{ W} + 4\text{ mW}} = \mathbf{0.999}$$

or, as a percentage, 99.9%.

Related Problem What happens to the efficiency of the amplifier if R_c is increased?

Clamper Bias for a Class C Amplifier

Figure 7–27 shows a class C amplifier with a base bias clamping circuit. The base-emitter junction functions as a diode.

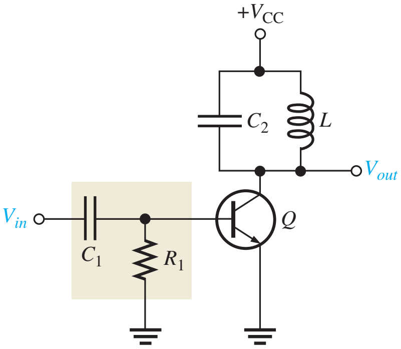
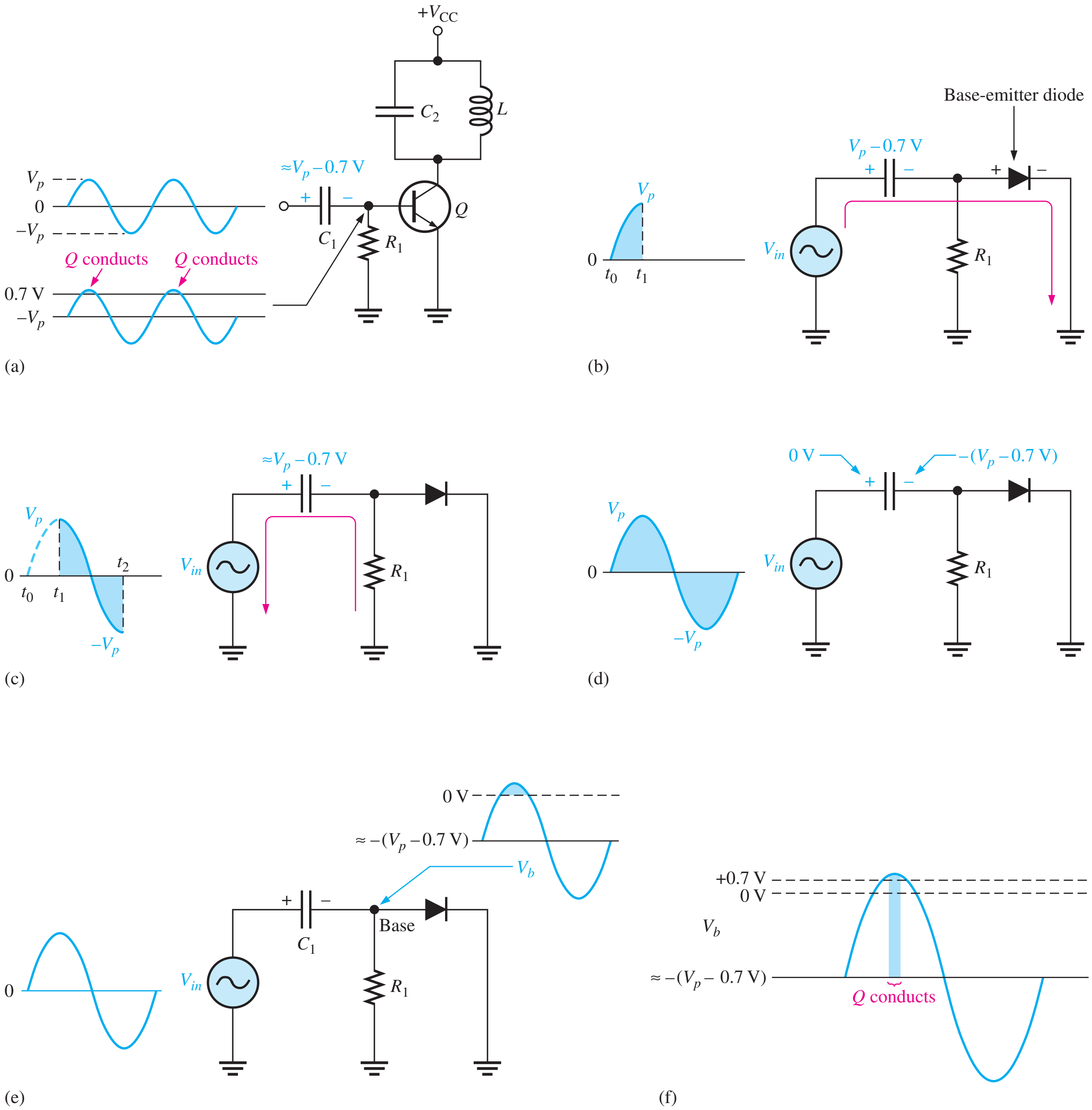


FIGURE 7–27

Tuned class C amplifier with clamper bias.

When the input signal goes positive, capacitor C_1 is charged to the peak value with the polarity shown in Figure 7–28(a). This action produces an average voltage at the base of approximately $-V_p$. This places the transistor in cutoff except at the positive peaks, when the transistor conducts for a short interval. For good clamping action, the R_1C_1 time constant of the clamping circuit must be much greater than the period of the input signal. Parts (b) through (f) of Figure 7–28 illustrate the bias clamping action in more detail. During the time up to the positive peak of the input (t_0 to t_1), the capacitor charges to $V_p - 0.7$ V through the base-emitter diode, as shown in part (b). During the time from t_1 to t_2, as shown in part (c), the capacitor discharges very little because of the large *RC* time constant. The capacitor, therefore, maintains an average charge slightly less than $V_p - 0.7$ V.

Since the dc value of the input signal is zero (positive side of C_1), the dc voltage at the base (negative side of C_1) is slightly more positive than $-(V_p - 0.7\text{ V})$, as indicated in Figure 7–28(d). As shown in Figure 7–28(e), the capacitor couples the ac input signal through to the base so that the voltage at the transistor's base is the ac signal riding on a dc level slightly more positive than $-(V_p - 0.7\text{ V})$. Near the positive peaks of the input voltage, the base voltage goes slightly above 0.7 V and causes the transistor to conduct for a short time, as shown in Figure 7–28(f).



+V_{CC}
C_2
L
V_p
0
$-V_p$
$\approx V_p - 0.7$ V
+
−
C_1
Q
R_1
Q conducts
Q conducts
0.7 V
$-V_p$
(a)
Base-emitter diode
$V_p - 0.7$ V
+
−
V_p
0
t_0
t_1
V_{in}
R_1
(b)
$\approx V_p - 0.7$ V
V_p
0
t_0
t_1
t_2
$-V_p$
V_{in}
R_1
(c)
0 V
$-(V_p - 0.7$ V$)$
V_p
0
$-V_p$
V_{in}
R_1
(d)
0 V
$\approx -(V_p - 0.7$ V$)$
V_b
Base
C_1
0
V_{in}
R_1
(e)
+0.7 V
0 V
V_b
$\approx -(V_p - 0.7$ V$)$
Q conducts
(f)

▲ **FIGURE 7–28**

Clamper bias action.

EXAMPLE 7–9

Determine the voltage at the base of the transistor, the resonant frequency, and the peak-to-peak value of the output signal voltage for the class C amplifier in Figure 7–29.

Solution

$$V_{s(p)} = (1.414)(1\text{ V}) \cong 1.4\text{ V}$$

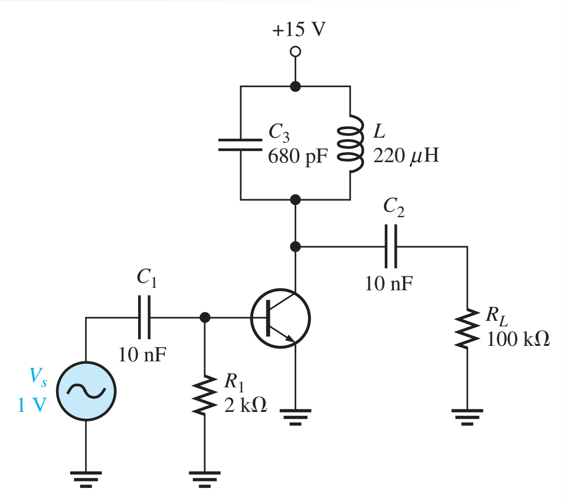
The base is clamped at

$$-(V_{s(p)} - 0.7) = \mathbf{-0.7\ V\ dc}$$

The signal at the base has a positive peak of +0.7 V and a negative peak of

$$-V_{s(p)} + (-0.7\text{ V}) = -1.4\text{ V} - 0.7\text{ V} = \mathbf{-2.1\ V}$$

▶ FIGURE 7–29



The resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(220\ \mu\text{H})(680\ \text{pF})}} = \mathbf{411\ kHz}$$

The output signal has a peak-to-peak value of

$$V_{pp} = 2V_{CC} = 2(15\ \text{V}) = \mathbf{30\ V}$$

Related Problem How could you make the circuit in Figure 7–29 a frequency doubler?

SECTION 7–3 CHECKUP

1. At what point is a class C amplifier normally biased?
2. What is the purpose of the tuned circuit in a class C amplifier?
3. A certain class C amplifier has a power dissipation of 100 mW and an output power of 1 W. What is its percent efficiency?

7–4 TROUBLESHOOTING

In this section, examples of isolating a component failure in a circuit are presented. We will use a class A amplifier and a class AB amplifier with the output voltage monitored by an oscilloscope. Several incorrect output waveforms will be examined and the most likely faults will be discussed.

After completing this section, you should be able to

- **Troubleshoot power amplifiers**
- Troubleshoot a class A amplifier for various faults
- Troubleshoot a class AB amplifier for various faults

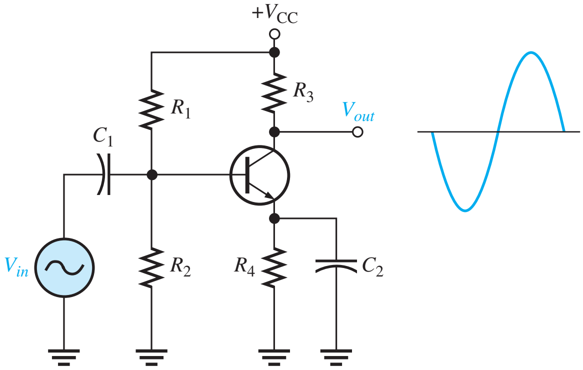
Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

Case 1: Class A

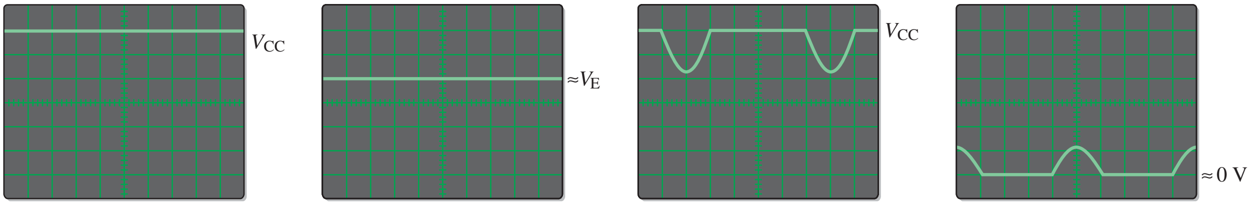
As shown in Figure 7–30, the class A power amplifier should have a normal sinusoidal output when a sinusoidal input signal is applied.

▶ FIGURE 7–30

Class A power amplifier with correct output voltage swing.



Now let's consider four incorrect output waveforms and the most likely causes in each case. In Figure 7–31(a), the scope displays a dc level equal to the dc supply voltage, indicating that the transistor is in cutoff. The two most likely causes of this condition are (1) the transistor has an open *pn* junction, or (2) R_4 is open, preventing collector and emitter current.



(a) Transistor in cutoff (b) CE short or R_2 open (c) Q-point shift or R_1 open (d) Transistor in saturation

▲ FIGURE 7–31

Oscilloscope displays showing output voltage for the amplifier in Figure 7–30 for several types of failures.

In Figure 7–31(b), the scope displays a dc level at the collector approximately equal to the dc emitter voltage. The two probable causes of this indication are (1) the transistor is shorted from collector to emitter, or (2) R_2 is open, causing the transistor to be biased in saturation. In the second case, a sufficiently large input signal can bring the transistor out of saturation on its negative peaks, resulting in short pulses on the output.

In Figure 7–31(c), the scope displays an output waveform that indicates the transistor is in cutoff except during a small portion of the input cycle. Possible causes of this indication are (1) the Q-point has shifted down due to a drastic out-of-tolerance change in a resistor value, or (2) R_1 is open, biasing the transistor in cutoff. The display shows that the input signal is sufficient to bring it out of cutoff for a small portion of the cycle.

In Figure 7–31(d), the scope displays an output waveform that indicates the transistor is saturated except during a small portion of the input cycle. Again, it is possible that an incorrect resistance value has caused a drastic shift in the Q-point up toward saturation, or R_2 is open, causing the transistor to be biased in saturation, and the input signal is bringing it out of saturation for a small portion of the cycle.

Case 2: Class AB

As shown in Figure 7–32, the class AB push-pull amplifier should have a sinusoidal output when a sinusoidal input signal is applied.

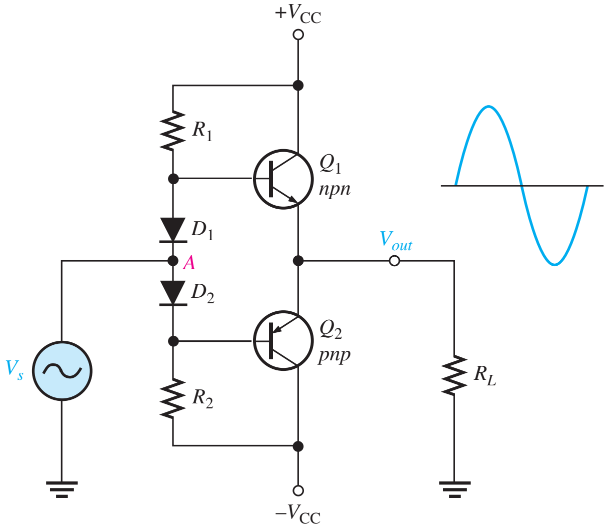
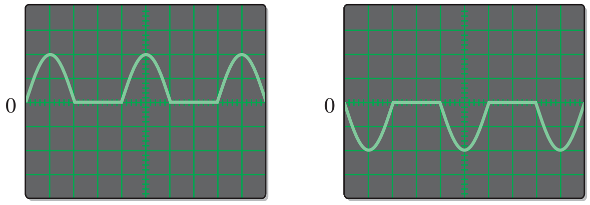


FIGURE 7–32

A class AB push-pull amplifier with correct output voltage.

Two incorrect output waveforms are shown in Figure 7–33. The waveform in part (a) shows that only the positive half of the input signal is present on the output. One possible cause is that diode D_1 is open. If this is the fault, the positive half of the input signal forward-biases D_2 and causes transistor Q_2 to conduct. Another possible cause is that the base-emitter junction of Q_2 is open so only the positive half of the input signal appears on the output because Q_1 is still working.



(a) D_1 open or Q_2 base-emitter open

(b) D_2 open or Q_1 base-emitter open

FIGURE 7–33

Incorrect output waveforms for the amplifier in Figure 7–32.

The waveform in Figure 7–33(b) shows that only the negative half of the input signal is present on the output. One possible cause is that diode D_2 is open. If this is the fault, the negative half of the input signal forward-biases D_1 and places the half-wave signal on the base of Q_1. Another possible cause is that the base-emitter junction of Q_1 is open so only the negative half of the input signal appears on the output because Q_2 is still working.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

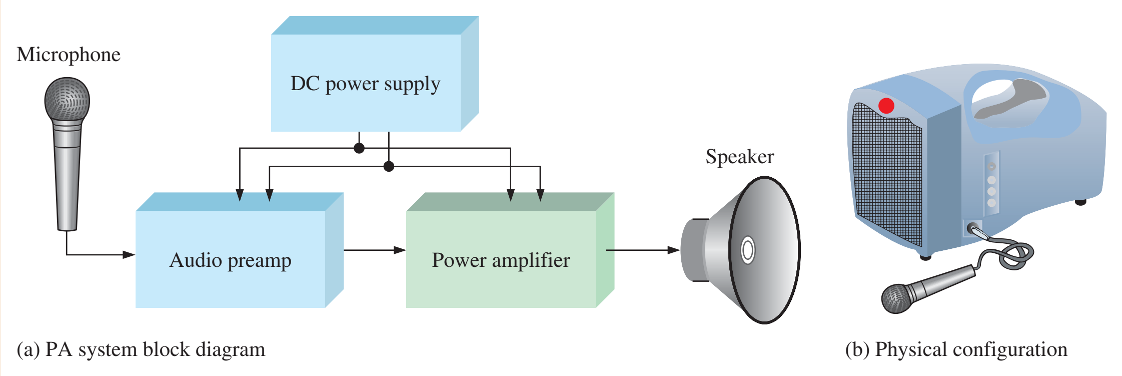
1. Multisim file TSE07-01
2. Multisim file TSE07-02
3. Multisim file TSE07-03
4. Multisim file TSE07-04

SECTION 7–4 CHECKUP

1. What would you check for if you noticed clipping at both peaks of the output waveform?
2. A significant loss of gain in the amplifier of Figure 7–30 would most likely be caused by what type of failure?

Application Activity: *The Complete PA System*

The class AB power amplifier follows the audio preamp and drives the speaker as shown in the PA system block diagram in Figure 7–34. In this application, the power amplifier is developed and interfaced with the preamp that was developed in Chapter 6. The maximum signal power to the speaker should be approximately 6 W for a frequency range of 70 Hz to 5 kHz. The dynamic range for the input voltage is up to 40 mV. Finally, the complete PA system is put together.


Microphone
DC power supply
Audio preamp
Power amplifier
Speaker

(a) PA system block diagram

(b) Physical configuration

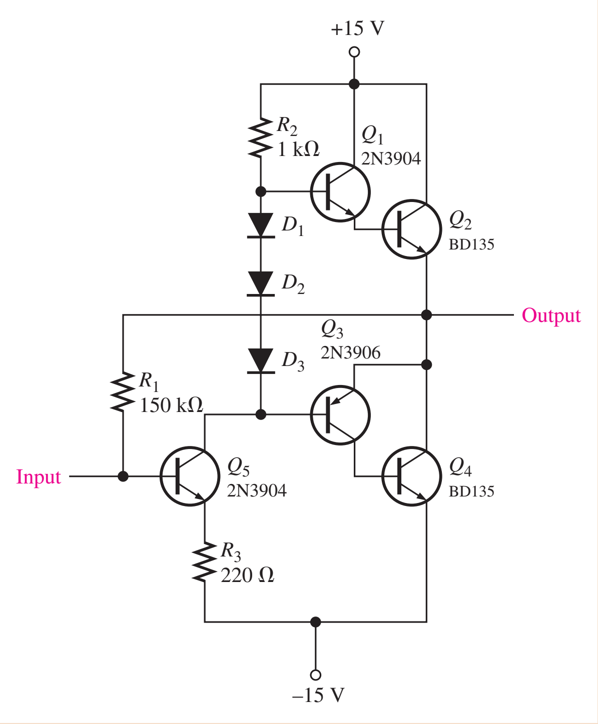
▲ FIGURE 7–34

The Power Amplifier Circuit

The schematic of the push-pull power amplifier is shown in Figure 7–35. The circuit is a class AB amplifier implemented with Darlington configurations and diode current mirror bias. Both a traditional Darlington pair and a complementary Darlington (Sziklai) pair are used to provide sufficient current to an 8 Ω speaker load. The signal from the preamp is

▶ FIGURE 7–35

Class AB power push-pull amplifier.


+15 V
R_2
1 kΩ
Q_1
2N3904
Q_2
BD135
D_1
D_2
Output
Q_3
2N3906
D_3
R_1
150 kΩ
Input
Q_5
2N3904
Q_4
BD135
R_3
220 Ω
–15 V

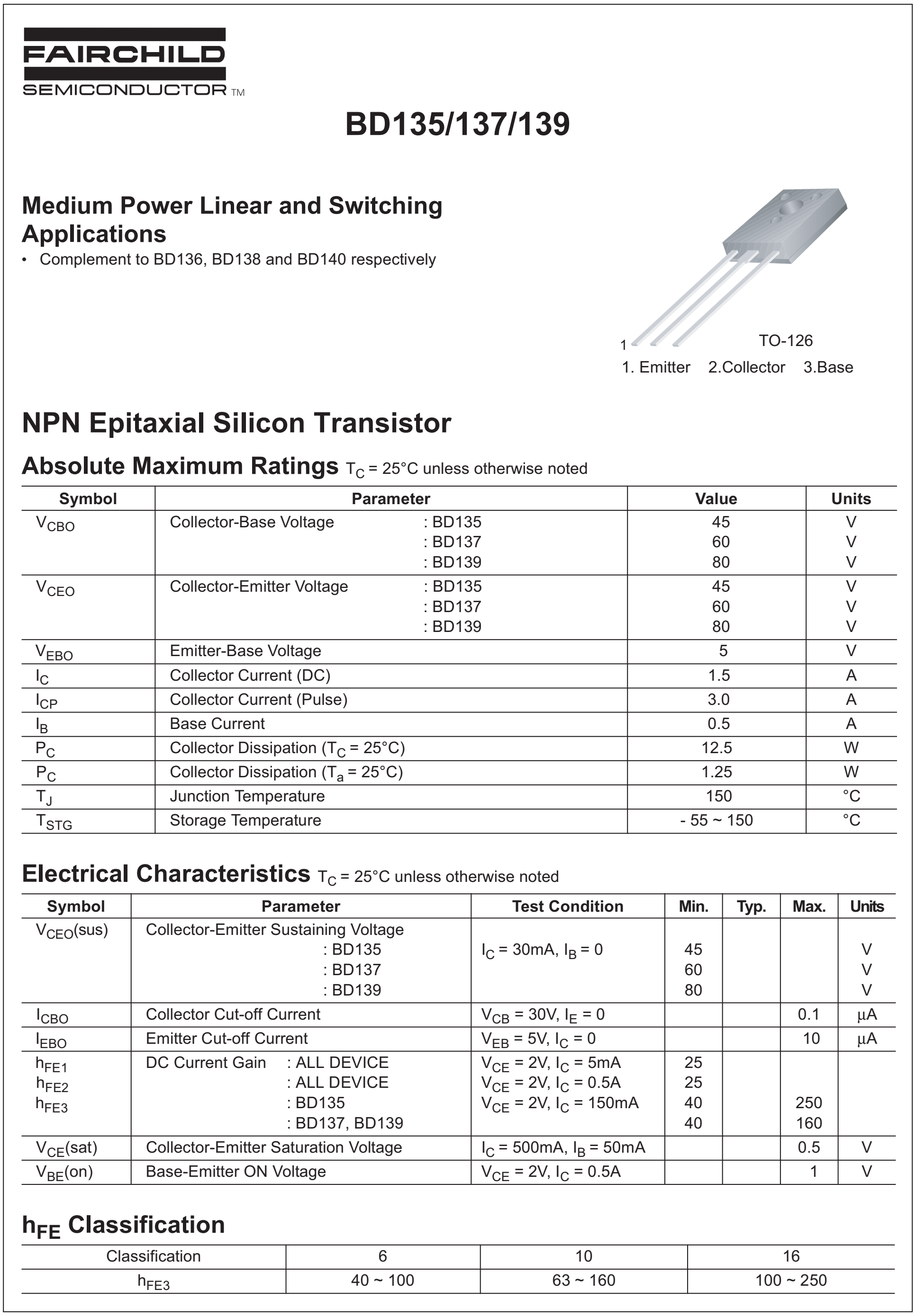
capacitively coupled to the driver stage, Q_5, which is used to prevent excessive loading on the preamp and provide additional gain. Notice that Q_5 is biased with the dc output voltage (0 V) fed back through R_1. Also, the signal voltage fed back to the base of Q_5 is out-of-phase with the signal from the preamp and has the effect of stabilizing the gain. This is called *negative feedback.* The amplifier will deliver up to 5 W to an 8 Ω speaker.

A partial datasheet for the BD135 power transistor is shown in Figure 7–36.

1. Estimate the input resistance of the power amplifier in Figure 7–35.
2. Calculate the approximate voltage gain of the power amplifier in Figure 7–35?

FIGURE 7–36

Partial datasheet for the BD135 power transistors. Copyright Fairchild semiconductor corporation. Used by permission.



FAIRCHILD SEMICONDUCTOR TM

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively

1
TO-126
1. Emitter 2.Collector 3.Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD135 : BD137 : BD139	45 60 80	V V V
V_{CEO}	Collector-Emitter Voltage	: BD135 : BD137 : BD139	45 60 80	V V V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C = 25°C)		12.5	W
P_C	Collector Dissipation (T_a = 25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage : BD135 : BD137 : BD139	I_C = 30mA, I_B = 0	45 60 80			V V V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	μA
h_{FE1}	DC Current Gain : ALL DEVICE	V_{CE} = 2V, I_C = 5mA	25			
h_{FE2}	: ALL DEVICE	V_{CE} = 2V, I_C = 0.5A	25			
h_{FE3}	: BD135	V_{CE} = 2V, I_C = 150mA	40		250	
	: BD137, BD139		40		160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

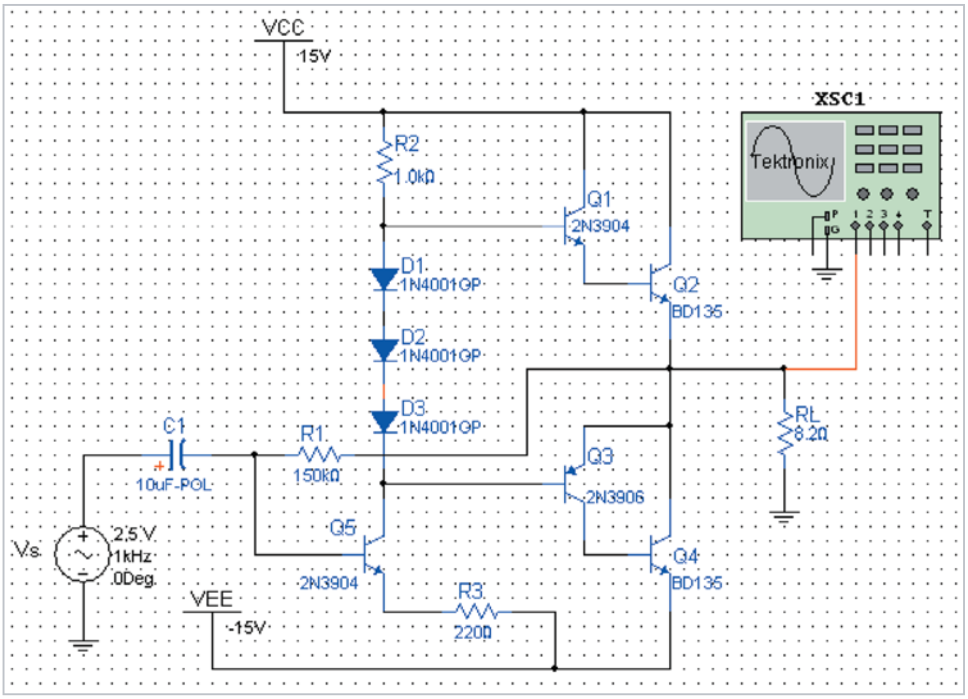
h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

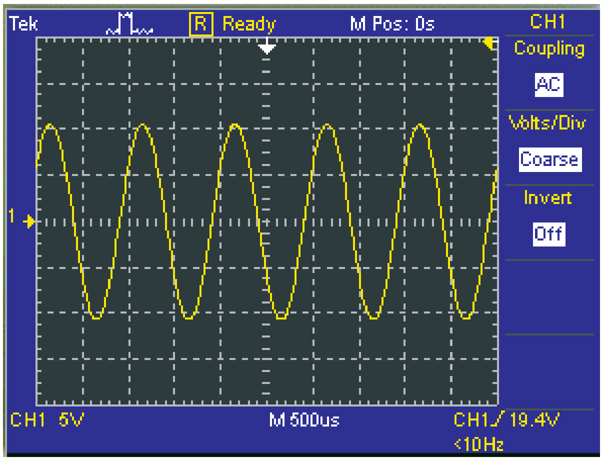
Simulation

The power amplifier is simulated using Multisim with a 1 kHz input signal at near its maximum linear operation. The results are shown in Figure 7–37 where an 8.2 Ω resistor is used to closely approximate the 8 Ω speaker.

3. Calculate the power to the load in Figure 7–37.
4. What is the measured voltage gain? The input is a peak value.
5. Compare the measured gain to the calculated gain for the amplifier in Figure 7–35.


VCC
15V
XSC1
Tektronix
R2
1.0kΩ
Q1
2N3904
D1
1N4001GP
Q2
BD135
D2
1N4001GP
D3
1N4001GP
RL
8.2Ω
C1
10uF-POL
R1
150kΩ
Q3
2N3906
Vs
2.5 V
1kHz
0Deg
Q5
2N3904
Q4
BD135
VEE
-15V
R3
220Ω

(a) Circuit screen


Tek
R
Ready
M Pos: 0s
1

CH1
Coupling
AC
Volts/Div
Coarse
Invert
Off
CH1 5V
M 500us
CH1 ⁄ 19.4V
<10Hz

(b) Output signal

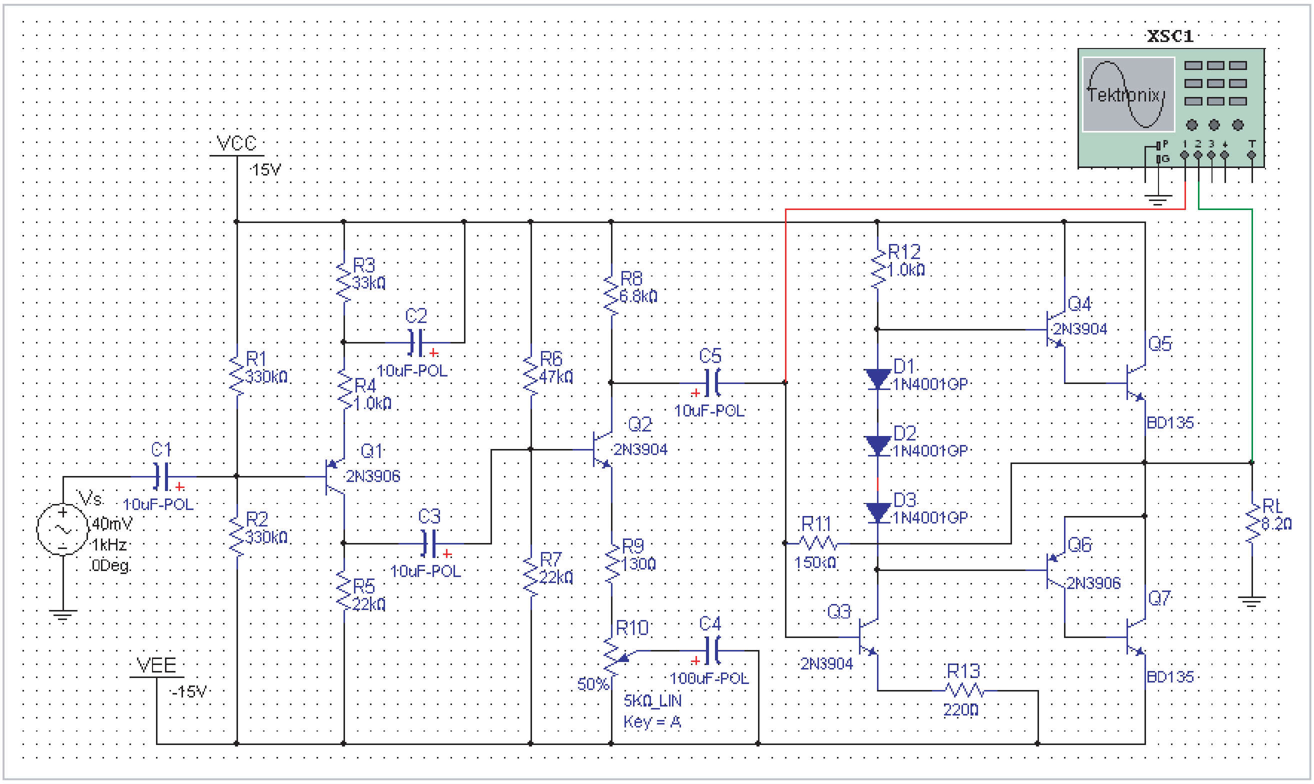
FIGURE 7–37

Simulation of the power amplifier.

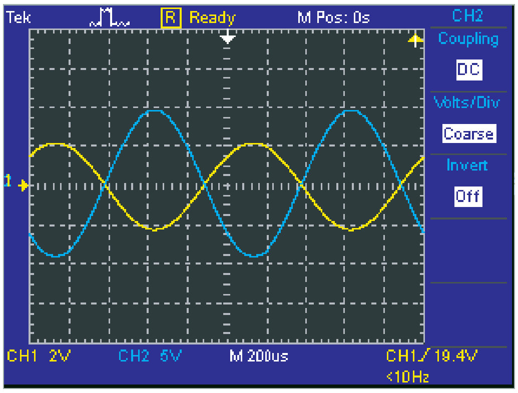
The Complete Audio Amplifier

Both the preamp and the power amp have been simulated individually. Now, they must work together to produce the required signal power to the speaker. Figure 7–38 is the simulation of the combined audio preamp and power amp. Components in the power amplifier are now numbered sequentially with the preamp components.

6. Calculate the power to the load in Figure 7–38.
7. What is the measured voltage gain of the power amplifier?
8. What is the measured overall voltage gain?


XSC1
Tektronix
P G 1 2 3 4 T
VCC
15V
R3 33kΩ
C2 10uF-POL
R1 330kΩ
R4 1.0kΩ
C1 10uF-POL
Vs 40mV 1kHz 0Deg
Q1 2N3906
R2 330kΩ
C3 10uF-POL
R5 22kΩ
VEE
-15V
R6 47kΩ
R7 22kΩ
R8 6.8kΩ
Q2 2N3904
C5 10uF-POL
R9 130Ω
R10
50%
5KΩ_LIN
Key = A
C4 100uF-POL
R12 1.0kΩ
D1 1N4001GP
D2 1N4001GP
D3 1N4001GP
R11 150kΩ
Q3 2N3904
R13 220Ω
Q4 2N3904
Q5 BD135
Q6 2N3906
Q7 BD135
RL 8.2Ω

(a) Circuit screen


Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
1
CH1 2V
CH2 5V
M 200us
CH1 ∫ 19.4V
<10Hz

(b) Preamp output and final output

▲ **FIGURE 7–38**

Simulation of the complete audio amplifier.

Simulate the audio amplifier using your Multisim software. Observe the operation with the virtual oscilloscope.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

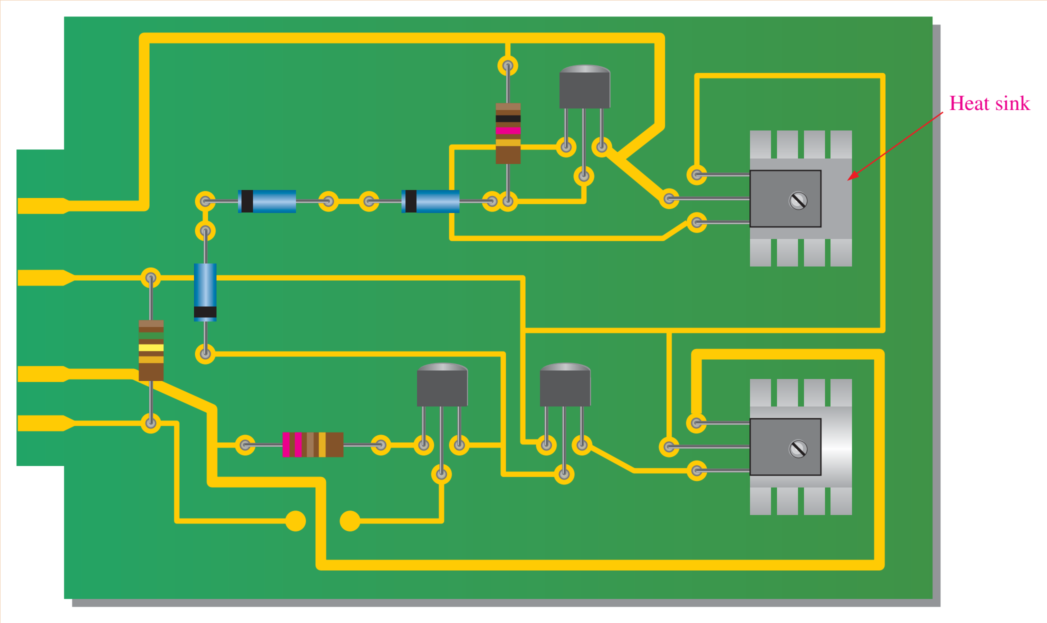
Lab Experiment

To build and test a similar circuit, go to Experiment 7 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The power amplifier is implemented on a printed circuit board as shown in Figure 7–39. Heat sinks are used to provide additional heat dissipation from the power transistors.

9. Check the printed circuit board and verify that it agrees with the schematic in Figure 7–35. The volume control potentiometer is mounted off the PC board for easy access.
10. Label each input and output pin according to function. Locate the single backside trace.



▲ FIGURE 7–39

Power amplifier circuit board.

Troubleshooting the Power Amplifier Board

A power amplifier circuit board has failed the production test. Test results are shown in Figure 7–40.

11. Based on the scope displays, list possible faults for the circuit board.

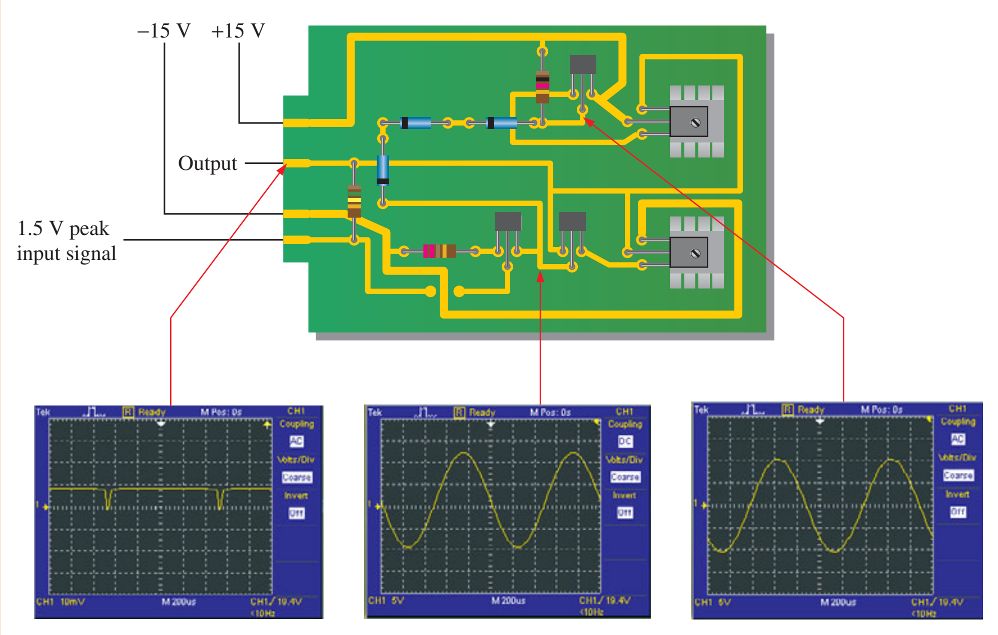
Putting the System Together

The preamp circuit board and the power amplifier circuit board are interconnected and the dc power supply (battery pack), microphone, speaker, and volume control potentiometer are attached, as shown in Figure 7–41.

12. Verify that the system interconnections are correct.

FIGURE 7–40

Test of faulty power amplifier board.


−15 V
+15 V
Output
1.5 V peak
input signal
Tek
Ready
M Pos: 0s
CH1
Coupling
AC
Volts/Div
Coarse
Invert
Off
CH1 10mV
M 200us
CH1 ∕ 19.4V
<10Hz
Tek
Ready
M Pos: 0s
CH1
Coupling
DC
Volts/Div
Coarse
Invert
Off
CH1 5V
M 200us
CH1 ∕ 19.4V
<10Hz
Tek
Ready
M Pos: 0s
CH1
Coupling
AC
Volts/Div
Coarse
Invert
Off
CH1 5V
M 200us
CH1 ∕ 19.4V
<10Hz

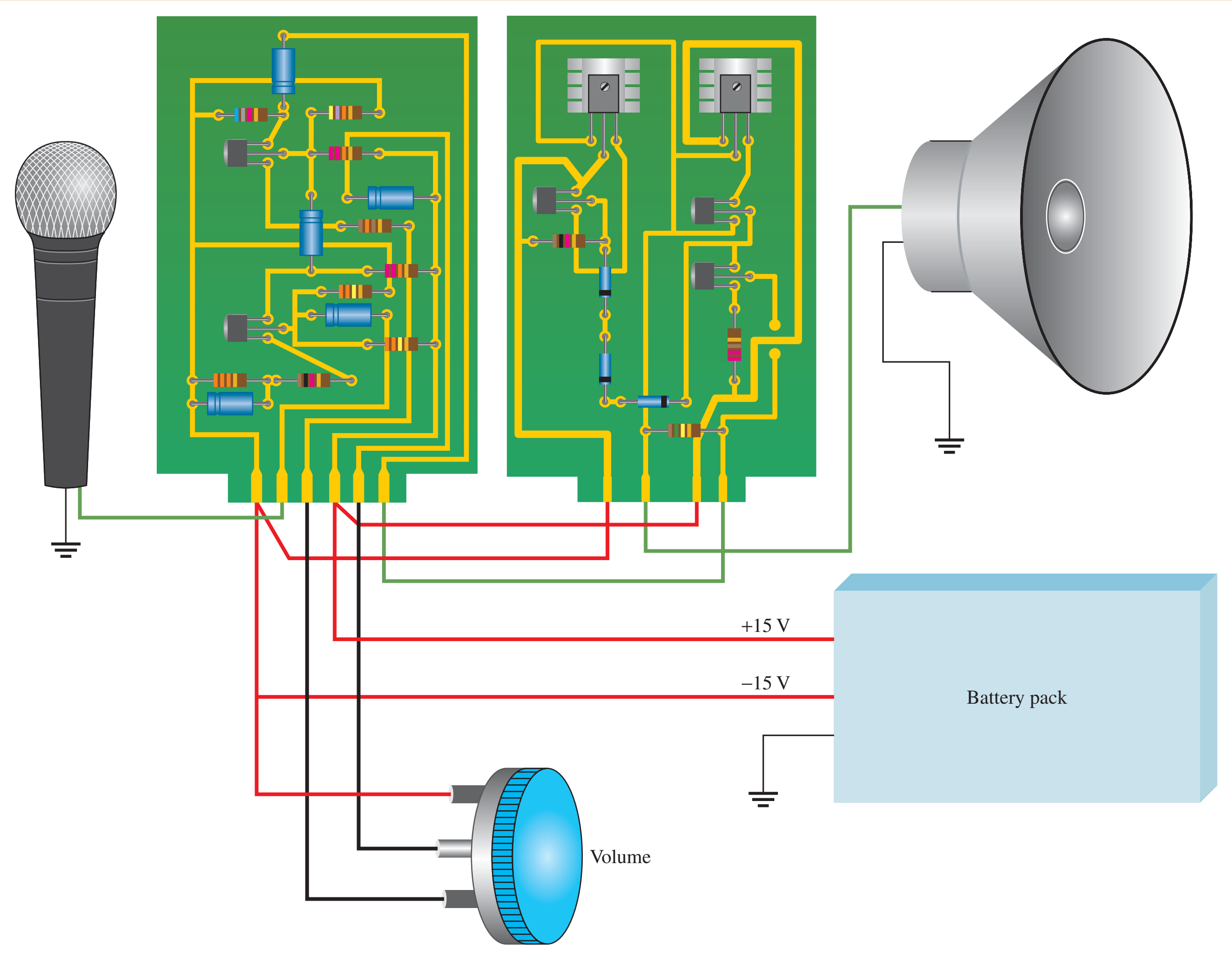

+15 V
−15 V
Battery pack
Volume

FIGURE 7–41

The complete public address system.

SUMMARY

Section 7–1

- A class A power amplifier operates entirely in the linear region of the transistor's characteristic curves. The transistor conducts during the full 360° of the input cycle.
- The Q-point must be centered on the load line for maximum class A output signal swing.
- The maximum efficiency of a class A power amplifier is 25 percent.

Section 7–2

- A class B amplifier operates in the linear region for half of the input cycle (180°), and it is in cutoff for the other half.
- The Q-point is at cutoff for class B operation.
- Class B amplifiers are normally operated in a push-pull configuration in order to produce an output that is a replica of the input.
- The maximum efficiency of a class B amplifier is 79 percent.
- A class AB amplifier is biased slightly above cutoff and operates in the linear region for slightly more than 180° of the input cycle.
- Class AB eliminates crossover distortion found in pure class B.

Section 7–3

- A class C amplifier operates in the linear region for only a small part of the input cycle.
- The class C amplifier is biased below cutoff.
- Class C amplifiers are normally operated as tuned amplifiers to produce a sinusoidal output.
- The maximum efficiency of a class C amplifier is higher than that of either class A or class B amplifiers. Under conditions of low power dissipation and high output power, the efficiency can approach 100 percent.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Class A A type of amplifier that operates entirely in its linear (active) region.

Class AB A type of amplifier that is biased into slight conduction.

Class B A type of amplifier that operates in the linear region for 180° of the input cycle because it is biased at cutoff.

Class C A type of amplifier that operates only for a small portion of the input cycle.

Efficiency The ratio of the signal power delivered to a load to the power from the power supply of an amplifier.

Power gain The ratio of output power to input power of an amplifier.

Push-Pull A type of class B amplifier with two transistors in which one transistor conducts for one half-cycle and the other conducts for the other half-cycle.

KEY FORMULAS

The Class A Power Amplifier

7–1	$A_p = \dfrac{P_L}{P_{in}}$	Power gain
7–2	$A_p = A_v^2\left(\dfrac{R_{in}}{R_L}\right)$	Power gain in terms of voltage gain
7–3	$P_{\mathrm{DQ}} = I_{\mathrm{CQ}}V_{\mathrm{CEQ}}$	DC quiescent power
7–4	$P_{out(max)} = 0.5I_{\mathrm{CQ}}V_{\mathrm{CEQ}}$	Maximum output power

The Class B/AB Push-Pull Amplifiers

7–5	$I_{c(sat)} = \dfrac{V_{\mathrm{CC}}}{R_L}$	AC saturation current
7–6	$P_{out} = 0.25I_{c(sat)}V_{\mathrm{CC}}$	Maximum average output power

7–7	$\eta_{\mathrm{max}} = 0.79$	Maximum efficiency
7–8	$R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2$	Input resistance

The Class C Amplifier

7–9	$P_{out} = \dfrac{0.5V_{\mathrm{CC}}^2}{R_c}$	Output power
7–10	$\eta = \dfrac{P_{out}}{P_{out} + P_{\mathrm{D(avg)}}}$	Efficiency

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. Class A power amplifiers are a type of large-signal amplifier.
2. Ideally, the Q-point should be centered on the load line in a class A amplifier.
3. The quiescent power dissipation occurs when the maximum signal is applied.
4. Efficiency is the ratio of output signal power to total power.
5. Each transistor in a class B amplifier conducts for the entire input cycle.
6. Class AB operation overcomes the problem of crossover distortion.
7. Complementary symmetry transistors must be used in a class AB amplifier.
8. A current mirror is implemented with a laser diode.
9. Darlington transistors can be used to increase the input resistance of a class AB amplifier.
10. The transistor in a class C amplifier conducts for a small portion of the input cycle.
11. The output of a class C amplifier is a replica of the input signal.
12. A class C amplifier usually employs a tuned circuit.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the value of R_3 in Figure 7–5 is decreased, the voltage gain of the first stage will
   (a) increase **(b)** decrease **(c)** not change
2. If the value of R_{E2} in Figure 7–5 is increased, the voltage gain of the first stage will
   (a) increase **(b)** decrease **(c)** not change
3. If C_2 in Figure 7–5 opens, the dc voltage at the emitter of Q_1 will
   (a) increase **(b)** decrease **(c)** not change
4. If the value of R_4 in Figure 7–5 is increased, the dc voltage at the base of Q_3 will
   (a) increase **(b)** decrease **(c)** not change
5. If V_{CC} in Figure 7–18 is increased, the peak output voltage will
   (a) increase **(b)** decrease **(c)** not change
6. If the value of R_L in Figure 7–18 is increased, the ac output power will
   (a) increase **(b)** decrease **(c)** not change
7. If the value of R_L in Figure 7–19 is decreased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
8. If the value of V_{CC} in Figure 7–19 is increased, the ac output power will
   (a) increase **(b)** decrease **(c)** not change
9. If the values of R_1 and R_2 in Figure 7–19 are increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
10. If the value of C_2 in Figure 7–24 is decreased, the resonant frequency will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 7–1

1. An amplifier that operates in the linear region at all times is

(a) Class A **(b)** Class AB **(c)** Class B **(d)** Class C

2. A certain class A power amplifier delivers 5 W to a load with an input signal power of 100 mW. The power gain is

(a) 100 **(b)** 50 **(c)** 250 **(d)** 5

3. The peak current a class A power amplifier can deliver to a load depends on the

(a) maximum rating of the power supply **(b)** quiescent current

(c) current in the bias resistors **(d)** size of the heat sink

4. For maximum output, a class A power amplifier must maintain a value of quiescent current that is

(a) one-half the peak load current **(b)** twice the peak load current

(c) at least as large as the peak load current **(d)** just above the cutoff value

5. A certain class A power amplifier has $V_{CEQ} = 12$ V and $I_{CQ} = 1$ A. The maximum signal power output is

(a) 6 W **(b)** 12 W **(c)** 1 W **(d)** 0.707 W

6. The efficiency of a power amplifier is the ratio of the power delivered to the load to the

(a) input signal power **(b)** power dissipated in the last stage

(c) power from the dc power supply **(d)** none of these answers

7. The maximum efficiency of a class A power amplifier is

(a) 25% **(b)** 50% **(c)** 79% **(d)** 98%

Section 7–2

8. The transistors in a class B amplifier are biased

(a) into cutoff **(b)** in saturation

(c) at midpoint of the load line **(d)** right at cutoff

9. Crossover distortion is a problem for

(a) class A amplifiers **(b)** class AB amplifiers

(c) class B amplifiers **(d)** all of these amplifiers

10. A BJT class B push-pull amplifier with no transformer coupling uses

(a) two *npn* transistors **(b)** two *pnp* transistors

(c) complementary symmetry transitors **(d)** none of these

11. A current mirror in a push-pull amplifier should give an I_{CQ} that is

(a) equal to the current in the bias resistors and diodes

(b) twice the current in the bias resistors and diodes

(c) half the current in the bias resistors and diodes

(d) zero

12. The maximum efficiency of a class B push-pull amplifier is

(a) 25% **(b)** 50% **(c)** 79% **(d)** 98%

13. The output of a certain two-supply class B push-pull amplifier has a V_{CC} of 20 V. If the load resistance is 50 Ω, the value of $I_{c(sat)}$ is

(a) 5 mA **(b)** 0.4 A **(c)** 4 mA **(d)** 40 mA

14. The maximum efficiency of a class AB amplifier is

(a) higher than a class B **(b)** the same as a class B

(c) about the same as a class A **(d)** slightly less than a class B

Section 7–3

15. The power dissipation of a class C amplifier is normally

(a) very low **(b)** very high **(c)** the same as a class B **(d)** the same as a class A

16. The efficiency of a class C amplifier is

(a) less than class A **(b)** less than class B

(c) less than class AB **(d)** greater than classes A, B, or AB

17. The transistor in a class C amplifier conducts for

(a) more than 180° of the input cycle
(b) one-half of the input cycle
(c) a very small percentage of the input cycle
(d) all of the input cycle

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 7–1

The Class A Power Amplifier

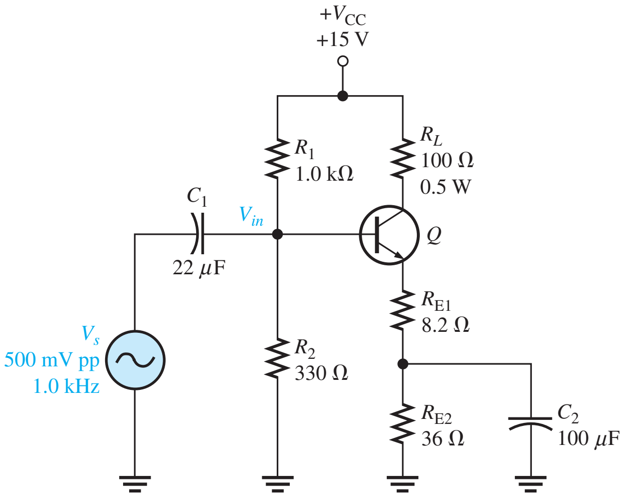
1. Figure 7–42 shows a CE power amplifier in which the collector resistor serves also as the load resistor. Assume $\beta_{DC} = \beta_{ac} = 100$.

(a) Determine the dc Q-point (I_{CQ} and V_{CEQ}).

(b) Determine the voltage gain and the power gain.

FIGURE 7–42

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F07-42).



+V_{CC}
+15 V
R1
1.0 kΩ
RL
100 Ω
0.5 W
C1
Vin
22 µF
Q
RE1
8.2 Ω
Vs
500 mV pp
1.0 kHz
R2
330 Ω
RE2
36 Ω
C2
100 µF

2. For the circuit in Figure 7–42, determine the following:

(a) the power dissipated in the transistor with no load

(b) the total power from the power supply with no load

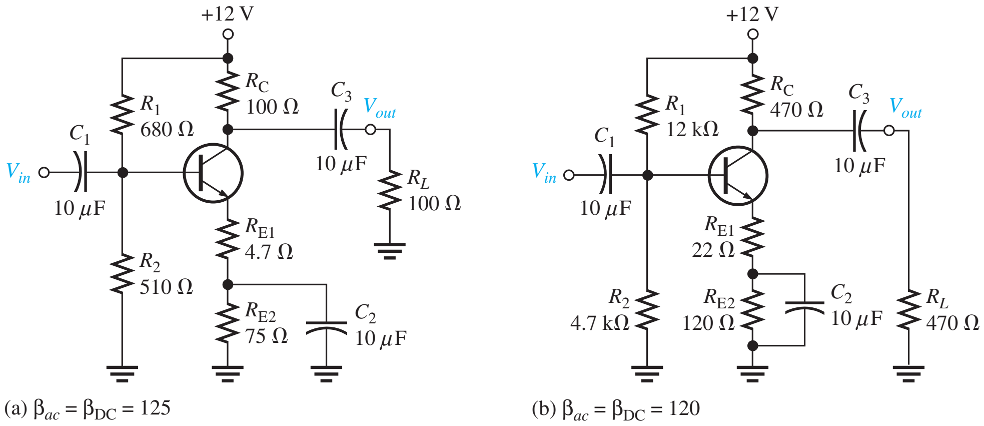
(c) the signal power in the load with a 500 mV input

3. Refer to the circuit in Figure 7–42. What changes would be necessary to convert the circuit to a *pnp* transistor with a positive supply? What advantage would this have?

4. Assume a CC amplifier has an input resistance of 2.2 kΩ and drives an output load of 50 Ω. What is the power gain?

5. Determine the Q-point for each amplifier in Figure 7–43.

FIGURE 7–43



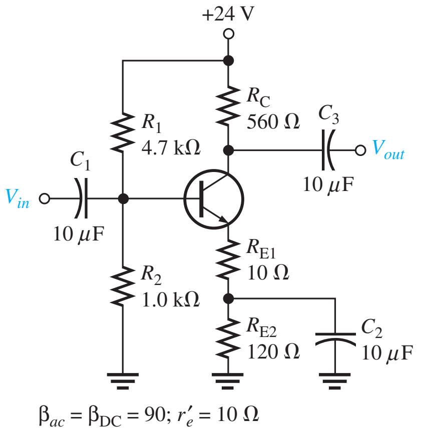
+12 V
RC
100 Ω
R1
680 Ω
C3
Vout
C1
Vin
10 µF
10 µF
RL
100 Ω
RE1
4.7 Ω
R2
510 Ω
RE2
75 Ω
C2
10 µF
+12 V
RC
470 Ω
R1
12 kΩ
C3
Vout
C1
Vin
10 µF
10 µF
RE1
22 Ω
R2
4.7 kΩ
RE2
120 Ω
C2
10 µF
RL
470 Ω

(a) $\beta_{ac} = \beta_{DC} = 125$

(b) $\beta_{ac} = \beta_{DC} = 120$

6. If the load resistor in Figure 7–43(a) is changed to 50 Ω, how much does the Q-point change?
7. What is the maximum peak value of collector current that can be realized in each circuit of Figure 7–43? What is the maximum peak value of output voltage in each circuit?
8. Find the power gain for each circuit in Figure 7–43. Neglect r'_e.
9. Determine the minimum power rating for the transistor in Figure 7–44.
10. Find the maximum output signal power to the load and efficiency for the amplifier in Figure 7–44 with a 500 Ω load resistor.

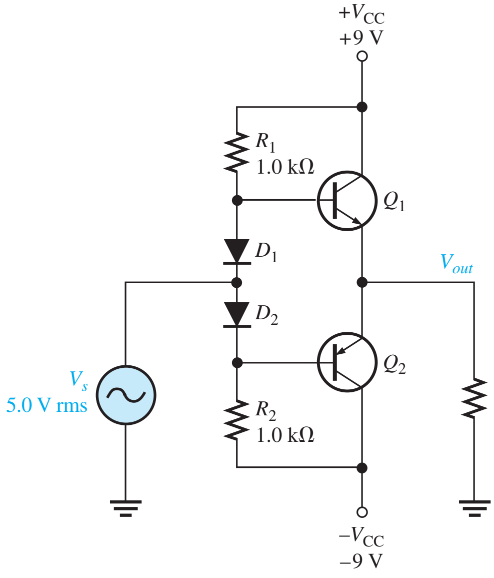
▶ **FIGURE 7–44**


+24 V
R_C
560 Ω
C_3
V_{out}
10 μF
R_1
4.7 kΩ
C_1
V_{in}
10 μF
R_{E1}
10 Ω
R_2
1.0 kΩ
R_{E2}
120 Ω
C_2
10 μF
$\beta_{ac} = \beta_{DC} = 90$; $r'_e = 10\ \Omega$

Section 7–2 The Class B and Class AB Push-Pull Amplifiers

11. Refer to the class AB amplifier in Figure 7–45.
    - **(a)** Determine the dc parameters $V_{B(Q1)}$, $V_{B(Q2)}$, V_E, I_{CQ}, $V_{CEQ(Q1)}$, $V_{CEQ(Q2)}$.
    - **(b)** For the 5 V rms input, determine the power delivered to the load resistor.

▶ **FIGURE 7–45**


$+V_{CC}$
+9 V
R_1
1.0 kΩ
Q_1
D_1
V_{out}
D_2
Q_2
V_s
5.0 V rms
R_2
1.0 kΩ
R_L
50 Ω
$-V_{CC}$
−9 V

12. Draw the load line for the *npn* transistor in Figure 7–45. Label the saturation current, $I_{c(sat)}$, and show the Q-point.

13. Determine the approximate input resistance seen by the signal source for the amplifier of Figure 7–45 if $\beta_{ac} = 100$.

14. If D_2 has more voltage drop than D_1, what effect does this have on the output?

15. Refer to the class AB amplifier in Figure 7–46 operating with a single power supply.

- **(a)** Determine the dc parameters $V_{B(Q1)}$, $V_{B(Q2)}$, V_E, I_{CQ}, $V_{CEQ(Q1)}$, $V_{CEQ(Q2)}$.
- **(b)** Assuming the input voltage is 10 V pp, determine the power delivered to the load resistor.

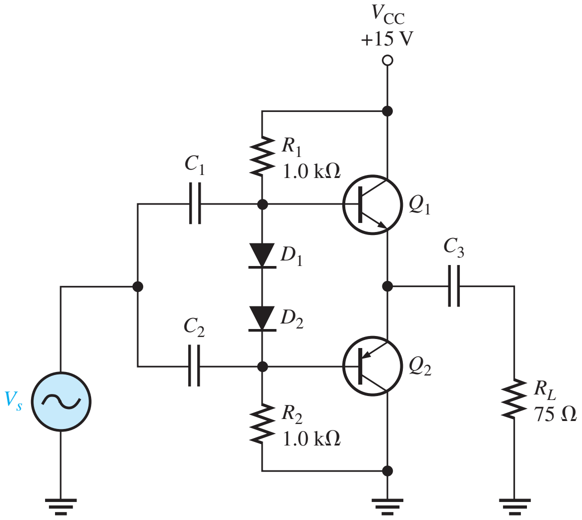
16. Refer to the class AB amplifier in Figure 7–46.

- **(a)** What is the maximum power that could be delivered to the load resistor?
- **(b)** Assume the power supply voltage is raised to 24 V. What is the new maximum power that could be delivered to the load resistor?

17. Refer to the class AB amplifier in Figure 7–46. What fault or faults could account for each of the following troubles?

- **(a)** a positive half-wave output signal
- **(b)** zero volts on both bases and the emitters
- **(c)** no output: emitter voltage = +15 V
- **(d)** crossover distortion observed on the output waveform

18. If a 1 V rms signal source with an internal resistance of 50 Ω is connected to the amplifier in Figure 7–46, what is the actual rms signal applied to the amplifier input? Assume $\beta_{ac} = 200$.



▲ FIGURE 7–46

Section 7–3 The Class C Amplifier

19. A certain class C amplifier transistor is on for 10 percent of the input cycle. If $V_{ce(sat)} = 0.18$ V and $I_{c(sat)} = 25$ mA, what is the average power dissipation for maximum output?

20. What is the resonant frequency of a tank circuit with $L = 10$ mH and $C = 0.001\ \mu$F?

21. What is the maximum peak-to-peak output voltage of a tuned class C amplifier with $V_{CC} = 12$ V?

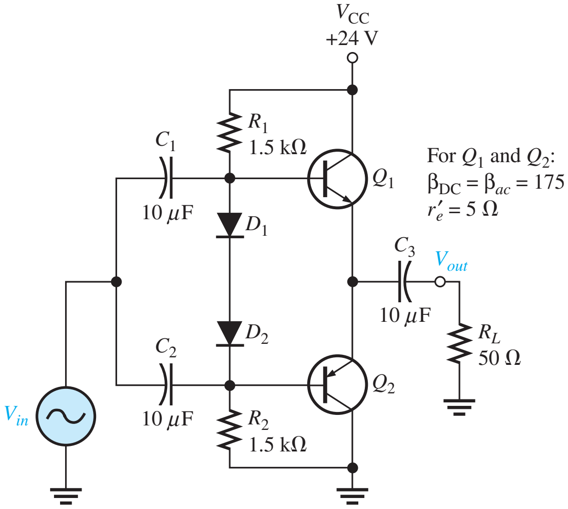
22. Determine the efficiency of the class C amplifier described in Problem 21 if $V_{CC} = 15$ V and the equivalent parallel resistance in the collector tank circuit is 50 Ω. Assume that the transistor is on for 10% of the period.

Section 7–4 Troubleshooting

23. Refer to Figure 7–47. What would you expect to observe across R_L if C_1 opened?

24. Your oscilloscope displays a half-wave output when connected across R_L in Figure 7–47. What is the probable cause?

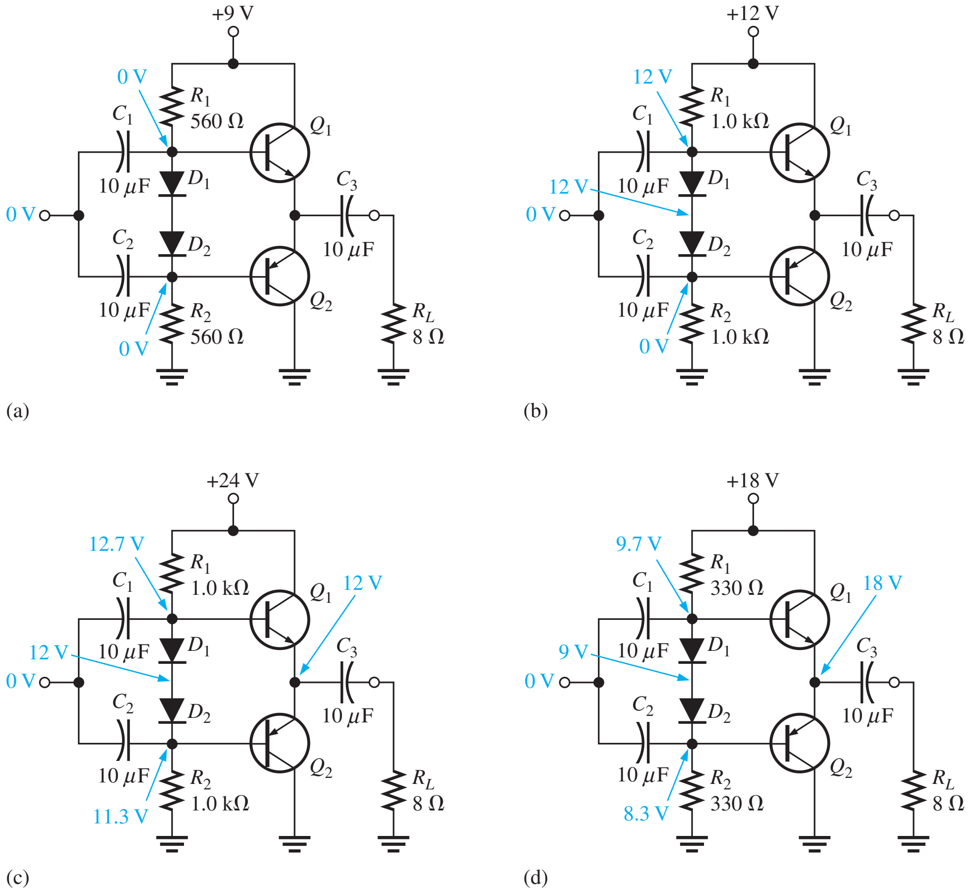
▶ FIGURE 7–47



V_{CC}
+24 V
R_1
1.5 kΩ
C_1
10 μF
Q_1
D_1
For Q_1 and Q_2:
$\beta_{DC} = \beta_{ac} = 175$
$r'_e = 5\ \Omega$
C_3
V_{out}
10 μF
R_L
50 Ω
D_2
C_2
10 μF
Q_2
V_{in}
R_2
1.5 kΩ

25. Determine the possible fault or faults, if any, for each circuit in Figure 7–48 based on the indicated dc voltage measurements.

▶ FIGURE 7–48



+9 V
0 V
R_1
560 Ω
C_1
Q_1
10 μF
D_1
C_3
0 V
10 μF
C_2
D_2
10 μF
Q_2
R_2
560 Ω
0 V
R_L
8 Ω
(a)
+12 V
12 V
R_1
1.0 kΩ
C_1
Q_1
12 V
10 μF
D_1
C_3
0 V
10 μF
C_2
D_2
10 μF
Q_2
R_2
1.0 kΩ
0 V
R_L
8 Ω
(b)
+24 V
12.7 V
R_1
1.0 kΩ
C_1
Q_1
12 V
12 V
10 μF
D_1
C_3
0 V
10 μF
C_2
D_2
10 μF
Q_2
R_2
1.0 kΩ
11.3 V
R_L
8 Ω
(c)
+18 V
9.7 V
R_1
330 Ω
C_1
Q_1
18 V
9 V
10 μF
D_1
C_3
0 V
10 μF
C_2
D_2
10 μF
Q_2
R_2
330 Ω
8.3 V
R_L
8 Ω
(d)

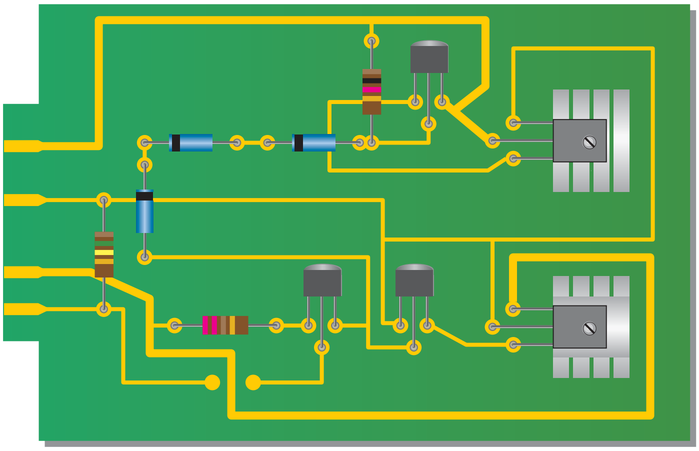
APPLICATION ACTIVITY PROBLEMS

26. Assume that the public address system represented by the block diagram in Figure 7–34 has quit working. You find there is no signal output from the power amplifier or the preamplifier, but you have verified that the microphone is working. Which two blocks are the most likely to be the problem? How would you narrow the choice down to one block?

27. Describe the output that would be observed in the push-pull amplifier of Figure 7–35 with a 2 V rms sinusoidal input voltage if the base-emitter junction of Q_2 opened.

28. Describe the output that would be observed in Figure 7–35 if the collector-emitter junction of Q_5 opened for the same input as in Problem 27.

29. After visually inspecting the power amplifier circuit board in Figure 7–49, describe any problems.



▲ FIGURE 7–49

DATASHEET PROBLEMS

30. Referring to the datasheet in Figure 7–50, determine the following:

- **(a)** minimum β_{DC} for the BD135 and the conditions
- **(b)** maximum collector-to-emitter voltage for the BD135
- **(c)** maximum power dissipation for the BD135 at a case temperature of 25°C
- **(d)** maximum continuous collector current for the BD135

31. Determine the maximum power dissipation for a BD135 at a case temperature of 50°C.

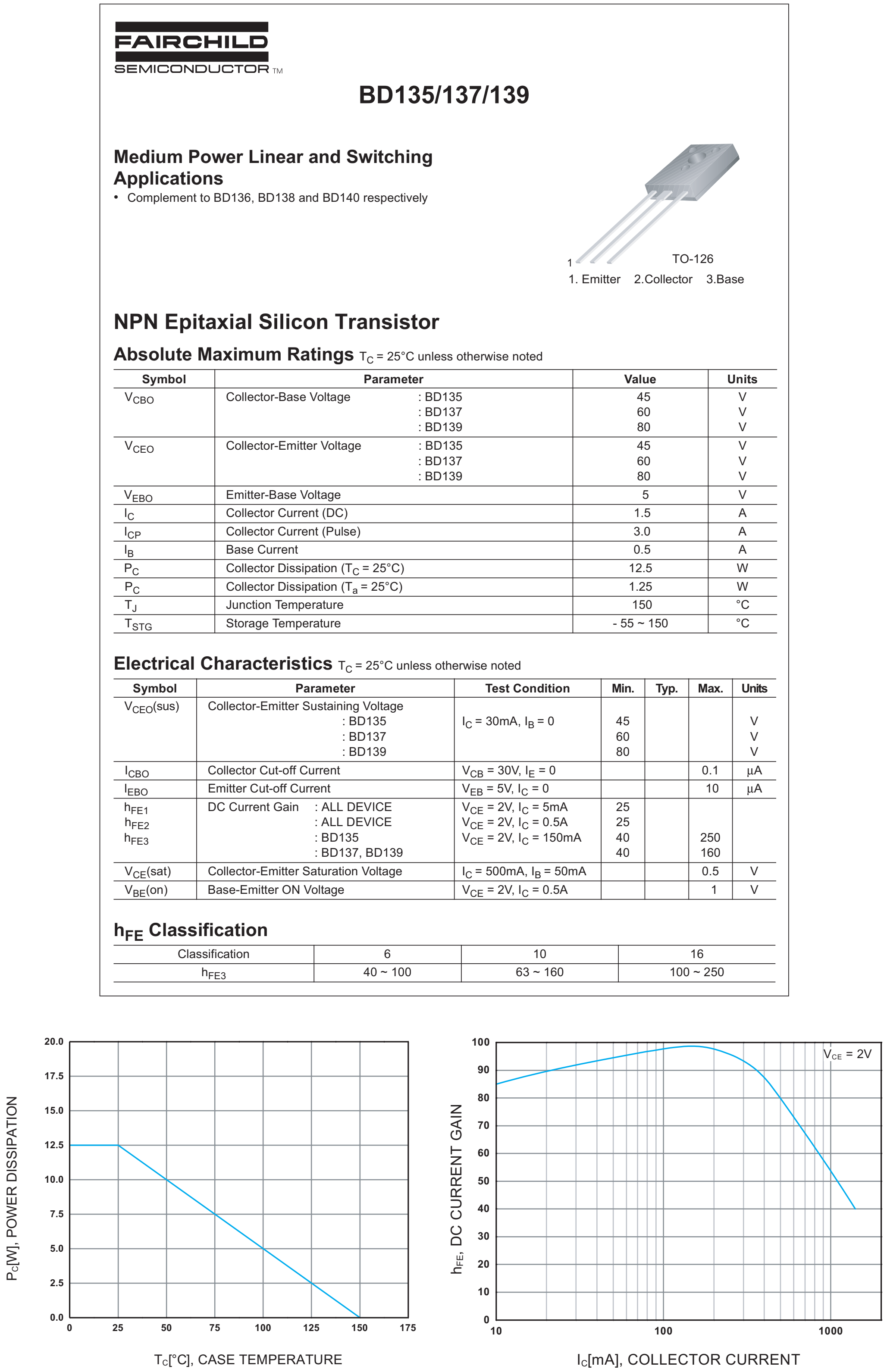
32. Determine the maximum power dissipation for a BD135 at an ambient temperature of 50°C.

33. Describe what happens to the dc current gain as the collector current increases.

34. Determine the approximate h_{FE} for the BD135 at $I_C = 20\text{ mA}$.

ADVANCED PROBLEMS

35. Explain why the specified maximum power dissipation of a power transistor at an ambient temperature of 25°C is much less than maximum power dissipation at a case temperature of 25°C.



FAIRCHILD SEMICONDUCTOR TM

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively

1
TO-126
1. Emitter 2.Collector 3.Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD135 : BD137 : BD139	45 60 80	V V V
V_{CEO}	Collector-Emitter Voltage	: BD135 : BD137 : BD139	45 60 80	V V V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C = 25°C)		12.5	W
P_C	Collector Dissipation (T_a = 25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage : BD135 : BD137 : BD139	I_C = 30mA, I_B = 0	45 60 80			V V V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	μA
h_{FE1} h_{FE2} h_{FE3}	DC Current Gain : ALL DEVICE : ALL DEVICE : BD135 : BD137, BD139	V_{CE} = 2V, I_C = 5mA V_{CE} = 2V, I_C = 0.5A V_{CE} = 2V, I_C = 150mA	25 25 40 40		 250 160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
0
25
50
75
100
125
150
175
P_C[W], POWER DISSIPATION
T_C[°C], CASE TEMPERATURE
100
90
80
70
60
50
40
30
20
10
0
10
100
1000
V_CE = 2V
h_FE, DC CURRENT GAIN
I_C[mA], COLLECTOR CURRENT

▲ FIGURE 7–50

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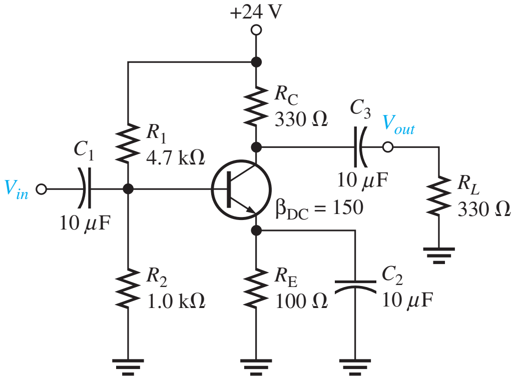
36. Draw the dc and the ac load lines for the amplifier in Figure 7–51.

▶ **FIGURE 7–51**



37. Design a swamped class A power amplifier that will operate from a dc supply of +15 V with an approximate voltage gain of 50. The quiescent collector current should be approximately 500 mA, and the total dc current from the supply should not exceed 750 mA. The output power must be at least 1 W.

38. The public address system in Figure 7–34 is a portable unit that is independent of 115 V ac. Determine the ampere-hour rating for the +15 V and the −15 V battery supply necessary for the system to operate for 4 hours on a continuous basis.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

39. Open file TSP07-39 and determine the fault.

40. Open file TSP07-40 and determine the fault.

41. Open file TSP07-41 and determine the fault.

42. Open file TSP07-42 and determine the fault.

43. Open file TSP07-43 and determine the fault.

8

Field-Effect Transistors (FETs)

CHAPTER OUTLINE

8–1 The JFET
8–2 JFET Characteristics and Parameters
8–3 JFET Biasing
8–4 The Ohmic Region
8–5 The MOSFET
8–6 MOSFET Characteristics and Parameters
8–7 MOSFET Biasing
8–8 The IGBT
8–9 Troubleshooting
Application Activity

CHAPTER OBJECTIVES

- Discuss the JFET and how it differs from the BJT
- Discuss, define, and apply JFET characteristics and parameters
- Discuss and analyze JFET biasing
- Discuss the ohmic region on a JFET characteristic curve
- Explain the operation of MOSFETs
- Discuss and apply MOSFET parameters
- Describe and analyze MOSFET bias circuits
- Discuss the IGBT
- Troubleshoot FET circuits

KEY TERMS

- JFET
- Drain
- Source
- Gate
- Pinch-off voltage
- Transconductance
- Ohmic region
- MOSFET
- Depletion
- Enhancement
- IGBT

APPLICATION ACTIVITY PREVIEW

The Application Activity involves the electronic control circuits for a waste water treatment system. In particular, you will focus on the application of field-effect transistors in the sensing circuits for chemical measurements.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

BJTs (bipolar junction transistors) were covered in previous chapters. Now we will discuss the second major type of transistor, the FET (field-effect transistor). **FETs** are unipolar devices because, unlike BJTs that use both electron and hole current, they operate only with one type of charge carrier. The two main types of FETs are the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET). The term *field-effect* relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate).

Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device. A major advantage of FETs is their very high input resistance. Because of their nonlinear characteristics, they are generally not as widely used in amplifiers as BJTs except where very high input impedances are required. However, FETs are the preferred device in low-voltage switching applications because they are generally faster than BJTs when turned on and off. The IGBT is generally used in high-voltage switching applications.

8–1 THE JFET

The **JFET** (junction field-effect transistor) is a type of FET that operates with a reverse-biased *pn* junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, *n* channel or *p* channel.

After completing this section, you should be able to

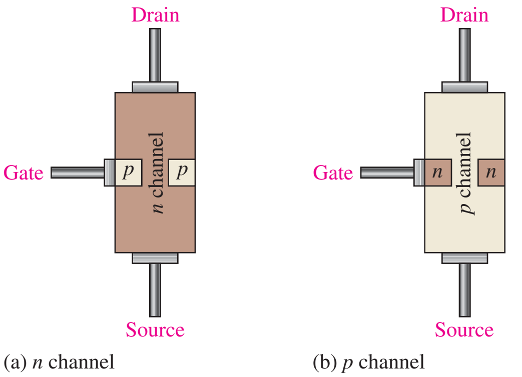
- ❑ **Discuss the JFET and how it differs from the BJT**
- ❑ Describe the basic structure of *n*-channel and *p*-channel JFETs
  - ◆ Name the terminals ◆ Explain a channel
- ❑ Explain the basic operation of a JFET
- ❑ Identify JFET schematic symbols

Basic Structure

Figure 8–1(a) shows the basic structure of an *n*-channel JFET (junction field-effect transistor). Wire leads are connected to each end of the *n*-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a **channel,** and both *p*-type regions are connected to the **gate** lead. For simplicity, the gate lead is shown connected to only one of the *p* regions. A *p*-channel JFET is shown in Figure 8–1(b).

HISTORY NOTE

In 1952, Ian Ross and George Dacey succeeded in making a unipolar device with a structure similar to today's JFET.



(a) *n* channel (b) *p* channel

FIGURE 8–1

A representation of the basic structure of the two types of JFET.

Basic Operation

To illustrate the operation of a JFET, Figure 8–2 shows dc bias voltages applied to an *n*-channel device. V_{DD} provides a drain-to-source voltage and supplies current from

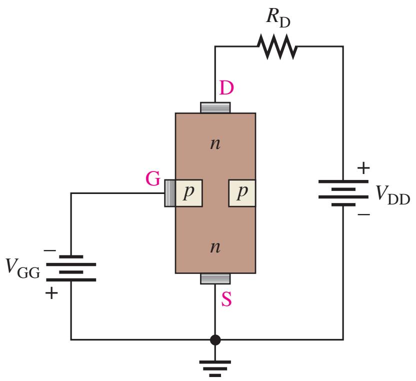


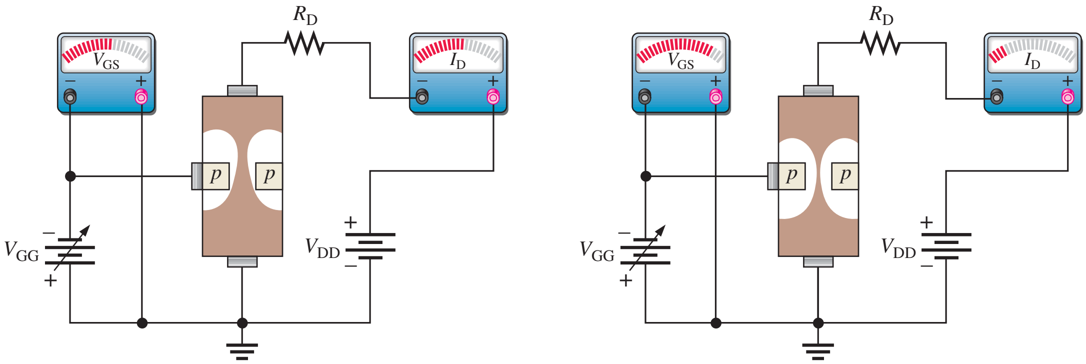
FIGURE 8–2

A biased *n*-channel JFET.

drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

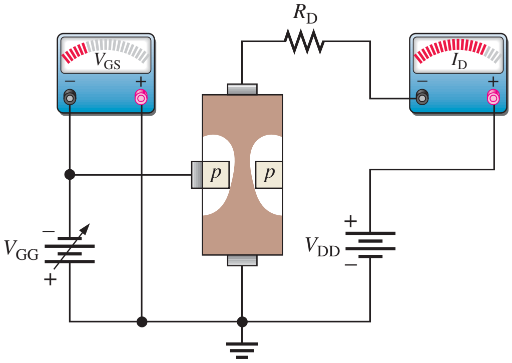
The JFET is always operated with the gate-source pn junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the *pn* junction, which extends into the *n* channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D. Figure 8–3 illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source. We will discuss JFET characteristic curves and some parameters in Section 8–2.



(a) JFET biased for conduction

(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.



(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

▲ **FIGURE 8–3**

Effects of V_{GS} on channel width, resistance, and drain current ($V_{GG} = V_{GS}$).

JFET Symbols

The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure 8–4. Notice that the arrow on the gate points "in" for *n* channel and "out" for *p* channel.

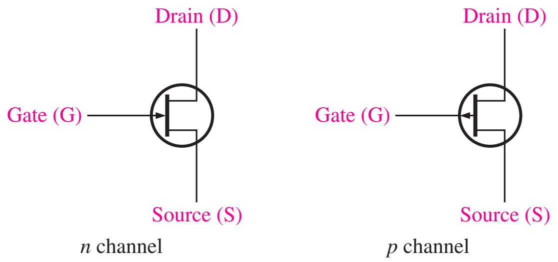


FIGURE 8–4

JFET schematic symbols.

SECTION 8–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. Name the three terminals of a JFET.
2. Does an *n*-channel JFET require a positive or negative value for V_{GS}?
3. How is the drain current controlled in a JFET?

8–2 JFET CHARACTERISTICS AND PARAMETERS

The JFET operates as a voltage-controlled, constant-current device. Cutoff and pinch-off as well as JFET transfer characteristics are covered in this section.

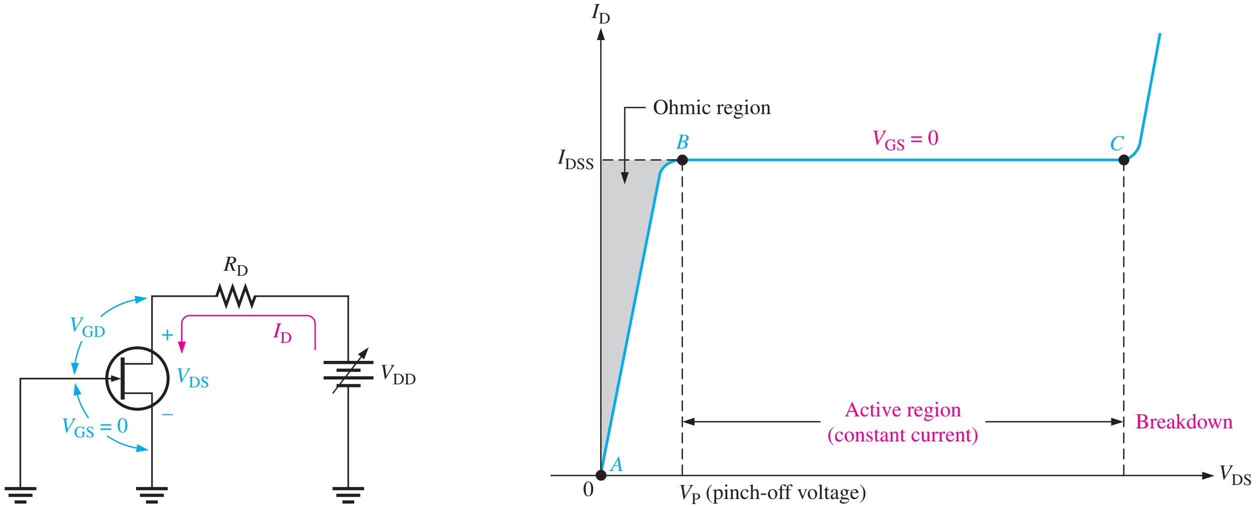
After completing this section, you should be able to

- ❑ **Discuss, define, and apply JFET characteristics and parameters**
- ❑ Discuss the drain characteristic curve
  - ◆ Identify the ohmic, active, and breakdown regions of the curve
- ❑ Define *pinch-off voltage*
- ❑ Discuss breakdown
- ❑ Explain how gate-to-source voltage controls the drain current
- ❑ Discuss the cutoff voltage
- ❑ Compare pinch-off and cutoff
- ❑ Explain the JFET universal transfer characteristic
  - ◆ Calculate the drain current using the transfer characteristic equation
  - ◆ Interpret a JFET datasheet
- ❑ Discuss JFET forward transconductance
  - ◆ Define *transconductance* ◆ Calculate forward transconductance
- ❑ Discuss JFET input resistance and capacitance
- ❑ Determine the ac drain-to-source resistance

Drain Characteristic Curve

Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0$ V). This is produced by shorting the gate to the source, as in Figure 8–5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 8–5(b) between points *A* and *B*. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the *ohmic region* because V_{DS} and I_D are related by Ohm's law. (Ohmic region is discussed further in Section 8–4.)

At point *B* in Figure 8–5(b), the curve levels off and enters the active region where I_D becomes essentially constant. As V_{DS} increases from point *B* to point *C*, the reverse-bias



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

▲ **FIGURE 8–5**

The drain characteristic curve of a JFET for $V_{GS} = 0$ showing pinch-off voltage.

voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

Pinch-Off Voltage For $V_{GS} = 0$ V, the value of V_{DS} at which I_D becomes essentially constant (point *B* on the curve in Figure 8–5(b)) is the **pinch-off voltage**, V_P. For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET datasheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0$ V.

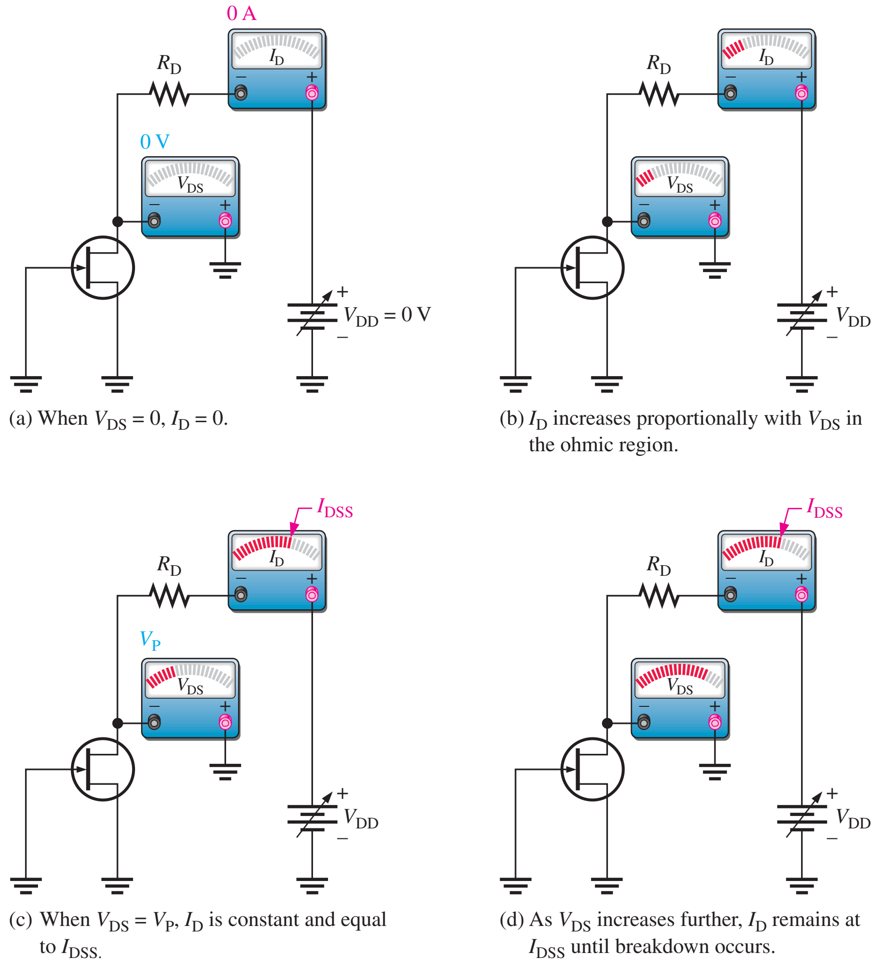
Breakdown As shown in the graph in Figure 8–5(b), **breakdown** occurs at point *C* when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points *B* and *C* on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for $V_{GS} = 0$ V is illustrated in Figure 8–6.

V_{GS} Controls I_D

Let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure 8–7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure 8–7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P. The term *pinch-off* is not the same as pinch-off voltage, V_p. Therefore, the amount of drain current is controlled by V_{GS}, as illustrated in Figure 8–8.

Cutoff Voltage

The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage,** $V_{GS(off)}$, as shown in Figure 8–8(d). The JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.



(a) When $V_{DS} = 0$, $I_D = 0$.

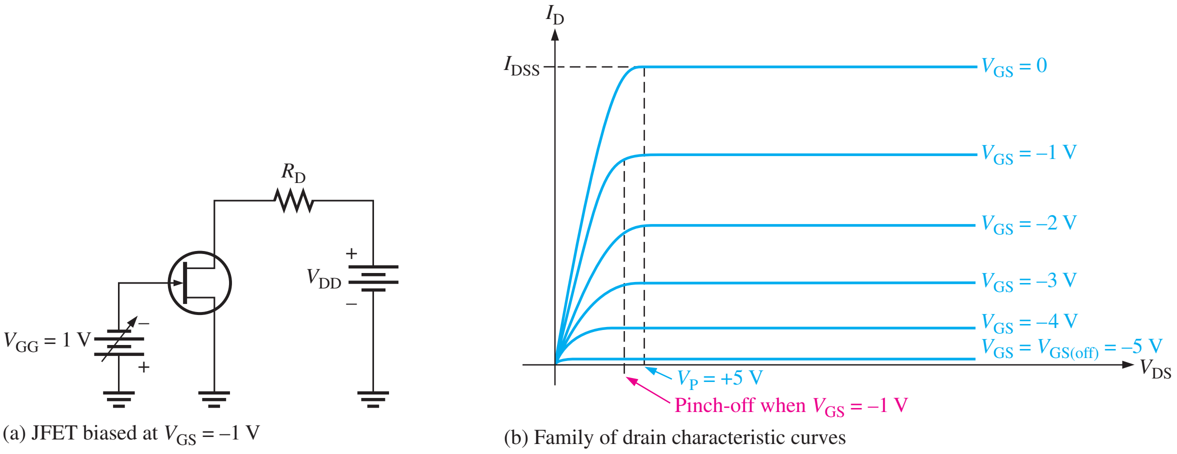
(b) I_D increases proportionally with V_{DS} in the ohmic region.

(c) When $V_{DS} = V_P$, I_D is constant and equal to I_{DSS}.

(d) As V_{DS} increases further, I_D remains at I_{DSS} until breakdown occurs.

FIGURE 8–6

JFET action that produces the characteristic curve for $V_{GS} = 0$ V.

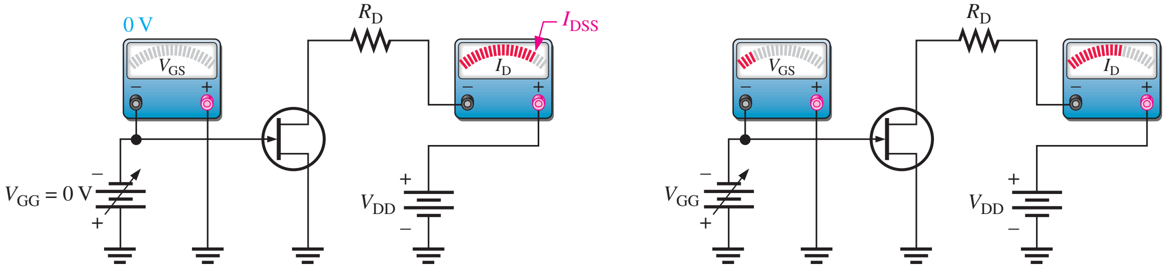


(a) JFET biased at $V_{GS} = -1$ V

(b) Family of drain characteristic curves

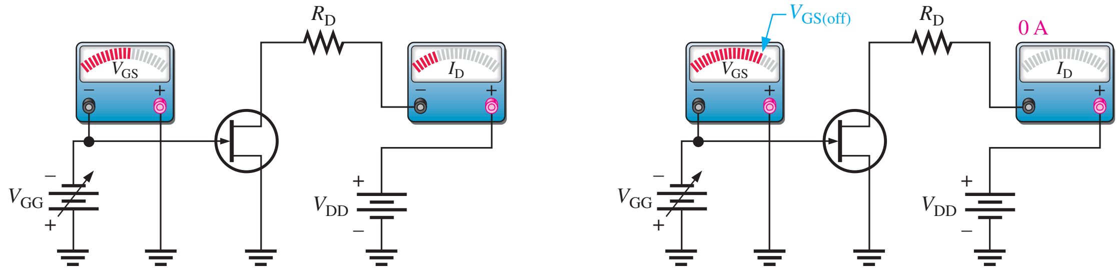
FIGURE 8–7

Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.



(a) $V_{GS} = 0$ V, $V_{DS} \geq V_P$, $I_D = I_{DSS}$

(b) When V_{GS} is negative, I_D decreases and is constant above pinch-off, which is less than V_P.



(c) As V_{GS} is made more negative, I_D continues to decrease but is constant above pinch-off, which has also decreased.

(d) Until $V_{GS} = -V_{GS(off)}$, I_D continues to decrease. When $V_{GS} \geq -V_{GS(off)}$, $I_D \cong 0$.

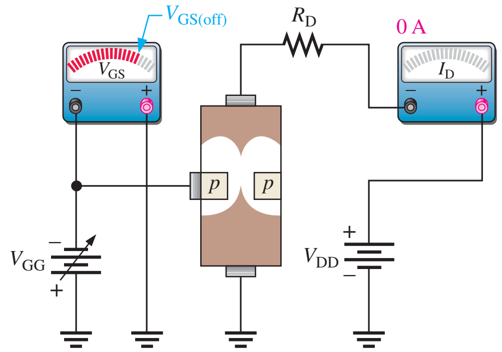
▲ **FIGURE 8–8**

V_{GS} controls I_D.

As you have seen, for an *n*-channel JFET, the more negative V_{GS} is, the smaller I_D becomes in the active region. When V_{GS} has a sufficiently large negative value, I_D is reduced to zero. This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel, as shown in Figure 8–9.

▶ **FIGURE 8–9**

JFET at cutoff.



The basic operation of a *p*-channel JFET is the same as for an *n*-channel device except that a *p*-channel JFET requires a negative V_{DD} and a positive V_{GS}, as illustrated in Figure 8–10.

Comparison of Pinch-Off Voltage and Cutoff Voltage

As you have seen, there is a difference between pinch-off and cutoff voltages. There is also a connection. The pinch-off voltage V_P is the value of V_{DS} at which the drain current becomes constant and equal to I_{DSS} and is always measured at $V_{GS} = 0$ V. However,

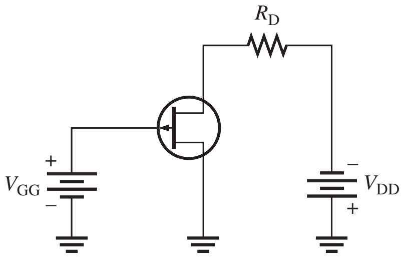


FIGURE 8–10

A biased *p*-channel JFET.

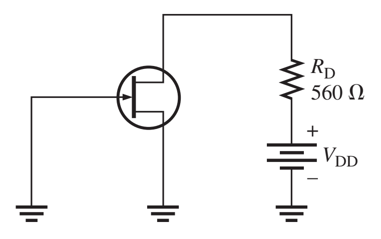
pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes constant varies with V_{GS}.

$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in sign. A datasheet usually will give either $V_{GS(off)}$ or V_P, but not both. However, when you know one, you have the other. For example, if $V_{GS(off)} = -5$ V, then $V_P = +5$ V, as shown in Figure 8–7(b).

EXAMPLE 8–1

For the JFET in Figure 8–11, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the *minimum* value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0$ V.

FIGURE 8–11



Solution Since $V_{GS(off)} = -4$ V, $V_P = 4$ V. The minimum value of V_{DS} for the JFET to be in its constant-current region is

$$V_{DS} = V_P = 4\text{ V}$$

In the constant-current region with $V_{GS} = 0$ V,

$$I_D = I_{DSS} = 12\text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12\text{ mA})(560\ \Omega) = 6.72\text{ V}$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{R_D} = 4\text{ V} + 6.72\text{ V} = \mathbf{10.7\ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

Related Problem[*] If V_{DD} is increased to 15 V, what is the drain current?

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

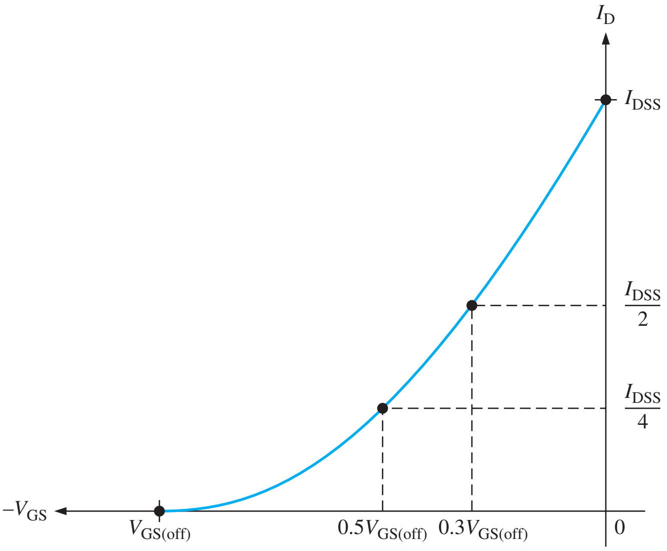
EXAMPLE 8–2 A particular *p*-channel JFET has a $V_{GS(off)} = +4$ V. What is I_D when $V_{GS} = +6$ V?

Solution The *p*-channel JFET requires a positive gate-to-source voltage. The more positive the voltage, the less the drain current. When $V_{GS} = 4$ V, $I_D = 0$. Any further increase in V_{GS} keeps the JFET cut off, so I_D remains **0**.

Related Problem What is V_P for the JFET described in this example?

JFET Universal Transfer Characteristic

You have learned that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an *n*-channel JFET, $V_{GS(off)}$ is negative, and for a *p*-channel JFET, $V_{GS(off)}$ is positive. Because V_{GS} does control I_D, the relationship between these two quantities is very important. Figure 8–12 is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D. This curve is also known as a transconductance curve.



▶ **FIGURE 8–12**

JFET universal transfer characteristic curve (*n*-channel).

Notice that the bottom end of the curve is at a point on the V_{GS} axis equal to $V_{GS(off)}$, and the top end of the curve is at a point on the I_D axis equal to I_{DSS}. This curve shows that

$$I_D = 0 \qquad \text{when } V_{GS} = V_{GS(off)}$$

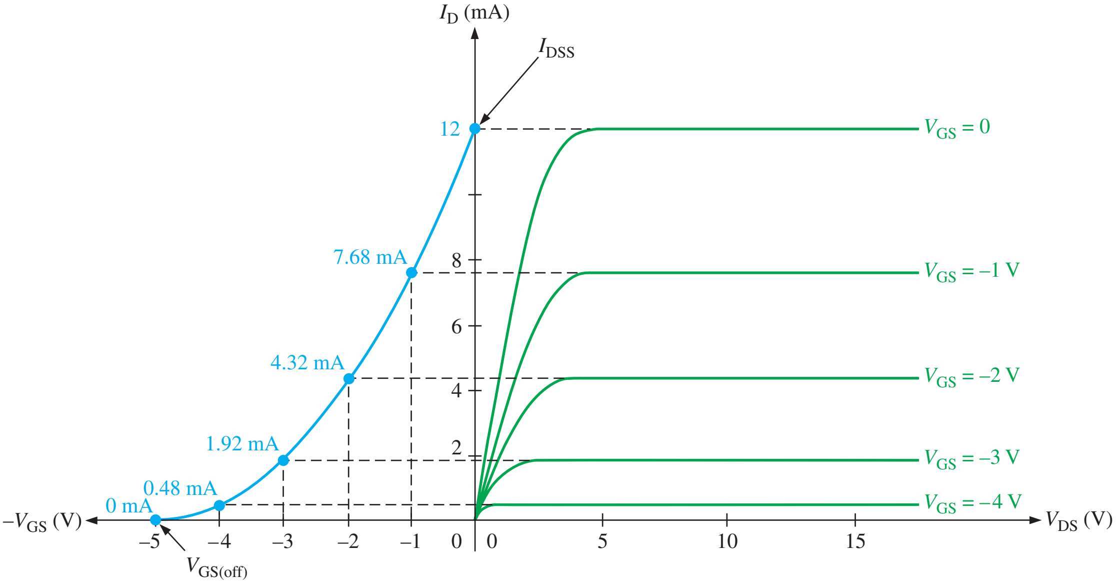
$$I_D = \frac{I_{DSS}}{4} \qquad \text{when } V_{GS} = 0.5V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{2} \qquad \text{when } V_{GS} = 0.3V_{GS(off)}$$

and

$$I_D = I_{DSS} \qquad \text{when } V_{GS} = 0$$

The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off, as illustrated in Figure 8–13 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves. For example, when $V_{GS} = -2$ V, $I_D = 4.32$ mA. Also, for this specific JFET, $V_{GS(off)} = -5$ V and $I_{DSS} = 12$ mA.



▲ FIGURE 8–13

Example of the development of an *n*-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

A JFET transfer characteristic curve is expressed approximately as

$$\mathbf{I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2}$$

Equation 8–1

With Equation 8–1, I_D can be determined for any V_{GS} if $V_{GS(off)}$ and I_{DSS} are known. These quantities are usually available from the datasheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a *square law,* and therefore, JFETs and MOSFETs are often referred to as *square-law devices.*

The datasheet for a typical JFET series is shown in Figure 8–14.

EXAMPLE 8–3

The partial datasheet in Figure 8–14 for a 2N5459 JFET indicates that typically $I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Using these values, determine the drain current for $V_{GS} = 0$ V, -1 V, and -4 V.

Solution For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\ mA}$$

For $V_{GS} = -1$ V, use Equation 8–1.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$

$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

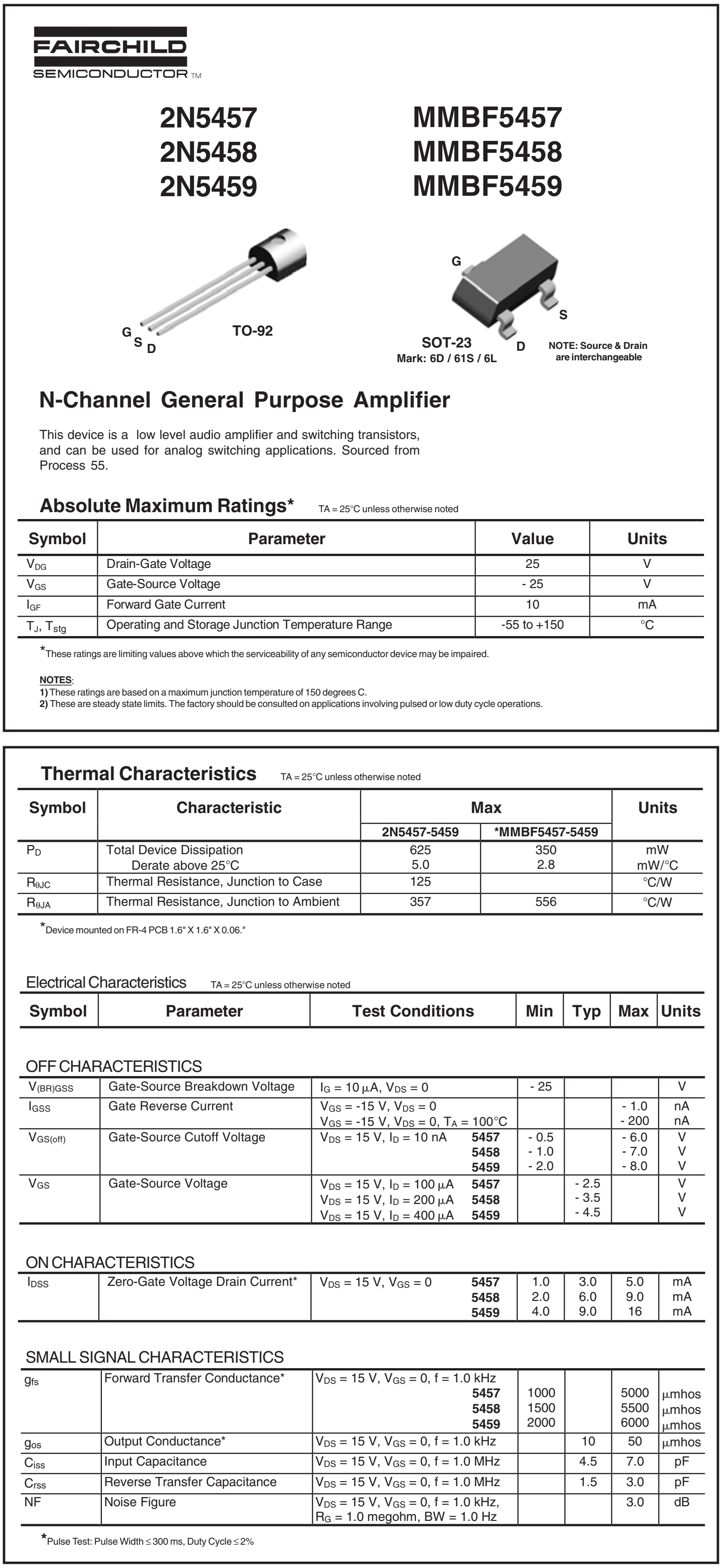
For $V_{GS} = -4$ V,

$$I_D \cong (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\ mA}$$

Related Problem Determine I_D for $V_{GS} = -3$ V for the 2N5459 JFET.

▶ **FIGURE 8–14**

JFET partial datasheet. Copyright Fairchild Semiconductor Corporation. Used by permission.



FAIRCHILD
SEMICONDUCTOR™

2N5457 MMBF5457
2N5458 MMBF5458
2N5459 MMBF5459

G
S
D
TO-92
G
S
D
SOT-23
Mark: 6D / 61S / 6L
NOTE: Source & Drain are interchangeable

N-Channel General Purpose Amplifier

This device is a low level audio amplifier and switching transistors, and can be used for analog switching applications. Sourced from Process 55.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		2N5457-5459	*MMBF5457-5459	
P_D	Total Device Dissipation	625	350	mW
	Derate above 25°C	5.0	2.8	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

Electrical Characteristics TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10\ \mu A$, $V_{DS} = 0$		- 25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$				- 1.0	nA
		$V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$				- 200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA	**5457**	- 0.5		- 6.0	V
			5458	- 1.0		- 7.0	V
			5459	- 2.0		- 8.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 100\ \mu A$	**5457**		- 2.5		V
		$V_{DS} = 15$ V, $I_D = 200\ \mu A$	**5458**		- 3.5		V
		$V_{DS} = 15$ V, $I_D = 400\ \mu A$	**5459**		- 4.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current*	$V_{DS} = 15$ V, $V_{GS} = 0$	**5457**	1.0	3.0	5.0	mA
			5458	2.0	6.0	9.0	mA
			5459	4.0	9.0	16	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance*	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz					
			5457	1000		5000	μmhos
			5458	1500		5500	μmhos
			5459	2000		6000	μmhos
g_{os}	Output Conductance*	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz			10	50	μmhos
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_G = 1.0$ megohm, BW = 1.0 Hz				3.0	dB

*Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2%

JFET Forward Transconductance

The forward **transconductance** (transfer conductance), g_m, is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are g_{fs} and y_{fs} (forward transfer admittance). As you will see in Chapter 9, g_m is an important factor in determining the voltage gain of a FET amplifier.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by V_{GS}. The value for g_m is greater near the top of the curve (near $V_{GS} = 0$) than it is near the bottom (near $V_{GS(off)}$), as illustrated in Figure 8–15.

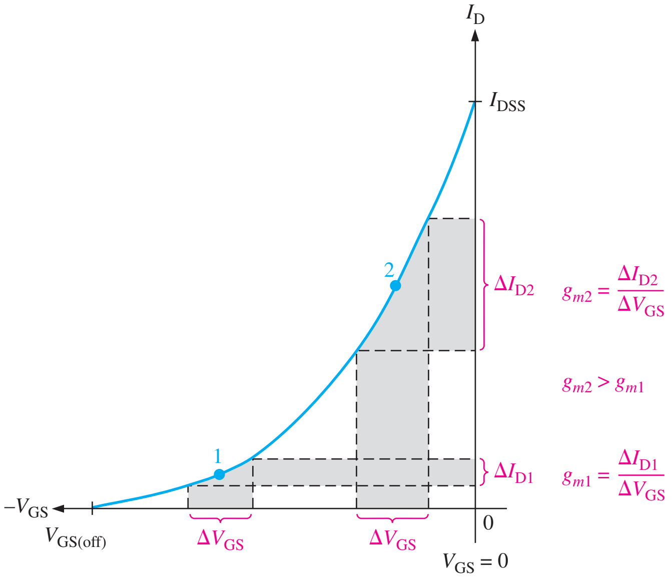


FIGURE 8–15

g_m varies depending on the bias point (V_{GS}).

A datasheet normally gives the value of g_m measured at $V_{GS} = 0$ V (g_{m0}). For example, the datasheet for the 2N5457 JFET specifies a minimum g_{m0} (g_{fs}) of 1000 μmhos (the mho is the same unit as the siemens (S)) with $V_{DS} = 15$ V.

Given g_{m0}, you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

$$\mathbf{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)}$$

Equation 8–2

When a value of g_{m0} is not available, you can calculate it using values of I_{DSS} and $V_{GS(off)}$. The vertical lines indicate an absolute value (no sign).

$$\mathbf{g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}}$$

Equation 8–3

EXAMPLE 8–4

The following information is included on the datasheet in Figure 8–14 for a 2N5457 JFET: typically, $I_{DSS} = 3.0$ mA, $V_{GS(off)} = -6$ V maximum, and $g_{fs(max)} = 5000$ μS. Using these values, determine the forward transconductance for $V_{GS} = -4$ V, and find I_D at this point.

Solution $g_{m0} = g_{fs} = 5000\ \mu\text{S}$. Use Equation 8–2 to calculate g_m.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = (5000\ \mu\text{S})\left(1 - \frac{-4\text{ V}}{-6\text{ V}}\right) = \mathbf{1667\ \mu S}$$

Next, use Equation 8–1 to calculate I_D at $V_{GS} = -4$ V.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (3.0\text{ mA})\left(1 - \frac{-4\text{ V}}{-6\text{ V}}\right)^2 = \mathbf{333\ \mu A}$$

Related Problem A given JFET has the following characteristics: $I_{DSS} = 12$ mA, $V_{GS(off)} = -5$ V, and $g_{m0} = g_{fs} = 3000\ \mu\text{S}$. Find g_m and I_D when $V_{GS} = -2$ V.

Input Resistance and Capacitance

As you know, a JFET operates with its gate-source junction reverse-biased, which makes the input resistance at the gate very high. This high input resistance is one advantage of the JFET over the BJT. (Recall that a bipolar junction transistor operates with a forward-biased base-emitter junction.) JFET datasheets often specify the input resistance by giving a value for the gate reverse current, I_{GSS}, at a certain gate-to-source voltage. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value (no sign):

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

For example, the 2N5457 datasheet in Figure 8–14 lists a maximum I_{GSS} of -1.0 nA for $V_{GS} = -15$ V at 25°C. I_{GSS} increases with temperature, so the input resistance decreases.

The input capacitance, C_{iss}, is a result of the JFET operating with a reverse-biased *pn* junction. Recall that a reverse-biased *pn* junction acts as a capacitor whose capacitance depends on the amount of reverse voltage. For example, the 2N5457 has a maximum C_{iss} of 7 pF for $V_{GS} = 0$.

EXAMPLE 8–5 A certain JFET has an I_{GSS} of -2 nA for $V_{GS} = -20$ V. Determine the input resistance.

Solution

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{20\text{ V}}{2\text{ nA}} = \mathbf{10{,}000\ M\Omega}$$

Related Problem Determine the input resistance for the 2N5458 from the datasheet in Figure 8–14.

AC Drain-to-Source Resistance

You learned from the drain characteristic curve that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a large change in V_{DS} produces only a very small change in I_D. The ratio of these changes is the ac drain-to-source resistance of the device, r'_{ds}.

$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

Datasheets often specify this parameter in terms of the output conductance, g_{os}, or output admittance, y_{os}, for $V_{GS} = 0$ V.

SECTION 8–2 CHECKUP

1. The drain-to-source voltage at the pinch-off point of a particular JFET is 7 V. If the gate-to-source voltage is zero, what is V_P?
2. The V_{GS} of a certain *n*-channel JFET is increased negatively. Does the drain current increase or decrease?
3. What value must V_{GS} have to produce cutoff in a *p*-channel JFET with a $V_p = -3$ V?

8–3 JFET BIASING

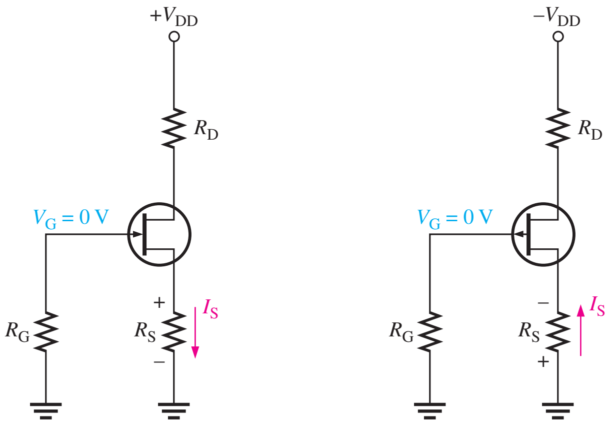
Using some of the JFET parameters discussed previously, you will now see how to dc-bias JFETs. Just as with the BJT, the purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and current-source bias.

After completing this section, you should be able to

- ❑ **Discuss and analyze JFET biasing**
- ❑ Describe self-bias
  - ◆ Calculate JFET currents and voltages
- ❑ Describe how to set the Q-point of a self-biased JFET
  - ◆ Determine midpoint bias
- ❑ Graphically analyze a self-biased JFET
- ❑ Discuss voltage-divider bias
  - ◆ Calculate JFET currents and voltages
- ❑ Graphically analyze a voltage-divider biased JFET
- ❑ Discuss Q-point stability
- ❑ Describe current-source bias

Self-Bias

Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an *n*-channel JFET and a positive V_{GS} for a *p*-channel JFET. This can be achieved using the self-bias arrangements shown in Figure 8–16. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to force the gate to be at 0 V and to isolate an ac signal from ground in amplifier applications, as you will see later.



(a) *n* channel (b) *p* channel

FIGURE 8–16

Self-biased JFETs ($I_S = I_D$ in all FETs).

For the *n*-channel JFET in Figure 8–16(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_D R_S$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Thus,

$$V_{GS} = -I_D R_S$$

For the *p*-channel JFET shown in Figure 8–16(b), the current through R_S produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since $I_S = I_D$,

$$V_{GS} = +I_D R_S$$

In the following example, the *n*-channel JFET in Figure 8–16(a) is used for illustration. Keep in mind that analysis of the *p*-channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

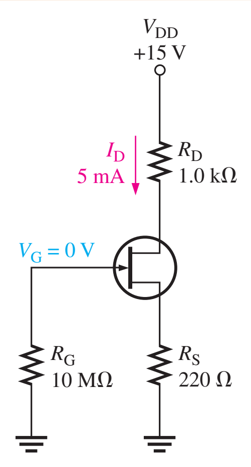
Since $V_S = I_D R_S$, the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$$

EXAMPLE 8–6

Find V_{DS} and V_{GS} in Figure 8–17. For the particular JFET in this circuit, the parameter values such as g_m, $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced. Another JFET, even of the same type, may not produce the same results when connected in this circuit due to the variations in parameter values.

▶ FIGURE 8–17



Solution

$$V_S = I_D R_S = (5\text{ mA})(220\ \Omega) = 1.1\text{ V}$$

$$V_D = V_{DD} - I_D R_D = 15\text{ V} - (5\text{ mA})(1.0\text{ k}\Omega) = 15\text{ V} - 5\text{ V} = 10\text{ V}$$

Therefore,

$$V_{DS} = V_D - V_S = 10\text{ V} - 1.1\text{ V} = \mathbf{8.9\ V}$$

Since $V_G = 0$ V,

$$V_{GS} = V_G - V_S = 0\text{ V} - 1.1\text{ V} = \mathbf{-1.1\ V}$$

Related Problem Determine V_{DS} and V_{GS} in Figure 8–17 when $I_D = 8$ mA. Assume that $R_D = 860\ \Omega$, $R_S = 390\ \Omega$, and $V_{DD} = 12$ V.

Open the Multisim file E08-06 in the Examples folder on the companion website. Measure I_D, V_{GS}, and V_{DS} and compare to the calculated values from the Related Problem.

Setting the Q-Point of a Self-Biased JFET

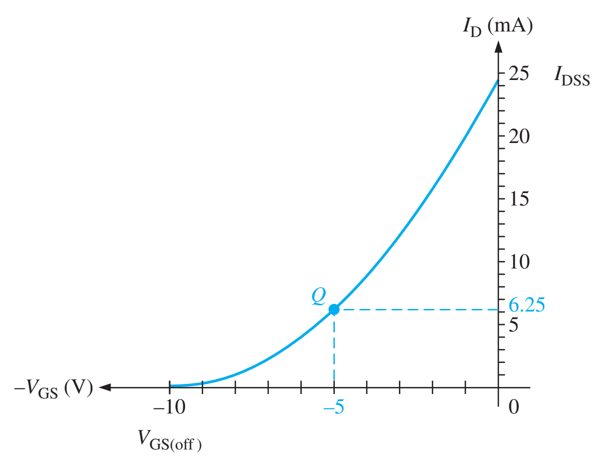
The basic approach to establishing a JFET bias point is to determine I_D for a desired value of V_{GS} or vice versa. Then calculate the required value of R_S using the following relationship. The vertical lines indicate an absolute value.

$$R_S = \left|\frac{V_{GS}}{I_D}\right|$$

For a desired value of V_{GS}, I_D can be determined in either of two ways: from the transfer characteristic curve for the particular JFET or, more practically, from Equation 8–1 using I_{DSS} and $V_{GS(off)}$ from the JFET datasheet. The next two examples illustrate these procedures.

EXAMPLE 8–7

Determine the value of R_S required to self-bias an *n*-channel JFET that has the transfer characteristic curve shown in Figure 8–18 at $V_{GS} = -5$ V.



▲ FIGURE 8–18

Solution From the graph, $I_D = 6.25$ mA when $V_{GS} = -5$ V. Calculate R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

Related Problem Find R_S for $V_{GS} = -3$ V.

EXAMPLE 8–8

Determine the value of R_S required to self-bias a *p*-channel JFET with datasheet values of $I_{DSS} = 25$ mA and $V_{GS(off)} = 15$ V. V_{GS} is to be 5 V.

Solution Use Equation 8–1 to calculate I_D.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (25\text{ mA})\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2$$

$$= (25\text{ mA})(1 - 0.333)^2 = 11.1\text{ mA}$$

Now, determine R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

Related Problem Find the value of R_S required to self-bias a *p*-channel JFET with $I_{DSS} = 18$ mA and $V_{GS(off)} = 8$ V. $V_{GS} = 4$ V.

Midpoint Bias It is usually desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. Under signal conditions, midpoint bias allows the maximum amount of drain current swing between I_{DSS} and 0. For Equation 8–1, it can be shown that I_D is approximately one-half of I_{DSS} when $V_{GS} = V_{GS(off)}/3.4$. The derivation is given in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS(off)}/3.4}{V_{GS(off)}}\right)^2 = 0.5I_{DSS}$$

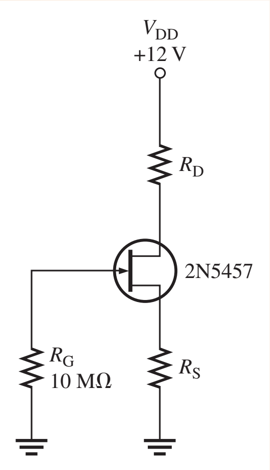
So, by selecting $V_{GS} = V_{GS(off)}/3.4$, you should get a midpoint bias in terms of I_D.

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop. Choose R_G arbitrarily large to prevent loading on the driving stage in a cascaded amplifier arrangement. Example 8–9 illustrates these concepts.

EXAMPLE 8–9

Looking at the datasheet in Figure 8–14, select resistor values for R_D and R_S in Figure 8–19 to set up an approximate midpoint bias. Use minimum datasheet values when given; otherwise, V_D should be approximately 6 V (one-half of V_{DD}).

▶ FIGURE 8–19



Solution For midpoint bias,

$$I_D \cong \frac{I_{DSS}}{2} = \frac{1.0\text{ mA}}{2} = 0.5\text{ mA}$$

and

$$V_{GS} \cong \frac{V_{GS(off)}}{3.4} = \frac{-0.5\text{ V}}{3.4} = -147\text{ mV}$$

Then

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{147\text{ mV}}{0.5\text{ mA}} = \mathbf{294\ \Omega}$$

$$V_D = V_{DD} - I_D R_D$$

$$I_D R_D = V_{DD} - V_D$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{ V} - 6\text{ V}}{0.5\text{ mA}} = \mathbf{12\ k\Omega}$$

Related Problem Select resistor values in Figure 8–19 to set up an approximate midpoint bias using a 2N5459.

Open the Multisim file E08-09 in the Examples folder on the companion website. The circuit has the calculated values for R_D and R_S from the Related Problem. Verify that an approximate midpoint bias is established by measuring V_D and I_D.

Graphical Analysis of a Self-Biased JFET

You can use the transfer characteristic curve of a JFET and certain parameters to determine the Q-point (I_D and V_{GS}) of a self-biased circuit. A circuit is shown in Figure 8–20(a), and a transfer characteristic curve is shown in Figure 8–20(b). If a curve is not available from a datasheet, you can plot it from Equation 8–1 using datasheet values for I_{DSS} and $V_{GS(off)}$.

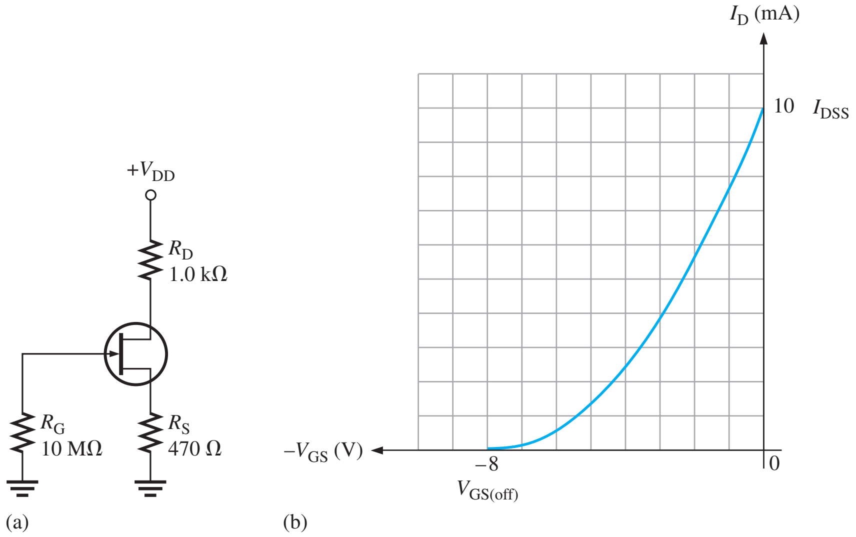


FIGURE 8–20

A self-biased JFET and its transfer characteristic curve.

To determine the Q-point of the circuit in Figure 8–20(a), a self-bias dc load line is established on the graph in part (b) as follows. First, calculate V_{GS} when I_D is zero.

$$V_{GS} = -I_D R_S = (0)(470\ \Omega) = 0\text{ V}$$

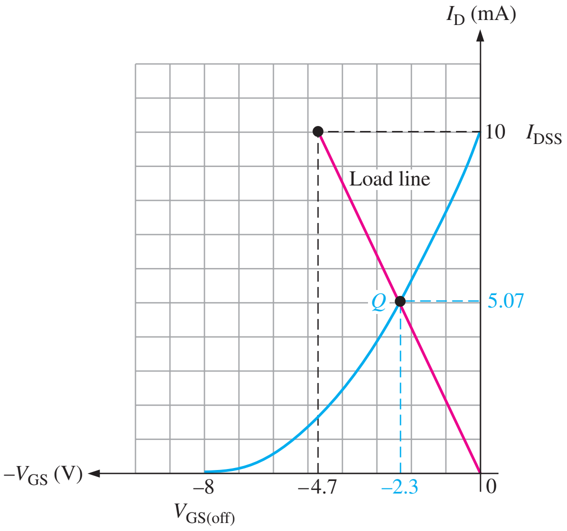
This establishes a point at the origin on the graph ($I_D = 0$, $V_{GS} = 0$). Next, calculate V_{GS} when $I_D = I_{DSS}$. From the curve in Figure 8–20(b), $I_{DSS} = 10$ mA.

$$V_{GS} = -I_D R_S = -(10\text{ mA})(470\ \Omega) = -4.7\text{ V}$$

This establishes a second point on the graph ($I_D = 10$ mA, $V_{GS} = -4.7$ V). Now, with two points, the load line can be drawn on the transfer characteristic curve as shown in Figure 8–21. The point where the load line intersects the transfer characteristic curve is the Q-point of the circuit as shown, where $I_D = 5.07$ mA and $V_{GS} = -2.3$ V.

▶ FIGURE 8–21

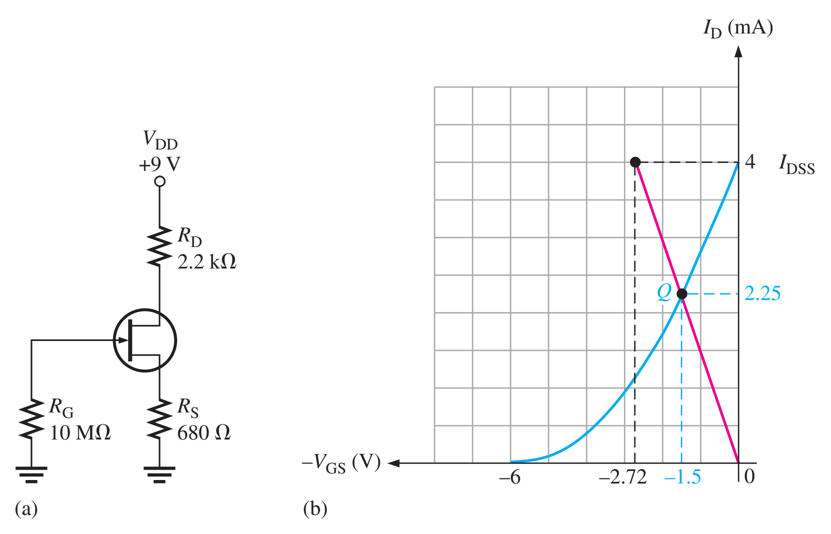
The intersection of the self-bias dc load line and the transfer characteristic curve is the Q-point.



EXAMPLE 8–10

Determine the Q-point for the JFET circuit in Figure 8–22(a). The transfer characteristic curve is given in Figure 8–22(b).

▶ FIGURE 8–22



Solution For $I_D = 0$,

$$V_{GS} = -I_D R_S = (0)(680\ \Omega) = 0\text{ V}$$

This gives a point at the origin. From the curve, $I_{DSS} = 4$ mA; so $I_D = I_{DSS} = 4$ mA.

$$V_{GS} = -I_D R_S = -(4\text{ mA})(680\ \Omega) = -2.72\text{ V}$$

This gives a second point at 4 mA and −2.72 V. A line is now drawn between the two points, and the values of I_D and V_{GS} at the intersection of the line and the curve are taken from the graph, as illustrated in Figure 8–22(b). The Q-point values from the graph are

$$I_D = \mathbf{2.25\ mA}$$
$$V_{GS} = \mathbf{-1.5\ V}$$

Related Problem If R_S is increased to 1.0 kΩ in Figure 8–22(a), what is the new Q-point?

For increased Q-point stability, the value of R_S in the self-bias circuit is increased and connected to a negative supply voltage. This is sometimes called *dual-supply bias.*

Voltage-Divider Bias

An *n*-channel JFET with voltage-divider bias is shown in Figure 8–23. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

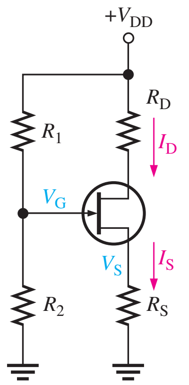


FIGURE 8–23

An *n*-channel JFET with voltage-divider bias ($I_S = I_D$).

The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

and the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

$$I_D = \frac{V_S}{R_S}$$

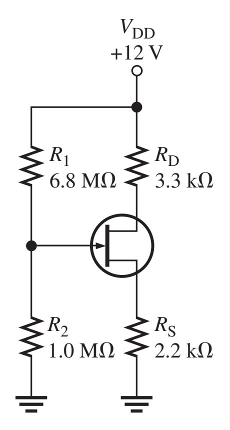
Substituting for V_S,

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

EXAMPLE 8–11

Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 8–24, given that for this particular JFET the parameter values are such that $V_D \cong 7\text{ V}$.

▶ FIGURE 8–24



Solution

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52\text{ mA})(2.2\text{ k}\Omega) = 3.34\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{1.0\text{ M}\Omega}{7.8\text{ M}\Omega}\right)12\text{ V} = 1.54\text{ V}$$

$$V_{GS} = V_G - V_S = 1.54\text{ V} - 3.34\text{ V} = \mathbf{-1.8\text{ V}}$$

If V_D had not been given in this example, the Q-point values could not have been found without the transfer characteristic curve.

Related Problem

Given that $V_D = 6\text{ V}$ when another JFET is inserted in the circuit of Figure 8–24, determine the Q-point.

Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.

In a JFET with voltage-divider bias when $I_D = 0$, V_{GS} is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For $I_D = 0$,

$$V_S = I_D R_S = (0)R_S = 0\text{ V}$$

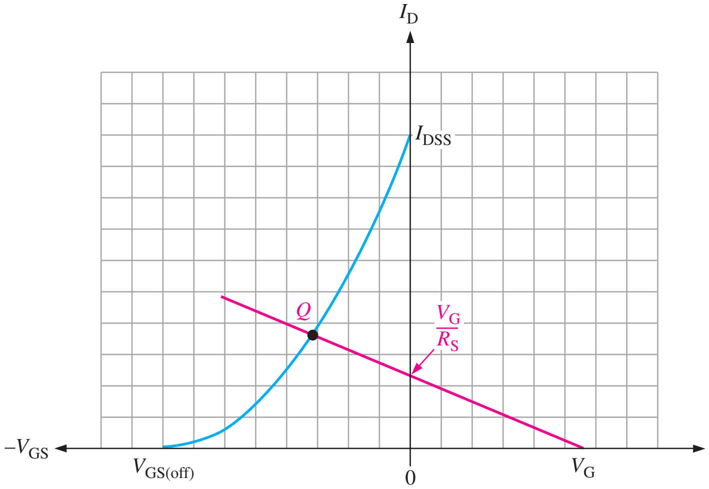
$$V_{GS} = V_G - V_S = V_G - 0\text{ V} = V_G$$

Therefore, one point on the line is at $I_D = 0$ and $V_{GS} = V_G$.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at $I_D = V_G/R_S$ and $V_{GS} = 0$. The generalized dc load line is shown in Figure 8–25. The point at which the load line intersects the transfer characteristic curve is the Q-point.

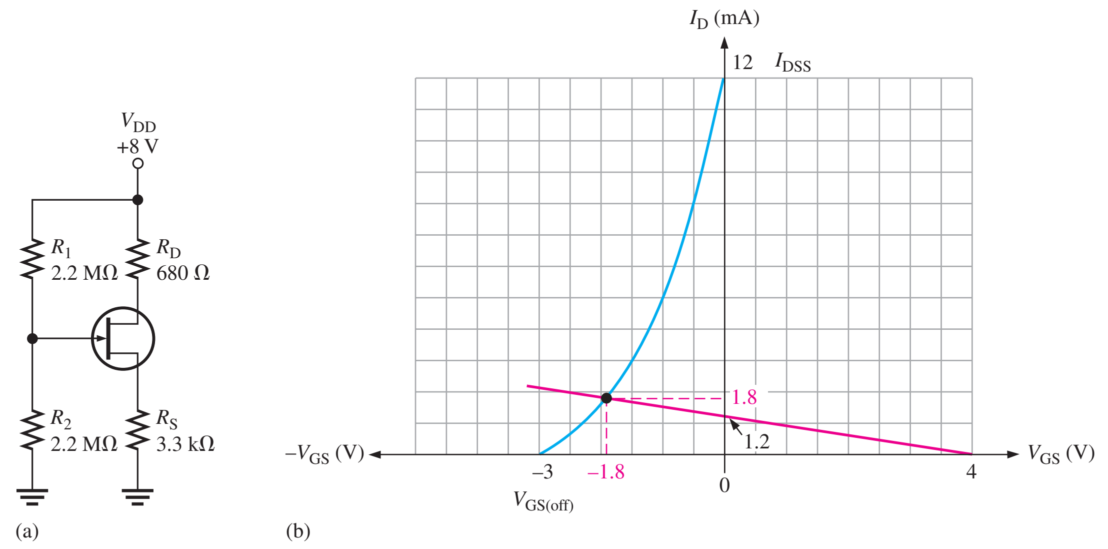


▲ **FIGURE 8–25**

Generalized dc load line (red) for a JFET with voltage-divider bias.

EXAMPLE 8–12

Determine the approximate Q-point for the JFET with voltage-divider bias in Figure 8–26(a), given that this particular device has a transfer characteristic curve as shown in Figure 8–26(b).


V_{DD}
+8 V
R_1
2.2 MΩ
R_D
680 Ω
R_2
2.2 MΩ
R_S
3.3 kΩ
(a)
I_D (mA)
12
I_{DSS}
1.8
1.2
$-V_{GS}$ (V)
V_{GS} (V)
−3
−1.8
0
4
$V_{GS(off)}$
(b)

▲ **FIGURE 8–26**

Solution First, establish the two points for the load line. For $I_D = 0$,

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{2.2\ \text{M}\Omega}{4.4\ \text{M}\Omega}\right)8\ \text{V} = 4\ \text{V}$$

The first point is at $I_D = 0$ and $V_{GS} = 4$ V. For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} = \frac{4\ \text{V}}{3.3\ \text{k}\Omega} = 1.2\ \text{mA}$$

The second point is at $I_D = 1.2$ mA and $V_{GS} = 0$.

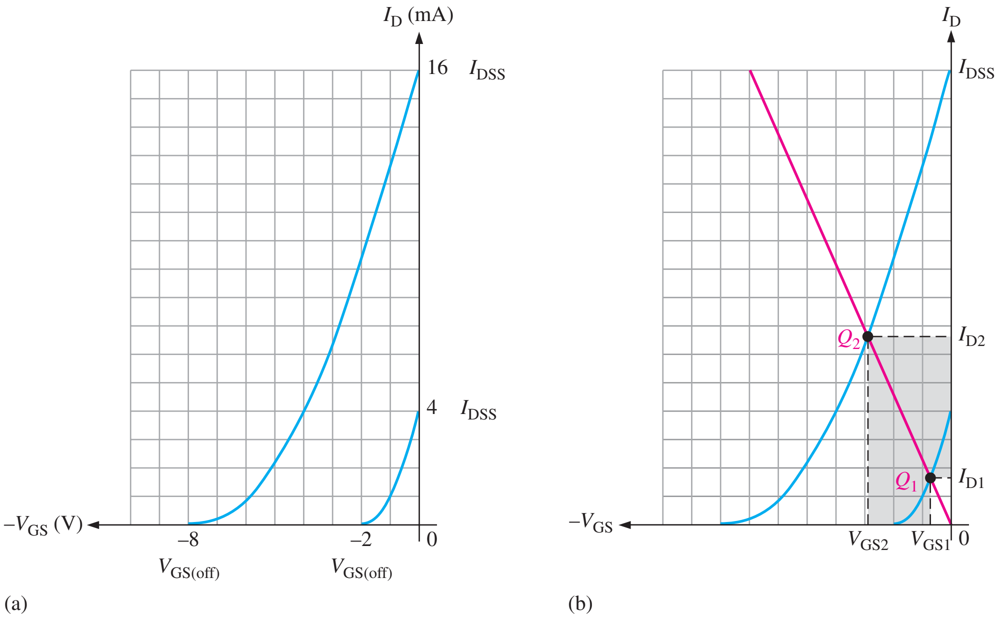
The load line is drawn in Figure 8–26(b), and the approximate Q-point values of $I_D \cong$ **1.8 mA** and $V_{GS} \cong$ **−1.8 V** are picked off the graph, as indicated.

Related Problem Change R_S to 4.7 kΩ and determine the Q-point for the circuit in Figure 8–26(a).

Open the Multisim file E08-12 in the Examples folder on the companion website. Measure the Q-point values of I_D and V_{GS} and see how they compare to the graphically determined values from the Related Problem.

Q-Point Stability

Unfortunately, the transfer characteristic of a JFET can differ considerably from one device to another of the same type. If, for example, a 2N5459 JFET is replaced in a given bias circuit with another 2N5459, the transfer characteristic curve can vary greatly, as illustrated in Figure 8–27(a). In this case, the maximum I_{DSS} is 16 mA and the minimum I_{DSS} is 4 mA. Likewise, the maximum $V_{GS(off)}$ is −8 V and the minimum $V_{GS(off)}$ is −2 V. This means that if you have a selection of 2N5459s and you randomly pick one out, it can have values anywhere within these ranges.

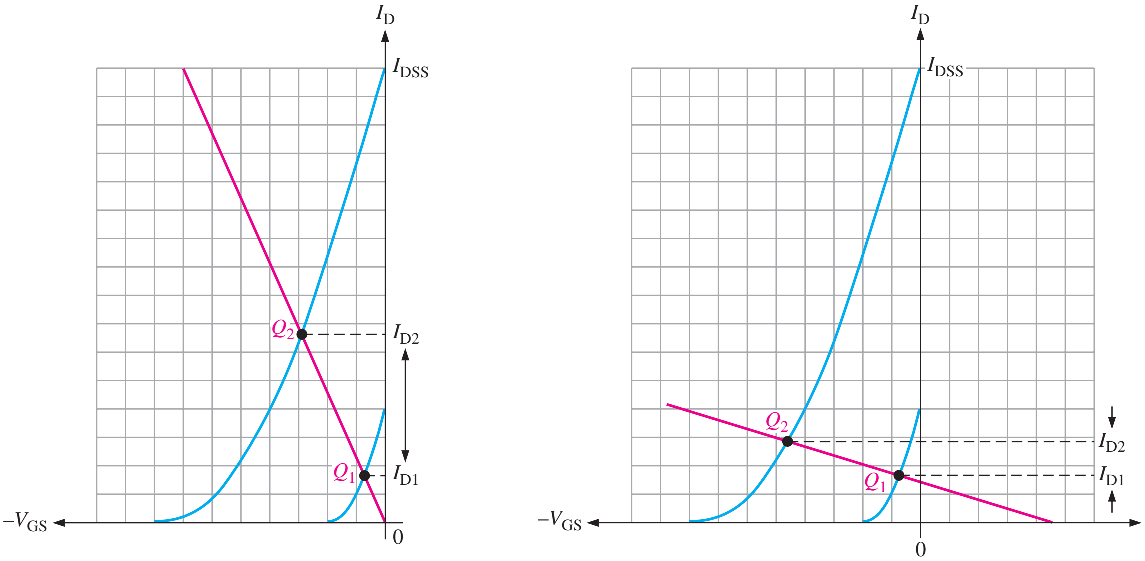


▲ **FIGURE 8–27**

Variation in the transfer characteristic of 2N5459 JFETs and the effect on the Q-point.

If a self-bias dc load line is drawn as illustrated in Figure 8–27(b), the same circuit using a 2N5459 can have a Q-point anywhere along the line from Q_1, the minimum bias point, to Q_2, the maximum bias point. Accordingly, the drain current can be any value between I_{D1} and I_{D2}, as shown by the shaded area. This means that the dc voltage at the drain can have a range of values depending on I_D. Also, the gate-to-source voltage can be any value between V_{GS1} and V_{GS2}, as indicated.

Figure 8–28 illustrates Q-point stability for a self-biased JFET and for a JFET with voltage-divider bias. With voltage-divider bias, the dependency of I_D on the range of Q-points is reduced because the slope of the load line is less than for self-bias for a given JFET. Although V_{GS} varies quite a bit for both self-bias and voltage-divider bias, I_D is much more stable with voltage-divider bias.



(a) Self-bias (b) Voltage-divider bias

▲ **FIGURE 8–28**

The change in I_D between the minimum and the maximum Q-points is much less for a JFET with voltage-divider bias than for a self-biased JFET.

Current-Source Bias

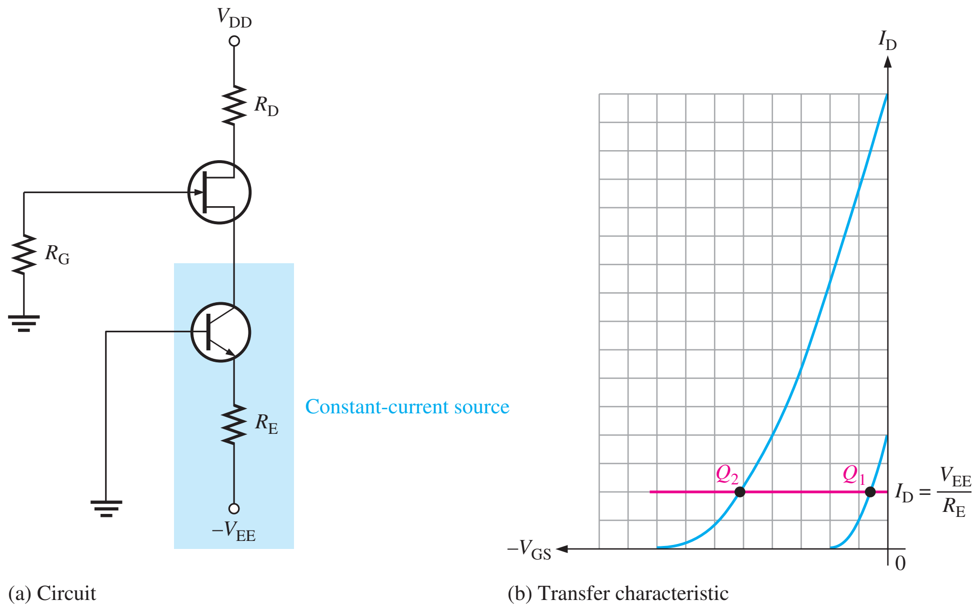
Current-source bias is a method for increasing the Q-point stability of a self-biased JFET by making the drain current essentially independent of V_{GS}. This is accomplished by using a constant-current source in series with the JFET source, as shown in Figure 8–29(a). In this circuit, a BJT acts as the constant-current source because its emitter current is essentially constant if $V_{EE} \gg V_{BE}$. A FET can also be used as a constant-current source.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \cong \frac{V_{EE}}{R_E}$$

Since $I_E \cong I_D$,

$$I_D \cong \frac{V_{EE}}{R_E}$$

As you can see in Figure 8–29(b), I_D remains constant for any transfer characteristic curve, as indicated by the horizontal load line.



(a) Circuit (b) Transfer characteristic

▲ **FIGURE 8–29**

Current-source bias.

EXAMPLE 8–13

A current-source bias circuit like Figure 8–29 has the following values: $V_{DD} = 9$ V, $V_{EE} = -6$ V, and $R_G = 10$ MΩ. To produce a 10 mA drain current and a 5 V drain voltage, determine the values of R_E and R_D.

Solution

$$R_E = \frac{V_{EE}}{I_D} = \frac{6\text{ V}}{10\text{ mA}} = \mathbf{600\ \Omega}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{9\text{ V} - 5\text{ V}}{10\text{ mA}} = \mathbf{400\ \Omega}$$

Related Problem If V_{DD} is increased to 12 V, how much does I_D change?

SECTION 8–3 CHECKUP

1. Should a *p*-channel JFET have a positive or a negative V_{GS}?
2. In a certain self-biased *n*-channel JFET circuit, $I_D = 8$ mA and $R_S = 1.0$ kΩ. Determine V_{GS}.
3. An *n*-channel JFET with voltage-divider bias has a gate voltage of 3 V and a source voltage of 5 V. Calculate V_{GS}.

8–4 THE OHMIC REGION

The **ohmic region** is the portion of the FET characteristic curves in which Ohm's law can be applied. When properly biased in the ohmic region, a JFET exhibits the properties of a variable resistance, where the value of resistance is controlled by V_{GS}.

After completing this section, you should be able to

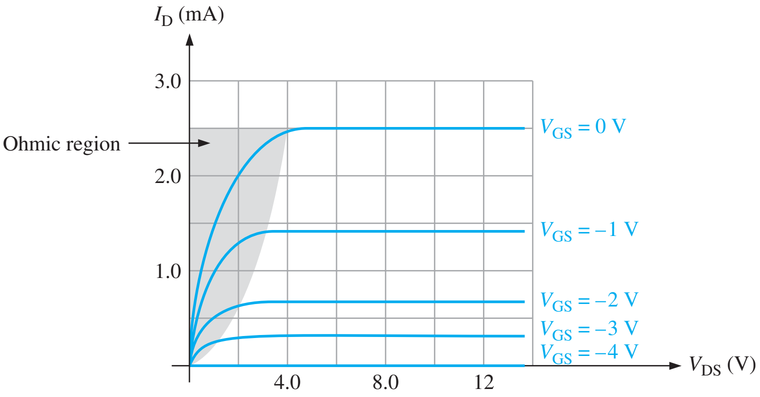
- ❑ **Discuss the ohmic region on a JFET characteristic curve**
    - ◆ Calculate slope and drain-to-source resistance
- ❑ Explain how a JFET can be used as a variable resistance
- ❑ Discuss JFET operation with the Q-point at the origin
    - ◆ Calculate transconductance

The ohmic region extends from the origin of the characteristic curves to the break point (where the active region begins) of the $V_{GS} = 0$ curve in a roughly parabolic shape, as shown on a typical set of curves in Figure 8–30. The characteristic curves in this region have a relatively constant slope for small values of I_D. The slope of the characteristic curve in the ohmic region is the dc drain-to-source conductance G_{DS} of the JFET.

$$\text{Slope} = G_{DS} \cong \frac{I_D}{V_{DS}}$$

Recall from your basic circuits course that resistance is the reciprocal of the conductance. Thus, the dc drain-to-source resistance is given by

$$R_{DS} = \frac{1}{G_{DS}} \cong \frac{V_{DS}}{I_D}$$



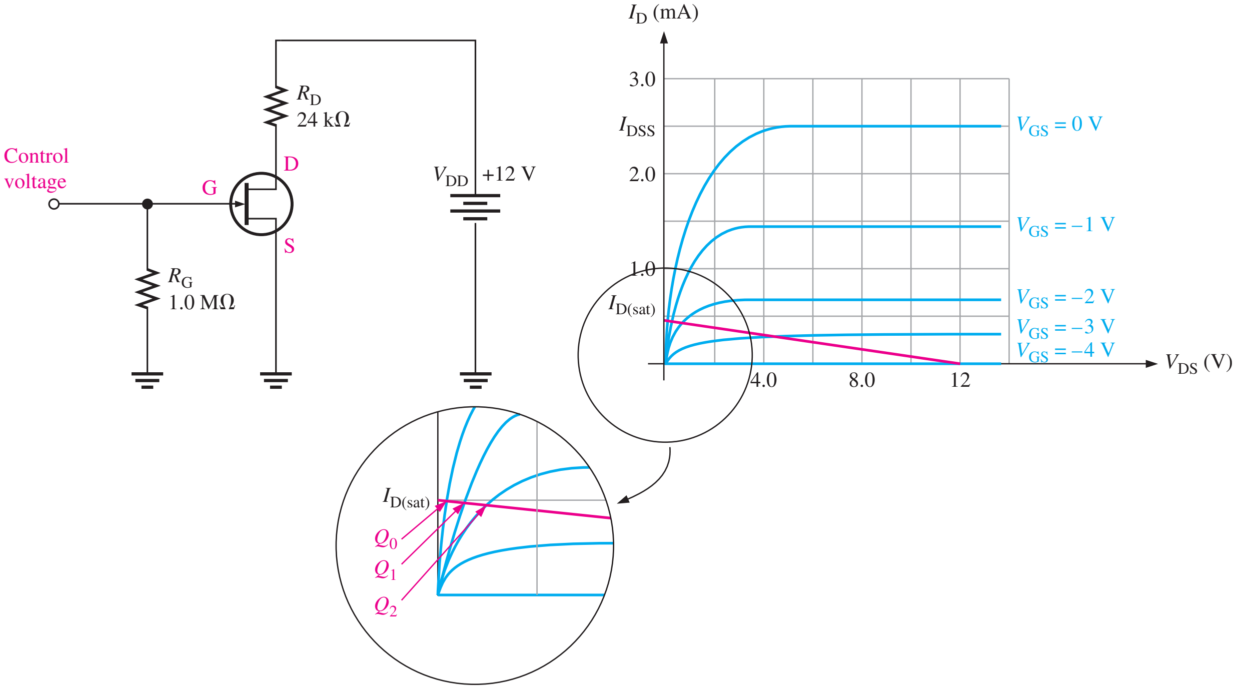
◄ FIGURE 8–30

The ohmic region is the shaded area.

The JFET as a Variable Resistance A JFET can be biased in either the active region or the ohmic region. JFETs are often biased in the ohmic region for use as a voltage-controlled variable resistor. The control voltage is V_{GS}, and it determines the resistance by varying the Q-point. To bias a JFET in the ohmic region, the dc load line must intersect the characteristic curve in the ohmic region, as illustrated in Figure 8–31. To do this in a way that allows V_{GS} to control R_{DS}, the dc saturation current is set for a value much less than I_{DSS} so that the load line intersects most of the characteristic curves in the ohmic region, as illustrated. In this case,

$$I_{D(sat)} = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{24\text{ k}\Omega} = 0.50\text{ mA}$$

Figure 8–31 shows the operating region expanded with three Q-points shown (Q_0, Q_1, and Q_2), depending on V_{GS}.



I_D (mA)
3.0
I_{DSS}
2.0
1.0
$I_{D(sat)}$
V_{GS} = 0 V
V_{GS} = −1 V
V_{GS} = −2 V
V_{GS} = −3 V
V_{GS} = −4 V
V_{DS} (V)
4.0
8.0
12
Control voltage
G
D
S
R_D 24 kΩ
R_G 1.0 MΩ
V_{DD} +12 V
$I_{D(sat)}$
Q_0
Q_1
Q_2

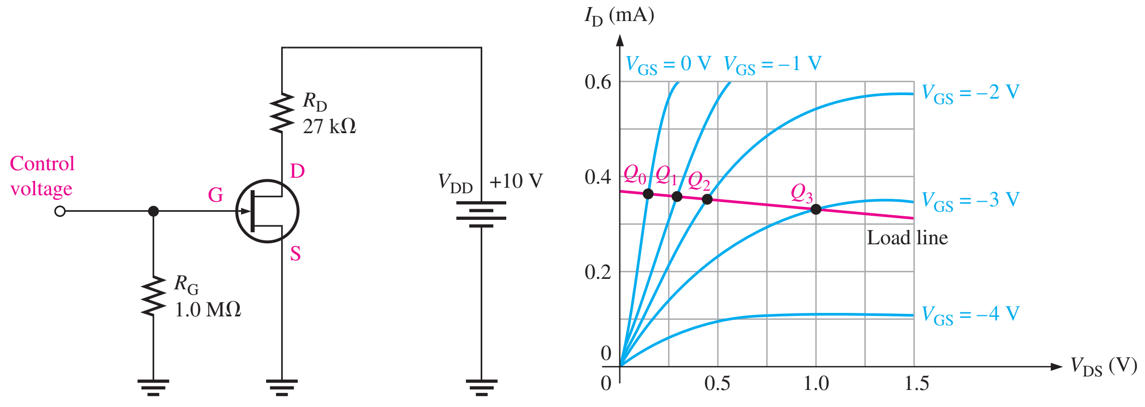
▲ **FIGURE 8–31**

The load line intersects the curves inside the ohmic region.

As you move along the load line in the ohmic region of Figure 8–31, the value of R_{DS} varies as the Q-point falls successively on curves with different slopes. The Q-point is moved along the load line by varying $V_{GS} = 0$ to $V_{GS} = -2$ V, in this case. As this happens, the slope of each successive curve is less than the previous one. A decrease in slope corresponds to less I_D and more V_{DS}, which implies an increase in R_{DS}. This change in resistance can be exploited in a number of applications where voltage control of a resistance is useful.

EXAMPLE 8–14

An *n*-channel JFET is biased in the ohmic region as shown in Figure 8–32. The graph shows an expanded section of the load line in the ohmic region. As V_{GS} is



Control voltage
G
D
S
R_D 27 kΩ
R_G 1.0 MΩ
V_{DD} +10 V
I_D (mA)
0.6
0.4
0.2
0
0
0.5
1.0
1.5
V_{DS} (V)
V_{GS} = 0 V
V_{GS} = −1 V
V_{GS} = −2 V
V_{GS} = −3 V
V_{GS} = −4 V
Q_0
Q_1
Q_2
Q_3
Load line

▲ **FIGURE 8–32**

varied from 0 V to −3 V as indicated, assume that the graph shows the following Q-point values:

Q_0: $I_D = 0.360\text{ mA}$, $V_{DS} = 0.13\text{ V}$
Q_1: $I_D = 0.355\text{ mA}$, $V_{DS} = 0.27\text{ V}$
Q_2: $I_D = 0.350\text{ mA}$, $V_{DS} = 0.42\text{ V}$
Q_3: $I_D = 0.33\text{ mA}$, $V_{DS} = 0.97\text{ V}$

Determine the range of R_{DS} as V_{GS} is varied from 0 V to −3 V.

Solution

$$Q_0\text{: } R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.13\text{ V}}{0.360\text{ mA}} = 361\ \Omega$$

$$Q_1\text{: } R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.27\text{ V}}{0.355\text{ mA}} = 760\ \Omega$$

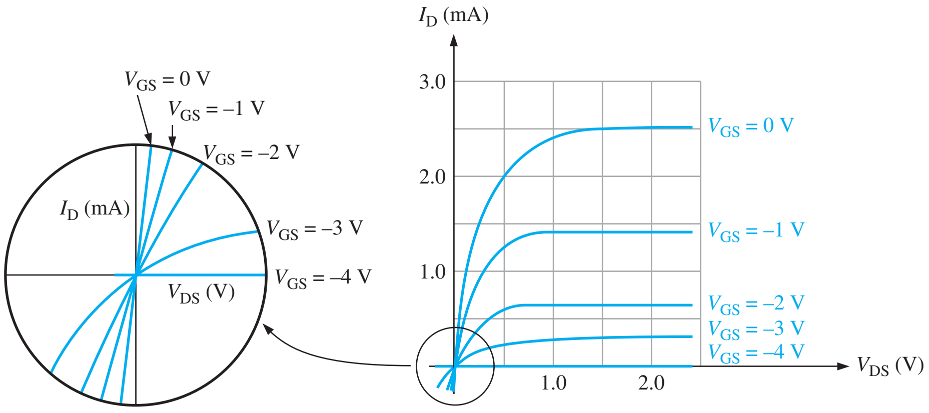
$$Q_2\text{: } R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.42\text{ V}}{0.27\text{ mA}} = 1.2\text{ k}\Omega$$

$$Q_3\text{: } R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.6\text{ V}}{0.26\text{ mA}} = 2.9\text{ k}\Omega$$

When V_{GS} is varied from 0 V to −3 V, **R_{DS} changes from 361 Ω to 2.9 kΩ.**

Related Problem If $I_{D(sat)}$ is reduced, what happens to the range of R_{DS} values?

Q-point at the Origin In certain amplifiers, you may want to change the resistance seen by the ac signal without affecting the dc bias in order to control the gain. Sometimes you will see a JFET used as a variable resistance in a circuit where both I_D and V_{DS} are set at 0, which means that the Q-point is at the origin. A Q-point at the origin is achieved by using a capacitor in the drain circuit of the JFET. This makes the dc quantities $V_{DS} = 0$ V and $I_D = 0$ mA, so the only variables are V_{GS} and I_d, the ac drain current. At the origin you have the ac drain current controlled by V_{GS}. As you learned earlier, transconductance is defined as a change in drain current for a given change in gate-to-source voltage. So, the key factor when you bias at the origin is the transconductance. Figure 8–33 shows the characteristic curves expanded at the origin. Notice that the ohmic region extends into the third quadrant.



▲ FIGURE 8–33

At the origin, where $V_{DS} = 0$ V and $I_D = 0$ mA, the formula for transconductance, introduced earlier in this chapter, is

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

where g_m is transconductance and g_{m0} is transconductance for $V_{GS} = 0$ V. g_{m0} can be calculated from the following equation, which was also given earlier:

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

EXAMPLE 8–15

For the characteristic curve in Figure 8–33, calculate the ac drain-to-source resistance for a JFET biased at the origin if $V_{GS} = -2$ V. Assume $I_{DSS} = 2.5$ mA and $V_{GS(off)} = -4$ V.

Solution First, find the transconductance for $V_{GS} = 0$ V.

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|} = \frac{2(2.5\text{ mA})}{4.0\text{ V}} = 1.25\text{ mS}$$

Next, calculate g_m at $V_{DS} = -2$ V.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = 1.25\text{ mS}\left(1 - \frac{-2\text{ V}}{-4\text{ V}}\right) = 0.625\text{ mS}$$

The ac drain-to-source resistance of the JFET is the reciprocal of the transconductance.

$$r'_{ds} = \frac{1}{g_m} = \frac{1}{0.625\text{ mS}} = 1.6\text{ k}\Omega$$

Related Problem What is the ac drain-to-source resistance if $V_{GS} = -1$ V?

SECTION 8–4 CHECKUP

1. For a certain Q-point in the ohmic region, $I_D = 0.3$ mA and $V_{DS} = 0.6$ V. What is the resistance of the JFET when it is biased at this Q-point?
2. How does the drain-to-source resistance change as V_{GS} becomes more negative?
3. For a JFET biased at the origin, $g_m = 0.850$ mS. Determine the corresponding ac resistance.

8–5 THE MOSFET

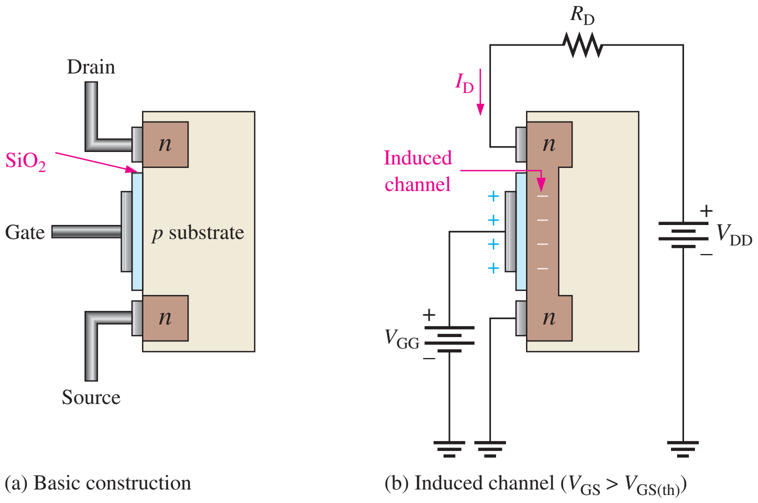
The **MOSFET** (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET, different from the JFET, has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are enhancement (E) and depletion (D). Of the two types, the enhancement MOSFET is more widely used. Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs).

After completing this section, you should be able to

- **Explain the operation of MOSFETs**
- Discuss the enhancement MOSFET (E-MOSFET)
  - Describe the structure ◆ Identify the symbols for E-MOSFET *n*-channel and *p*-channel devices
- Discuss the depletion MOSFET (D-MOSFET)
  - Describe the structure ◆ Discuss the depletion and enhancement modes
  - Identify the symbols for D-MOSFET *n*-channel and *p*-channel devices
- Discuss power MOSFETs
  - Describe LDMOSFET structure ◆ Describe VMOSFET structure
  - Describe TMOSFET structure
- Describe the dual-gate MOSFET
  - Identify the symbols for dual-gate D-MOSFETs and E-MOSFETs

Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates *only* in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET, which is discussed next, in that it has no structural channel. Notice in Figure 8–34(a) that the substrate extends completely to the SiO_2 layer. For an *n*-channel device, a positive gate voltage above a threshold value *induces* a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure 8–34(b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.



(a) Basic construction (b) Induced channel ($V_{GS} > V_{GS(th)}$)

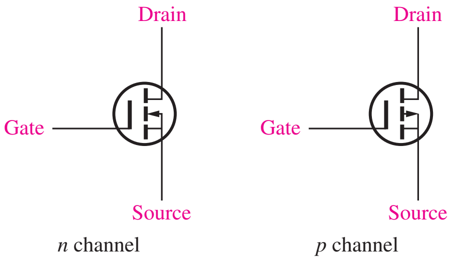
▲ FIGURE 8–34

Representation of the basic E-MOSFET construction and operation (*n*-channel).

The schematic symbols for the *n*-channel and *p*-channel E-MOSFETs are shown in Figure 8–35. The broken lines symbolize the absence of a physical channel. An inward-pointing substrate arrow is for *n* channel, and an outward-pointing arrow is for *p* channel. Some E-MOSFET devices have a separate substrate connection.

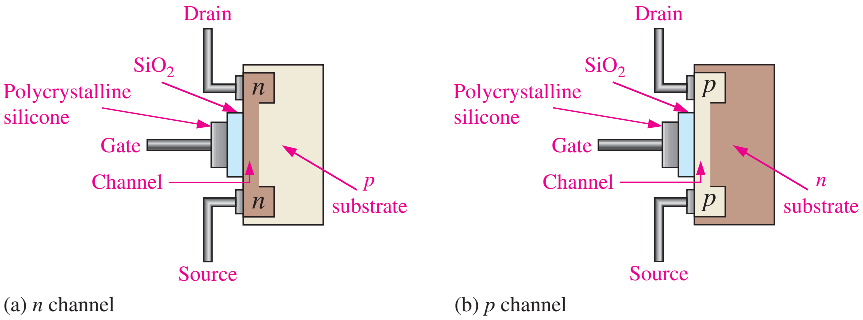
▶ FIGURE 8–35

E-MOSFET schematic symbols.



Depletion MOSFET (D-MOSFET)

Another type of MOSFET is the depletion MOSFET (D-MOSFET), and Figure 8–36 illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both *n*-channel and *p*-channel devices are shown in the figure. We will use the *n*-channel device to describe the basic operation. The *p*-channel operation is the same, except the voltage polarities are opposite those of the *n*-channel.



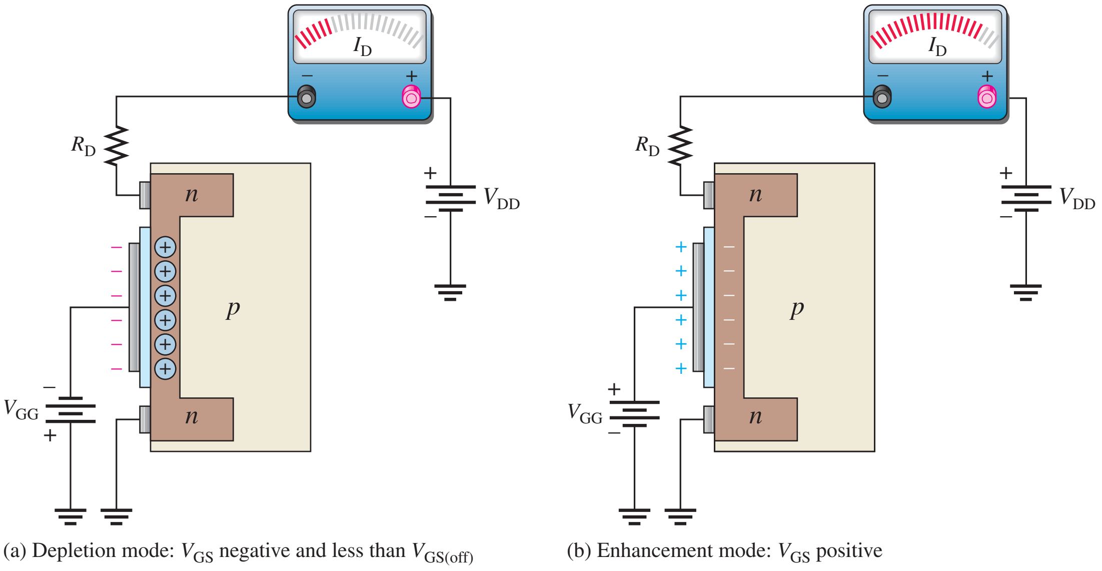
(a) *n* channel (b) *p* channel

▲ FIGURE 8–36

Representation of the basic structure of D-MOSFETs.

The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode—and is sometimes called a *depletion/enhancement MOSFET*. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The *n*-channel MOSFET operates in the **depletion** mode when a negative gate-to-source voltage is applied and in the **enhancement** mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.

Depletion Mode Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the *n* channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of *n*-channel electrons. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure 8–37(a). Like the *n*-channel JFET, the *n*-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.



(a) Depletion mode: V_{GS} negative and less than $V_{GS(off)}$ (b) Enhancement mode: V_{GS} positive

FIGURE 8–37

Operation of *n*-channel D-MOSFET.

Enhancement Mode With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure 8–37(b).

D-MOSFET Symbols The schematic symbols for both the *n*-channel and the *p*-channel depletion MOSFETs are shown in Figure 8–38. The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin.

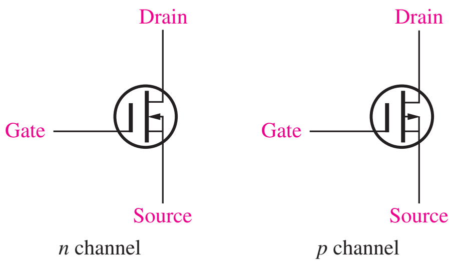


FIGURE 8–38

D-MOSFET schematic symbols.

Power MOSFET Structures

The conventional enhancement MOSFETs have a long thin lateral channel as shown in the structural view in Figure 8–39. This results in a relatively high drain-to-source resistance and limits the E-MOSFET to low power applications. When the gate is positive, the channel is formed close to the gate between the source and the drain, as shown.

Laterally Diffused MOSFET (LDMOSFET) The LDMOSFET has a lateral channel structure and is a type of enhancement MOSFET designed for power applications. This device has a shorter channel between drain and source than does the conventional E-MOSFET. The shorter channel results in lower resistance, which allows higher current and voltage.

FYI

A new type of field-effect transistor uses a fin-like structure instead of the conventional flat silicon structure. It is much smaller than the conventional silicon transistors. The fins are made from a semiconductor material called indium-gallium-arsenide instead of silicon. In addition to making computer chips much smaller in size, the finFET can operate many times faster than conventional FETs.

▶ FIGURE 8–39

Cross section of conventional E-MOSFET structure. Channel is shown as white area.

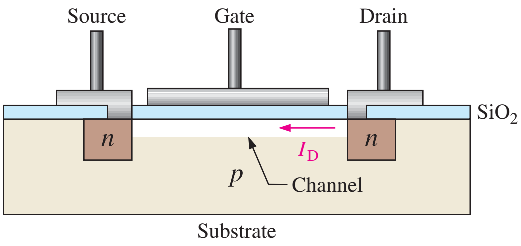
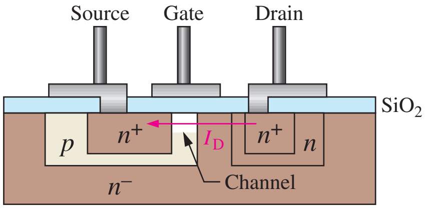


Figure 8–40 shows the basic structure of an LDMOSFET. When the gate is positive, a very short *n* channel is induced in the *p* layer between the lightly doped source and the n^- region. There is current between the drain and source through the *n* regions and the induced channel as indicated.

▶ FIGURE 8–40

Cross section of LDMOSFET lateral channel structure.

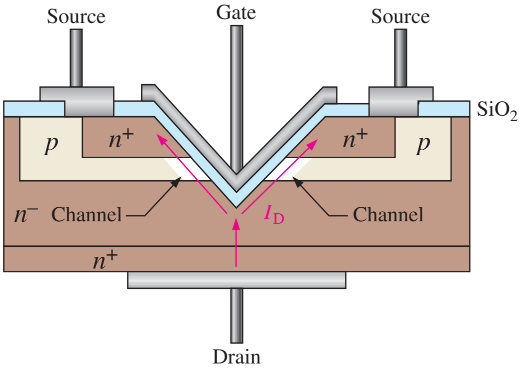


VMOSFET The V-groove MOSFET is another example of the conventional E-MOSFET designed to achieve higher power capability by creating a shorter and wider channel with less resistance between the drain and source using a vertical channel structure. The shorter, wider channels allow for higher currents and, thus, greater power dissipation. Frequency response is also improved.

The VMOSFET has two source connections, a gate connection on top, and a drain connection on the bottom, as shown in Figure 8–41. The channel is induced vertically along both sides of the V-shaped groove between the drain (n^+ substrate where n^+ means a higher doping level than n^-) and the source connections. The channel length is set by the thickness of the layers, which is controlled by doping densities and diffusion time rather than by mask dimensions.

▶ FIGURE 8–41

Cross section of VMOSFET vertical channel structure.



TMOSFET The vertical channel structure of the TMOSFET is illustrated in Figure 8–42. The gate structure is embedded in a silicon dioxide layer, and the source contact is continuous over the entire surface area. The drain is on the bottom. TMOSFET achieves greater packing density than VMOSFET, while retaining the short vertical channel advantage.

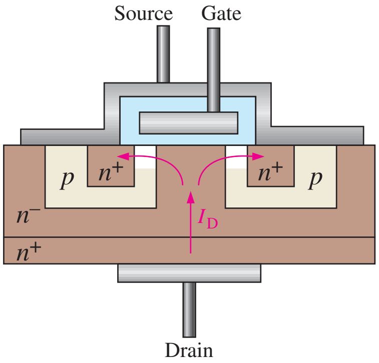
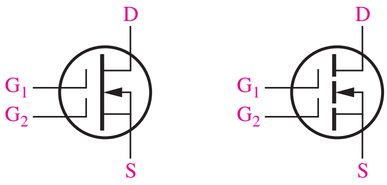


FIGURE 8–42

Cross section of TMOSFET vertical channel structure.

Dual-Gate MOSFETs

The dual-gate MOSFET can be either a depletion or an enhancement type. The only difference is that it has two gates, as shown in Figure 8–43. As previously mentioned, one drawback of a FET is its high input capacitance, which restricts its use at higher frequencies. By using a dual-gate device, the input capacitance is reduced, thus making the device useful in high-frequency RF amplifier applications. Another advantage of the dual-gate arrangement is that it allows for an automatic gain control (AGC) input in RF amplifiers. Another application is demonstrated in the Application Activity where the bias on the second gate is used to adjust the transconductance curve.



(a) D-MOSFET (b) E-MOSFET

FIGURE 8–43

Dual-gate *n*-channel MOSFET symbols.

SECTION 8–5 CHECKUP

1. Name the two basic types of MOSFETs.
2. If the gate-to-source voltage in an *n*-channel E-MOSFET is made more positive, does the drain current increase or decrease?
3. If the gate-to-source voltage in an *n*-channel depletion MOSFET is made more negative, does the drain current increase or decrease?

8–6 MOSFET CHARACTERISTICS AND PARAMETERS

Much of the discussion concerning JFET characteristics and parameters applies equally to MOSFETs. In this section, MOSFET parameters are discussed.

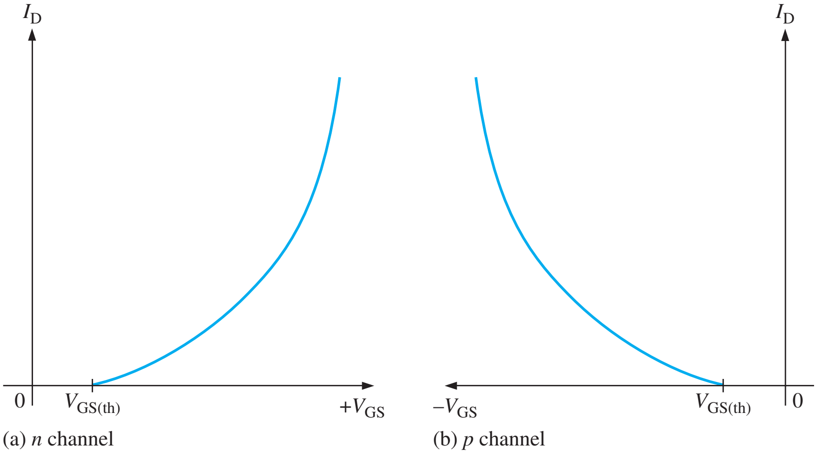
After completing this section, you should be able to

- **Discuss and apply MOSFET parameters**
- Describe an E-MOSFET transfer characteristic curve
  - Calculate drain current using an equation for the curve
  - Use an E-MOSFET datasheet

- ❑ Describe a D-MOSFET transfer characteristic curve
  - ◆ Calculate drain current using an equation for the curve
- ❑ Discuss the handling precautions for MOSFETS
  - ◆ Explain why MOSFETs must be handled properly ◆ List the precautions

E-MOSFET Transfer Characteristic

The E-MOSFET uses only channel enhancement. Therefore, an *n*-channel device requires a positive gate-to-source voltage, and a *p*-channel device requires a negative gate-to-source voltage. Figure 8–44 shows the general transfer characteristic curves for both types of E-MOSFETs. As you can see, there is no drain current when $V_{GS} = 0$. Therefore, the E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET. Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the *threshold voltage,* $V_{GS(th)}$.



(a) *n* channel (b) *p* channel

▲ FIGURE 8–44

E-MOSFET general transfer characteristic curves.

The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E-MOSFET transfer characteristic curve is

Equation 8–4

$$\mathbf{I_D = K(V_{GS} - V_{GS(th)})^2}$$

The constant K depends on the particular MOSFET and can be determined from the datasheet by taking the specified value of I_D, called $I_{D(on)}$, at the given value of V_{GS} and substituting the values into Equation 8–4 as illustrated in Example 8–16.

EXAMPLE 8–16

The datasheet (see www.fairchild.com) for a 2N7002 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

Solution First, solve for K using Equation 8–4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

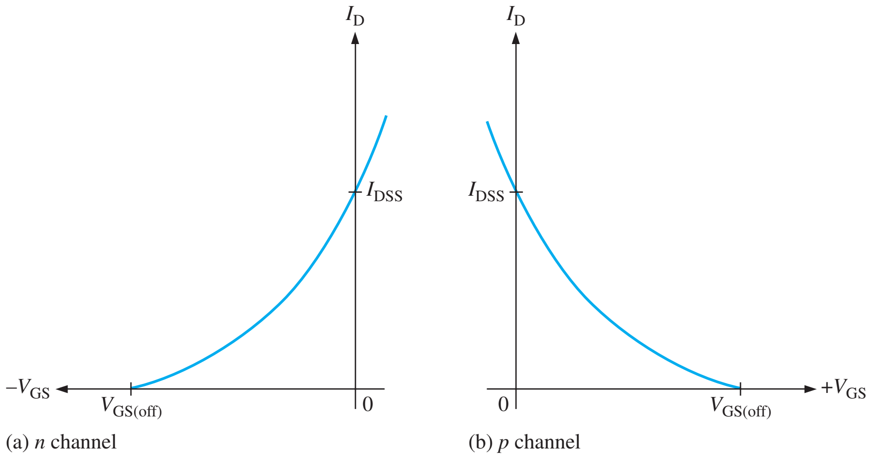
$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

Related Problem The datasheet for an E-MOSFET gives $I_{D(on)} = 100$ mA at $V_{GS} = 8$ V and $V_{GS(th)} = 4$ V. Find I_D when $V_{GS} = 6$ V.

D-MOSFET Transfer Characteristic

As previously discussed, the D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure 8–45 for both *n*-channel and *p*-channel MOSFETs. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_P$.

The square-law expression in Equation 8–1 for the JFET curve also applies to the D-MOSFET curve, as Example 8–17 demonstrates.



(a) *n* channel (b) *p* channel

FIGURE 8–45

D-MOSFET general transfer characteristic curves.

EXAMPLE 8–17

For a certain D-MOSFET, $I_{DSS} = 10$ mA and $V_{GS(off)} = -8$ V.

(a) Is this an *n*-channel or a *p*-channel?

(b) Calculate I_D at $V_{GS} = -3$ V.

(c) Calculate I_D at $V_{GS} = +3$ V.

Solution **(a)** The device has a negative $V_{GS(off)}$; therefore, it is an ***n*-channel** MOSFET.

(b) $$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left(1 - \frac{-3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{3.91\text{ mA}}$$

(c) $$I_D \cong (10\text{ mA})\left(1 - \frac{+3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{18.9\text{ mA}}$$

Related Problem For a certain D-MOSFET, $I_{DSS} = 18$ mA and $V_{GS(off)} = +10$ V.

(a) Is this an *n*-channel or a *p*-channel?

(b) Determine I_D at $V_{GS} = +4$ V.

(c) Determine I_D at $V_{GS} = -4$ V.

Handling Precautions

All MOS devices are subject to damage from electrostatic discharge (ESD). Because the gate of a MOSFET is insulated from the channel, the input resistance is extremely high (ideally infinite). The gate leakage current, I_{GSS}, for a typical MOSFET is in the pA range, whereas the gate reverse current for a typical JFET is in the nA range. The input capacitance results from the insulated gate structure. Excess static charge can be accumulated because the input capacitance combines with the very high input resistance and can result in damage to the device. To avoid damage from ESD, certain precautions should be taken when handling MOSFETs:

1. Carefully remove MOSFET devices from their packaging. They are shipped in conductive foam or special foil conductive bags. Usually they are shipped with a wire ring around the leads, which is removed just prior to installing the MOSFET in a circuit.
2. All instruments and metal benches used in assembly or test should be connected to earth ground (round or third prong of 110 V wall outlets).
3. The assembler's or handler's wrist should be connected to a commercial grounding strap, which has a high-value series resistor for safety. The resistor prevents accidental contact with voltage from becoming lethal.
4. Never remove a MOS device (or any other device, for that matter) from the circuit while the power is on.
5. Do not apply signals to a MOS device while the dc power supply is off.

SECTION 8–6 CHECKUP

1. What is the major difference in construction of the D-MOSFET and the E-MOSFET?
2. Name two parameters of an E-MOSFET that are not specified for D-MOSFETs?
3. What is ESD?

8–7 MOSFET BIASING

Three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias. Biasing is important in FET amplifiers, which you will study in the next chapter.

After completing this section, you should be able to

- **Describe and analyze MOSFET bias circuits**
- Analyze E-MOSFET bias
  - Discuss and analyze voltage-divider bias
  - Discuss and analyze drain-feedback bias
- Analyze D-MOSFET bias
  - Discuss and analyze zero bias

E-MOSFET Bias

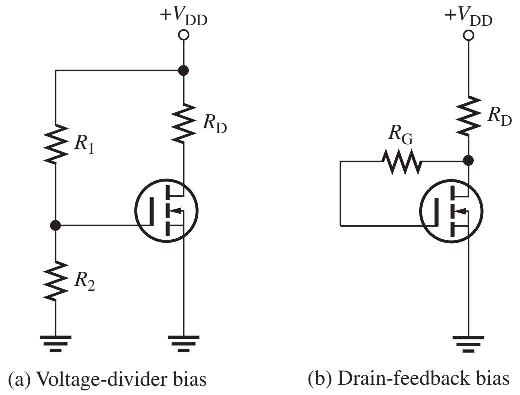
Because E-MOSFETs must have a V_{GS} greater than the threshold value, $V_{GS(th)}$, zero bias cannot be used. Figure 8–46 shows two ways to bias an E-MOSFET (D-MOSFETs can also be biased using these methods). An *n*-channel device is used for purposes of illustration. In either the voltage-divider or drain-feedback bias arrangement, the purpose is to make the gate voltage more positive than the source by an amount exceeding $V_{GS(th)}$. Equations for the analysis of the voltage-divider bias in Figure 8–46(a) are as follows:

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

where $I_D = K(V_{GS} - V_{GS(th)})^2$ from Equation 8–4.

In the drain-feedback bias circuit in Figure 8–46(b), there is negligible gate current and, therefore, no voltage drop across R_G. This makes $V_{GS} = V_{DS}$.



(a) Voltage-divider bias (b) Drain-feedback bias

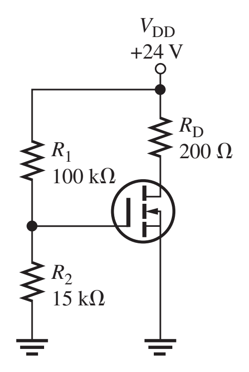
FIGURE 8–46

Common E-MOSFET biasing arrangements.

EXAMPLE 8–18

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure 8–47. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 2$ V.

FIGURE 8–47



Solution For the E-MOSFET in Figure 8–47, the gate-to-source voltage is

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\text{ k}\Omega}{115\text{ k}\Omega}\right)24\text{ V} = \mathbf{3.13\ V}$$

To determine V_{DS}, first find K using the minimum value of $I_{D(on)}$ and the specified voltage values.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = \frac{200\text{ mA}}{4\text{ V}^2} = 50\text{ mA/V}^2$$

Now calculate I_D for $V_{GS} = 3.13$ V.

$$\begin{aligned} I_D &= K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(3.13\text{ V} - 2\text{ V})^2 \\ &= (50\text{ mA/V}^2)(1.13\text{ V})^2 = 63.8\text{ mA} \end{aligned}$$

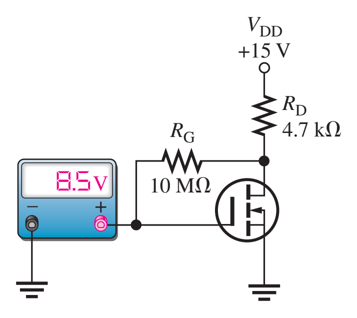
Finally, calculate V_{DS}.

$$V_{DS} = V_{DD} - I_DR_D = 24\text{ V} - (63.8\text{ mA})(200\ \Omega) = \mathbf{11.2\ V}$$

Related Problem Determine V_{GS} and V_{DS} for the circuit in Figure 8–47 given $I_{D(on)} = 100$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 3$ V.

EXAMPLE 8–19 Determine the amount of drain current in Figure 8–48. The MOSFET has a $V_{GS(th)} = 3$ V.

▶ FIGURE 8–48



Solution The meter indicates $V_{GS} = 8.5$ V. Since this is a drain-feedback configuration, $V_{DS} = V_{GS} = 8.5$ V.

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{15\text{ V} - 8.5\text{ V}}{4.7\text{ k}\Omega} = \mathbf{1.38\ mA}$$

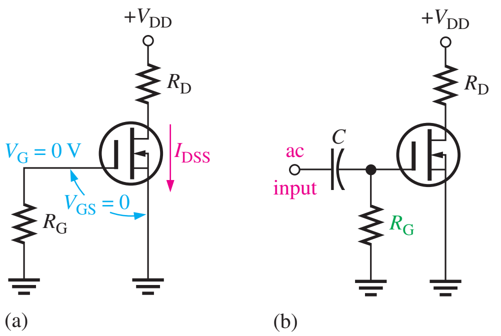
Related Problem Determine I_D if the meter in Figure 8–48 reads 5 V.

D-MOSFET Bias

Recall that D-MOSFETs can be operated with either positive or negative values of V_{GS}. A simple bias method is to set $V_{GS} = 0$ so that an ac signal at the gate varies the gate-to-source voltage above and below this 0 V bias point. A MOSFET with zero bias is shown in Figure 8–49(a). Since $V_{GS} = 0$, $I_D = I_{DSS}$ as indicated. The drain-to-source voltage is expressed as follows:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The purpose of R_G is to accommodate an ac signal input by isolating it from ground, as shown in Figure 8–49(b). Since there is no dc gate current, R_G does not affect the zero gate-to-source bias.



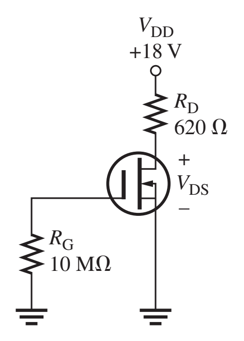
◀ **FIGURE 8–49**

A zero-biased D-MOSFET.

EXAMPLE 8–20

Determine the drain-to-source voltage in the circuit of Figure 8–50. The MOSFET datasheet gives $V_{GS(off)} = -8$ V and $I_{DSS} = 12$ mA.

▶ **FIGURE 8–50**



Solution Since $I_D = I_{DSS} = 12$ mA, the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_{DSS}R_D = 18\text{ V} - (12\text{ mA})(620\ \Omega) = \mathbf{10.6\ V}$$

Related Problem Find V_{DS} in Figure 8–50 when $V_{GS(off)} = -10$ V and $I_{DSS} = 20$ mA.

SECTION 8–7 CHECKUP

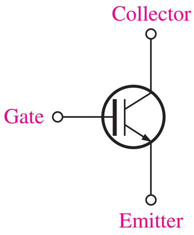
1. For a D-MOSFET biased at $V_{GS} = 0$, is the drain current equal to zero, I_{GSS}, or I_{DSS}?
2. For an *n*-channel E-MOSFET with $V_{GS(th)} = 2$ V, V_{GS} must be in excess of what value in order to conduct?

8–8 THE IGBT

The IGBT (insulated-gate bipolar transistor) combines features from both the MOSFET and the BJT that make it useful in high-voltage and high-current switching applications. The IGBT has largely replaced the MOSFET and the BJT in many of these applications.

After completing this section, you should be able to

- **Discuss the IGBT**
  - Compare the IGBT to the MOSFET and the BJT
  - Identify the IGBT symbol
- Describe IGBT operation
  - Explain how an IGBT is turned on and off
  - Discuss and analyze drain-feedback bias
  - Describe the IGBT equivalent circuit



▲ **FIGURE 8–51**

A symbol for the IGBT (insulated-gate bipolar transistor).

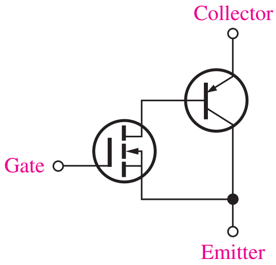
The **IGBT** is a device that has the output conduction characteristics of a BJT but is voltage controlled like a MOSFET; it is an excellent choice for many high-voltage switching applications. The IGBT has three terminals: gate, collector, and emitter. One common circuit symbol is shown in Figure 8–51. As you can see, it is similar to the BJT symbol except there is an extra bar representing the gate structure of a MOSFET rather than a base.

The IGBT has MOSFET input characteristics and BJT output characteristics. BJTs are capable of higher currents than FETs, but MOSFETs have no gate current because of the insulated gate structure. IGBTs exhibit a lower saturation voltage than MOSFETs and have about the same saturation voltage as BJTs. IGBTs are superior to MOSFETs in some applications because they can handle high collector-to-emitter voltages exceeding 200 V and exhibit less saturation voltage when they are in the *on* state. IGBTs are superior to BJTs in some applications because they can switch faster. In terms of switching speed, MOSFETs switch fastest, then IGBTs, followed by BJTs, which are slowest. A general comparison of IGBTs, MOSFETs, and BJTs is given in Table 8–1.

▶ **TABLE 8–1**

Comparison of several device features for switching applications.

FEATURES	IGBT	MOSFET	BJT
Type of input drive	Voltage	Voltage	Current
Input resistance	High	High	Low
Operating frequency	Medium	High	Low
Switching speed	Medium	Fast (ns)	Slow (μs)
Saturation voltage	Low	High	Low



▲ **FIGURE 8–52**

Simplified equivalent circuit for an IGBT.

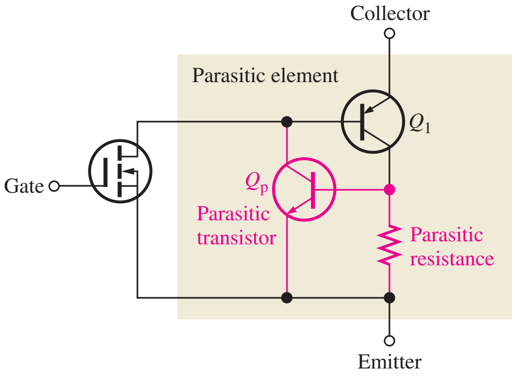
Operation

The IGBT is controlled by the gate voltage just like a MOSFET. Essentially, an IGBT can be thought of as a voltage-controlled BJT, but with faster switching speeds. Because it is controlled by voltage on the insulated gate, the IGBT has essentially no input current and does not load the driving source. A simplified equivalent circuit for an IGBT is shown in Figure 8–52. The input element is a MOSFET, and the output element is a bipolar transistor. When the gate voltage with respect to the emitter is less than a threshold voltage, V_{thresh}, the device is turned off. The device is turned on by increasing the gate voltage to a value exceeding the threshold voltage.

The *npnp* structure of the IGBT forms a parasitic transistor and an inherent parasitic resistance within the device, as shown in red in Figure 8–53. These parasitic components have no effect during normal operation. However, if the maximum collector current is exceeded under certain conditions, the parasitic transistor, Q_p can turn on. If Q_p turns on, it

▶ **FIGURE 8–53**

Parasitic components of an IGBT that can cause latch-up.



effectively combines with Q_1 to form a parasitic element, as shown in Figure 8–53, in which a latchup condition can occur. In latch-up, the device will stay on and cannot be controlled by the gate voltage. Latch-up can be avoided by always operating within the specified limits of the device.

SECTION 8–8 CHECKUP

1. What does IGBT stand for?
2. What is a major application area for IGBTs?
3. Name an advantage of an IGBT over a power MOSFET.
4. Name an advantage of an IGBT over a power BJT.
5. What is latch-up?

8–9 TROUBLESHOOTING

In this section, some common faults that may be encountered in FET circuits and the probable causes for each fault are discussed.

After completing this section, you should be able to

- **Troubleshoot FET circuits**
- Determine faults in self-biased JFET circuits
- Determine faults in MOSFET circuits
  - ◆ Troubleshoot a D-MOSFET with zero bias
  - ◆ Troubleshoot an E-MOSFET with voltage-divider bias

Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections of Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

Faults in Self-Biased JFET Circuits

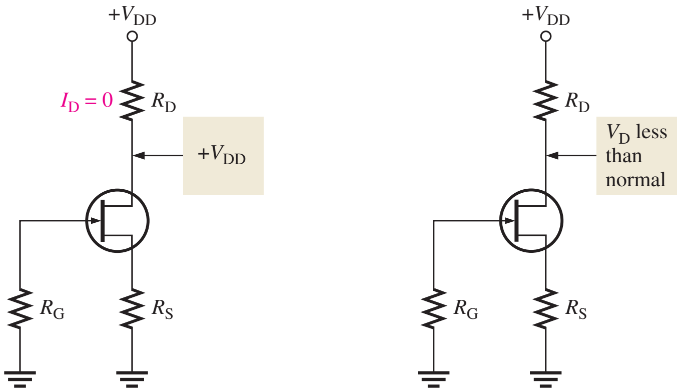
Symptom 1: $V_D = V_{DD}$ For this condition, the drain current must be zero because there is no voltage drop across R_D, as illustrated in Figure 8–54(a). As in any circuit, it is good troubleshooting practice to first check for obvious problems such as open or poor connections, as well as charred resistors. Next, disconnect power and measure suspected resistors for opens. If these are okay, the JFET is probably bad. Any of the following faults can produce this symptom:

1. No ground connection at R_S
2. R_S open
3. Open drain lead connection
4. Open source lead connection
5. FET internally open between drain and source

Symptom 2: V_D Significantly Less Than Normal For this condition, unless the supply voltage is lower than it should be, the drain current must be larger than normal because the

FIGURE 8–54

Two symptoms in a self-biased JFET circuit.



(a) *Symptom 1*: Drain voltage equal to supply voltage

(b) *Symptom 2*: Drain voltage less than normal

drop across R_D is too much. Figure 8–54(b) indicates this situation. This symptom can be caused by any of the following:

1. Open R_G
2. Open gate lead
3. FET internally open at gate

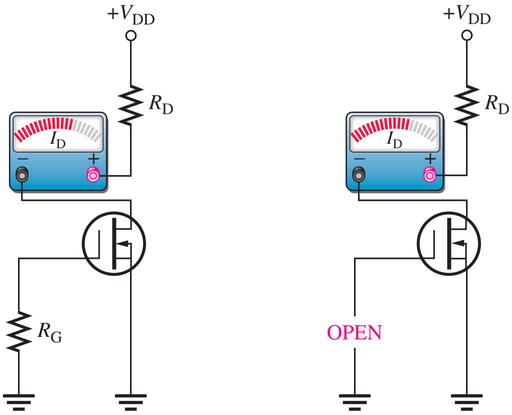
Any of these three faults will cause the depletion region in the JFET to disappear and the channel to widen so that the drain current is limited only by R_D, R_S, and the small channel resistance.

Faults in D-MOSFET and E-MOSFET Circuits

One fault that is difficult to detect is when the gate opens in a zero-biased D-MOSFET. In a zero-biased D-MOSFET, the gate-to-source voltage ideally remains zero when an open occurs in the gate circuit; thus, the drain current doesn't change, and the bias appears normal, as indicated in Figure 8–55. However, static charge as a result of the open may cause I_D to behave irratically.

FIGURE 8–55

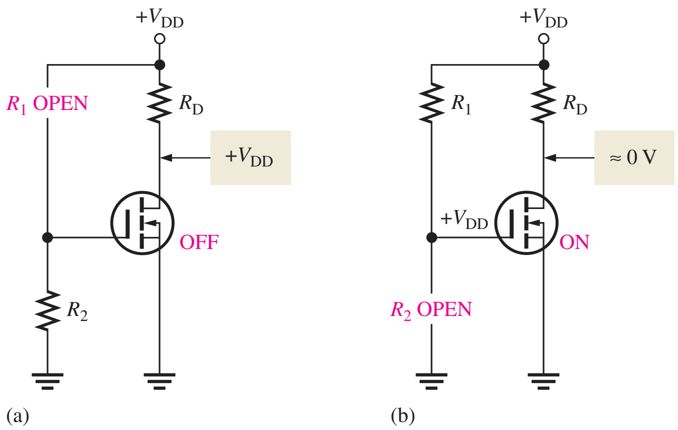
An open fault in the gate circuit of a D-MOSFET causes no change in I_D.



(a) Normal operation

(b) Gate circuit open (can be either external or internal)

In an E-MOSFET circuit with voltage-divider bias, an open R_1 makes the gate voltage zero. This causes the transistor to be off and act like an open switch because a gate-to-source threshold voltage greater than zero is required to turn the device on. This condition is illustrated in Figure 8–56(a). If R_2 opens, the gate is at $+V_{DD}$ and the channel resistance is very low so the device approximates a closed switch. The drain current is limited only by R_D. This condition is illustrated in Figure 8–56(b).



(a) (b)

FIGURE 8–56

Failures in an E-MOSFET circuit with voltage-divider bias.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

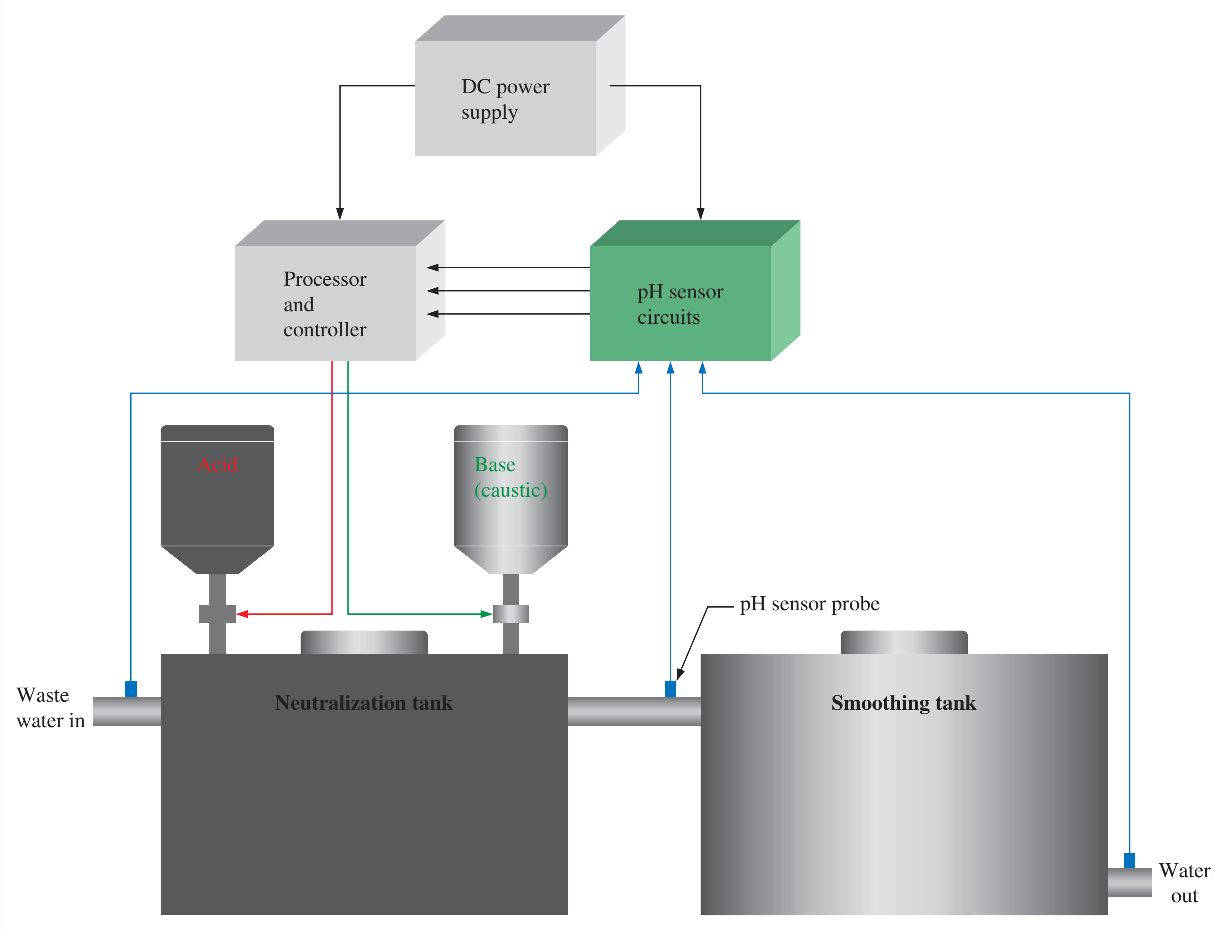
1. Multisim file TSE08-01
2. Multisim file TSE08-02
3. Multisim file TSE08-03
4. Multisim file TSE08-04

SECTION 8–9 CHECKUP

1. In a self-biased JFET circuit, the drain voltage equals V_{DD}. If the JFET is okay, what are other possible faults?
2. Why doesn't the drain current change when an open occurs in the gate circuit of a zero-biased D-MOSFET circuit?
3. If the gate of an E-MOSFET becomes shorted to ground in a circuit with voltage-divider bias, what is the drain voltage?

Application Activity: *pH Sensor Circuit*

This application involves electronic instrumentation in a waste water treatment facility. The system controls the amount of acid and base reagent added to waste water in order to neutralize it. The diagram of the waste water neutralization pH system is shown in Figure 8–57. The system measures and controls the pH of the water, which is a measure of the degree of acidity or alkalinity. The pH scale ranges from 0 for the strongest acids through 7 for neutral solutions and up to 14 for the strongest bases (caustics). Typically, the pH for waste water ranges from greater than 2 and less than 11. The pH of the water is measured by sensor probes at the inlets and outlets of the tanks. The processor and controller unit uses the inputs from the pH sensor circuits to adjust the amount of acid or base introduced into the neutralization tank. The pH should be 7 at the outlet of the smoothing tank.


DC power supply
Processor and controller
pH sensor circuits
Acid
Base (caustic)
pH sensor probe
Waste water in
Neutralization tank
Smoothing tank
Water out

▲ FIGURE 8–57

Simplified waste water pH neutralization system.

Generally, waste water treatment is done in three steps as follows:

- *Primary treatment* Collecting, screening, and initial storage
- *Secondary treatment* Removal of solids and the majority of contaminants using filters, coagulation, flocculation, and membranes
- *Tertiary treatment* Polishing, pH adjustment, carbon treatment to remove taste and smells, disinfection, and temporary storage to allow the disinfecting agent to work

In this application, we are focusing on the process of pH adjustment in the tertiary stage of treatment.

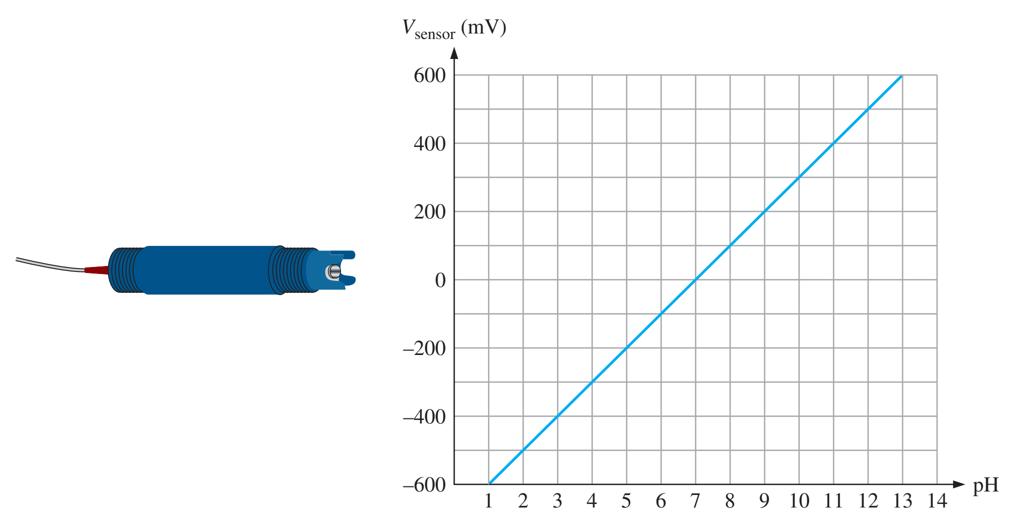
The Sensor Circuit

There are three identical pH sensor circuits, one for each of the inlet/outlets indicated in Figure 8–57. The pH sensor produces a small voltage (mV) proportional to the pH of the water in which it is immersed. The pH sensor produces a negative voltage if the water is acidic, no voltage if it is neutral, and a positive voltage if it is basic. The sensor output goes to the gate of a MOSFET circuit, which amplifies the sensor voltage for processing by the digital controller.

Figure 8–58 shows the pH sensor probe and a graph of output voltage versus pH. Figure 8–59 is the sensor circuit using a BF998 dual-gate *n*-channel MOSFET. A rheostat in the drain of the MOSFET is used to calibrate the circuit so that each of the three sensor circuits produce the same output voltage for a given value of pH.

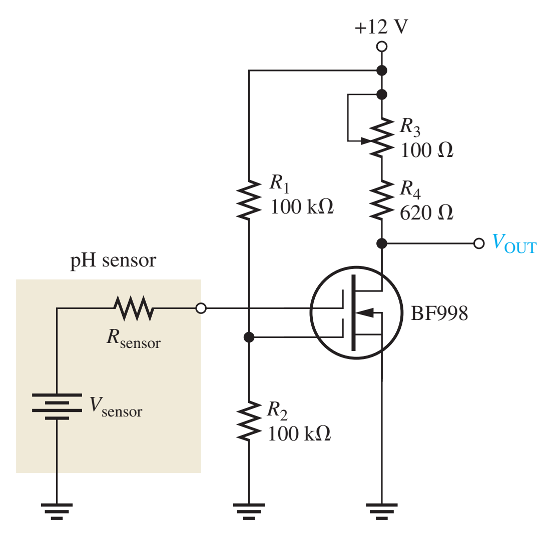
1. Determine the approximate sensor voltage for a pH of 8.
2. Determine the approximate sensor voltage for a pH of 3.

The partial datasheet for the BF998 D-MOSFET is shown in Figure 8–60. In this application, the MOSFET is used as a dc amplifier. Recall that a D-MOSFET can operate with



▲ **FIGURE 8–58**

pH sensor and graph of pH vs. output voltage.



▲ **FIGURE 8–59**

pH sensor circuit.

FIGURE 8–60

Partial datasheet for a BF998 MOSFET. Datasheet courtesy of Vishay Intertechnology, Inc.

Absolute Maximum Ratings

T_{amb} = 25°C, unless otherwise specified

Parameter	Test Conditions	Symbol	Value	Unit
Drain - source voltage		V_{DS}	12	V
Drain current		I_D	30	mA
Gate 1/Gate 2 - source peak current		$\pm I_{G1/G2SM}$	10	mA
Gate 1/Gate 2 - source voltage		$\pm V_{G1S/G2S}$	7	V
Total power dissipation	$T_{amb} \leq 60$ °C	P_{tot}	200	mW
Channel temperature		T_{Ch}	150	°C
Storage temperature range		T_{stg}	–65 to +150	°C

Electrical DC Characteristics

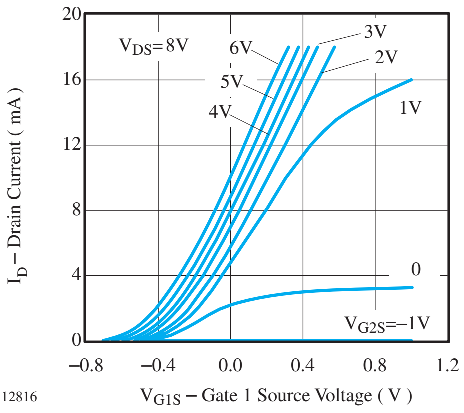
T_{amb} = 25°C, unless otherwise specified

Parameter	Test Conditions	Type	Symbol	Min	Typ	Max	Unit
Drain - source breakdown voltage	$I_D = 10\ \mu A$, $-V_{G1S} = -V_{G2S} = 4$ V		$V_{(BR)DS}$	12			V
Gate 1 - source breakdown voltage	$\pm I_{G1S} = 10$ mA, $V_{G2S} = V_{DS} = 0$		$\pm V_{(BR)G1SS}$	7		14	V
Gate 2 - source breakdown voltage	$\pm I_{G2S} = 10$ mA, $V_{G1S} = V_{DS} = 0$		$\pm V_{(BR)G2SS}$	7		14	V
Gate 1 - source leakage current	$\pm V_{G1S} = 5$ V, $V_{G2S} = V_{DS} = 0$		$\pm I_{G1SS}$			50	nA
Gate 2 - source leakage current	$\pm V_{G2S} = 5$ V, $V_{G1S} = V_{DS} = 0$		$\pm I_{G2SS}$			50	nA
Drain current	$V_{DS} = 8$ V, $V_{G1S} = 0$, $V_{G2S} = 4$ V	BF998/BF998R/ BF998RW	I_{DSS}	4		18	mA
		BF998A/BF998RA/ BF998RAW	I_{DSS}	4		10.5	mA
		BF998B/BF998RB/ BF998RBW	I_{DSS}	9.5		18	mA
Gate 1 - source cut-off voltage	$V_{DS} = 8$ V, $V_{G2S} = 4$ V, $I_D = 20\ \mu A$		$-V_{G1S(OFF)}$		1.0	2.0	V
Gate 2 - source cut-off voltage	$V_{DS} = 8$ V, $V_{G1S} = 0$, $I_D = 20\ \mu A$		$-V_{G2S(OFF)}$		0.6	1.0	V

Electrical AC Characteristics

$V_{DS} = 8$ V, $I_D = 10$ mA, $V_{G2S} = 4$ V, f = 1 MHz , T_{amb} = 25°C, unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Forward transadmittance		$\lvert y_{21s} \rvert$	21	24		mS
Gate 1 input capacitance		C_{issg1}		2.1	2.5	pF
Gate 2 input capacitance	$V_{G1S} = 0$, $V_{G2S} = 4$ V	C_{issg2}		1.1		pF
Feedback capacitance		C_{rss}		25		fF
Output capacitance		C_{oss}		1.05		pF
Power gain	$G_S = 2$ mS, $G_L = 0.5$ mS, f = 200 MHz	G_{ps}		28		dB
	$G_S = 3{,}3$ mS, $G_L = 1$ mS, f = 800 MHz	G_{ps}	16.5	20		dB
AGC range	$V_{G2S} = 4$ to –2 V, f = 800 MHz	ΔG_{ps}	40			dB
Noise figure	$G_S = 2$ mS, $G_L = 0.5$ mS, f = 200 MHz	F		1.0		dB
	$G_S = 3{,}3$ mS, $G_L = 1$ mS, f = 800 MHz	F		1.5		dB



both positive and negative gate voltages, making it ideal for this particular application where the input voltage can have either polarity. The graph in Figure 8–60 shows that the transconductance curve depends on the value of the voltage on the second gate which, in this particular design, is set at 6 V by the R_1-R_2 voltage divider. The input from the sensor is applied to the first gate.

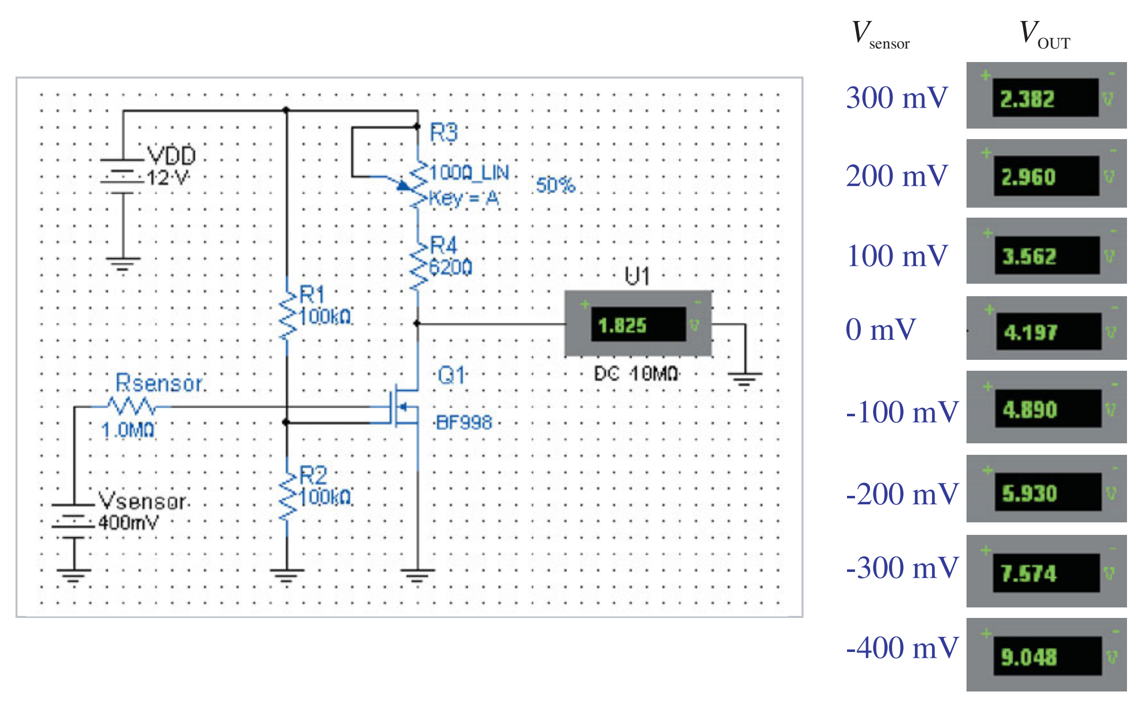
3. What is the specified typical transconductance (transadmittance) for the BF998?
4. If the drain-to-source voltage is 10 V, determine the maximum allowable drain current.
5. If one gate is biased to 1 V, what is I_D when the other gate is 0 V?

Simulation

The pH sensor circuit is simulated in Multisim, and the results for a series of sensor input voltages are shown in Figure 8–61. The sensor is modeled as a dc source in series with an internal resistance. Notice that the output of the circuit increases as the sensor input decreases. Rheostat R_3 is used to calibrate each of the three sensor circuits so that they have an identical output voltage for a given sensor input voltage.

6. If the output of the sensor circuit is 7 V, is the solution acidic, neutral, or basic (caustic)?
7. Plot a graph of V_{OUT} vs. pH for each measurement in Figure 8–61.

Simulate the pH sensor circuit using your Multisim software. Measure the output voltage for $V_{sensor} = 50$ mV, $V_{sensor} = 150$ mV, and $V_{sensor} = -25$ mV.



V_{sensor}	V_{OUT}
300 mV	2.382
200 mV	2.960
100 mV	3.562
0 mV	4.197
-100 mV	4.890
-200 mV	5.930
-300 mV	7.574
-400 mV	9.048

▲ FIGURE 8–61

Simulation results for the pH sensor circuit.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. A dc voltage source can be used to provide the sensor input voltages. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

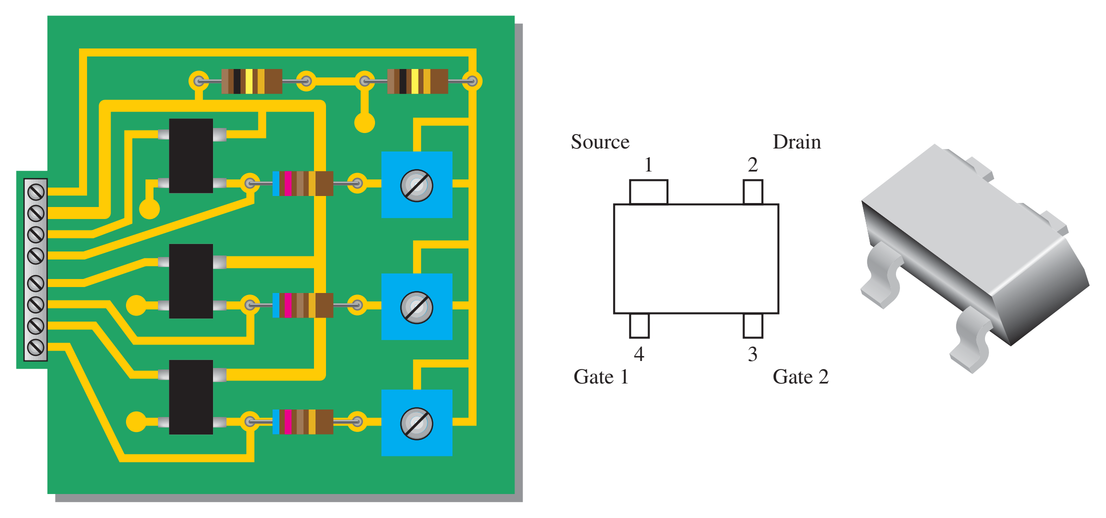
Lab Experiment

To build and test a similar circuit, go to Experiment 8 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The pH sensor circuits are implemented on a printed circuit board as shown in Figure 8–62. Each circuit monitors one of the three pH sensors in the system. Note that a single voltage divider provides +6 V to the second gate of each transistor.

8. Check the printed circuit board for correctness by comparing with the schematic in Figure 8–59.
9. Identify the connections on the back side of the board.
10. Label each input and output pin according to function.



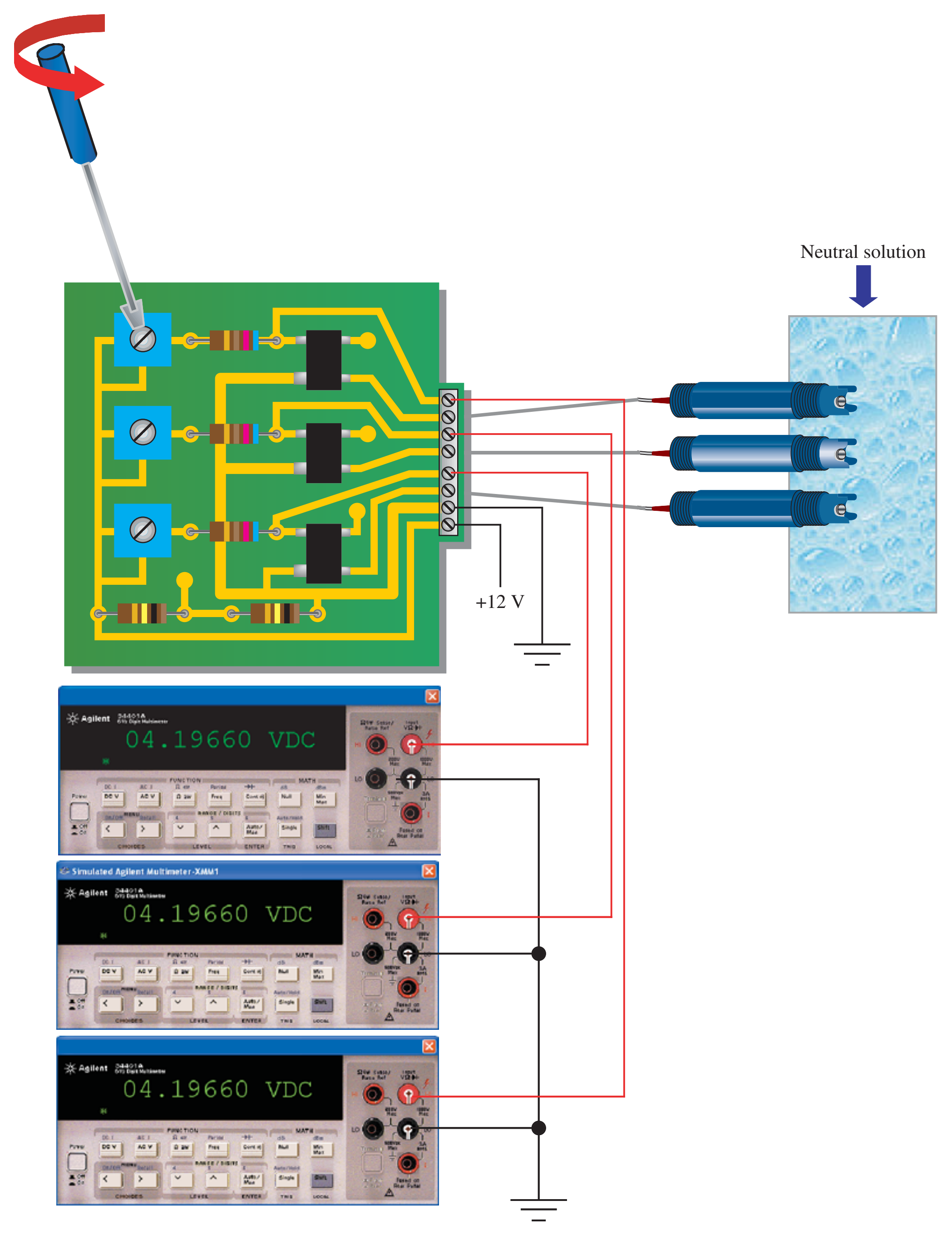
▲ FIGURE 8–62

pH sensor circuit board.

Calibration and Testing

The first step is to calibrate each of the three circuits for a pH of 7. Using a known neutral test solution in a container into which the sensors are placed, the rheostat is adjusted (if necessary) to produce the same output voltage for each circuit. In this case it is 4.197 V, as shown in Figure 8–63.

The next step is to replace the neutral solution with one that has an acidity with a known pH. All the circuits should produce the same voltage within a specified tolerance. Finally, using a basic solution with a known pH, measure the output voltages. Again, they should all agree.

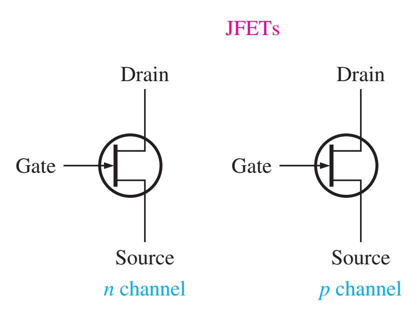

Neutral solution
+12 V
04.19660 VDC
Simulated Agilent Multimeter-XMM1
04.19660 VDC
04.19660 VDC

▲ FIGURE 8–63

Calibration and testing of the pH sensor circuits.

SUMMARY OF FIELD-EFFECT TRANSISTORS

JFETS


JFETs
Drain
Gate
Source
n channel
Drain
Gate
Source
p channel

- Gate-source *pn* junction must be reverse-biased.
- V_{GS} controls I_D.
- Value of V_{DS} at which I_D becomes constant is the pinch-off voltage.
- Value of V_{GS} at which I_D becomes zero is the cutoff voltage, $V_{GS(off)}$.
- I_{DSS} is drain current when $V_{GS} = 0$.
- Transfer characteristic:

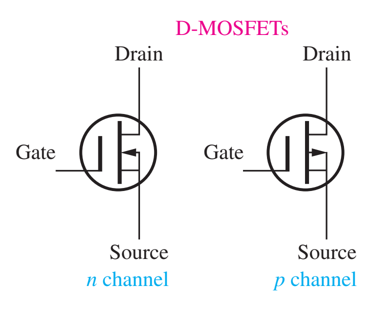
$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- Forward transconductance:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

E-MOSFETS


D-MOSFETs
Drain
Gate
Source
n channel
Drain
Gate
Source
p channel

Operates in enhancement mode only.

- V_{GS} must exceed $V_{GS(th)}$.
- *Enhancement mode:*

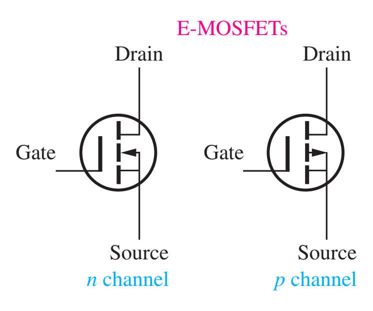
  n channel: V_{GS} positive

  p channel: V_{GS} negative
- V_{GS} controls I_D.
- Value of V_{GS} at which I_D begins is the threshold voltage, $V_{GS(th)}$.
- Transfer characteristic:

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

- K in formula can be calculated by substituting datasheet values $I_{D(on)}$ for I_D and V_{GS} at which $I_{D(on)}$ is specified for V_{GS}.

D-MOSFETS


E-MOSFETs
Drain
Gate
Source
n channel
Drain
Gate
Source
p channel

Can be operated in either depletion or enhancement modes. V_{GS} can be either polarity when biased at $V_{GS} = 0$ V.

- *Depletion mode:*

  n channel: V_{GS} negative

  p channel: V_{GS} positive
- *Enhancement mode:*

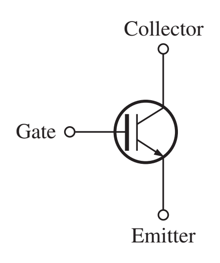
  n channel: V_{GS} positive

  p channel: V_{GS} negative

- V_{GS} controls I_D.
- Value of V_{GS} at which I_D becomes zero is the cutoff voltage, $V_{GS(off)}$.
- I_{DSS} is drain current when $V_{GS} = 0$.
- Transfer characteristic:

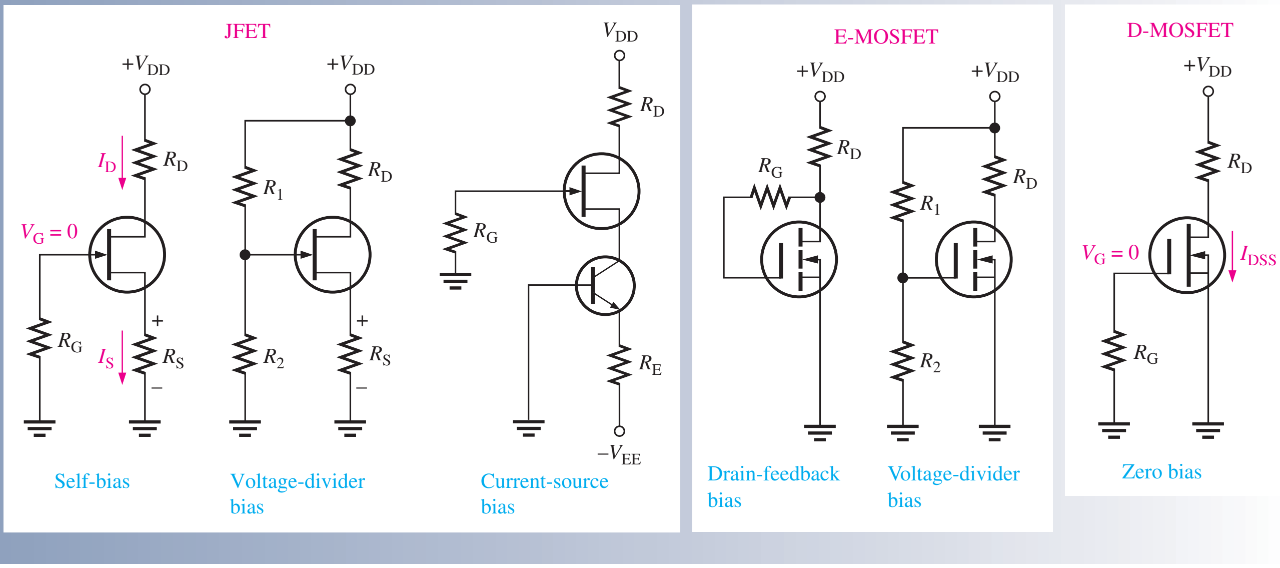
$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

IGBT


Collector
Gate
Emitter

- Voltage controlled like a MOSFET
- Output characteristics like a BJT
- Three terminals: gate, collector, emitter

FET BIASING (Voltage polarities and current directions reverse for *p* channel)


JFET
$+V_{DD}$
I_D
R_D
$V_G = 0$
R_G
I_S
R_S
+
−
Self-bias
$+V_{DD}$
R_1
R_D
R_2
R_S
+
−
Voltage-divider bias
V_{DD}
R_D
R_G
R_E
$-V_{EE}$
Current-source bias
E-MOSFET
$+V_{DD}$
R_G
R_D
Drain-feedback bias
$+V_{DD}$
R_1
R_D
R_2
Voltage-divider bias
D-MOSFET
$+V_{DD}$
R_D
$V_G = 0$
I_{DSS}
R_G
Zero bias

SUMMARY

Section 8–1

- Field-effect transistors are unipolar devices (one-charge carrier).
- The three FET terminals are source, drain, and gate.
- The JFET operates with a reverse-biased *pn* junction (gate-to-source).
- The high input resistance of a JFET is due to the reverse-biased gate-source junction.
- Reverse bias of a JFET produces a depletion region within the channel, thus increasing channel resistance.

Section 8–2

- For an *n*-channel JFET, V_{GS} can vary from zero negatively to cutoff, $V_{GS(off)}$. For a *p*-channel JFET, V_{GS} can vary from zero positively to $V_{GS(off)}$.
- I_{DSS} is the constant drain current when $V_{GS} = 0$. This is true for both JFETs and D-MOSFETs.
- A FET is called a *square-law device* because of the relationship of I_D to the square of a term containing V_{GS}.

Section 8–3

- Midpoint bias for a JFET is $I_D = I_{DSS}/2$, obtained by setting $V_{GS} \cong V_{GS(off)}/3.4$.
- The Q-point in a JFET with voltage-divider bias is more stable than in a self-biased JFET.
- Current-source bias increases the stability of a self-biased JFET.

Section 8–4

- A JFET used as a variable resistor is biased in the ohmic region.
- To bias in the ohmic region, I_D must be much smaller than I_{DSS}.
- The gate voltage controls R_{DS} in the ohmic region.
- When a JFET is biased at the origin ($V_{DS} = 0$, $I_D = 0$), the ac channel resistance is controlled by the gate voltage.

Section 8–5

- MOSFETs differ from JFETs in that the gate of a MOSFET is insulated from the channel by an SiO_2 layer, whereas the gate and channel in a JFET are separated by a *pn* junction.
- A depletion MOSFET (D-MOSFET) can operate with a zero, positive, or negative gate-to-source voltage.
- The D-MOSFET has a physical channel between the drain and source.
- For an *n*-channel D-MOSFET, negative values of V_{GS} produce the depletion mode and positive values produce the enhancement mode.
- The enhancement MOSFET (E-MOSFET) has no physical channel.
- Unlike JFETs and D-MOSFETs, the E-MOSFET cannot operate with $V_{GS} = 0$ V.
- A channel is induced in an E-MOSFET by the application of a V_{GS} greater than the threshold value, $V_{GS(th)}$.

Section 8–6

- An E-MOSFET has no I_{DSS} parameter. It is extremely small, if specified (ideally 0).
- An *n*-channel E-MOSFET has a positive $V_{GS(th)}$. A *p*-channel E-MOSFET has a negative $V_{GS(th)}$.
- The transfer characteristic curve for a D-MOSFET intersects the vertical I_D axis.
- The transfer characteristic curve for an E-MOSFET does not intersect the I_D axis.
- All MOS devices are subject to damage from electrostatic discharge (ESD).

Section 8–7

- Midpoint bias for a D-MOSFET is $I_D = I_{DSS}$ obtained by setting $V_{GS} = 0$.
- The gate of a zero-biased D-MOSFET is at 0 V due to a large resistor to ground.
- An E-MOSFET must have a V_{GS} greater than the threshold value.

Section 8–8

- The insulated-gate bipolar transistor (IGBT) combines the input characteristics of a MOSFET with the output characteristics of a BJT.
- The IGBT has three terminals: emitter, gate, and collector.
- IGBTs are used in high-voltage switching applications.

Section 8–9

- An open gate is hard to detect in a zero-biased D-MOSFET because the gate is normally at 0 V; however, erratic behavior may occur.
- An open gate is easy to detect in an E-MOSFET because the gate is normally at a voltage other than 0 V.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Depletion In a MOSFET, the process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.

Drain One of the three terminals of a FET analogous to the collector of a BJT.

Enhancement In a MOSFET, the process of creating a channel or increasing the conductivity of the channel by the addition of charge carriers.

Gate One of the three terminals of a FET analogous to the base of a BJT.

IGBT Insulated-gate bipolar transistor; a device that combines features of the MOSFET and the BJT and used mainly for high-voltage switching applications.

JFET Junction field-effect transistor; one of two major types of field-effect transistors.

MOSFET Metal oxide semiconductor field-effect transistor; one of two major types of FETs; sometimes called IGFET for insulated-gate FET.

Ohmic region The portion of the FET characteristic curve lying below pinch-off in which Ohm's law applies.

Pinch-off voltage The value of the drain-to-source voltage of a FET at which the drain current becomes constant when the gate-to-source voltage is zero.

Source One of the three terminals of a FET analogous to the emitter of a BJT.

Transconductance (g_m) The ratio of a change in drain current to a change in gate-to-source voltage in a FET.

KEY FORMULAS

8–1	$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$	JFET/D-MOSFET transfer characteristic
8–2	$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$	Transconductance
8–3	$g_{m0} = \frac{2I_{DSS}}{\lvert V_{GS(off)}\rvert}$	Transconductance at $V_{GS} = 0$
8–4	$I_D = K(V_{GS} - V_{GS(th)})^2$	E-MOSFET transfer characteristic

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. The JFET always operates with a reverse-biased gate-to-source *pn* junction.
2. The channel resistance of a JFET is a constant.
3. The gate-to-source voltage of an *n*-channel JFET must be negative.
4. I_D becomes zero at the pinch-off voltage.
5. V_{GS} has no effect on I_D.
6. $V_{GS(off)}$ and V_P are always equal in magnitude but opposite in polarity.
7. The JFET is a square-law device because of the mathematical expression of its transfer characteristic curve.
8. Forward transconductance is the change in drain voltage for a given change in gate voltage.
9. The parameters g_m and y_{fs} are the same.
10. The D-MOSFET can be operated in two modes.
11. An E-MOSFET operates in the depletion mode.
12. A D-MOSFET has a physical channel and an E-MOSFET has an induced channel.
13. ESD means *electronic semiconductor device.*
14. MOSFETs must be handled with care.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the drain current in Figure 8–17 is increased, V_{DS} will
   (a) increase **(b)** decrease **(c)** not change
2. If the drain current in Figure 8–17 is increased, V_{GS} will
   (a) increase **(b)** decrease **(c)** not change

3. If the value of R_D in Figure 8–24 is increased, I_D will

(a) increase **(b)** decrease **(c)** not change

4. If the value of R_2 in Figure 8–24 is decreased, V_G will

(a) increase **(b)** decrease **(c)** not change

5. If V_{GS} in Figure 8–47 is increased, I_D will

(a) increase **(b)** decrease **(c)** not change

6. If R_2 in Figure 8–47 opens, V_{GS} will

(a) increase **(b)** decrease **(c)** not change

7. If the value of R_G in Figure 8–50 is increased, V_G will

(a) increase **(b)** decrease **(c)** not change

8. If the value of I_{DSS} in Figure 8–50 is increased, V_{DS} will

(a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 8–1

1. The JFET is

(a) a unipolar device
(b) a voltage-controlled device
(c) a current-controlled device
(d) answers (a) and (c)
(e) answers (a) and (b)

2. The channel of a JFET is between the

(a) gate and drain
(b) drain and source
(c) gate and source
(d) input and output

3. A JFET always operates with

(a) the gate-to-source *pn* junction reverse-biased
(b) the gate-to-source *pn* junction forward-biased
(c) the drain connected to ground
(d) the gate connected to the source

Section 8–2

4. For $V_{GS} = 0$ V, the drain current becomes constant when V_{DS} exceeds

(a) cutoff
(b) V_{DD}
(c) V_P
(d) 0 V

5. The constant-current region of a FET lies between

(a) cutoff and saturation
(b) cutoff and pinch-off
(c) 0 and I_{DSS}
(d) pinch-off and breakdown

6. I_{DSS} is

(a) the drain current with the source shorted
(b) the drain current at cutoff
(c) the maximum possible drain current
(d) the midpoint drain current

7. Drain current in the constant-current region increases when

(a) the gate-to-source bias voltage decreases

(b) the gate-to-source bias voltage increases

(c) the drain-to-source voltage increases

(d) the drain-to-source voltage decreases

8. In a certain FET circuit, $V_{GS} = 0$ V, $V_{DD} = 15$ V, $I_{DSS} = 15$ mA, and $R_D = 470\ \Omega$. If R_D is decreased to 330 Ω, I_{DSS} is

(a) 19.5 mA **(b)** 10.5 mA

(c) 15 mA **(d)** 1 mA

9. At cutoff, the JFET channel is

(a) at its widest point

(b) completely closed by the depletion region

(c) extremely narrow

(d) reverse-biased

10. A certain JFET datasheet gives $V_{GS(off)} = -4$ V. The pinch-off voltage, V_P,

(a) cannot be determined

(b) is −4 V

(c) depends on V_{GS}

(d) is +4 V

11. The JFET in Question 10

(a) is an *n* channel

(b) is a *p* channel

(c) can be either

12. For a certain JFET, $I_{GSS} = 10$ nA at $V_{GS} = 10$ V. The input resistance is

(a) 100 MΩ **(b)** 1 MΩ

(c) 1000 MΩ **(d)** 1000 MΩ

Section 8–3

13. For a certain *p*-channel JFET, $V_{GS(off)} = 8$ V. The value of V_{GS} for an approximate midpoint bias is

(a) 4 V **(b)** 0 V

(c) 1.25 V **(d)** 2.34 V

14. In a self-biased JFET, the gate is at

(a) a positive voltage

(b) 0 V

(c) a negative voltage

(d) ground

Section 8–4

15. The drain-to-source resistance in the ohmic region depends on

(a) V_{GS}

(b) the Q-point values

(c) the slope of the curve at the Q-point

(d) all of these

16. To be used as a variable resistor, a JFET must be

(a) an *n*-channel device

(b) a *p*-channel device

(c) biased in the ohmic region

(d) biased in saturation

17. When a JFET is biased at the origin, the ac channel resistance is determined by

(a) the Q-point values **(b)** V_{GS}

(c) the transconductance **(d)** answers (b) and (c)

Section 8–5

18. A MOSFET differs from a JFET mainly because
  (a) of the power rating
  (b) the MOSFET has two gates
  (c) the JFET has a *pn* junction
  (d) MOSFETs do not have a physical channel

19. A D-MOSFET operates in
  (a) the depletion mode only
  (b) the enhancement mode only
  (c) the ohmic region only
  (d) both the depletion and enhancement modes

Section 8–6

20. An *n*-channel D-MOSFET with a positive V_{GS} is operating in
  (a) the depletion mode
  (b) the enhancement mode
  (c) cutoff
  (d) saturation

21. A certain *p*-channel E-MOSFET has a $V_{GS(th)} = -2$ V. If $V_{GS} = 0$ V, the drain current is
  (a) 0 A **(b)** $I_{D(on)}$
  (c) maximum **(d)** I_{DSS}

22. In an E-MOSFET, there is no drain current until V_{GS}
  (a) reaches $V_{GS(th)}$ **(b)** is positive
  (c) is negative **(d)** equals 0 V

23. All MOS devices are subject to damage from
  (a) excessive heat
  (b) electrostatic discharge
  (c) excessive voltage
  (d) all of these

Section 8–7

24. A certain D-MOSFET is biased at $V_{GS} = 0$ V. Its datasheet specifies $I_{DSS} = 20$ mA and $V_{GS(off)} = -5$ V. The value of the drain current
  (a) is 0 A
  (b) cannot be determined
  (c) is 20 mA

Section 8–8

25. An IGBT is generally used in
  (a) low-power applications
  (b) rf applications
  (c) high-voltage applications
  (d) low-current applications

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 8–1

The JFET

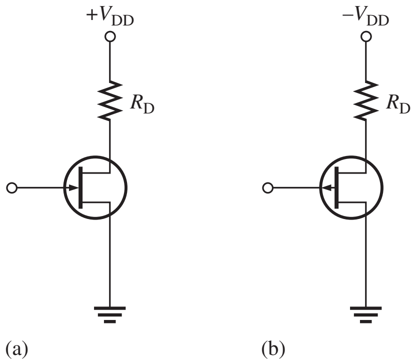
1. The V_{GS} of a *p*-channel JFET is increased from 1 V to 3 V.
  (a) Does the depletion region narrow or widen?
  (b) Does the resistance of the channel increase or decrease?

2. Why must the gate-to-source voltage of an *n*-channel JFET always be either 0 or negative?

3. Draw the schematic diagrams for a *p*-channel and an *n*-channel JFET. Label the terminals.

4. Show how to connect bias voltages between the gate and source of the JFETs in Figure 8–64.

▶ FIGURE 8–64



Section 8–2 JFET Characteristics and Parameters

5. A JFET has a specified pinch-off voltage of 5 V. When $V_{GS} = 0$, what is V_{DS} at the point where the drain current becomes constant?

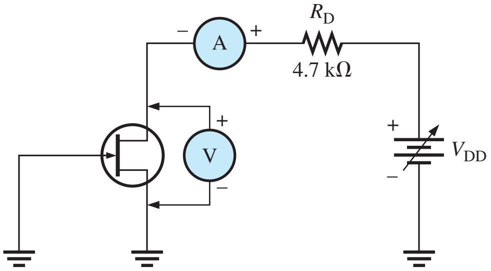
6. A certain *n*-channel JFET is biased such that $V_{GS} = -2$ V. What is the value of $V_{GS(off)}$ if V_P is specified to be 6 V? Is the device on?

7. A certain JFET datasheet gives $V_{GS(off)} = -8$ V and $I_{DSS} = 10$ mA. When $V_{GS} = 0$, what is I_D for values of V_{DS} above pinch off? $V_{DD} = 15$ V.

8. A certain *p*-channel JFET has a $V_{GS(off)} = 6$ V. What is I_D when $V_{GS} = 8$ V?

9. The JFET in Figure 8–65 has a $V_{GS(off)} = -4$ V. Assume that you increase the supply voltage, V_{DD}, beginning at zero until the ammeter reaches a steady value. What does the voltmeter read at this point?

▶ FIGURE 8–65



10. The following parameters are obtained from a certain JFET datasheet: $V_{GS(off)} = -8$ V and $I_{DSS} = 5$ mA. Determine the values of I_D for each value of V_{GS} ranging from 0 V to −8 V in 1 V steps. Plot the transfer characteristic curve from these data.

11. For the JFET in Problem 10, what value of V_{GS} is required to set up a drain current of 2.25 mA?

12. For a particular JFET, $g_{m0} = 3200\ \mu$S. What is g_m when $V_{GS} = -4$ V, given that $V_{GS(off)} = -8$ V?

13. Determine the forward transconductance of a JFET biased at $V_{GS} = -2$ V. From the datasheet, $V_{GS(off)} = -7$ V and $g_m = 2000\ \mu$S at $V_{GS} = 0$ V. Also determine the forward transfer conductance, g_{fs}.

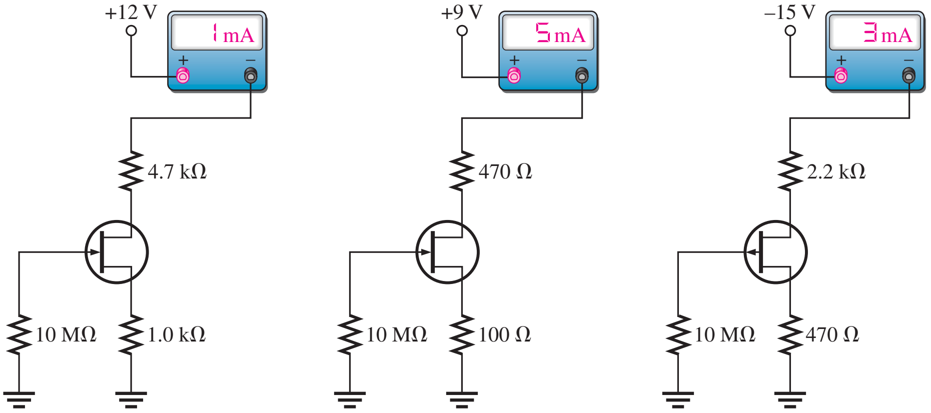
14. A *p*-channel JFET datasheet shows that $I_{GSS} = 5$ nA at $V_{GS} = 10$ V. Determine the input resistance.

15. Using Equation 8–1, plot the transfer characteristic curve for a JFET with $I_{DSS} = 8$ mA and $V_{GS(off)} = -5$ V. Use at least four points.

Section 8–3 JFET Biasing

16. An *n*-channel self-biased JFET has a drain current of 12 mA and a 100 Ω source resistor. What is the value of V_{GS}?

17. Determine the value of R_S required for a self-biased JFET to produce a V_{GS} of -4 V when $I_D = 5$ mA.
18. Determine the value of R_S required for a self-biased JFET to produce $I_D = 2.5$ mA when $V_{GS} = -3$ V.
19. $I_{DSS} = 20$ mA and $V_{GS(off)} = -6$ V for a particular JFET.
    - **(a)** What is I_D when $V_{GS} = 0$ V?
    - **(b)** What is I_D when $V_{GS} = V_{GS(off)}$?
    - **(c)** If V_{GS} is increased from -4 V to -1 V, does I_D increase or decrease?
20. For each circuit in Figure 8–66, determine V_{DS} and V_{GS}.

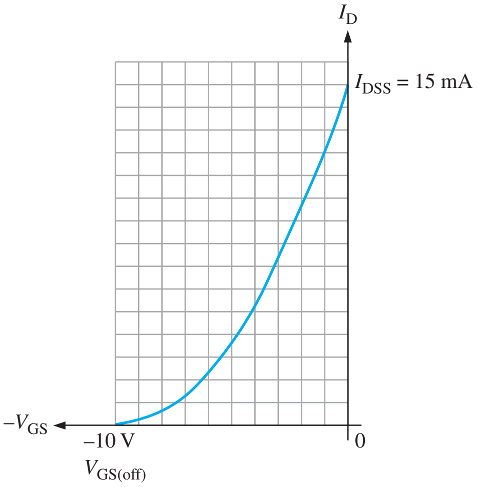


(a) (b) (c)

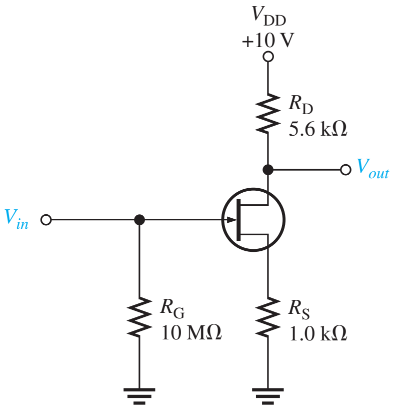
▲ FIGURE 8–66

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F08-66).

21. Using the curve in Figure 8–67, determine the value of R_S required for a 9.5 mA drain current.
22. Set up a midpoint bias for a JFET with $I_{DSS} = 14$ mA and $V_{GS(off)} = -10$ V. Use a 24 V dc source as the supply voltage. Show the circuit and resistor values. Indicate the values of I_D, V_{GS}, and V_{DS}.
23. Determine the total input resistance in Figure 8–68. $I_{GSS} = 20$ nA at $V_{GS} = -10$ V.

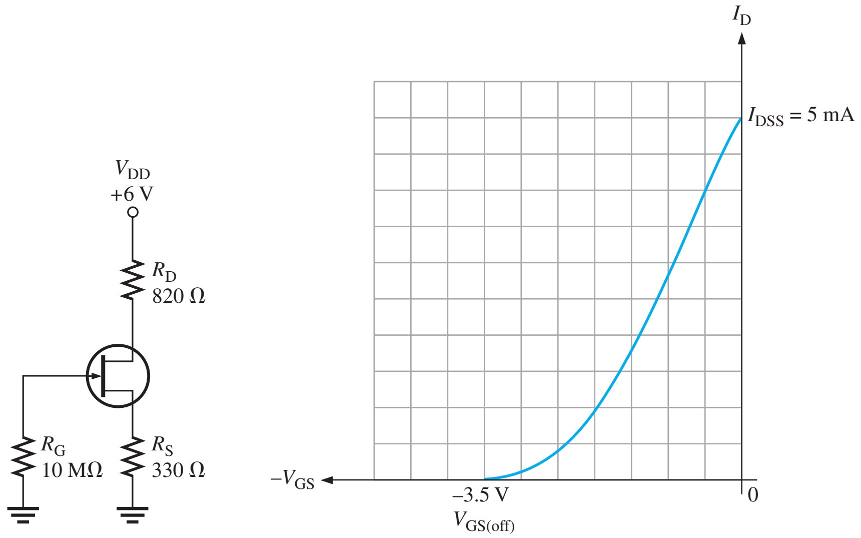


▲ FIGURE 8–67



▲ FIGURE 8–68

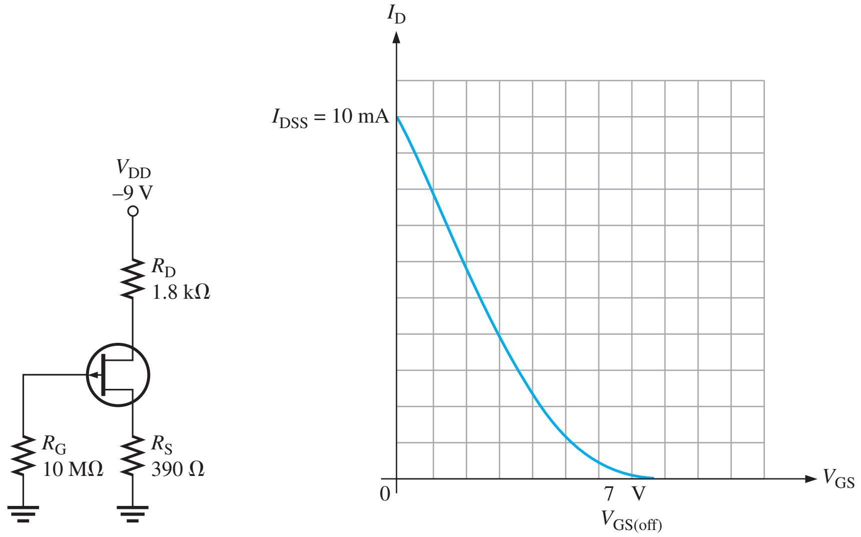
24. Graphically determine the Q-point for the circuit in Figure 8–69(a) using the transfer characteristic curve in Figure 8–69(b).


V_{DD}
+6 V
R_D
820 Ω
R_G
10 MΩ
R_S
330 Ω
I_D
I_{DSS} = 5 mA
$-V_{GS}$
–3.5 V
$V_{GS(off)}$
0

(a) (b)

▲ FIGURE 8–69

25. Find the Q-point for the *p*-channel JFET circuit in Figure 8–70.


V_{DD}
–9 V
R_D
1.8 kΩ
R_G
10 MΩ
R_S
390 Ω
I_D
I_{DSS} = 10 mA
V_{GS}
0
7 V
$V_{GS(off)}$

(a) (b)

▲ FIGURE 8–70

26. Given that the drain-to-ground voltage in Figure 8–71 is 5 V, determine the Q-point of the circuit.

27. Find the Q-point values for the JFET with voltage-divider bias in Figure 8–72.

FIGURE 8–71

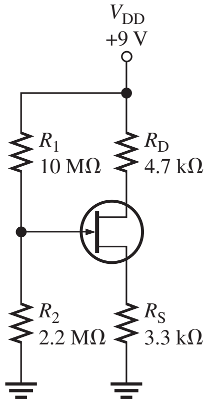
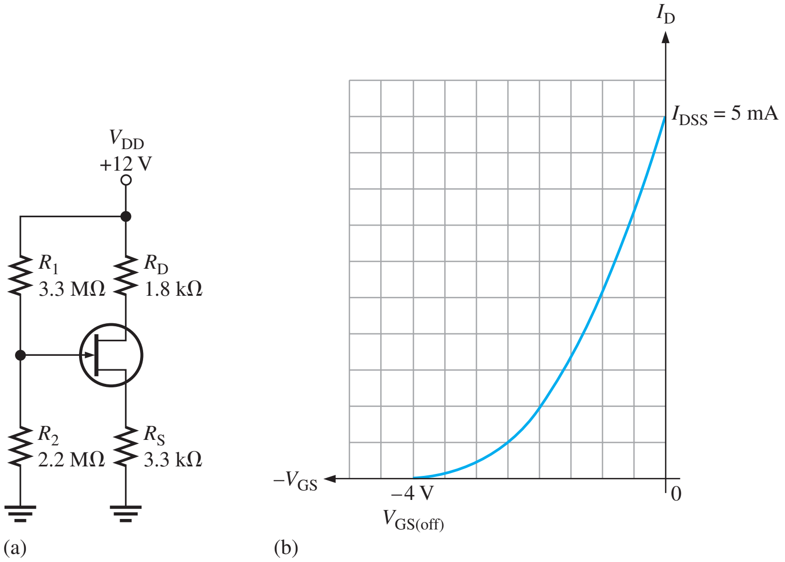


FIGURE 8–72



Section 8–4 The Ohmic Region

28. A certain JFET is biased in the ohmic region at $V_{DS} = 0.8$ V and $I_D = 0.20$ mA. What is the drain-to-source resistance?

29. The Q-point of a JFET is varied from $V_{DS} = 0.4$ V and $I_D = 0.15$ mA to $V_{DS} = 0.6$ V and $I_D = 0.45$ mA. Determine the range of R_{DS} values.

30. Determine the transconductance of a JFET biased at the origin given that $g_{m0} = 1.5$ mS, $V_{GS} = -1$ V, and $V_{GS(off)} = -3.5$ V.

31. Determine the ac drain-to-source resistance of the JFET in Problem 30.

Section 8–5 The MOSFET

32. Draw the schematic symbols for *n*-channel and *p*-channel E-MOSFETs and D-MOSFETs. Label the terminals.

33. In what mode is an *n*-channel D-MOSFET with a positive V_{GS} operating?

34. Describe the basic difference between an E-MOSFET and a D-MOSFET.

35. Explain why both types of MOSFETs have an extremely high input resistance at the gate.

Section 8–6 MOSFET Characteristics and Parameters

36. The datasheet for an E-MOSFET reveals that $I_{D(on)} = 10$ mA at $V_{GS} = -12$ V and $V_{GS(th)} = -3$ V. Find I_D when $V_{GS} = -6$ V.

37. Determine I_{DSS}, given $I_D = 3$ mA, $V_{GS} = -2$ V, and $V_{GS(off)} = -10$ V.

38. The datasheet for a certain D-MOSFET gives $V_{GS(off)} = -5$ V and $I_{DSS} = 8$ mA.

(a) Is this device *p* channel or *n* channel?

(b) Determine I_D for values of V_{GS} ranging from -5 V to $+5$ V in increments of 1 V.

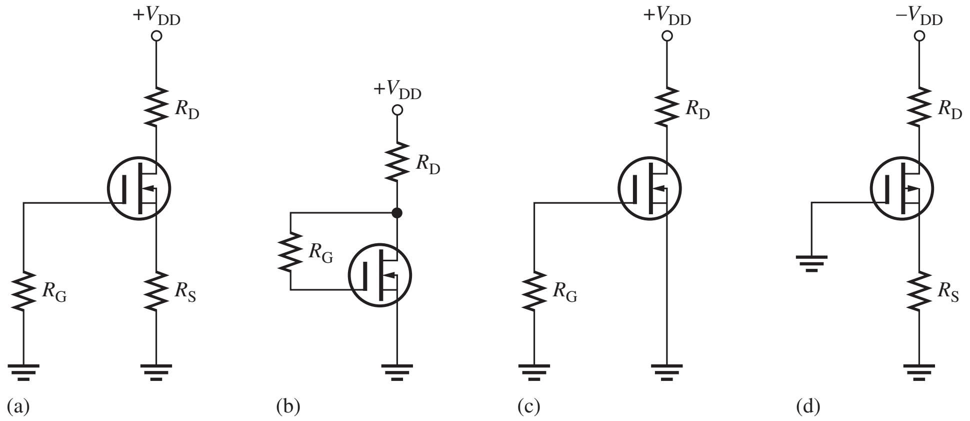
(c) Plot the transfer characteristic curve using the data from part (b).

Section 8–7

MOSFET Biasing

39. Determine in which mode (depletion, enhancement or neither) each D-MOSFET in Figure 8–73 is biased.

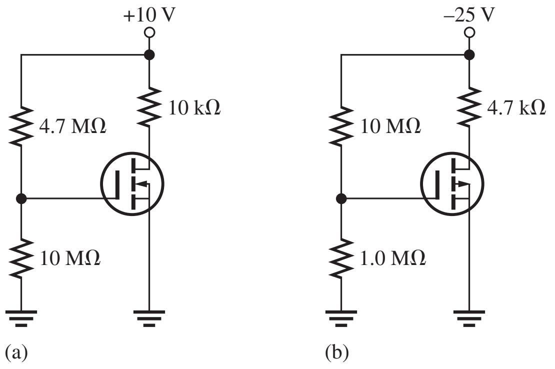
▶ **FIGURE 8–73**



+V_DD
R_D
R_G
R_S
+V_DD
R_D
R_G
+V_DD
R_D
R_G
–V_DD
R_D
R_S
(a)
(b)
(c)
(d)

40. Each E-MOSFET in Figure 8–74 has a $V_{GS(th)}$ of $+5$ V or -5 V, depending on whether it is an *n*-channel or a *p*-channel device. Determine whether each MOSFET is on or off.

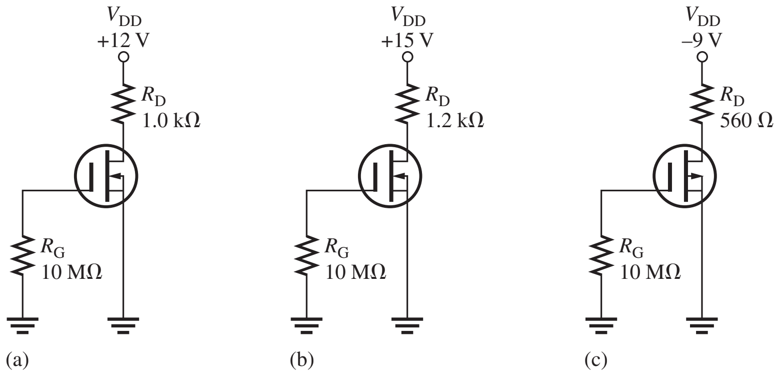
▶ **FIGURE 8–74**



+10 V
4.7 MΩ
10 kΩ
10 MΩ
–25 V
10 MΩ
4.7 kΩ
1.0 MΩ
(a)
(b)

41. Determine V_{DS} for each circuit in Figure 8–75. $I_{DSS} = 8$ mA.

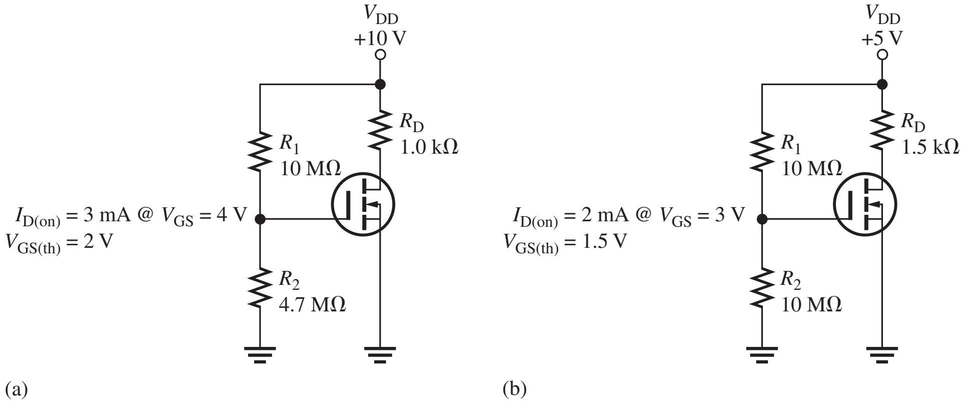
▶ **FIGURE 8–75**



V_DD
+12 V
R_D
1.0 kΩ
R_G
10 MΩ
V_DD
+15 V
R_D
1.2 kΩ
R_G
10 MΩ
V_DD
–9 V
R_D
560 Ω
R_G
10 MΩ
(a)
(b)
(c)

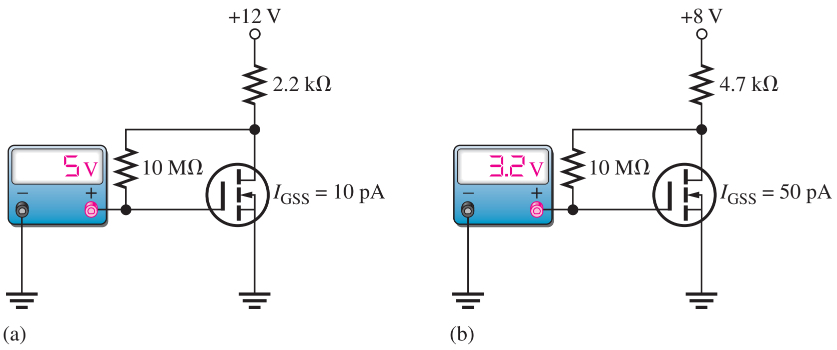
42. Find V_{GS} and V_{DS} for the E-MOSFETs in Figure 8–76. Datasheet information is listed with each circuit.

FIGURE 8–76


V_{DD}
+10 V
R_D
1.0 kΩ
R_1
10 MΩ
$I_{D(on)}$ = 3 mA @ V_{GS} = 4 V
$V_{GS(th)}$ = 2 V
R_2
4.7 MΩ
(a)
V_{DD}
+5 V
R_D
1.5 kΩ
R_1
10 MΩ
$I_{D(on)}$ = 2 mA @ V_{GS} = 3 V
$V_{GS(th)}$ = 1.5 V
R_2
10 MΩ
(b)

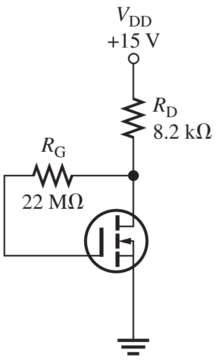
43. Based on the V_{GS} measurements, determine the drain current and drain-to-source voltage for each circuit in Figure 8–77.

FIGURE 8–77


+12 V
2.2 kΩ
5 V
10 MΩ
I_{GSS} = 10 pA
(a)
+8 V
4.7 kΩ
3.2 V
10 MΩ
I_{GSS} = 50 pA
(b)

44. Determine the actual gate-to-source voltage in Figure 8–78 by taking into account the gate leakage current, I_{GSS}. Assume that I_{GSS} is 50 pA and I_D is 1 mA under the existing bias conditions.

FIGURE 8–78


V_{DD}
+15 V
R_D
8.2 kΩ
R_G
22 MΩ

Section 8–8 The IGBT

45. Explain why the IGBT has a very high input resistance.

46. Explain how an excessive collector current can produce a latch-up condition in an IGBT.

Section 8–9 Troubleshooting

47. The current reading in Figure 8–66(a) suddenly goes to zero. What are the possible faults?

48. The current reading in Figure 8–66(b) suddenly jumps to approximately 16 mA. What are the possible faults?

49. If the supply voltage in Figure 8–66(c) is changed to −20 V, what would you see on the ammeter?

50. You measure +10 V at the drain of the MOSFET in Figure 8–74(a). The transistor checks good and the ground connections are okay. What can be the problem?

51. You measure approximately 0 V at the drain of the MOSFET in Figure 8–74(b). You can find no shorts and the transistor checks good. What is the most likely problem?

APPLICATION ACTIVITY PROBLEMS

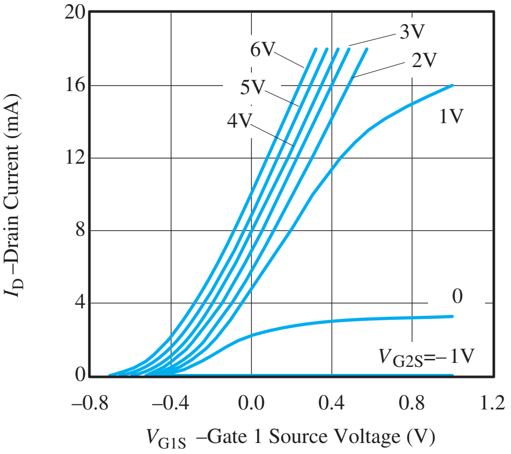
52. Refer to Figure 8–58 and determine the sensor voltage for each of the following pH values.

(a) 2 **(b)** 5 **(c)** 7 **(d)** 11

53. Referring to the transconductance curves for the BF998 in Figure 8–79, determine the change in I_D when the bias on the second gate is changed from 6 V to 1 V and V_{G1S} is 0.0 V. Each curve represents a different V_{G2S} value.

▶ **FIGURE 8–79**

Transconductance curves for BF998.



54. Refer to Figure 8–61 and plot the transconductance curve (I_D vs. V_{G1S}).

55. Refer to Figure 8–79. Determine the output voltage of the circuit in Figure 8–61 if $V_{G1S} = V_{sensor} = 0$ V and R_2 is changed to 50 kΩ.

DATASHEET PROBLEMS

56. What type of FET is the 2N5457?

57. Referring to the datasheet in Figure 8–14, determine the following:

(a) Minimum $V_{GS(off)}$ for the 2N5457.

(b) Maximum drain-to-source voltage for the 2N5457.

(c) Maximum power dissipation for the 2N5458 at an ambient temperature of 25°C.

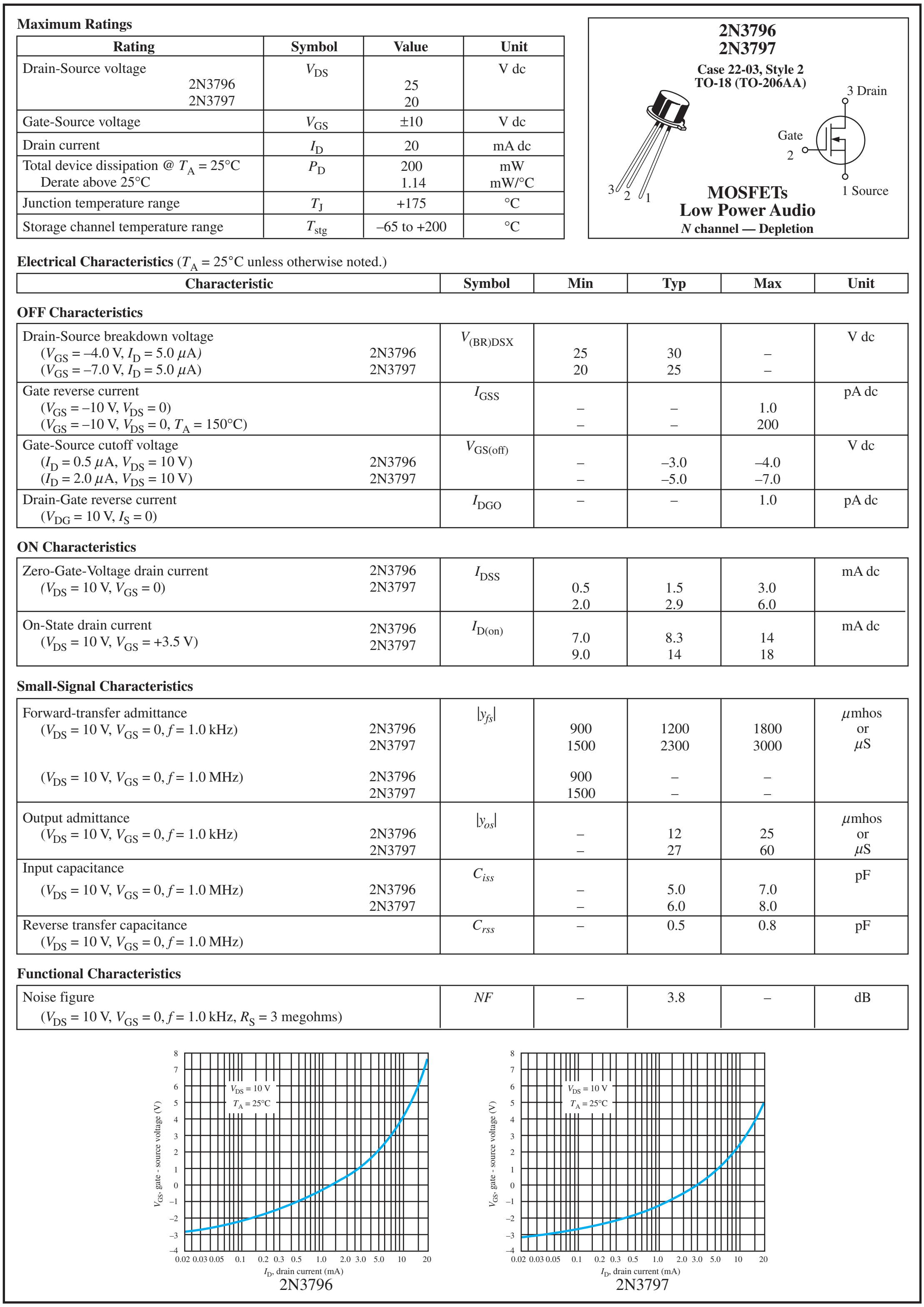
(d) Maximum reverse gate-to-source voltage for the 2N5459.

58. Referring to Figure 8–14, determine the maximum power dissipation for a 2N5457 at an ambient temperature of 65°C.

59. Referring to Figure 8–14, determine the minimum g_{m0} for the 2N5459 at a frequency of 1 kHz.

60. Referring to Figure 8–14, what is the typical drain current in a 2N5459 for $V_{GS} = 0$ V?

61. Referring to the 2N3796 datasheet in Figure 8–80, determine the drain current for $V_{GS} = 0$ V.



Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DS}		V dc
2N3796		25	
2N3797		20	
Gate-Source voltage	V_{GS}	±10	V dc
Drain current	I_D	20	mA dc
Total device dissipation @ $T_A = 25°C$	P_D	200	mW
Derate above 25°C		1.14	mW/°C
Junction temperature range	T_J	+175	°C
Storage channel temperature range	T_{stg}	–65 to +200	°C

2N3796
2N3797

Case 22-03, Style 2
TO-18 (TO-206AA)

3 Drain
Gate
2
1 Source
3
2
1

MOSFETs
Low Power Audio
***N* channel — Depletion**

Electrical Characteristics ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF Characteristics						
Drain-Source breakdown voltage		$V_{(BR)DSX}$				V dc
($V_{GS} = –4.0$ V, $I_D = 5.0\ \mu A$)	2N3796		25	30	–	
($V_{GS} = –7.0$ V, $I_D = 5.0\ \mu A$)	2N3797		20	25	–	
Gate reverse current		I_{GSS}				pA dc
($V_{GS} = –10$ V, $V_{DS} = 0$)			–	–	1.0	
($V_{GS} = –10$ V, $V_{DS} = 0$, $T_A = 150°C$)			–	–	200	
Gate-Source cutoff voltage		$V_{GS(off)}$				V dc
($I_D = 0.5\ \mu A$, $V_{DS} = 10$ V)	2N3796		–	–3.0	–4.0	
($I_D = 2.0\ \mu A$, $V_{DS} = 10$ V)	2N3797		–	–5.0	–7.0	
Drain-Gate reverse current ($V_{DG} = 10$ V, $I_S = 0$)		I_{DGO}	–	–	1.0	pA dc
ON Characteristics						
Zero-Gate-Voltage drain current		I_{DSS}				mA dc
($V_{DS} = 10$ V, $V_{GS} = 0$)	2N3796		0.5	1.5	3.0	
	2N3797		2.0	2.9	6.0	
On-State drain current		$I_{D(on)}$				mA dc
($V_{DS} = 10$ V, $V_{GS} = +3.5$ V)	2N3796		7.0	8.3	14	
	2N3797		9.0	14	18	
Small-Signal Characteristics						
Forward-transfer admittance		$\lvert y_{fs} \rvert$				μmhos or μS
($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz)	2N3796		900	1200	1800	
	2N3797		1500	2300	3000	
($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	2N3796		900	–	–	
	2N3797		1500	–	–	
Output admittance		$\lvert y_{os} \rvert$				μmhos or μS
($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz)	2N3796		–	12	25	
	2N3797		–	27	60	
Input capacitance		C_{iss}				pF
($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	2N3796		–	5.0	7.0	
	2N3797		–	6.0	8.0	
Reverse transfer capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)		C_{rss}	–	0.5	0.8	pF
Functional Characteristics						
Noise figure ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz, $R_S = 3$ megohms)		NF	–	3.8	–	dB

2N3796

2N3797

▲ **FIGURE 8–80**

Partial datasheet for the 2N3797 D-MOSFET.

62. Referring to Figure 8–80, what is the drain current for a 2N3796 when $V_{GS} = 6$ V?

63. Referring to the datasheet in Figure 8–80, determine I_D in a 2N3797 when $V_{GS} = +3$ V. Determine I_D when $V_{GS} = -2$ V.

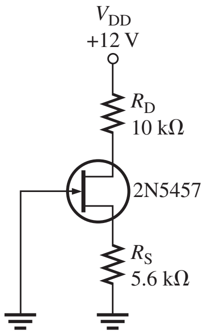
64. Referring to Figure 8–80, how much does the maximum forward transconductance of a 2N3796 change over a range of signal frequencies from 1 kHz to 1 MHz?

65. Referring to Figure 8–80, determine the typical value of gate-to-source voltage at which the 2N3796 will go into cutoff.

ADVANCED PROBLEMS

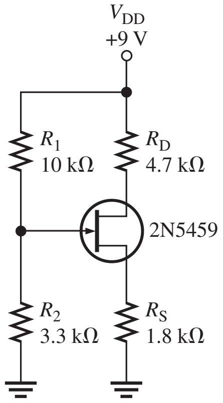
66. Find V_{DS} and V_{GS} in Figure 8–81 using minimum datasheet values.

▶ **FIGURE 8–81**



67. Determine the maximum I_D and V_{GS} for the circuit in Figure 8–82.

▶ **FIGURE 8–82**



68. Determine the range of possible Q-point values from minimum to maximum for the circuit in Figure 8–81.

69. Find the drain-to-source voltage for the pH sensor circuit in Figure 8–59 when a pH of 5 is measured. Assume the rheostat is set to produce 4 V at the drain when a pH of 7 is measured.

70. Design a MOSFET circuit with zero bias using a 2N3797 that operates from a +9 V dc supply and produces a V_{DS} of 4.5 V. The maximum current drawn from the source is to be 1 mA.

71. Design a circuit using an *n*-channel E-MOSFET with the following datasheet specifications: $I_{D(on)} = 500$ mA@ $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Use a +12 V dc supply voltage with voltage-divider bias. The voltage at the drain with respect to ground is to be +8 V. The maximum current from the supply is to be 20 mA.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

72. Open file TSP08-72 and determine the fault.

73. Open file TSP08-73 and determine the fault.

74. Open file TSP08-74 and determine the fault.

75. Open file TSP08-75 and determine the fault.

76. Open file TSP08-76 and determine the fault.

77. Open file TSP08-77 and determine the fault.

78. Open file TSP08-78 and determine the fault.

79. Open file TSP08-79 and determine the fault.

80. Open file TSP08-80 and determine the fault.

FET AMPLIFIERS AND SWITCHING CIRCUITS

9

CHAPTER OUTLINE

9–1 The Common-Source Amplifier
9–2 The Common-Drain Amplifier
9–3 The Common-Gate Amplifier
9–4 The Class D Amplifier
9–5 MOSFET Analog Switching
9–6 MOSFET Digital Switching
9–7 Troubleshooting
Application Activity

CHAPTER OBJECTIVES

- Explain and analyze the operation of common-source FET amplifiers
- Explain and analyze the operation of common-drain FET amplifiers
- Explain and analyze the operation of common-gate FET amplifiers
- Discuss the operation of a class D amplifier
- Describe how MOSFETs can be used in analog switching applications
- Describe how MOSFETs are used in digital switching applications
- Troubleshoot FET amplifiers

KEY TERMS

- Common-source
- Common-drain
- Source-follower
- Common-gate
- Class D amplifier
- Pulse-width modulation
- Analog switch
- CMOS

APPLICATION ACTIVITY PREVIEW

A JFET common-source amplifier and a common-gate amplifier are combined in a cascode arrangement for an active antenna. Cascode amplifiers are often used for RF (radio frequency) applications to achieve improved high-frequency performance. In this application, the cascode amplifier provides a high resistance input for a whip antenna, as well as high gain to amplify extremely small antenna signals.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

Because of their extremely high input resistance and low noise, FET amplifiers are a good choice for certain applications, such as amplifying low-level signals in the first stage of a communication receiver. FETs also have the advantage in certain power amplifiers and in switching circuits because biasing is simple and more efficient. The standard amplifier configurations are common-source (CS), common-drain (CD) and common-base (CB), which are analogous to CE, CC, and CB configurations of BJTs.

FETs can be used in any of the amplifier types introduced earlier (class A, class B, and class C). In some cases, the FET circuit will perform better; in other cases, the BJT circuit is superior because BJTs have higher gain and better linearity. Another type of amplifier (class D) is introduced in this chapter because FETs are always superior to BJTs in class D and you will rarely see BJTs used in class D. The class D amplifier is a switching amplifier that is normally either in cutoff or saturation. It is used in analog power amplifiers with a circuit called a pulse-width modulator, introduced in Section 9–4.

FETs are superior to BJTs in nearly all switching applications. Various switching circuits—analog switches, analog multiplexers, and switched capacitors—are discussed. In addition, common digital switching circuits are introduced using CMOS (complementary MOS).

9–1 THE COMMON-SOURCE AMPLIFIER

When used in amplifier applications, the FET has an important advantage compared to the BJT due to the FET's extremely high input impedance. Disadvantages, however, include higher distortion and lower gain. The particular application will usually determine which type of transistor is best suited. The common-source (CS) amplifier is comparable to the common-emitter BJT amplifier that you studied in Chapter 6.

After completing this section, you should be able to

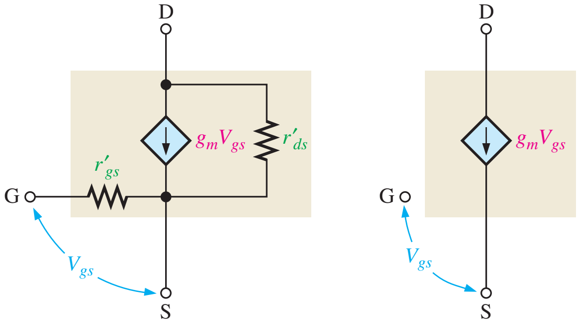
- **Explain and analyze the operation of common-source FET amplifiers**
- Discuss and analyze the FET ac model
- Describe and analyze common-source JFET amplifier operation
- Perform dc analysis of a JFET amplifier
  - Use the graphical approach
  - Use the mathematical approach
  - Use the TI-89 calculator* (if available)
- Discuss and analyze the ac equivalent circuit of a JFET amplifier
  - Determine the signal voltage at the gate
  - Determine the voltage gain
- Explain the effect of an ac load on the voltage gain
- Discuss phase inversion
- Determine amplifier input resistance
- Describe and analyze D-MOSFET amplifier operation
- Describe and analyze E-MOSFET amplifier operation
  - Determine input resistance

FET AC Model

An equivalent FET model is shown in Figure 9–1. In part (a), the internal resistance, r'_{gs}, appears between the gate and source, and a current source equal to g_mV_{gs} appears between the drain and source. Also, the internal drain-to-source resistance, r'_{ds}, is included. In part (b), a simplified ideal model is shown. The resistance, r'_{gs}, is assumed to be extremely large so that an open circuit between the gate and source can be assumed. Also, r'_{ds} is assumed large enough to neglect.

▶ FIGURE 9–1

Internal FET equivalent circuits.

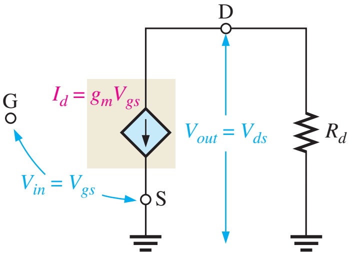


(a) Complete

(b) Simplified

An ideal FET circuit model with an external ac drain resistance is shown in Figure 9–2. The ac voltage gain of this circuit is V_{out}/V_{in}, where $V_{in} = V_{gs}$ and $V_{out} = V_{ds}$. The voltage gain expression is, therefore,

$$A_v = \frac{V_{ds}}{V_{gs}}$$



▲ FIGURE 9–2

Simplified FET equivalent circuit with an external ac drain resistance.

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[*] **The following website is a tutorial for the TI-89 calculator: *http://www.math.lsu.edu/~neal/TI_89/index.html***

From the equivalent circuit,

$$V_{ds} = I_d R_d$$

and from the definition of transconductance, $g_m = I_d/V_{gs}$,

$$V_{gs} = \frac{I_d}{g_m}$$

Substituting the two preceding expressions into the equation for voltage gain yields

$$A_v = \frac{I_d R_d}{I_d/g_m} = \frac{g_m I_d R_d}{I_d}$$

$$\boldsymbol{A_v = g_m R_d} \qquad \text{Equation 9–1}$$

EXAMPLE 9–1

A certain JFET has a $g_m = 4$ mS. With an external ac drain resistance of 1.5 kΩ, what is the ideal voltage gain?

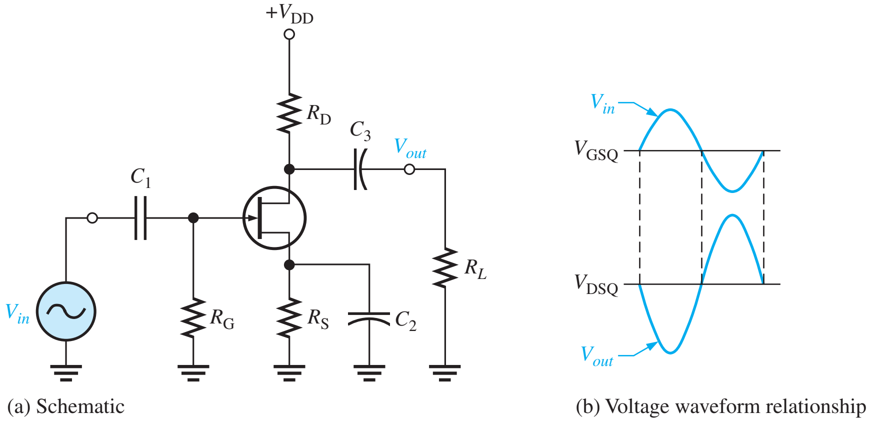
Solution $A_v = g_m R_d = (4\text{ mS})(1.5\text{ k}\Omega) = \mathbf{6}$

*Related Problem** What is the ideal voltage gain when $g_m = 6000\ \mu\text{S}$ and $R_d = 2.2\text{ k}\Omega$?

***Answers can be found at www.pearsonhighered.com/floyd.**

JFET Amplifier Operation

A **common-source** JFET amplifier is one in which the ac input signal is applied to the gate and the ac output signal is taken from the drain. The source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source *n*-channel JFET amplifier with an ac source capacitively coupled to the gate is shown in Figure 9–3(a). The resistor, R_G, serves two purposes: It keeps the gate at approximately 0 V dc (because I_{GSS} is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. A bias voltage is produced by the drop across R_S. The bypass capacitor, C_2, keeps the source of the JFET at ac ground.



(a) Schematic

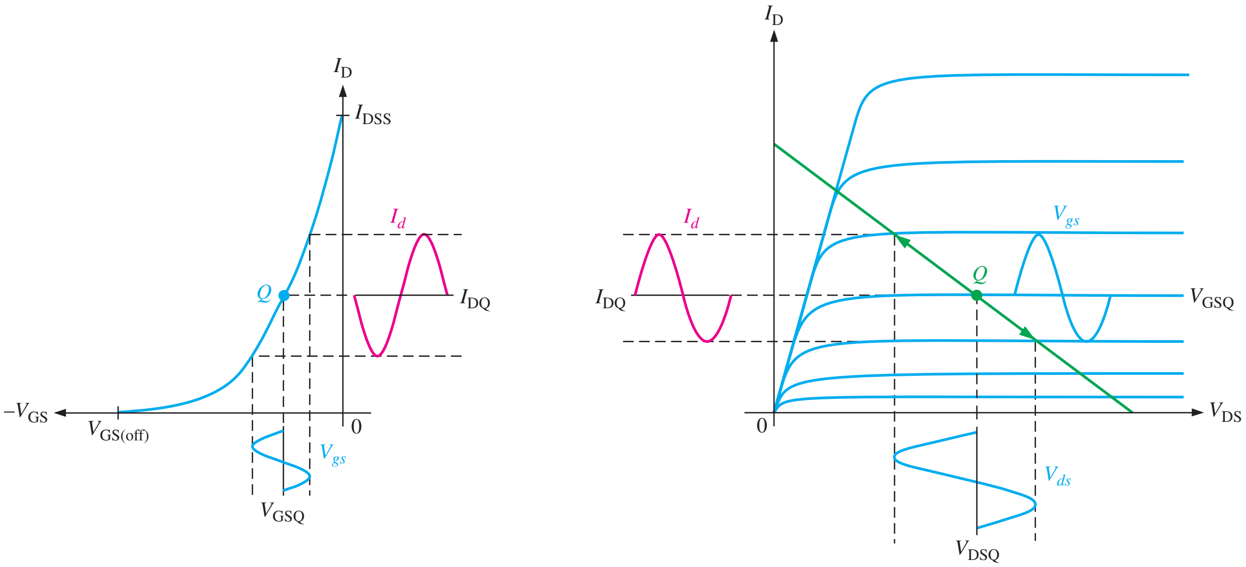
(b) Voltage waveform relationship

◀ FIGURE 9–3

JFET common-source amplifier.

The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (V_{GSQ}), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across R_D also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (V_{DSQ}) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure 9–3(b).

A Graphical Picture The operation just described for an *n*-channel JFET is illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure 9–4. Part (a) shows how a sinusoidal variation, V_{gs}, produces a corresponding sinusoidal variation in I_d. As V_{gs} swings from its Q-point value to a more negative value, I_d decreases from its Q-point value. As V_{gs} swings to a less negative value, I_d increases. Figure 9–4(b) shows a view of the same operation using the drain curves. The signal at the gate drives the drain current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the I_{D} axis and down to the V_{DS} axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.



(a) JFET (*n*-channel) transfer characteristic curve showing signal operation

(b) JFET (*n*-channel) drain curves showing signal operation

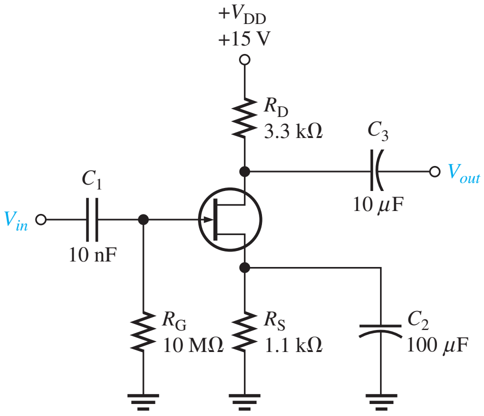
▲ **FIGURE 9–4**

JFET characteristic curves.

DC Analysis

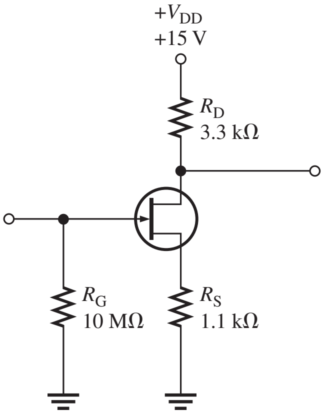
The first step in analyzing a JFET amplifier is to determine the dc conditions including I_{D} and V_{S}. I_{D} determines the *Q*-point for an amplifier and enables you to calculate V_{D}, so it is useful to determine its value. It can be found either graphically or mathematically. The graphical approach, introduced in Chapter 8 using the transconductance curve, will be applied to an amplifier here. The same result can be obtained by expanding Equation 8–1, which is the mathematical description of the transconductance curve. The amplifier shown in Figure 9–5 will be used to illustrate both approaches. To simplify the dc analysis, the equivalent circuit is shown in Figure 9–6; capacitors appear open to dc, so they are removed.

Graphical Approach Recall from Section 8–2 that the JFET universal transfer characteristic (transconductance curve) illustrates the relationship between the output current and the input voltage. The endpoints of the transconductance curve are at I_{DSS} and $V_{\mathrm{GS(off)}}$. A dc graphical solution is done by plotting the load line (for the self-biased case shown) on the same plot and reading the values of V_{GS} and I_{D} at the intersection of these plots (*Q*-point).



▲ FIGURE 9–5

JFET common-source amplifier.



▲ FIGURE 9–6

DC equivalent for the amplifier in Figure 9–5.

EXAMPLE 9–2 Determine I_D and V_{GS} at the Q-point for the JFET amplifier in Figure 9–6. The typical I_{DSS} for this particular JFET is 4.3 mA and $V_{GS(off)}$ is -7.7 V.

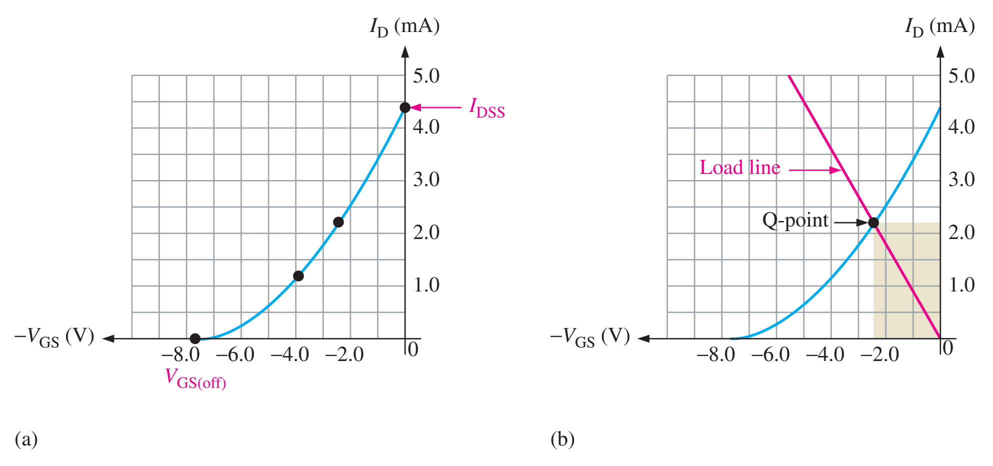
Solution Plot the transconductance curve. The end points are at I_{DSS} and $V_{GS(off)}$. You can plot two additional points quickly by noting from the universal curve in Figure 8–12, that

$$V_{GS} = 0.3V_{GS(off)} = -2.31\text{ V} \qquad \text{when } I_D = \frac{I_{DSS}}{2} = 2.15\text{ mA}$$

and

$$V_{GS} = 0.5V_{GS(off)} = -3.85\text{ V} \qquad \text{when } I_D = \frac{I_{DSS}}{4} = 1.075\text{ mA}$$

For this particular JFET, the points are plotted as shown in Figure 9–7(a). Recall from Chapter 8 that the load line starts at the origin and goes to a point where $I_D = I_{DSS}$ and $V_{GS} = I_{DSS}R_S$. Add the load line to the graph and read the I_D and V_{GS} values from the intersection (Q-point), as shown in Figure 9–7(b). For the graph shown, $I_D =$ **2.2 mA** and $V_{GS} =$ **−2.4 V.**



▲ FIGURE 9–7

Related Problem Show the Q-point if the transistor is replaced with one with an $I_{DSS} = 5.0$ mA and a $V_{GS(off)} = -8$ V.

Mathematical Approach The mathematical approach is more tedious than the graphical approach because it involves expanding the equation into quadratic form and solving the quadratic equation. To determine I_D mathematically from the known quantities, substitute $V_{GS} = I_D R_S$ into Equation 8–1. The result is shown as Equation 9–2, which has I_D on both sides. Isolating I_D requires the solution of the quadratic form, which is given in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd. A much easier approach is to enter Equation 9–2 into a graphing calculator such as the TI-89. The steps for determining I_D using the TI-89 are given in Example 9–3.

Equation 9–2

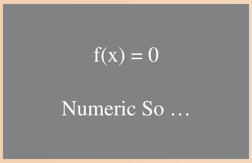
$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$$

EXAMPLE 9–3

Determine I_D and V_{GS} at the Q-point for the JFET amplifier in Figure 9–6 using the mathematical approach. The I_{DSS} for this particular JFET is 4.3 mA and $V_{GS(off)}$ is −7.7 V.

Solution To calculate I_D using the TI-89, follow these six steps.

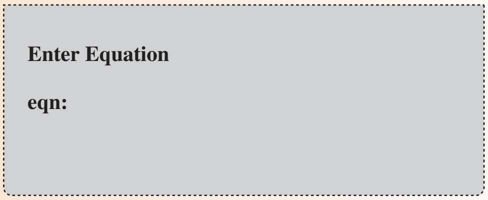
Step 1: On the Applications screen select the Numeric Solver logo.



f(x) = 0

Numeric So …

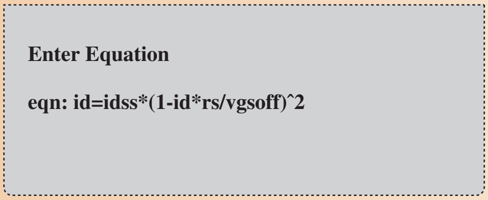
Step 2: Press ENTER to display the Numeric Solver screen.



Enter Equation

eqn:

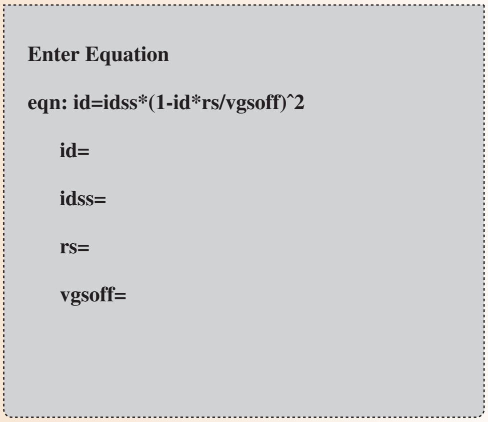
Step 3: Enter the equation. Each letter in the variables must be preceded by ALPHA.



Enter Equation

eqn: id=idss*(1-id*rs/vgsoff)ˆ2

Step 4: Press ENTER to display the variables.



Enter Equation

eqn: id=idss*(1-id*rs/vgsoff)ˆ2

id=

idss=

rs=

vgsoff=

Step 5: Enter the value of each variable except id.

```
Enter Equation

eqn: id=idss*(1-id*rs/vgsoff)^2

   id=

   idss=.0043

   rs=1100

   vgsoff=7.7
```

Step 6: Move the cursor to id and Press F2 to solve. The answer is **.0021037……**(2.104 mA).

Calculate V_{GS}.

$$V_{GS} = -I_D R_S = -(2.1\text{ mA})(1.1\text{ k}\Omega) = \mathbf{-2.31\ V}$$

Related Problem Calculate the solution for the Related Problem in Example 9–2.

AC Equivalent Circuit

To analyze the signal operation of the amplifier in Figure 9–5, develop an ac equivalent circuit as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that $X_C \cong 0$ at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The V_{DD} terminal is at a zero-volt ac potential and therefore acts as an ac ground.

The ac equivalent circuit is shown in Figure 9–8(a). Notice that the $+V_{DD}$ end of R_d and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.

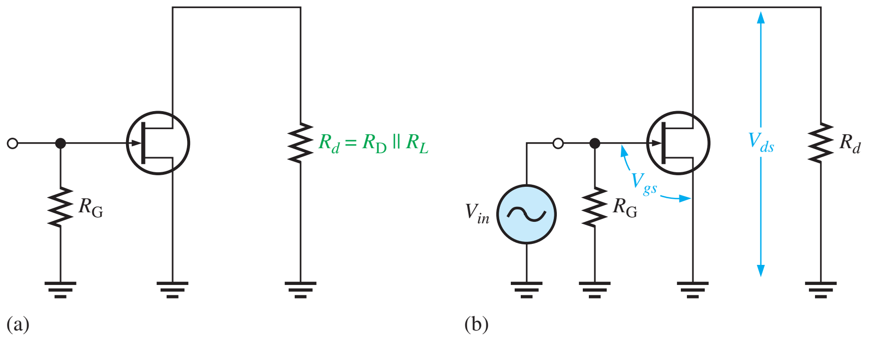


FIGURE 9–8

AC equivalent for the amplifier in Figure 9–5.

Signal Voltage at the Gate An ac voltage source is shown connected to the input in Figure 9–8(b). Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance.

$$V_{gs} = V_{in}$$

Voltage Gain The expression for JFET voltage gain that was given in Equation 9–1 applies to the common-source amplifier.

Equation 9–3

$$\boldsymbol{A_v = g_m R_d}$$

The output signal voltage V_{ds} at the drain is

$$V_{out} = V_{ds} = A_v V_{gs}$$

or

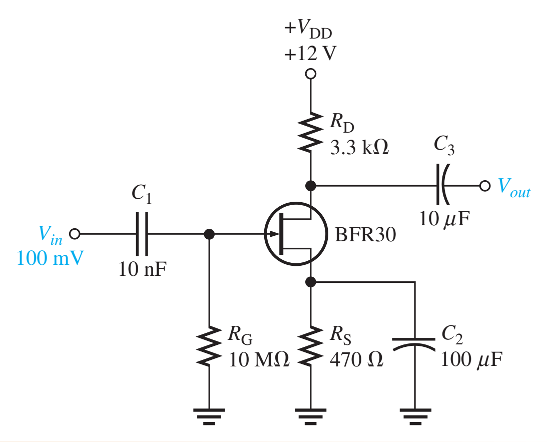
$$V_{out} = g_m R_d V_{in}$$

where $R_d = R_D \| R_L$ and $V_{in} = V_{gs}$.

EXAMPLE 9–4

What is the total output voltage for the unloaded amplifier in Figure 9–9? I_{DSS} is 4.3 mA; $V_{GS(off)}$ is −2.7 V.

▶ FIGURE 9–9



Solution Use either a graphical approach, as shown in Example 9–2, or a mathematical approach with a graphing calculator, as shown in Example 9–3, to determine I_D. The calculator solution gives

$$I_D = 1.91\text{ mA}$$

Using this value, calculate V_D.

$$V_D = V_{DD} - I_D R_D = 12\text{ V} - (1.91\text{ mA})(3.3\text{ k}\Omega) = 5.70\text{ V}$$

Next calculate g_m as follows:

$$V_{GS} = -I_D R_S = -(1.91\text{ mA})(470\ \Omega) = -0.90\text{ V}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|} = \frac{2(4.3\text{ mA})}{2.7\text{ V}} = 3.18\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = 3.18\text{ mS}\left(1 - \frac{-0.90\text{ V}}{-2.7\text{ V}}\right) = 2.12\text{ mS}$$

Finally, find the ac output voltage.

$$V_{out} = A_v V_{in} = g_m R_D V_{in} = (2.12\text{ mS})(3.3\text{ k}\Omega)(100\text{ mV}) = \mathbf{700\text{ mV}}$$

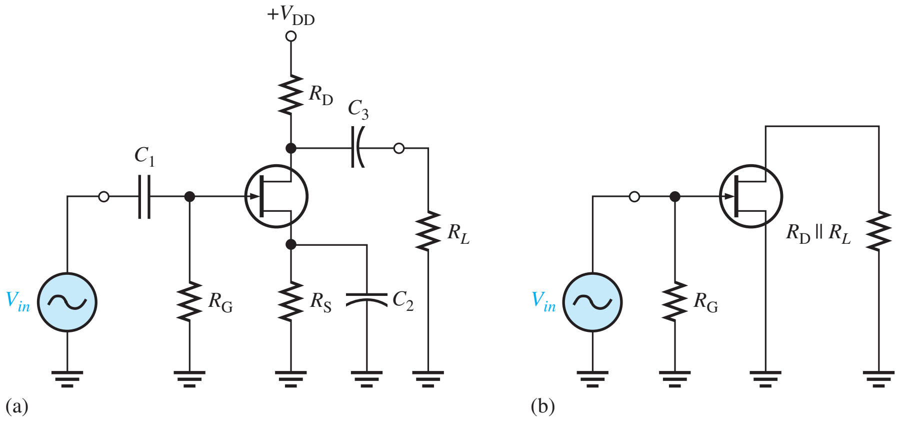
Related Problem Confirm the calculator solution for I_D is correct by using the graphical method.

Effect of an AC Load on Voltage Gain

When a load is connected to an amplifier's output through a coupling capacitor, as shown in Figure 9–10(a), the ac drain resistance is effectively R_D in parallel with R_L because the upper end of R_D is at ac ground. The ac equivalent circuit is shown in Figure 9–10(b). The total ac drain resistance is

$$R_d = \frac{R_D R_L}{R_D + R_L}$$

The effect of R_L is to reduce the unloaded voltage gain, as Example 9–5 illustrates.



◀ **FIGURE 9–10**

JFET amplifier and its ac equivalent.

EXAMPLE 9–5 If a 4.7 kΩ load resistor is ac coupled to the output of the amplifier in Example 9–4, what is the resulting rms output voltage?

Solution The ac drain resistance is

$$R_d = \frac{R_D R_L}{R_D + R_L} = \frac{(3.3\text{ k}\Omega)(4.7\text{ k}\Omega)}{8\text{ k}\Omega} = 1.94\text{ k}\Omega$$

Calculation of V_{out} yields

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (2.12\text{ mS})(1.94\text{ k}\Omega)(100\text{ mV}) = \mathbf{411\text{ mV rms}}$$

The unloaded ac output voltage was 700 mV in Example 9–4.

Related Problem If a 3.3 kΩ load resistor is ac coupled to the output of the amplifier in Example 9–4, what is the resulting rms output voltage?

Phase Inversion

The output voltage (at the drain) is 180° out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, $-A_v$. Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance

Because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased *pn* junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is the gate-to-ground resistor, R_G, in parallel with the FET's input resistance, V_{GS}/I_{GSS}. The reverse leakage current, I_{GSS}, is typically given on the datasheet for a specific value of V_{GS} so that the input resistance of the device can be calculated.

Equation 9–4

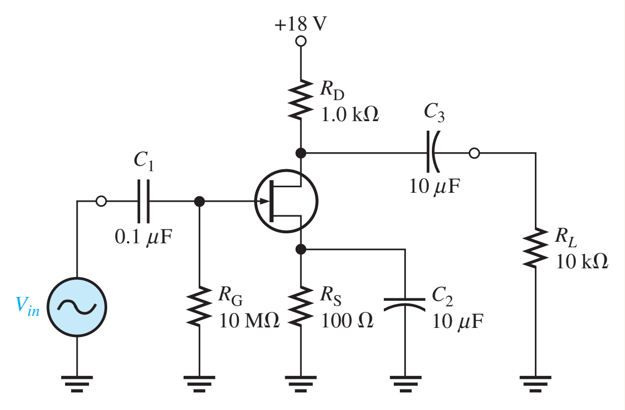
$$\boldsymbol{R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}}\right)}$$

Since the term V_{GS}/I_{GSS} is typically much larger than R_G, the input resistance is very close to the value of R_G, as Example 9–6 shows.

EXAMPLE 9–6

What input resistance is seen by the signal source in Figure 9–11? $I_{GSS} = 30$ nA at $V_{GS} = 10$ V.

▶ FIGURE 9–11



Solution The input resistance at the gate of the JFET is

$$R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{10\text{ V}}{30\text{ nA}} = 333\text{ M}\Omega$$

The input resistance seen by the signal source is

$$R_{in} = R_G \| R_{IN(gate)} = 10\text{ M}\Omega \| 333\text{ M}\Omega = \mathbf{9.7\text{ M}\Omega}$$

For all practical purposes, R_{IN} can be assumed equal to R_G.

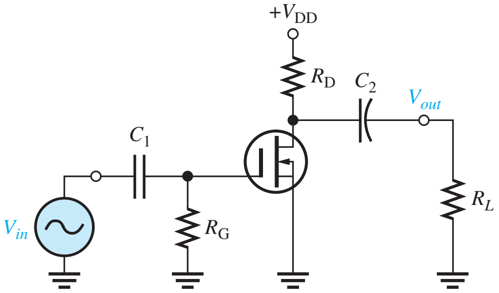
Related Problem How much is the total input resistance if $I_{GSS} = 1$ nA at $V_{GS} = 10$ V?

D-MOSFET Amplifier Operation

A zero-biased common-source n-channel D-MOSFET with an ac source capacitively coupled to the gate is shown in Figure 9–12. The gate is at approximately 0 V dc and the source terminal is at ground, thus making $V_{GS} = 0$ V.

▶ FIGURE 9–12

Zero-biased D-MOSFET common-source amplifier.



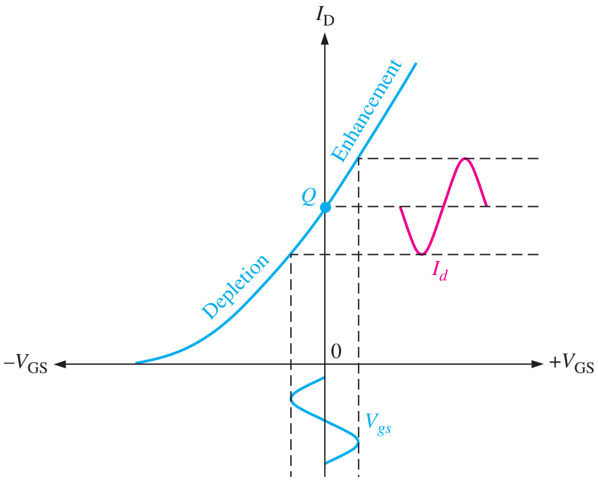


FIGURE 9–13

Depletion-enhancement operation of D-MOSFET shown on transfer characteristic curve.

The signal voltage causes V_{gs} to swing above and below its zero value, producing a swing in I_d, as shown in Figure 9–13. The negative swing in V_{gs} produces the depletion mode, and I_d decreases. The positive swing in V_{gs} produces the enhancement mode, and I_d increases. Note that the enhancement mode is to the right of the vertical axis ($V_{GS} = 0$), and the depletion mode is to the left. The dc analysis of this amplifier is somewhat easier than for a JFET because $I_D = I_{DSS}$ at $V_{GS} = 0$. Once I_D is known, the analysis involves calculating only V_D.

$$V_D = V_{DD} - I_D R_D$$

The ac analysis is the same as for the JFET amplifier.

E-MOSFET Amplifier Operation

A common-source n-channel E-MOSFET with voltage-divider bias with an ac source capacitively coupled to the gate is shown in Figure 9–14. The gate is biased with a positive voltage such that $V_{GS} > V_{GS(th)}$.

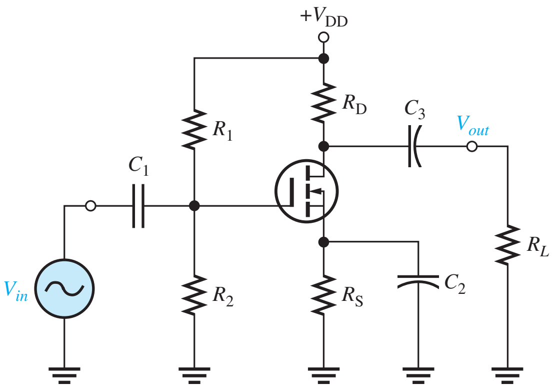
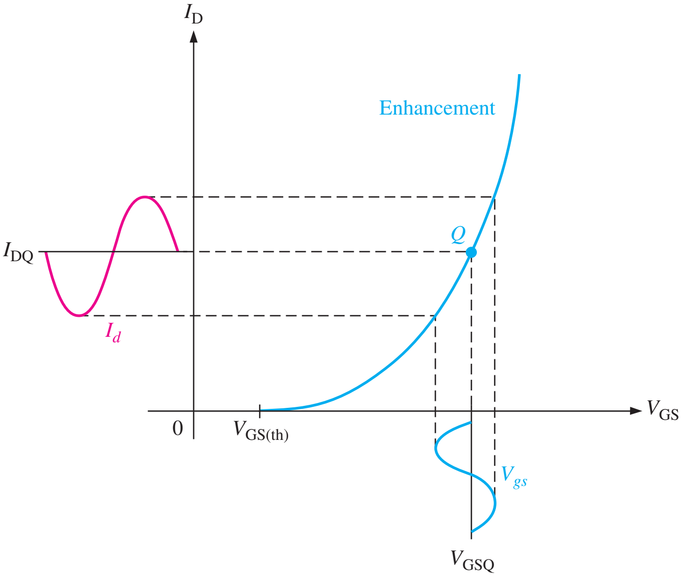


FIGURE 9–14

Common-source E-MOSFET amplifier with voltage-divider bias.

As with the JFET and D-MOSFET, the signal voltage produces a swing in V_{gs} above and below its Q-point value, V_{GSQ}. This, in turn, causes a swing in I_d above and below its Q-point value, I_{DQ}, as illustrated in Figure 9–15. Operation is entirely in the enhancement mode.

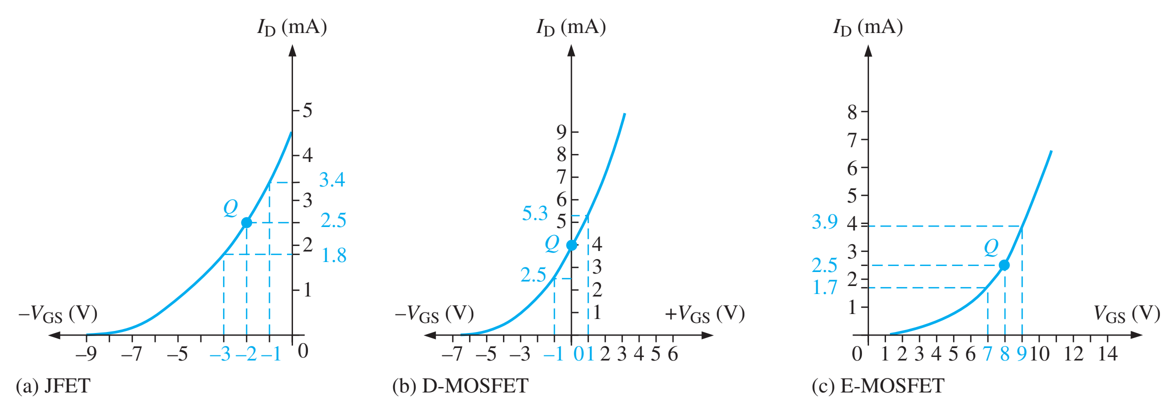


▶ FIGURE 9–15

E-MOSFET (*n*-channel) operation shown on transfer characteristic curve.

EXAMPLE 9–7

Transfer characteristic curves for a particular *n*-channel JFET, D-MOSFET, and E-MOSFET are shown in Figure 9–16. Determine the peak-to-peak variation in I_d when V_{gs} is varied ±1 V about its Q-point value for each curve.



(a) JFET (b) D-MOSFET (c) E-MOSFET

▲ FIGURE 9–16

Solution

(a) The JFET Q-point is at $V_{GS} = -2$ V and $I_D = 2.5$ mA. From the graph in Figure 9–16(a), $I_D = 3.4$ mA when $V_{GS} = -1$ V, and $I_D = 1.8$ mA when $V_{GS} = -3$ V. The peak-to-peak drain current is therefore **1.6 mA.**

(b) The D-MOSFET Q-point is at $V_{GS} = 0$ V and $I_D = I_{DSS} = 4$ mA. From the graph in Figure 9–16(b), $I_D = 2.5$ mA when $V_{GS} = -1$ V, and $I_D = 5.3$ mA when $V_{GS} = +1$ V. The peak-to-peak drain current is therefore **2.8 mA.**

(c) The E-MOSFET Q-point is at $V_{GS} = +8$ V and $I_D = 2.5$ mA. From the graph in Figure 9–16(c), $I_D = 3.9$ mA when $V_{GS} = +9$ V, and $I_D = 1.7$ mA when $V_{GS} = +7$ V. The peak-to-peak drain current is therefore **2.2 mA.**

Related Problem

As the Q-point is moved toward the bottom end of the curves in Figure 9–16, does the variation in I_D increase or decrease for the same ±1 V variation in V_{GS}? In addition to the change in the amount that I_D varies, what else will happen?

The circuit in Figure 9–14 uses voltage-divider bias to achieve a V_{GS} above threshold. The general dc analysis proceeds as follows using the E-MOSFET characteristic equation (Equation 8–4) to solve for I_D.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

The voltage gain expression is the same as for the JFET and D-MOSFET circuits. The ac input resistance is

$$\boldsymbol{R_{in} = R_1 \| R_2 \| R_{IN(gate)}}$$

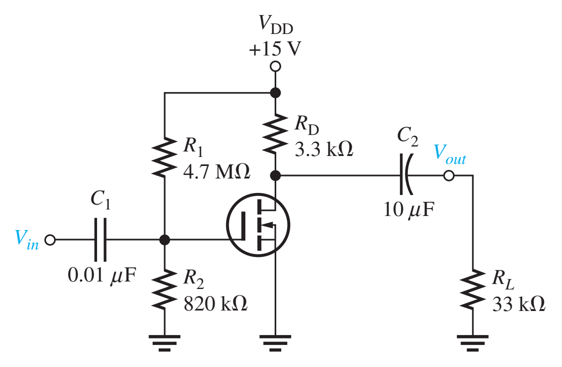
Equation 9–5

where $R_{IN(gate)} = V_{GS}/I_{GSS}$.

EXAMPLE 9–8

A common-source amplifier using an E-MOSFET is shown in Figure 9–17. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. Assume that for this particular device, $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V, $V_{GS(th)} = 2$ V, and $g_m = 23$ mS. $V_{in} = 25$ mV.

▶ FIGURE 9–17



Solution

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{820\text{ k}\Omega}{5.52\text{ M}\Omega}\right)15\text{ V} = \mathbf{2.23\ V}$$

For $V_{GS} = 4$ V,

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = 50\text{ mA/V}^2$$

Therefore,

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(2.23\text{ V} - 2\text{ V})^2 = \mathbf{2.65\ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 15\text{ V} - (2.65\text{ mA})(3.3\text{ k}\Omega) = \mathbf{6.26\ V}$$

$$R_d = R_D \| R_L = 3.3\text{ k}\Omega \| 33\text{ k}\Omega = 3\text{ k}\Omega$$

The ac output voltage is

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (23\text{ mS})(3\text{ k}\Omega)(25\text{ mV}) = \mathbf{1.73\ V}$$

Related Problem For the E-MOSFET in Figure 9–17, $I_{D(on)} = 25$ mA at $V_{GS} = 5$ V, $V_{GS(th)} = 1.5$ V, and $g_m = 10$ mS. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. $V_{in} = 25$ mV.

Open the Multisim file E09-08 in the Examples folder on the companion website. Determine I_D, V_{DS}, and V_{out} using the specified value of V_{in}. Compare with the calculated values.

SECTION 9–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. One FET has a transconductance of 3000 μS and another has a transconductance of 3.5 mS. Which one can produce the higher voltage gain, with all other circuit components the same?
2. A FET circuit has a $g_m = 2500\ \mu\text{S}$ and an $R_d = 10\ \text{k}\Omega$. Ideally, what voltage gain can it produce?
3. When V_{gs} is at its positive peak, at what points are I_d and V_{ds}?
4. What is the difference between V_{gs} and V_{GS}?
5. What factors determine the voltage gain of a common-source FET amplifier?
6. A certain amplifier has an $R_D = 1.0\ \text{k}\Omega$. When a load resistance of 1.0 kΩ is capacitively coupled to the drain, how much does the gain change?

9–2 THE COMMON-DRAIN AMPLIFIER

The common-drain (CD) amplifier is comparable to the common-collector BJT amplifier. Recall that the CC amplifier is called an emitter-follower. Similarly, the common-drain amplifier is called a source-follower because the voltage at the source is approximately the same amplitude as the input (gate) voltage and is in phase with it. In other words, the source voltage follows the gate input voltage.

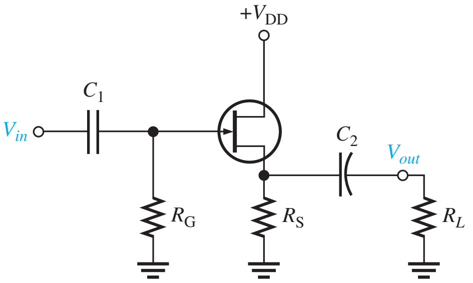
After completing this section, you should be able to

- ☐ **Explain and analyze the operation of common-drain FET amplifiers**
  - ◆ Define the term *source-follower*
- ☐ Analyze common-drain JFET amplifier operation
  - ◆ Determine the voltage gain ◆ Determine the input resistance ◆ Use a datasheet

A **common-drain** JFET amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain JFET amplifier is shown in Figure 9–18. A common-drain amplifier is also called a **source-follower**. Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, C_1, and the output signal is coupled to the load resistor through C_2.

▶ FIGURE 9–18

JFET common-drain amplifier (source-follower).



Voltage Gain

As in all amplifiers, the voltage gain is $A_v = V_{out}/V_{in}$. For the source-follower, V_{out} is I_dR_s and V_{in} is $V_{gs} + I_dR_s$, as shown in Figure 9–19. Therefore, the gate-to-source

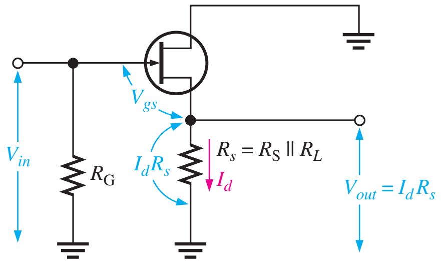


FIGURE 9–19

Voltages in a common-drain amplifier with a load resistor shown combined with R_S.

voltage gain is $I_dR_s/(V_{gs} + I_dR_s)$. Substituting $I_d = g_mV_{gs}$ into the expression gives the following result:

$$A_v = \frac{g_mV_{gs}R_s}{V_{gs} + g_mV_{gs}R_s}$$

The V_{gs} terms cancel, so

$$\boldsymbol{A_v = \frac{g_mR_s}{1 + g_mR_s}}$$

Equation 9–6

Notice here that the gain is always slightly less than 1. If $g_mR_s \gg 1$, then a good approximation is $A_v \cong 1$. Since the output voltage is at the source, it is in phase with the gate (input) voltage.

Input Resistance

Because the input signal is applied to the gate, the input resistance seen by the input signal source is extremely high, just as in the common-source amplifier configuration. The gate resistor, R_G, in parallel with the input resistance looking in at the gate is the total input resistance.

$$\boldsymbol{R_{in} = R_G \parallel R_{IN(gate)}}$$

Equation 9–7

where $R_{IN(gate)} = V_{GS}/I_{GSS}$.

EXAMPLE 9–9

Determine the voltage gain of the amplifier in Figure 9–20 using the datasheet information in Figure 9–21. Also, determine the input resistance. Use minimum datasheet values where available. V_{DD} is negative because it is a *p*-channel device.

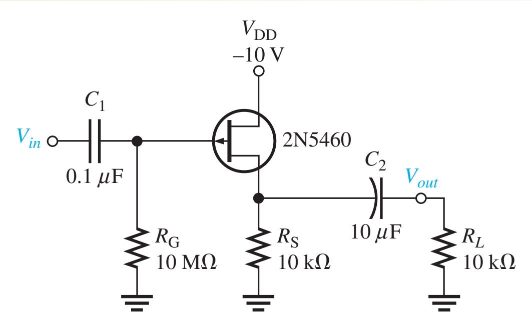
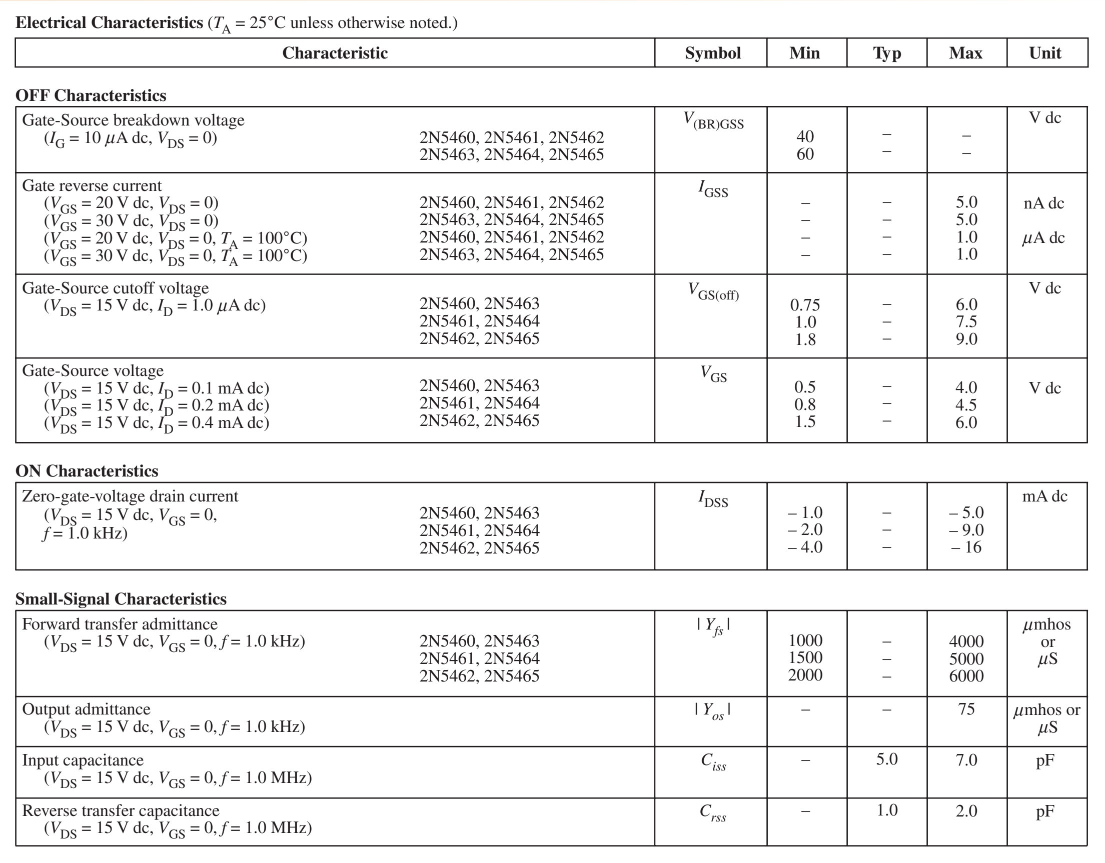


FIGURE 9–20



Electrical Characteristics (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF Characteristics						
Gate-Source breakdown voltage (I_G = 10 μA dc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	$V_{(BR)GSS}$	40	–	–	V dc
	2N5463, 2N5464, 2N5465		60	–	–	
Gate reverse current (V_{GS} = 20 V dc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	I_{GSS}	–	–	5.0	nA dc
(V_{GS} = 30 V dc, V_{DS} = 0)	2N5463, 2N5464, 2N5465		–	–	5.0	
(V_{GS} = 20 V dc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462		–	–	1.0	μA dc
(V_{GS} = 30 V dc, V_{DS} = 0, T_A = 100°C)	2N5463, 2N5464, 2N5465		–	–	1.0	
Gate-Source cutoff voltage (V_{DS} = 15 V dc, I_D = 1.0 μA dc)	2N5460, 2N5463	$V_{GS(off)}$	0.75	–	6.0	V dc
	2N5461, 2N5464		1.0	–	7.5	
	2N5462, 2N5465		1.8	–	9.0	
Gate-Source voltage (V_{DS} = 15 V dc, I_D = 0.1 mA dc)	2N5460, 2N5463	V_{GS}	0.5	–	4.0	V dc
(V_{DS} = 15 V dc, I_D = 0.2 mA dc)	2N5461, 2N5464		0.8	–	4.5	
(V_{DS} = 15 V dc, I_D = 0.4 mA dc)	2N5462, 2N5465		1.5	–	6.0	
ON Characteristics						
Zero-gate-voltage drain current (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463	I_{DSS}	– 1.0	–	– 5.0	mA dc
	2N5461, 2N5464		– 2.0	–	– 9.0	
	2N5462, 2N5465		– 4.0	–	– 16	
Small-Signal Characteristics						
Forward transfer admittance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463	$\lvert Y_{fs} \rvert$	1000	–	4000	μmhos or μS
	2N5461, 2N5464		1500	–	5000	
	2N5462, 2N5465		2000	–	6000	
Output admittance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 kHz)		$\lvert Y_{os} \rvert$	–	–	75	μmhos or μS
Input capacitance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	5.0	7.0	pF
Reverse transfer capacitance (V_{DS} = 15 V dc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.0	2.0	pF

▲ FIGURE 9–21

Partial datasheet for the 2N5460–2N5465 *p*-channel JFETs.

Solution Since $R_L \gg R_S$, $R_s \cong R_S$. From the partial datasheet in Figure 9–21, $g_m = y_{fs} =$ 1000 μS (minimum). The voltage gain is

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(1000\ \mu\text{S})(10\ \text{k}\Omega)}{1 + (1000\ \mu\text{S})(10\ \text{k}\Omega)} = \mathbf{0.909}$$

From the datasheet, $I_{GSS} = 5$ nA (maximum) at $V_{GS} = 20$ V. Therefore,

$$R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{20\ \text{V}}{5\ \text{nA}} = 4000\ \text{M}\Omega$$

$$R_{IN} = R_G \parallel R_{IN(gate)} = 10\ \text{M}\Omega \parallel 4000\ \text{M}\Omega \cong \mathbf{10\ M\Omega}$$

Related Problem If the maximum value of g_m of the 2N5460 JFET in the source-follower of Figure 9–20 is used, what is the voltage gain?

Open the Multisim file E09-09 in the Examples folder on the companion website. Measure the voltage gain using an input voltage of 10 mV rms to see how it compares with the calculated value.

SECTION 9–2 CHECKUP

1. What is the ideal maximum voltage gain of a common-drain amplifier?
2. What factors influence the voltage gain of a common-drain amplifier?

9–3 THE COMMON-GATE AMPLIFIER

The common-gate FET amplifier configuration is comparable to the common-base BJT amplifier. Like the CB, the common-gate (CG) amplifier has a low input resistance. This is different from the CS and CD configurations, which have very high input resistances.

After completing this section, you should be able to

- **Explain and analyze the operation of common-gate FET amplifiers**
- Analyze common-gate JFET amplifier operation
  - Determine the voltage gain
  - Determine the input resistance
- Describe and analyze the cascode amplifier
  - Determine the voltage gain
  - Determine the input resistance

Common-Gate Amplifier Operation

A self-biased **common-gate** amplifier is shown in Figure 9–22. The gate is connected directly to ground. The input signal is applied at the source terminal through C_1. The output is coupled through C_2 from the drain terminal.

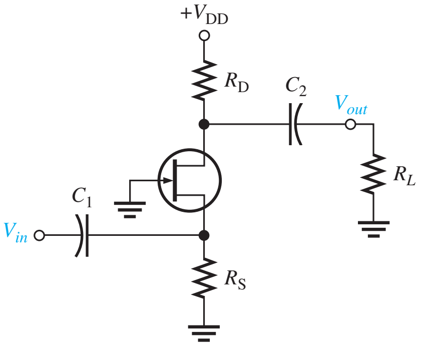


FIGURE 9–22

JFET common-gate amplifier.

Voltage Gain The voltage gain from source to drain is developed as follows:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_d}{V_{gs}} = \frac{I_dR_d}{V_{gs}} = \frac{g_mV_{gs}R_d}{V_{gs}}$$

$$\boldsymbol{A_v = g_mR_d} \qquad \text{Equation 9–8}$$

where $R_d = R_D \| R_L$. Notice that the gain expression is the same as for the common-source JFET amplifier.

Input Resistance As you have seen, both the common-source and common-drain configurations have extremely high input resistances because the gate is the input terminal. In contrast, the common-gate configuration where the source is the input terminal has a low input resistance. This is shown as follows. First, the input current is equal to the drain current.

$$I_{in} = I_s = I_d = g_mV_{gs}$$

Second, the input voltage equals V_{gs}.

$$V_{in} = V_{gs}$$

Therefore, the input resistance at the source terminal is

$$R_{in(source)} = \frac{V_{in}}{I_{in}} = \frac{V_{gs}}{g_mV_{gs}}$$

$$\boldsymbol{R_{in(source)} = \frac{1}{g_m}} \qquad \text{Equation 9–9}$$

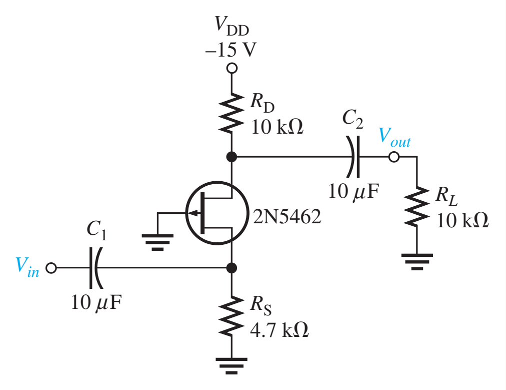
If, for example, g_m has a value of 4000 μS, then

$$R_{in(source)} = \frac{1}{4000\ \mu\text{S}} = 250\ \Omega$$

EXAMPLE 9–10

Determine the minimum voltage gain and input resistance of the amplifier in Figure 9–23. V_{DD} is negative because it is a *p*-channel device.

► FIGURE 9–23



Solution From the datasheet in Figure 9–21, $g_m = 2000\ \mu\text{S}$ minimum. This common-gate amplifier has a load resistor, so the effective drain resistance is $R_D \| R_L$ and the minimum voltage gain is

$$A_v = g_m(R_D \| R_L) = (2000\ \mu\text{S})(10\ \text{k}\Omega \| 10\ \text{k}\Omega) = \mathbf{10}$$

The input resistance at the source terminal is

$$R_{in(source)} = \frac{1}{g_m} = \frac{1}{2000\ \mu\text{S}} = 500\ \Omega$$

The signal source actually sees R_S in parallel with $R_{in(source)}$, so the total input resistance is

$$R_{in} = R_{in(source)} \| R_S = 500\ \Omega \| 4.7\ \text{k}\Omega = \mathbf{452\ \Omega}$$

Related Problem What is the input resistance in Figure 9–23 if R_S is changed to 10 kΩ?

Open the Multisim file E09-10 in the Examples folder on the companion website. Measure the voltage using a 10 mV rms input voltage.

The Cascode Amplifier

One application in which the common-gate configuration is found is the cascode amplifier, commonly used for RF (radio frequency) applications. A **cascode** amplifier is one in which a common-source amplifier and a common-gate amplifier are connected in a series arrangement. BJTs can also be used to form cascode amplifiers (a common-emitter and a common-base). A JFET cascode amplifier circuit is shown in Figure 9–24. The input stage is a common-source amplifier, and its load is a common-gate amplifier connected in the drain circuit.

The cascode amplifier using JFETs provides a very high input resistance and significantly reduces capacitive effects to allow for operation at much higher frequencies than a common-source amplifier alone. Internal capacitances, which exist in every type of transistor, become significant at higher frequencies and reduce the gain of inverting amplifiers as described by the Miller effect, covered in Chapter 10. The first stage is a CS amplifier that inverts the signal. However, the gain is very low because of the low input resistance of

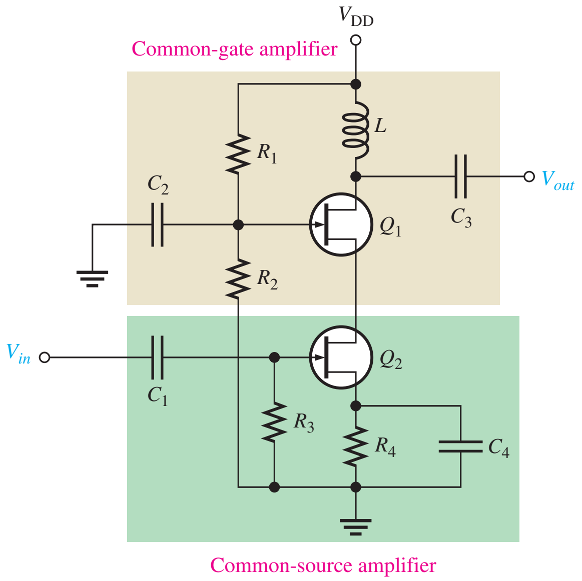


FIGURE 9–24

A JFET cascode amplifier.

the CB amplifier that it is driving. As a result, the effect of internal capacitances on the high-frequency response is very small. The second stage is a CG amplifier that does not invert the signal, so it can have high gain without degrading the high-frequency response. The combination of the two amplifiers provides the best of both circuits, resulting in high gain, high input resistance, and an excellent high-frequency response.

The voltage gain of the cascode amplifier in Figure 9–24 is a product of the gains of both the CS and the CG stages. However, as mentioned, the gain is primarily provided by the CG amplifier.

$$A_v = A_{v(\text{CS})}A_{v(\text{CG})} = (g_{m(\text{CS})}R_d)(g_{m(\text{CG})}X_L)$$

Since R_d of the CS amplifier stage is the input resistance of the CG stage and X_L is the reactance of the inductor in the drain of the CG stage, the voltage gain is

$$A_v = \left(g_{m(\text{CS})}\left(\frac{1}{g_{m(\text{CG})}}\right)\right)(g_{m(\text{CG})}X_L) \cong g_{m(\text{CG})}X_L$$

assuming the transconductances of both transistors are approximately the same. From the equation you can see that the voltage gain increases with frequency because X_L increases. As the frequency continues to increase, eventually capacitance effects become significant enough to begin reducing the gain.

The input resistance to the cascade amplifier is the input resistance to the CS stage.

$$R_{in} = R_3 \,\|\, \left(\frac{V_{\text{GS}}}{I_{\text{GSS}}}\right)$$

EXAMPLE 9–11

For the cascode amplifier in Figure 9–24, the transistors are 2N5485s and have a minimum g_m (g_{fs}) of 3500 μS. Also, $I_{\text{GSS}} = -1$ nA at $V_{\text{GS}} = 20$ V. If $R_3 = 10$ MΩ and $L = 1.0$ mH, determine the voltage gain and the input resistance at a frequency of 100 MHz.

Solution

$$A_v \cong g_{m(\text{CG})}X_L = g_{m(\text{CG})}(2\pi fL) = (3500\ \mu\text{S})\,2\pi(100\ \text{MHz})(1.0\ \text{mH}) = \mathbf{2199}$$

$$R_{in} = R_3 \,\|\, \left(\frac{V_{\text{GS}}}{I_{\text{GSS}}}\right) = 10\ \text{M}\Omega \,\|\, \left(\frac{20\ \text{V}}{1\ \text{nA}}\right) = \mathbf{9.995\ M\Omega}$$

Related Problem

What happens to the voltage gain in the cascode amplifier if the inductance value is increased?

SECTION 9–3 CHECKUP

1. What is a major difference between a common-gate amplifier and the other two configurations?
2. What common factor determines the voltage gain and the input resistance of a common-gate amplifier?
3. Name the advantages of a cascode amplifier.

9–4 THE CLASS D AMPLIFIER

In Chapter 7, class A, class B, and class AB amplifiers were introduced. Those types of amplifiers are generally implemented with either BJTs or FETs. The class D amplifier, however, primarily uses only MOSFETs. The class D differs fundamentally from the other classes because its output transistors are switched *on* and *off* in response to an analog input instead of operating linearly over a continuous range of input values.

After completing this section, you should be able to

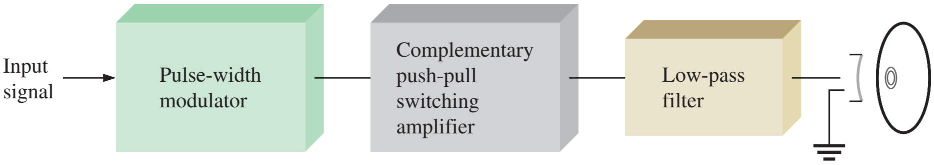
- ❑ **Discuss the operation of a class D amplifier**
- ❑ Explain pulse-width modulation (PWM)
  - ◆ Describe a basic pulse-width modulator ◆ Discuss frequency spectra
- ❑ Describe the complementary MOSFET stage
  - ◆ Determine the efficiency
- ❑ Describe the purpose of the low-pass filter
- ❑ Describe the signal flow through a class D amplifier

In a **class D amplifier**, the output transistors are operated as switches instead of operating linearly as in the classes A, B, and AB. An advantage in audio applications is that a class D amplifier can operate at a maximum theoretical efficiency of 100% compared to class A at 25% and class B/AB at 79%. In practice, efficiencies over 90% can be achieved with class D.

A basic block diagram of a class D amplifier driving a speaker is shown in Figure 9–25. It consists of a pulse-width modulator driving complementary MOSFET output transistors operating as switches and followed by a low-pass filter. Most class D amplifiers operate on dual-polarity power supplies. The MOSFETs are basically push-pull amplifiers that are operated as switching devices, rather than linear devices as in the case of class B amplifiers.

▶ FIGURE 9–25

Basic class D audio amplifier.



Pulse-Width Modulation (PWM)

Pulse-width modulation is a process in which an input signal is converted to a series of pulses with widths that vary proportionally to the amplitude of the input signal. This is illustrated in Figure 9–26 for one cycle of a sinusoidal signal. Notice that the pulse width is wider when the amplitude is positive and narrower when the amplitude is negative. The output will be a square wave if the input is zero.

The PWM signal is typically produced using a comparator circuit. Comparators are discussed in more detail in Chapter 13, but here is a basic explanation of how they work. A

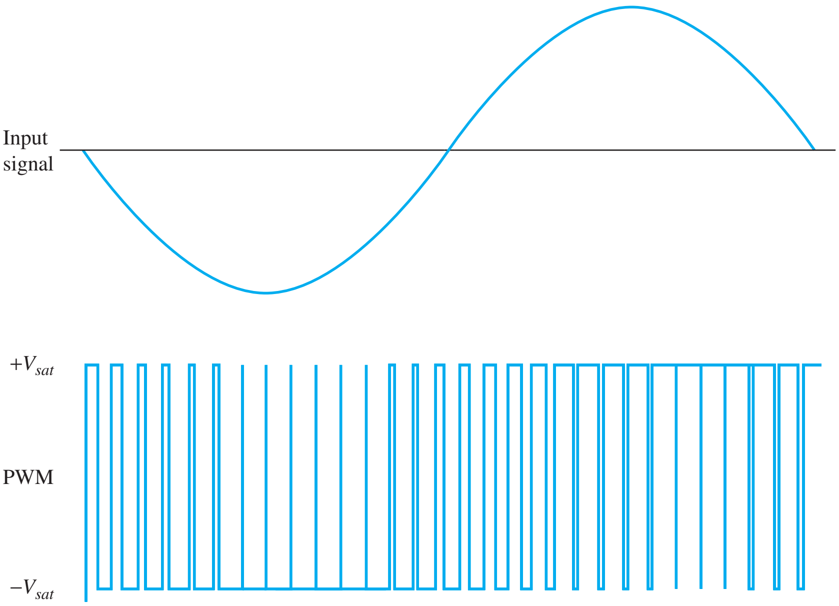


FIGURE 9–26

Pulse-width modulated sine wave.

comparator has two inputs and one output, as shown by the symbol in Figure 9–27. The input labeled + is called the noninverting input, and the input labeled − is the inverting input. When the voltage on the inverting input exceeds the voltage on the noninverting input, the comparator switches to its *negative* saturated output state. When the voltage on the noninverting input exceeds the voltage on the inverting input, the comparator switches to its *positive* saturated output state. This is illustrated in Figure 9–27 for one cycle of a sine wave voltage on the noninverting input and a higher frequency triangular wave voltage on the inverting input.

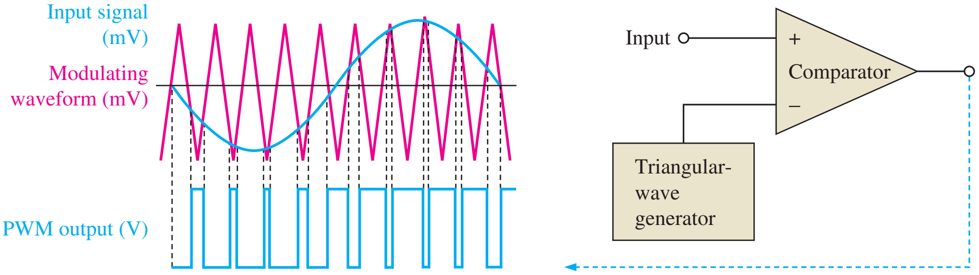


FIGURE 9–27

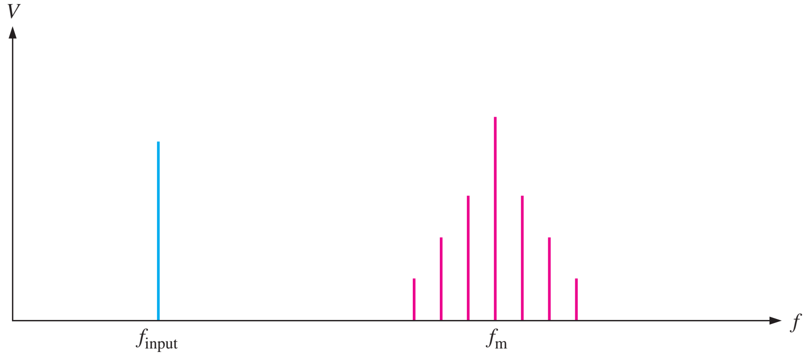
A basic pulse-width modulator.

The comparator inputs are typically very small voltages (mV range); and the comparator output is "rail-to-rail," which means that the positive maximum is near the positive dc supply voltage and the negative maximum is near the negative dc supply voltage. An output of ±12 V or 24 V peak-to-peak is not unusual. From this, you can see that the gain can be quite high. For example, if the input signal is 10 mVpp, the voltage gain is 24 Vpp/10 mVpp = 2400. Since the comparator output amplitude is constant for a specified range of input voltages, the gain is dependent on the input signal voltage. If the input signal is 100 mVpp, the output is still 24 Vpp, and the gain is 240 instead of 2400.

Frequency Spectra All nonsinusoidal waveforms are made up of harmonic frequencies. The frequency content of a particular waveform is called its *spectrum*. When the triangular waveform modulates the input sine wave, the resulting spectrum contains the sine wave frequency, f_{input}, plus the fundamental frequency of the triangular modulating signal, f_m, and harmonic frequencies above and below the fundamental frequency. These harmonic frequencies are due to the fast rise and fall times of the PWM signal and the flat areas between the pulses. A simplified frequency spectrum of a PWM signal is shown in Figure 9–28. The frequency of the triangular waveform must be significantly higher than the highest input signal frequency so that the lowest frequency harmonic is well above the range of input signal frequencies.

FIGURE 9–28

Frequency spectrum of a PWM signal.

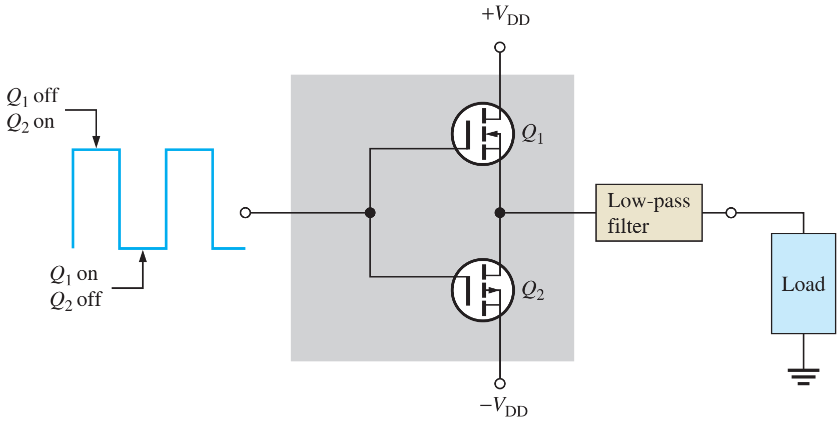


The Complementary MOSFET Stage

The MOSFETs are arranged in a common-source complementary configuration to provide power gain. Each transistor switches between the *on* state and the *off* state and when one transistor is *on,* the other one is *off,* as shown in Figure 9–29. When a transistor is *on,* there is very little voltage across it and, therefore, there is very little power dissipated even though it may have a high current through it. When a transistor is *off,* there is no current through it and, therefore, there is no power dissipated. The only time power is dissipated in the transistors is during the short switching time. Power delivered to a load can be very high because a load will have a voltage across it nearly equal to the supply voltages and a high current through it.

FIGURE 9–29

Complementary MOSFETs operating as switches to amplify power.



Efficiency When Q_1 is *on,* it is providing current to the load. However, ideally the voltage across it is zero so the internal power dissipated by Q_1 is

$$P_{DQ} = V_{Q1}I_L = (0\text{ V})I_L = 0\text{ W}$$

At the same time, Q_2 is *off* and the current through it is zero, so the internal power is

$$P_{DQ} = V_{Q2}I_L = V_{Q2}(0\text{ A}) = 0\text{ W}$$

Ideally, the output power to the load is $2V_QI_L$. The maximum ideal efficiency is, therefore,

$$\eta_{max} = \frac{P_{out}}{P_{tot}} = \frac{P_{out}}{P_{out} + P_{DQ}} = \frac{2V_QI_L}{2V_QI_L + 0\text{ W}} = 1$$

As a percentage, $\eta_{max} = 100\%$.

In a practical case, each MOSFET would have a few tenths of a volt across it in the *on* state. There is also a small internal power dissipation in the comparator and triangular wave generator. Also, power is dissipated during the finite switching time, so the ideal efficiency of 100% can never be reached in practice.

EXAMPLE 9–12

A certain class D amplifier dissipates an internal power of 100 mW in the comparator, triangular-wave generator, and filter combined. Each MOSFET in the complementary stage has a voltage of 0.4 V across it in the *on* state. The amplifier operates from ±15 V dc sources and provides 0.5 A to the load. Neglecting any voltage dropped across the filter, determine the output power and the overall efficiency.

Solution The output power to the load is

$$P_{out} = (V_{\text{DD}} - V_Q)I_L = (15\text{ V} - 0.4\text{ V})(0.5\text{ A}) = \mathbf{7.3\text{ W}}$$

The total internal power dissipation ($P_{tot(int)}$) is the power in the complementary stage in the *on* state (P_{DQ}) plus the internal power in the comparator, triangular-wave generator, and filter (P_{int}).

$$\begin{aligned} P_{tot(int)} &= P_{DQ} + P_{int} = (400\text{ mV})(0.5\text{ A}) + 100\text{ mW} \\ &= 200\text{ mW} + 100\text{ mW} = 300\text{ mW} \end{aligned}$$

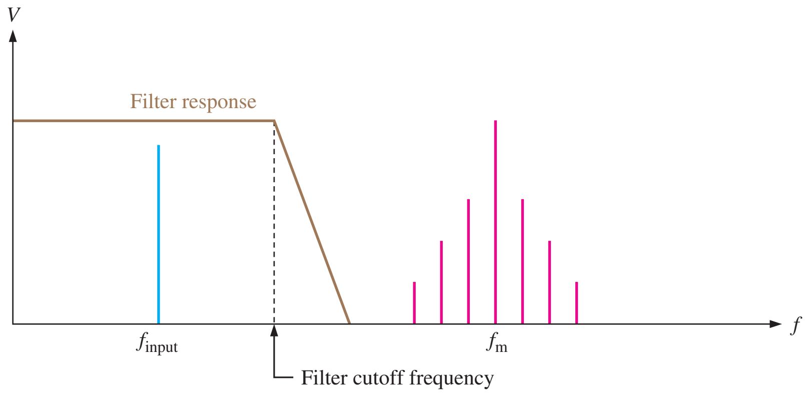
The efficiency is

$$\eta = \frac{P_{out}}{P_{out} + P_{tot(int)}} = \frac{7.3\text{ W}}{7.6\text{ W}} = \mathbf{0.961}$$

Related Problem There is 0.5 V across each MOSFET when it is *on* and the class D amplifier operates with ±12 V dc supply voltages. Assuming all other circuits in the amplifier dissipate 75 mW and 0.8 A is supplied to the load, determine the efficiency.

Low-Pass Filter

The low-pass filter removes the modulating frequency and harmonics and passes only the original signal to the output. The filter has a bandwidth that passes only the input signal frequencies, as illustrated in Figure 9–30.

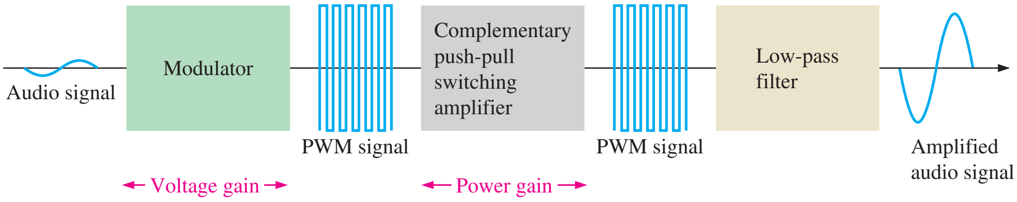


◀ FIGURE 9–30

The low-pass filter removes all but the input signal frequency from the PWM signal.

Signal Flow

Figure 9–31 shows the signals at each point in a class D amplifier. A small audio signal is applied and pulse-width modulated to produce a PWM signal at the output of the modulator where voltage gain is achieved. The PWM drives the complementary MOSFET stage to achieve power amplification. The PWM signal is filtered and the amplified audio signal appears on the output with sufficient power to drive a speaker.



▲ FIGURE 9–31

Signal flow in a class D amplifier.

SECTION 9–4 CHECKUP

1. Name the three stages of a class D amplifier.
2. In pulse-width modulation, to what is the pulse width proportional?
3. How is the PWM signal changed to an audio signal?

9–5 MOSFET ANALOG SWITCHING

MOSFETs are widely used in analog and digital switching applications. In the preceding section, you saw how MOSFETs are used in the switching mode in Class D amplifiers. Generally, they exhibit very low *on*-resistance, very high *off*-resistance, and fast switching times.

After completing this section, you should be able to

- ❑ **Describe how MOSFETs can be used in analog switching applications**
- ❑ Explain how a MOSFET operates as a switch
  - ◆ Discuss load line operation ◆ Discuss the ideal switch
- ❑ Describe a MOSFET analog switch
- ❑ Discuss analog switch applications
  - ◆ Explain a sampling circuit ◆ Explain an analog multiplexer ◆ Explain a switched-capacitor circuit

MOSFET Switching Operation

E-MOSFETs are generally used for switching applications because of their threshold characteristic, $V_{GS(th)}$. When the gate-to-source voltage is less than the threshold value, the MOSFET is *off*. When the gate-to-source voltage is greater than the threshold value, the MOSFET is *on*. When V_{GS} is varied between $V_{GS(th)}$ and $V_{GS(on)}$, the MOSFET is being operated as a switch, as illustrated in Figure 9–32. In the *off* state, when $V_{GS} < V_{GS(th)}$, the device is operating at the lower end of the load line and acts like an open switch (very high R_{DS}). When V_{GS} is sufficently greater than $V_{GS(th)}$, the device is operating at the upper end of the load line in the ohmic region and acts like a closed switch (very low R_{DS}).

The Ideal Switch Refer to Figure 9–33(a). When the gate voltage of the *n*-channel MOSFET is $+V$, the gate is more positive than the source by an amount exceeding $V_{GS(th)}$. The MOSFET is *on* and appears as a closed switch between the drain and source. When the gate voltage is zero, the gate-to-source voltage is 0 V. The MOSFET is *off* and appears as an open switch between the drain and source.

Refer to Figure 9–33(b). When the gate voltage of the *p*-channel MOSFET is 0 V, the gate is less positive than the source by an amount exceeding $V_{GS(th)}$. The MOSFET is *on* and appears as a closed switch between the drain and source. When the gate voltage is $+V$, the gate-to-source voltage is 0 V. The MOSFET is *off* and appears as an open switch between the drain and source.

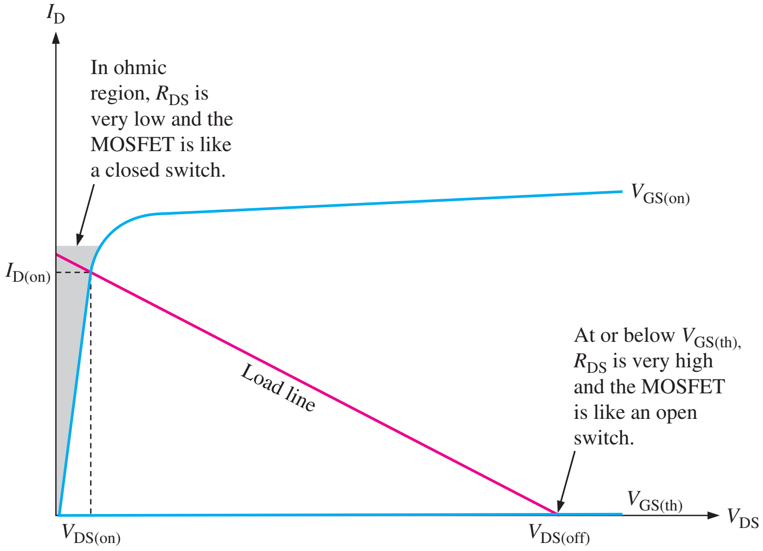
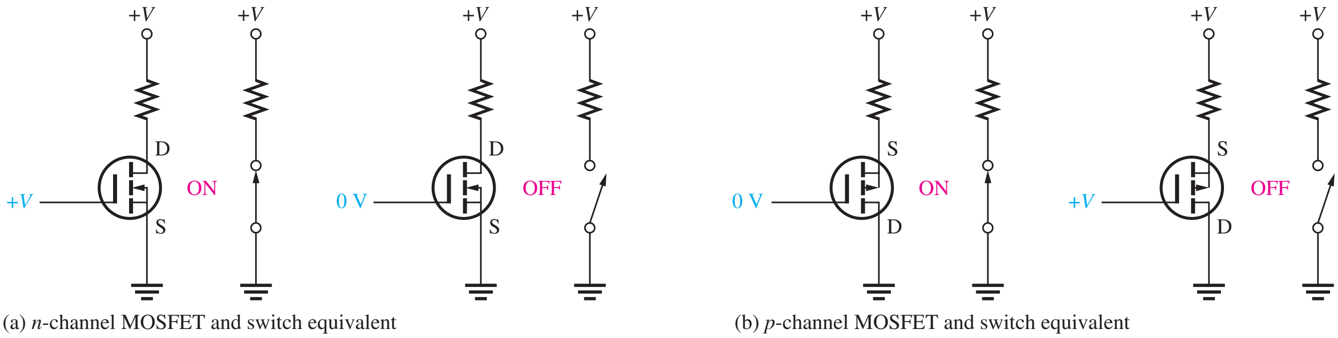


FIGURE 9–32

Switching operation on the load line.



(a) *n*-channel MOSFET and switch equivalent

(b) *p*-channel MOSFET and switch equivalent

FIGURE 9–33

The MOSFET as a switch.

The Analog Switch

MOSFETs are commonly used for switching analog signals. Basically, a signal applied to the drain can be switched through to the source by a voltage on the gate. A major restriction is that the signal level at the source must not cause the gate-to-source voltage to drop below $V_{GS(th)}$.

A basic *n*-channel MOSFET **analog switch** is shown in Figure 9–34. The signal at the drain is connected to the source when the MOSFET is turned on by a positive V_{GS} and is disconnected when V_{GS} is 0, as indicated.

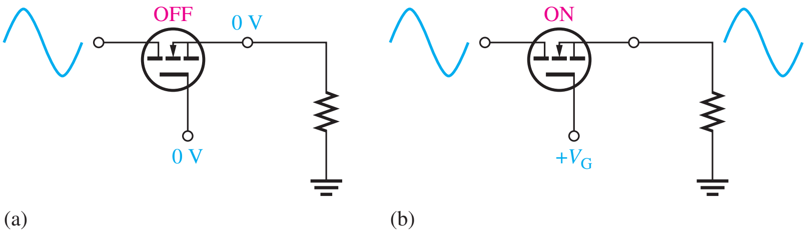


FIGURE 9–34

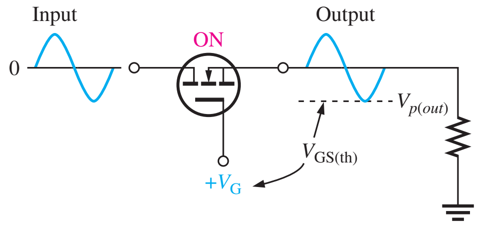
Operation of an *n*-channel MOSFET analog switch.

When the analog switch is *on,* as illustrated in Figure 9–35, the minimum gate-to-source voltage occurs at the negative peak of the signal. The difference in V_G and $-V_{p(out)}$ is the gate-to-source voltage at the instant of the negative peak and must be equal to or greater than $V_{GS(th)}$ to keep the MOSFET in conduction.

$$V_{GS} = V_G - V_{p(out)} \geq V_{GS(th)}$$

FIGURE 9–35

Signal amplitude is limited by $V_{GS(th)}$.



EXAMPLE 9–13

A certain analog switch similar to the one shown in Figure 9–35 uses an *n*-channel MOSFET with $V_{GS(th)} = 2$ V. A voltage of +5 V is applied at the gate to turn the switch *on*. Determine the maximum peak-to-peak input signal that can be applied, assuming no voltage drop across the switch.

Solution The difference between the gate voltage and the negative peak of the signal voltage must equal or exceed the threshold voltage. For maximum $V_{p(out)}$,

$$V_G - V_{p(out)} = V_{GS(th)}$$

$$V_{p(out)} = V_G - V_{GS(th)} = 5\text{ V} - 2\text{ V} = 3\text{ V}$$

$$V_{pp(in)} = 2V_{p(out)} = 2(3\text{ V}) = \mathbf{6\text{ V}}$$

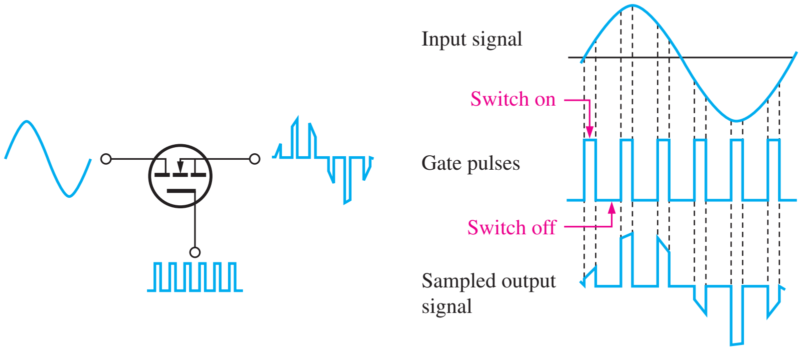
Related Problem What would happen if $V_{p(in)}$ exceeded the maximum value?

Analog Switch Applications

Sampling Circuit One application of analog switches is in analog-to-digital conversion. The analog switch is used in a *sample-and-hold* circuit to sample the input signal at a certain rate. Each sampled signal value is then temporarily stored on a capacitor until it can be converted to a digital code by an analog-to-digital converter (ADC). To accomplish this, the MOSFET is turned *on* for short intervals during one cycle of the input signal by pulses applied to the gate. The basic operation, showing only a few samples for clarity, is illustrated in Figure 9–36.

FIGURE 9–36

The analog switch operating as a sampling circuit.



(a) Circuit action

(b) Waveform diagram

The minimum rate at which a signal can be sampled and reconstructed from the samples must be more than twice the maximum frequency contained in the signal. The minimum sampling frequency is called the *Nyquist frequency.*

$$f_{\text{sample (min)}} > 2f_{\text{signal (max)}}$$

When a gate pulse is at its high level, the switch is turned *on* and the small portion of the input waveform occurring during that pulse appears on the output. When the pulse waveform is at its 0 V level, the switch is turned *off* and the output is also at 0 V.

EXAMPLE 9–14 An analog switch is used to sample an audio signal with a maximum frequency of 8 kHz. Determine the minimum frequency of the pulses applied to the MOSFET gate.

Solution

$$f_{\text{sample (min)}} > 2f_{\text{signal (max)}} = 2(8\text{ kHz}) = \mathbf{16\text{ kHz}}$$

The sampling frequency must be greater than 16 kHz.

Related Problem What is the minimum sampling frequency if the highest frequency in the audio signal is 12 kHz?

Analog Multiplexer Analog multiplexers are used where two or more signals are to be routed to the same destination. For example, a two-channel analog sampling multiplexer is shown in Figure 9–37. The MOSFETs are alternately turned *on* and *off* so that first one signal sample is connected to the output and then the other. The pulses are applied to the gate of switch A, and the inverted pulses are applied to the gate of switch B. A digital circuit known as an *inverter* is used for this. When the pulses are high, switch A is *on* and switch B is *off.* When the pulses are low, switch B is *on* and switch A is *off.* This is called *time-division multiplexing* because signal A appears on the output during time intervals when the pulse is high and signal B appears during the time intervals when the pulse is low. That is, they are interleaved on a time basis for transmission on a single line.

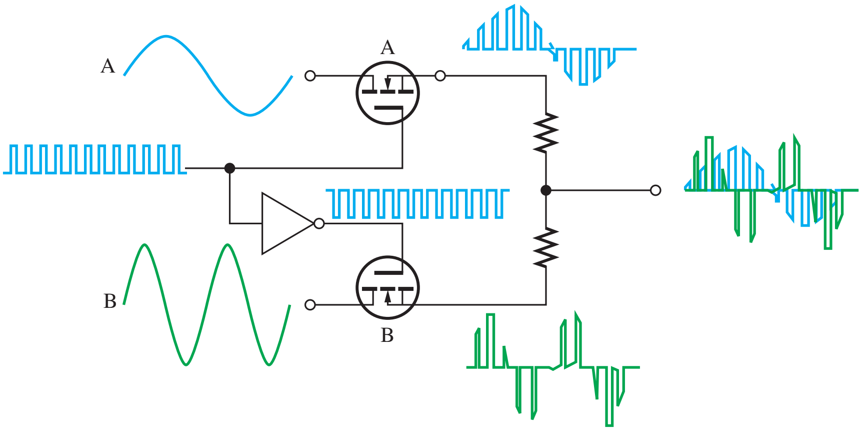


FIGURE 9–37

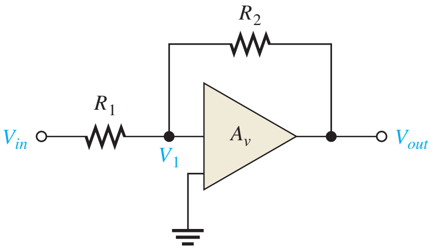
The analog multiplexer is alternately sampling two signals and interleaving them on a single output line.

Switched-Capacitor Circuit Another application of MOSFETs is in **switched-capacitor circuits** commonly used in integrated circuit programmable analog devices known as *analog signal processors.* Because capacitors can be implemented in ICs more easily than a resistor, they are used to emulate resistors. Capacitors also take up less space on a chip than an IC resistor and dissipate no power. Many types of analog circuits use resistors to determine voltage gain and other characteristics and by using switched capacitors to emulate resistors, dynamic programming of analog circuits can be achieved.

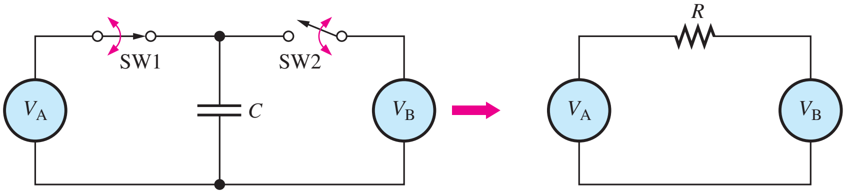
For example, in a certain type of IC amplifier circuit that you will study later, two external resistors are required as shown in Figure 9–38. The values of these resistors establish the voltage gain of the amplifier as $A_v = R_2/R_1$.

▶ FIGURE 9–38

A type of IC amplifier.



A switched-capacitor can be used to emulate a resistor as shown in Figure 9–39 using a mechanical switch analogy (MOSFETs are actually used as the switches). Switch 1 and switch 2 are alternately turned *on* and *off* at a certain frequency to charge or discharge C, depending on the values of the voltage sources. In the case of R_1 in Figure 9–38, V_{in} and V_1 are represented by V_A and V_B, respectively. For R_2, V_1 and V_{out} are represented by V_A and V_B, respectively.



▲ FIGURE 9–39

A switched capacitor emulates a resistance.

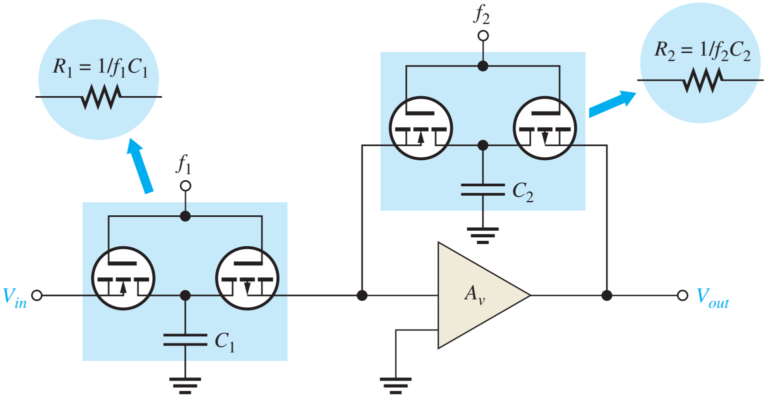
It can be shown (see Appendix B) that the capacitor emulates a resistance with a value that depends on the frequency at which the switches are turned *on* and *off* and the capacitance value.

Equation 9–10

$$R = \frac{1}{fC}$$

By changing the frequency, the effective resistance value can be altered.

Complementary E-MOSFETs and capacitors can be used to replace the resistors in the amplifier, as shown in Figure 9–40. When Q_1 is *on*, Q_2 is *off* and vice versa. The frequency f_1 and C_1 are selected to provide the required value of R_1. Likewise, f_2 and C_2 provide the required value of R_2. To reprogram the amplifier for a different gain, the frequencies are changed.



▲ FIGURE 9–40

The IC amplifier in Figure 9–38 with switched-capacitor circuits replacing the resistors.

SECTION 9–5 CHECKUP

1. When does an E-MOSFET act as an open switch?
2. When does an E-MOSFET act as a closed switch?
3. What type of voltage is generally used to control an analog switch?
4. In a switched-capacitor circuit, on what does the emulated resistance depend?

9–6 MOSFET DIGITAL SWITCHING

In the preceding section, you saw how MOSFETs are used to switch analog signals. MOSFETs are also used in switching applications in digital integrated circuits and in power control circuits. MOSFETs used in digital ICs are low-power types, and those used in power control are high-power devices.

After completing this section, you should be able to

- **Describe how MOSFETs are used in digital switching applications**
- Discuss complementary MOS (CMOS)
  - Explain CMOS inverter operation
  - Explain CMOS NAND gate operation
  - Explain CMOS NOR gate operation
- Discuss MOSFETs in power switching

CMOS (Complementary MOS)

CMOS combines *n*-channel and *p*-channel E-MOSFETs in a series arrangement as shown in Figure 9–41(a). The input voltage at the gates is either 0 V or V_{DD}. Notice that V_{DD} and ground are both connected to source terminals of the transistors. To avoid confusion, the term V_{DD} is used for the positive voltage, which is on the *p*-channel device's source terminal. When $V_{in} = 0$ V, Q_1 is *on* and Q_2 is *off,* as shown in part (b). Because Q_1 is acting as a closed switch, the output is approximately V_{DD}. When $V_{in} = V_{DD}$, Q_2 is *on* and Q_1 is *off,* as shown in part (c). Because Q_2 is acting as a closed switch, the output is essentially connected to ground (0 V).

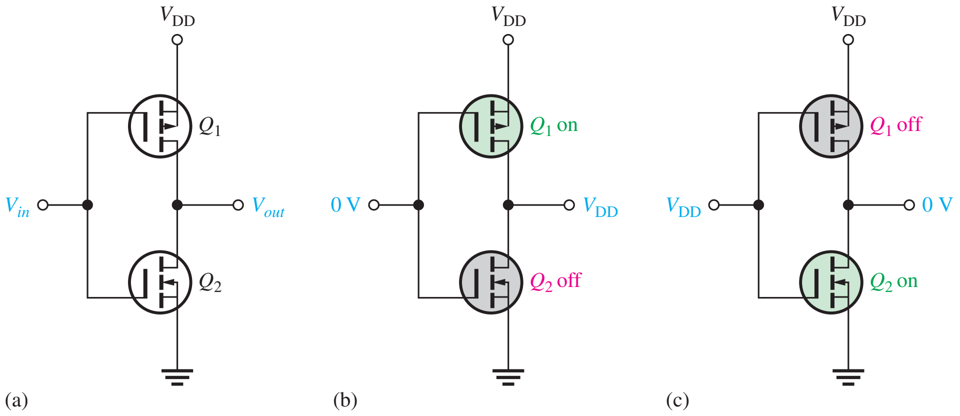


FIGURE 9–41

CMOS inverter operation.

A major advantage of CMOS is that it consumes very little dc power. Because the MOSFETs are in series and one of them is always *off,* there is essentially no current from the dc supply in the quiescent state. When the MOSFETs are switching, there is current for a very short time because both transistors are *on* during this very short transition from one state to the other.

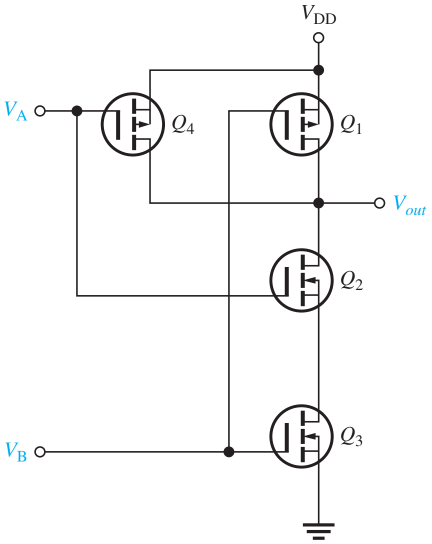
Inverter Notice that the circuit in Figure 9–41 actually inverts the input because when the input is 0 V or low, the output is V_{DD} or high. When the input is V_{DD} or high, the output is 0 V or low. For this reason, this circuit is called an *inverter* in digital electronics.

NAND Gate In Figure 9–42(a), two additional MOSFETs and a second input are added to the CMOS pair to create a digital circuit known as a NAND gate. Q_4 is connected in parallel with Q_1, and Q_3 is connected in series with Q_2. When both inputs, V_A and V_B, are 0, Q_1 and Q_4 are *on* while Q_2 and Q_3 are *off*, making $V_{out} = V_{DD}$. When both inputs are equal to V_{DD}, Q_1 and Q_4 are *off* while Q_2 and Q_3 are *on*, making $V_{out} = 0$. You can verify that when the inputs are different, one at V_{DD} and the other at 0, the output is equal to V_{DD}. The operation is summarized in the table of Figure 9–42(b) and can be stated:

When V_A *AND* V_B are high, the output is low; otherwise, the output is high.

▶ FIGURE 9–42

CMOS NAND gate operation.



(a)

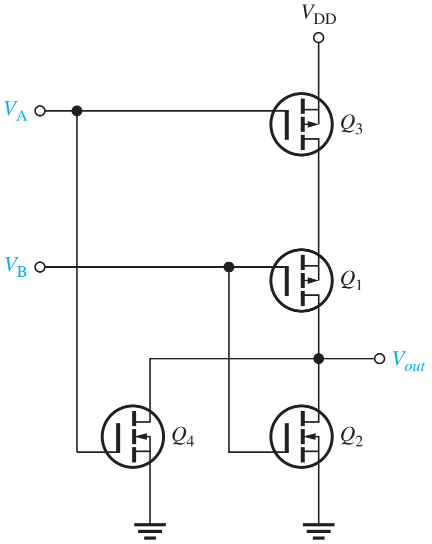
V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	off	on	V_{DD}
0	V_{DD}	off	off	off	on	V_{DD}
V_{DD}	0	on	off	off	off	V_{DD}
V_{DD}	V_{DD}	off	on	on	off	0

(b)

NOR Gate In Figure 9–43(a), two additional MOSFETs and a second input are added to the CMOS pair to create a digital circuit known as a NOR gate. Q_4 is connected in parallel with Q_2, and Q_3 is connected in series with Q_1. When both inputs, V_A and V_B, are 0, Q_1 and

▶ FIGURE 9–43

CMOS NOR gate operation.



(a)

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	on	off	V_{DD}
0	V_{DD}	off	on	on	off	0
V_{DD}	0	on	off	on	off	0
V_{DD}	V_{DD}	off	on	off	on	0

(b)

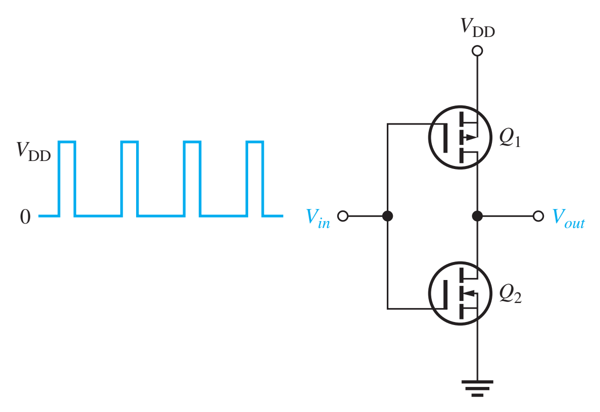
Q_3 are *on* while Q_2 and Q_4 are *off,* making $V_{out} = V_{DD}$. When both inputs are equal to V_{DD}, Q_1 and Q_3 are *off* while Q_2 and Q_4 are *on,* making $V_{out} = 0$. You can verify that when the inputs are different, one at V_{DD} and the other at 0, the output is equal to 0. The operation is summarized in the table of Figure 9–43(b) and can be stated:

When V_A *OR* V_B *OR* both are high, the output is low; otherwise, the output is high.

EXAMPLE 9–15

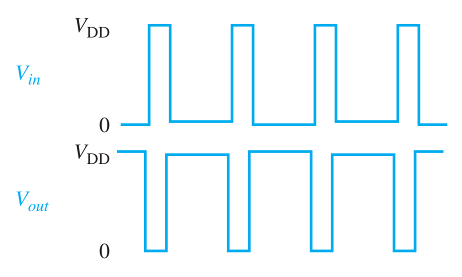
A pulse waveform is applied to a CMOS inverter as shown in Figure 9–44. Determine the output waveform and explain the operation.

▶ FIGURE 9–44



Solution The output waveform is shown in Figure 9–45 in relation to the input. When the input pulse is at V_{DD}, Q_1 is *off* and Q_2 is *on,* connecting the output to ground (0 V). When the input pulse is at 0, Q_1 is *on* and Q_2 is *off,* connecting the output to V_{DD}.

▶ FIGURE 9–45



Related Problem If the output of the CMOS inverter in Figure 9–44 is connected to the input of a second CMOS inverter, what is the output of the second inverter?

MOSFETs in Power Switching

The BJT was the only power transistor until the MOSFET was introduced. The BJT requires a base current to turn on, has relatively slow turn-off characteristics, and is susceptible to thermal runaway due to a negative temperature coefficient. The MOSFET, however, is voltage controlled and has a positive temperature coefficient, which prevents thermal runaway. The MOSFET can turn *off* faster than the BJT, and the low *on*-state-resistance results in conduction power losses lower than with BJTs. Power MOSFETs are used for motor control, dc-to-ac conversion, dc-to-dc conversion, load switching, and other applications that require high current and precise digital control.

SECTION 9–6 CHECKUP

1. Describe a basic CMOS inverter.
2. What type of 2-input digital CMOS circuit has a low output only when both inputs are high?
3. What type of 2-input digital CMOS circuit has a high output only when both inputs are low?

9–7 TROUBLESHOOTING

A technician who understands the basics of circuit operation and who can, if necessary, perform basic analysis on a given circuit is much more valuable than one who is limited to carrying out routine test procedures. In this section, you will see how to test a circuit board that has only a schematic with no specified test procedure or voltage levels. In this case, basic knowledge of how the circuit operates and the ability to do a quick circuit analysis are useful.

After completing this section, you should be able to

- **Troubleshoot FET amplifiers**
- Troubleshoot a two-stage common-source amplifier
  - Explain each step in the troubleshooting procedure
  - Use a datasheet
  - Relate the circuit board to the schematic

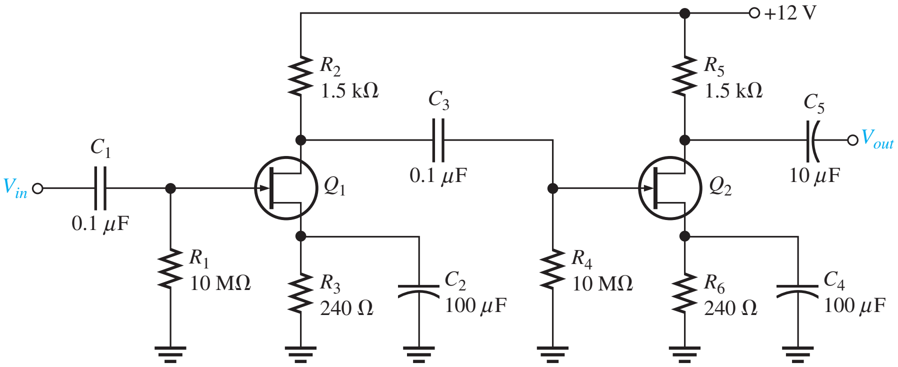
Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

A Two-Stage Common-Source Amplifier

Assume that you are given a circuit board containing an audio amplifier and told simply that it is not working properly. The circuit is a two-stage CS JFET amplifier, as shown in Figure 9–46.

FIGURE 9–46

A two-stage CS JFET amplifier circuit.



The problem is approached in the following sequence.

Step 1: Determine what the voltage levels in the circuit should be so that you know what to look for. First, pull a datasheet on the particular transistor (assume both Q_1 and Q_2 are found to be the same type of transistor) and determine the g_m so that you can calculate the typical voltage gain. Assume that for this particular device, a typical g_m of 5000 μS is specified. Calculate the expected typical voltage gain of each stage (notice they are identical) based on the typical value of g_m. The g_m of actual devices may be any value between the specified minimum and maximum values. Because the input resistance is very high, the second stage does not significantly load the first stage, as in a BJT amplifier. So, the unloaded voltage gain for each stage is

$$A_v = g_m R_2 = (5000\,\mu\text{S})(1.5\,\text{k}\Omega) = 7.5$$

Since the stages are identical, the typical overall gain should be

$$A'_v = (7.5)(7.5) = 56.3$$

Assume the dc levels have been checked and verified. You are now ready to move to ac signal checks.

Step 2: Arrange a test setup to permit connection of an input test signal, a dc supply voltage, and ground to the circuit. The schematic shows that the dc supply voltage must be +12 V. Choose 10 mV rms as an input test signal. This value is arbitrary (although the capability of your signal source is a factor), but small enough that the expected output signal voltage is well below the absolute peak-to-peak limit of 12 V set by the supply voltage and ground (you know that the output voltage swing cannot go higher than 12 V or lower than 0 V). Set the frequency of the sinusoidal signal source to an arbitrary value in the audio range (say 10 kHz) because you know this is an audio amplifier. The audio frequency range is generally accepted as 20 Hz to 20 kHz.

Step 3: Check the input signal at the gate of Q_1 and the output signal at the drain of Q_2 with an oscilloscope. The results are shown in Figure 9–47. The measured output voltage has a peak value of 226 mV. The expected typical peak output voltage is

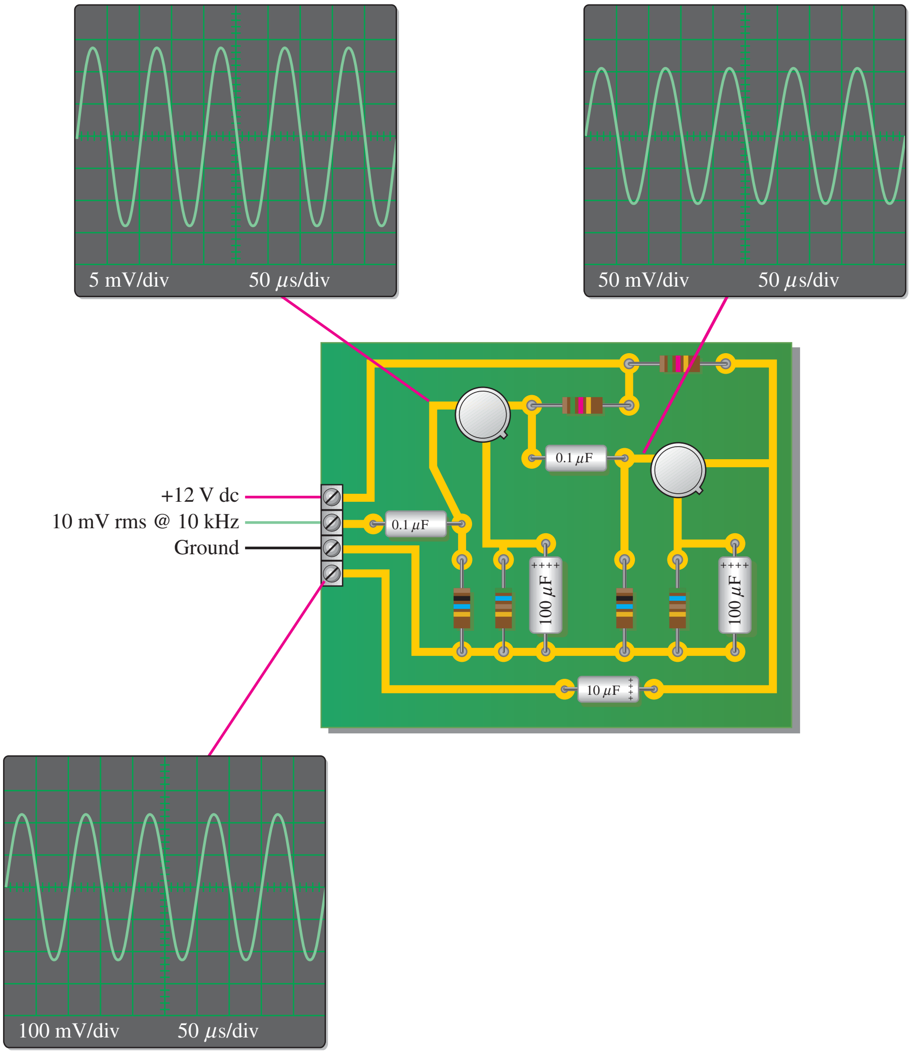
$$V_{out} = V_{in}A'_v = (14.14\,\text{mV})(56.3) = 796\,\text{mV peak}$$

The output is much less than it should be.

Step 4: Trace the signal from the output toward the input to determine the fault. Figure 9–47 shows the oscilloscope displays of the measured signal voltages. The voltage at the gate of Q_2 is 106 mV peak, as expected ($14.14\,\text{mV} \times 7.5 = 106\,\text{mV}$). This signal is properly coupled from the drain of Q_1. Therefore, the problem lies in the second stage. From the oscilloscope displays, the gain of Q_2 is much lower than it should be (213 mV/100 mV = 2.13 instead of 7.5).

Step 5: Analyze the possible causes of the observed malfunction. There are three possible reasons the gain is low:

1. Q_2 has a lower transconductance (g_m) than the specified typical value. Check the datasheet to see if the minimum g_m accounts for the lower measured gain.
2. R_5 has a lower value than shown on the schematic. An incorrect value should show up with dc voltage checks, particularly if the value is much different than specified, so this is not the likely cause in this case.
3. The bypass capacitor C_4 is open.



▲ FIGURE 9–47

Oscilloscope displays of signals in the two-stage JFET amplifier.

The best way to check the g_m is by replacing Q_2 with a new transistor of the same type and rechecking the output signal. You can make certain that R_5 is the proper value by removing one end of the resistor from the circuit board and measuring the resistance with an ohmmeter. To avoid having to unsolder a component, the best way to start isolating the fault is by checking the signal voltage at the source of Q_2. If the capacitor is working properly, there will be only a dc voltage at the source. The presence of a signal voltage at the source indicates that C_4 is open. With R_6 unbypassed, the gain expression is $g_mR_d/(1 + g_mR_s)$ rather than simply g_mR_d, thus resulting in less gain.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE09-01
2. Multisim file TSE09-02

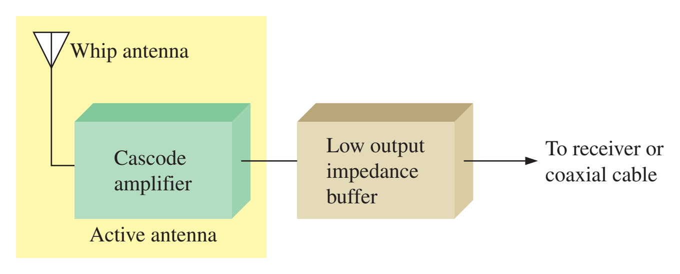
3. Multisim file TSE09-03
4. Multisim file TSE09-04
5. Multisim file TSE09-05

SECTION 9–7 CHECKUP

1. What is the prerequisite to effective troubleshooting?
2. Assume that C_2 in the amplifier of Figure 9–46 opened. What symptoms would indicate this failure?
3. If C_3 opened in the amplifier of Figure 9–46, would the voltage gain of the first stage be affected?

Application Activity: *Active Antenna*

In this application, a broadband JFET amplifier is used to provide a high input impedance and voltage gain for a whip antenna. When an antenna is connected to the input of a receiver or a coaxial cable, signal deterioration may be unacceptable due to a distant station, noisy conditions, or an impedance mismatch. An active antenna can alleviate this problem by providing a stronger signal. The block diagram in Figure 9–48 shows an active antenna, followed by a low impedance output buffer to drive a coaxial cable or a receiver input. The focus in this application is the active antenna. The low output impedance buffer can be a BJT emitter-follower or an impedance-matching transformer.



▶ FIGURE 9–48

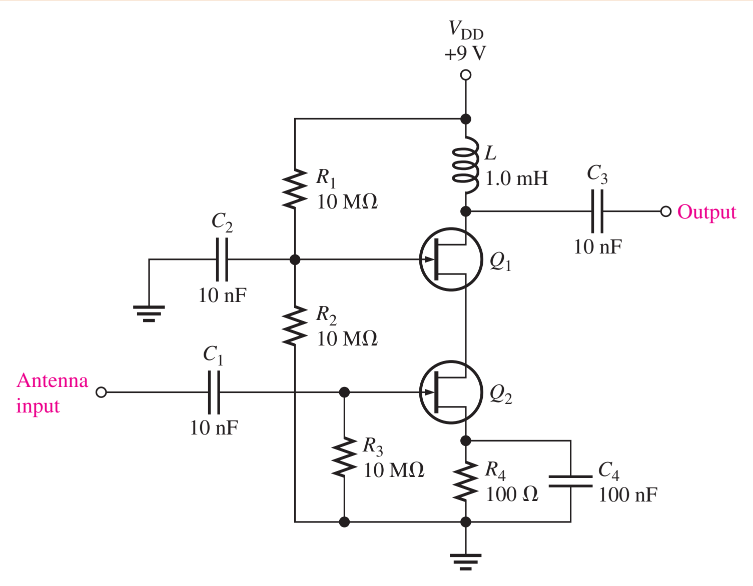
An active antenna driving a receiver or a coax through a buffer.

The Amplifier Circuit

Figure 9–49 is a broadband amplifier using two JFETs in a cascode arrangement commonly used in RF (radio frequency) applications. The advantage of using a JFET is that its high input impedance does not load the antenna and cause a reduction in signal voltage, resulting in poor signal reception. It also is a low noise device and can be located close to the antenna before additional noise is picked up by the system. Generally, an antenna produces signal voltages in the microvolt range, and any signal loss because of loading or noise can significantly degrade the signal. The active antenna also provides a large voltage gain that results in a stronger signal to the receiver with improved signal-to-noise ratio. The active antenna is powered by a separate 9 V battery, which also provides isolation from noise pickup in the signal lines and is located in an enclosed metal box to provide additional isolation.

▶ FIGURE 9–49

Cascode amplifier for active antenna.



This active antenna has a voltage gain of approximately 2000 at 88 MHz and a gain of approximately 10,000 at 1 GHz which makes it applicable for the FM broadcast band, some TV channel bands, some amateur radio (HAM) bands, cell phone bands, and many others. Also below the FM band, the gain may be adequate for other radio and TV bands as well, depending on receiver requirements. The coil can be changed to optimize gain within a specified band or to adjust the band downward.

1. Research the Internet to determine the frequency band for TV channels 7–13.
2. Research the Internet to find the frequency bands allocated for cellular telephones.
3. What is the purpose of C_2 in Figure 9–49?

The transistors used in the active antenna are 2N5484 *n*-channel JFETs. The partial datasheet is shown in Figure 9–50.

4. Using the datasheet, determine $R_{IN(gate)}$ of the JFET (Q_2).
5. What input resistance is presented to the antenna in Figure 9–49?
6. From the datasheet, what is the minimum forward transconductance?

Simulation

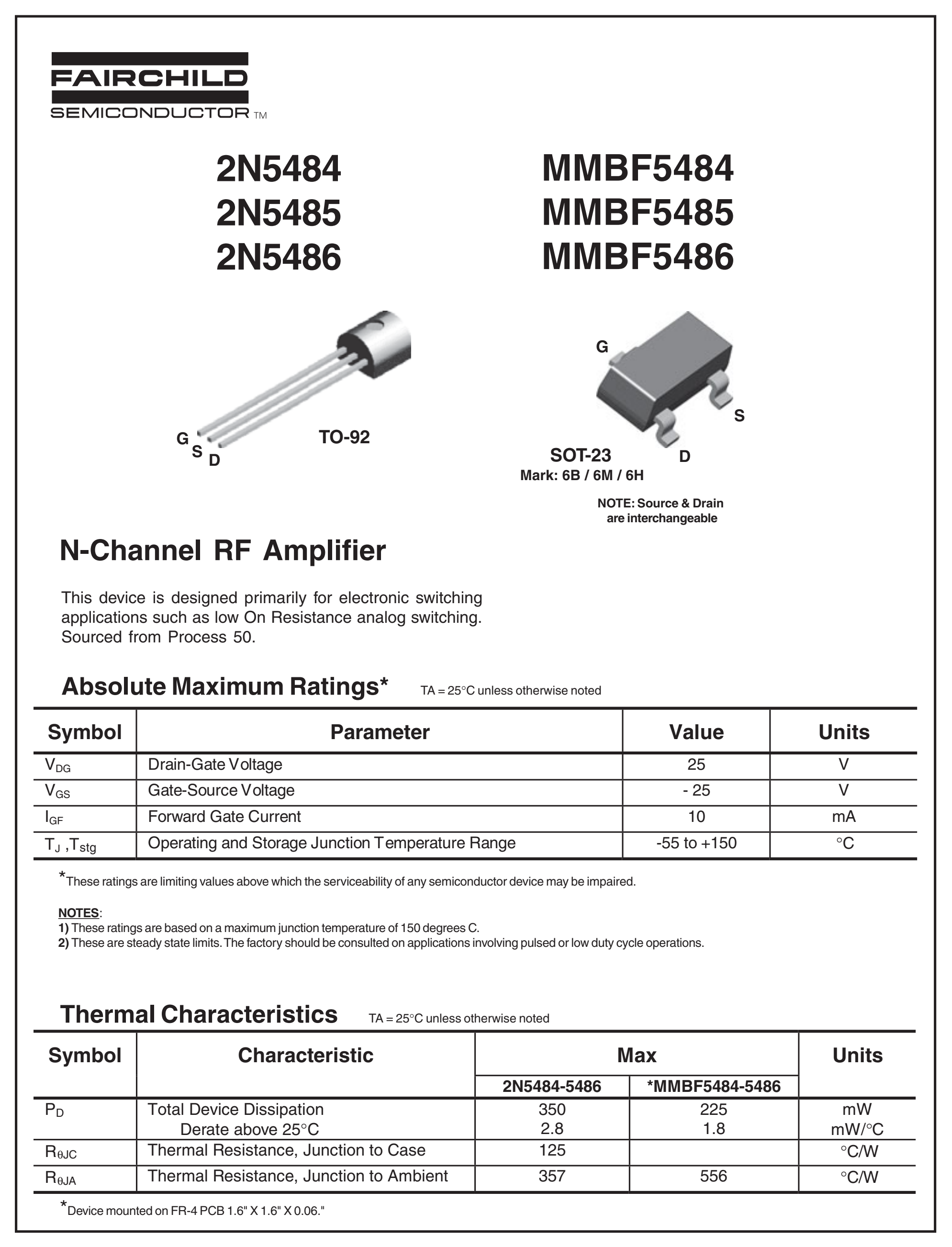
The active antenna circuit is simulated in Multisim with the antenna input represented by a 10 μV peak source. The output signal is shown for 88 MHz and 1 GHz inputs in Figure 9–51 on page 489.

7. What is the significance of the 88 MHz frequency?
8. Determine the rms output voltage in Figure 9–51(b) and (c), and calculate the gain for both frequencies.

Simulate the active antenna circuit using your Multisim software. Measure the output voltage at 10 MHz, 100 MHz, and 500 MHz.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested, it is ready to be finalized. Because you are working at high frequencies where stray capacitances can cause unwanted resonant conditions, the circuit layout is very critical.



FAIRCHILD
SEMICONDUCTOR TM

2N5484
2N5485
2N5486

MMBF5484
MMBF5485
MMBF5486

G S D TO-92

G S D SOT-23
Mark: 6B / 6M / 6H

NOTE: Source & Drain
are interchangeable

N-Channel RF Amplifier

This device is designed primarily for electronic switching applications such as low On Resistance analog switching. Sourced from Process 50.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J ,T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

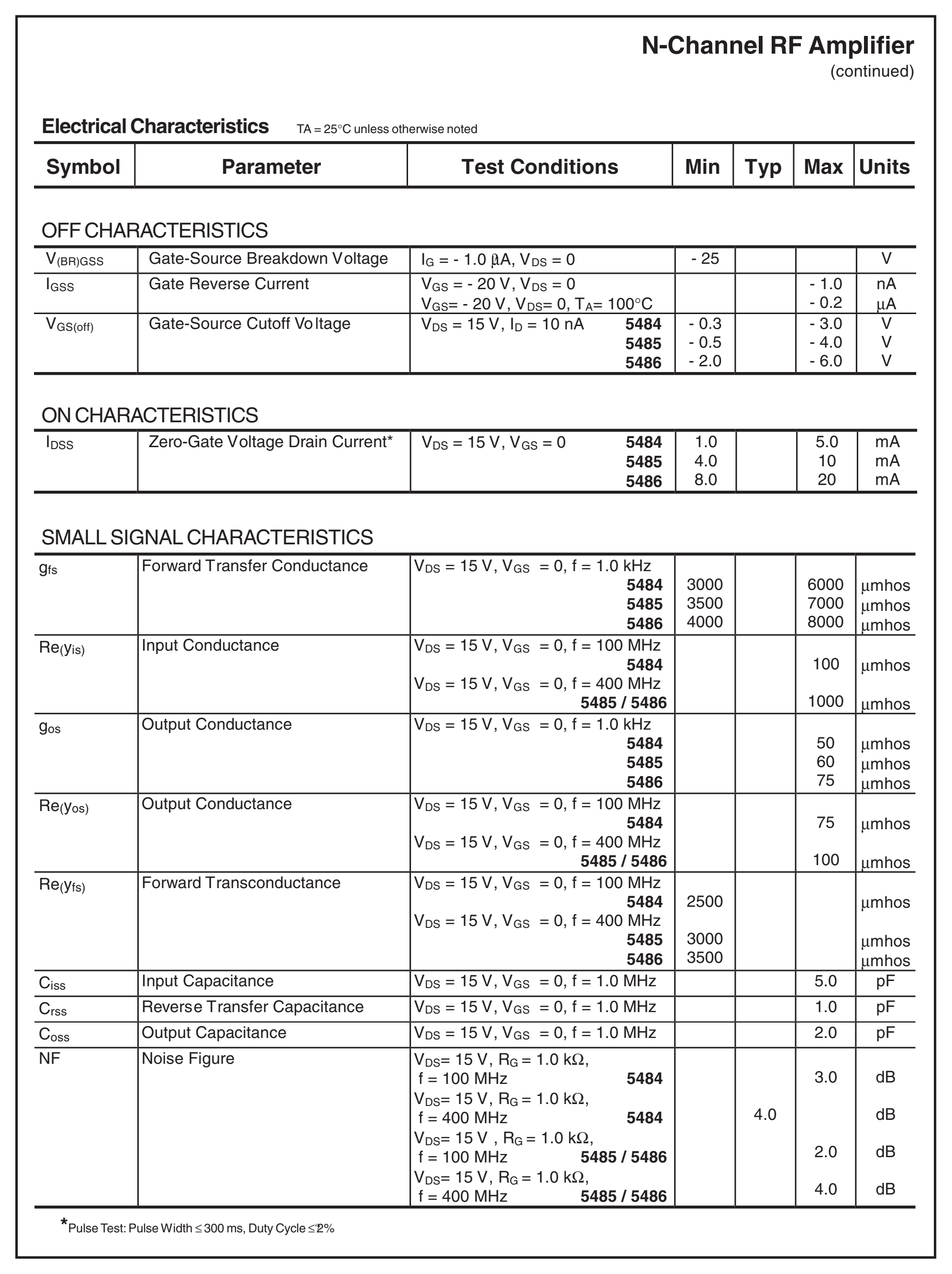
TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		2N5484-5486	*MMBF5484-5486	
P_D	Total Device Dissipation Derate above 25°C	350 2.8	225 1.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

▲ FIGURE 9–50

Partial datasheet for the 2N5484 RF *n*-channel JFET. Copyright Fairchild semiconductor corporation. Used by permission. (*continued on next page*)



N-Channel RF Amplifier
(continued)

Electrical Characteristics TA = 25°C unless otherwise noted

OFF CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = -1.0\ \mu A$, $V_{DS} = 0$	- 25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -20$ V, $V_{DS} = 0$ $V_{GS} = -20$ V, $V_{DS} = 0$, $T_A = 100°C$			- 1.0 - 0.2	nA µA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA **5484** **5485** **5486**	- 0.3 - 0.5 - 2.0		- 3.0 - 4.0 - 6.0	V V V

ON CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{DSS}	Zero-Gate Voltage Drain Current*	$V_{DS} = 15$ V, $V_{GS} = 0$ **5484** **5485** **5486**	1.0 4.0 8.0		5.0 10 20	mA mA mA

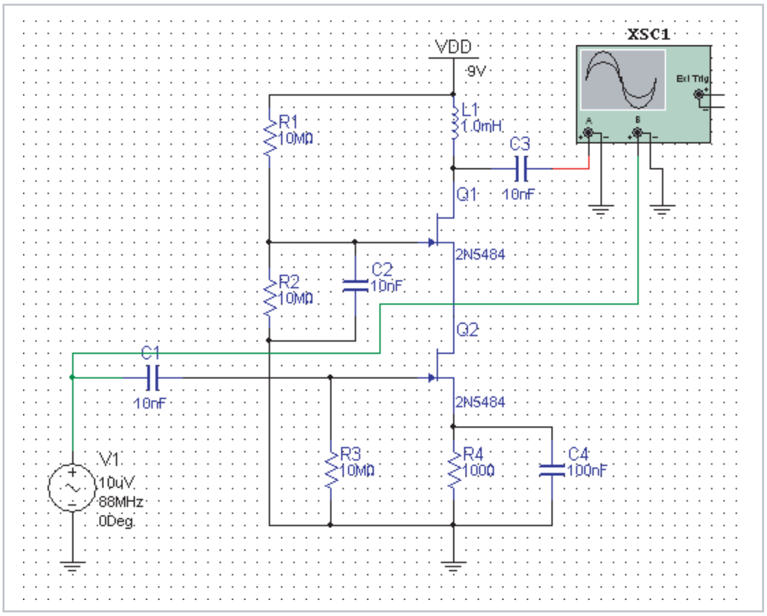
SMALL SIGNAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
g_{fs}	Forward Transfer Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz **5484** **5485** **5486**	3000 3500 4000		6000 7000 8000	µmhos µmhos µmhos
$Re(y_{is})$	Input Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz **5484** $V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz **5485 / 5486**			100 1000	µmhos µmhos
g_{os}	Output Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz **5484** **5485** **5486**			50 60 75	µmhos µmhos µmhos
$Re(y_{os})$	Output Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz **5484** $V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz **5485 / 5486**			75 100	µmhos µmhos
$Re(y_{fs})$	Forward Transconductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz **5484** $V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz **5485** **5486**	2500 3000 3500			µmhos µmhos µmhos
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			5.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			1.0	pF
C_{oss}	Output Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			2.0	pF
NF	Noise Figure	$V_{DS} = 15$ V, $R_G = 1.0\ k\Omega$, f = 100 MHz **5484** $V_{DS} = 15$ V, $R_G = 1.0\ k\Omega$, f = 400 MHz **5484** $V_{DS} = 15$ V, $R_G = 1.0\ k\Omega$, f = 100 MHz **5485 / 5486** $V_{DS} = 15$ V, $R_G = 1.0\ k\Omega$, f = 400 MHz **5485 / 5486**		 4.0 	3.0 2.0 4.0	dB dB dB dB

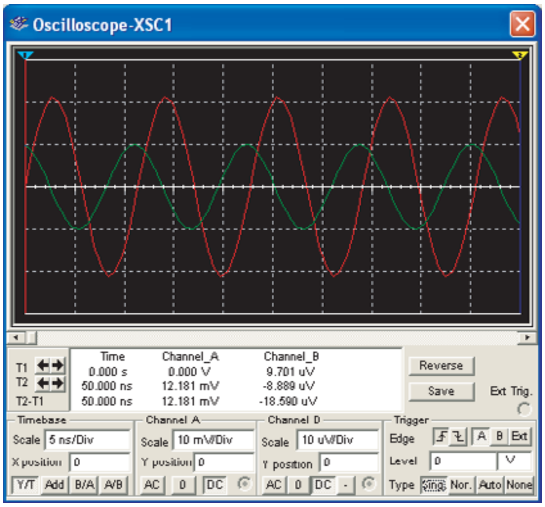
*Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2%

▲ FIGURE 9–50

(*continued*)


VDD
9V
XSC1
Ext Trig
A
B
R1
10MΩ
L1
1.0mH
C3
10nF
Q1
2N5484
R2
10MΩ
C2
10nF
Q2
2N5484
C1
10nF
V1
10uV
88MHz
0Deg
R3
10MΩ
R4
100Ω
C4
100nF

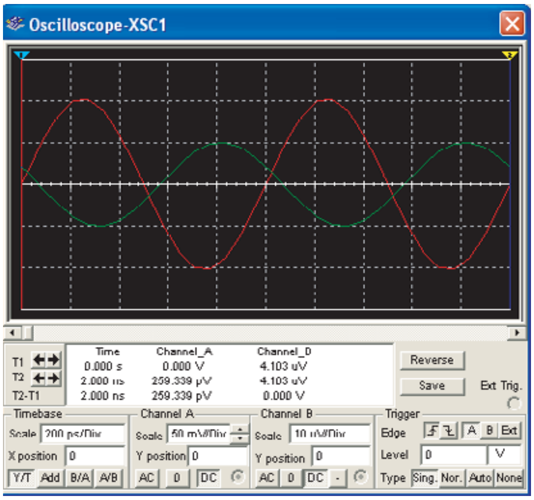
(a) Cascode amplifier circuit


Oscilloscope-XSC1
Reverse
Save
Ext Trig.

```
        Time        Channel_A    Channel_B
T1      0.000 s     0.000 V      9.701 uV
T2      50.000 ns   12.181 mV    -8.889 uV
T2-T1   50.000 ns   12.181 mV    -18.590 uV
```

Timebase: Scale 5 ns/Div; X position 0; Y/T
Channel A: Scale 10 mV/Div; Y position 0; DC
Channel B: Scale 10 uV/Div; Y position 0; DC
Trigger: Edge A; Level 0 V; Type Sing.

(b) Input and output signals at 88 MHz


Oscilloscope-XSC1
Reverse
Save
Ext Trig.

```
        Time        Channel_A    Channel_B
T1      0.000 s     0.000 V      4.103 uV
T2      2.000 ns    259.339 pV   4.103 uV
T2-T1   2.000 ns    259.339 pV   0.000 V
```

Timebase: Scale 200 ps/Div; X position 0; Y/T
Channel A: Scale 50 mV/Div; Y position 0; DC
Channel B: Scale 10 uV/Div; Y position 0; DC
Trigger: Edge A; Level 0 V; Type Sing.

(c) Input and output signals at 1 GHz

▲ **FIGURE 9–51**

Simulation results for the active antenna circuit. Input is green and output is red.

Lab Experiment

To build and test a similar circuit, go to Experiment 9 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

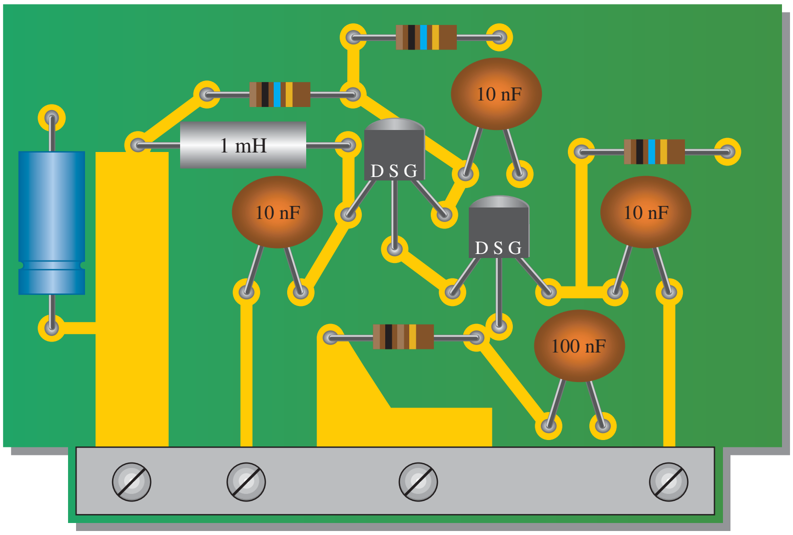
Circuit Board

Certain considerations should be observed when laying out a printed circuit board for RF circuits. EMI (electromagnetic interference), line inductance, and stray capacitance all become important at high frequencies. A few basic features that should be incorporated on an RF circuit board are

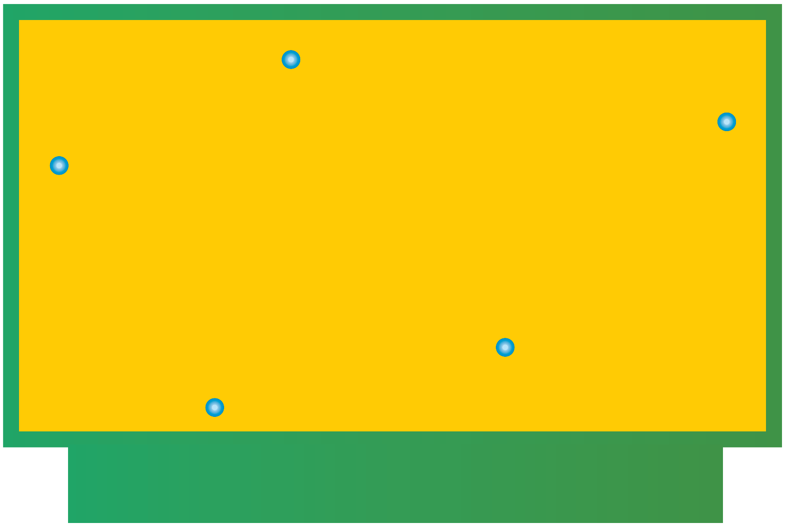
- Keep traces as short and wide as possible.
- Do not run parallel signal lines that are in close proximity.
- Capacitively decouple supply voltages.
- Provide a large ground plane for shielding and to minimize noise.

▶ FIGURE 9–52

Active antenna circuit board.



(a) Component side. Terminated pads are feedthroughs to backside ground plane.



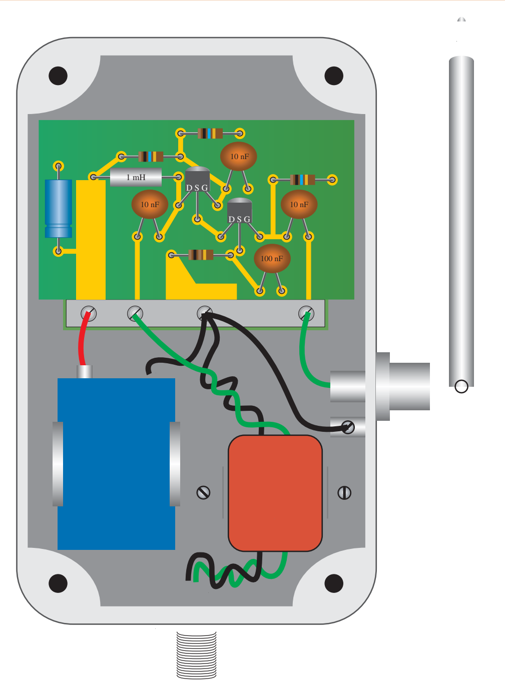
(b) Backside of board showing ground plane with feedthroughs indicated.

The circuit board for the active antenna is shown in Figure 9–52. A large ground plane is on the back side. Components are connected to the ground plane with feedthrough connections as indicated.

9. Check the printed circuit board for correctness by comparing with the schematic in Figure 9–49.
10. State the purpose of the large blue capacitor that is not shown on the schematic.
11. Label each input and output pin according to function.

The Complete Active Antenna Unit

Typically, the active antenna circuit should be enclosed in a metal box for proper shielding, similar to that shown in Figure 9–53. The particular configuration shown includes an impedance-matching transformer connected to a type of connector (BNC) used with coaxial cables for illustration. Other interface configurations, such as an emitter-follower output may be used for interfacing. The particular antenna shown is a telescoping whip antenna.


10 nF
1 mH
D S G
10 nF
D S G
10 nF
100 nF

▶ FIGURE 9–53

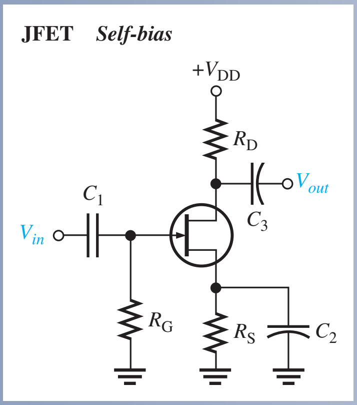
A configuration of the active antenna in a metal housing (cover removed) with a 9 V battery and an impedance-matching transformer.

SUMMARY OF FET AMPLIFIERS

N channels are shown. V_{DD} is negative for *p* channel.

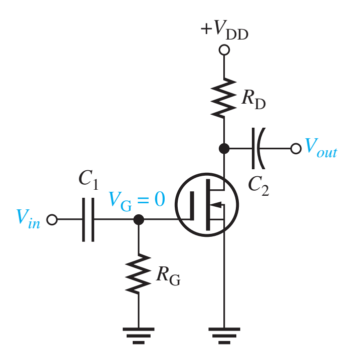
COMMON-SOURCE AMPLIFIERS

JFET ***Self-bias***


$+V_{DD}$
R_D
V_{out}
C_1
C_3
V_{in}
R_G
R_S
C_2

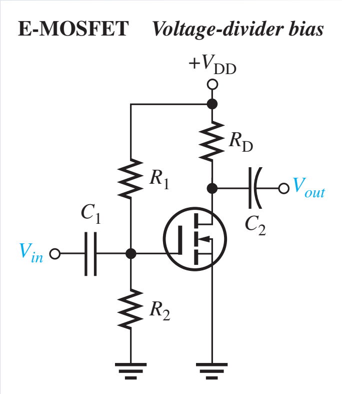
- $I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$
- $A_v = g_m R_d$
- $R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}}\right)$

D-MOSFET ***Zero-bias***


$+V_{DD}$
R_D
V_{out}
C_1
$V_G = 0$
C_2
V_{in}
R_G

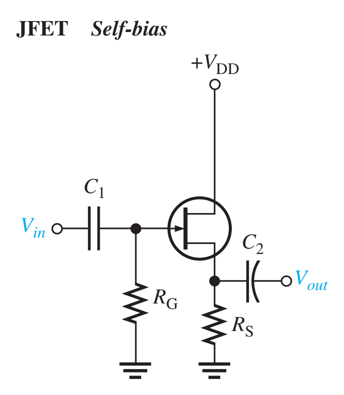
- $I_D = I_{DSS}$
- $A_v = g_m R_d$
- $R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}}\right)$

E-MOSFET ***Voltage-divider bias***


$+V_{DD}$
R_D
R_1
V_{out}
C_1
C_2
V_{in}
R_2

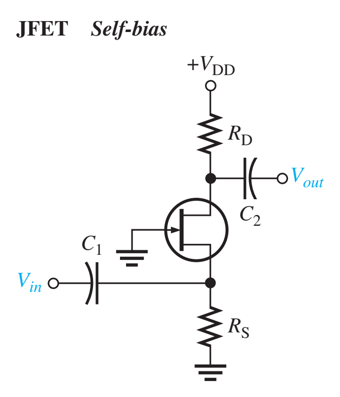
- $I_D = K(V_{GS} - V_{GS(th)})^2$
- $A_v = g_m R_d$
- $R_{in} = R_1 \| R_2 \| \left(\frac{V_{GS}}{I_{GSS}}\right)$

COMMON-DRAIN AMPLIFIER


JFET Self-bias
$+V_{DD}$
C_1
V_{in}
C_2
V_{out}
R_G
R_S

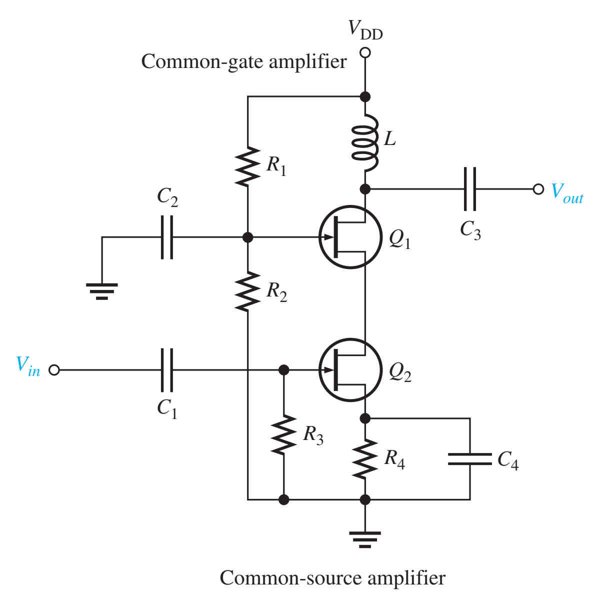
- $I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$
- $A_v = \frac{g_m R_s}{1 + g_m R_s}$
- $R_{in} = R_G \parallel \left(\frac{V_{GS}}{I_{GSS}}\right)$

COMMON-GATE AMPLIFIER


JFET Self-bias
$+V_{DD}$
R_D
V_{out}
C_2
C_1
V_{in}
R_S

- $I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$
- $A_v = g_m R_d$
- $R_{in} = \left(\frac{1}{g_m}\right) \parallel R_S$

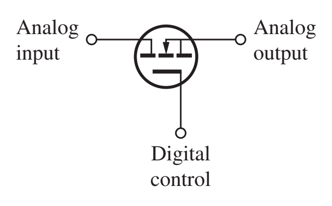
CASCODE AMPLIFIER


V_{DD}
Common-gate amplifier
L
R_1
C_2
V_{out}
Q_1
C_3
R_2
V_{in}
Q_2
C_1
R_3
R_4
C_4
Common-source amplifier

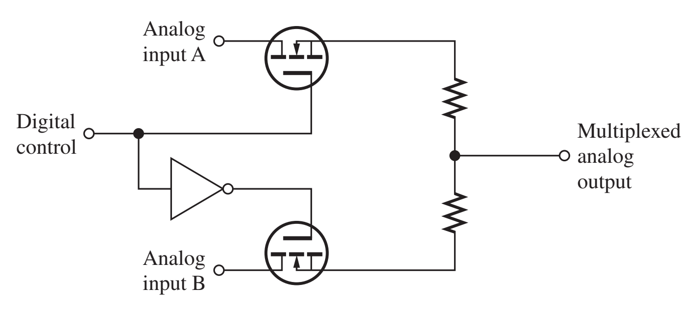
- $A_v \cong g_{m(CG)} X_L$

SUMMARY OF FET SWITCHING CIRCUITS

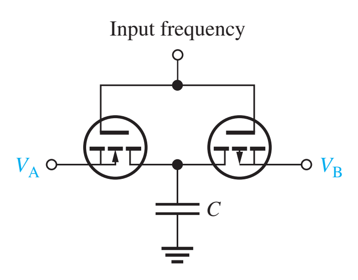
ANALOG SWITCH


Analog input
Analog output
Digital control

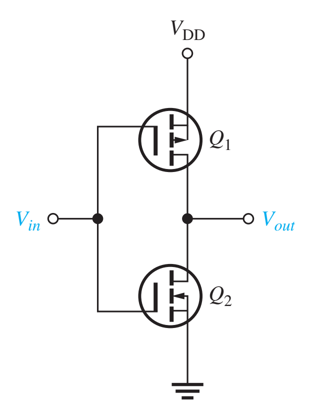
ANALOG MULTIPLEXER


Analog input A
Digital control
Multiplexed analog output
Analog input B

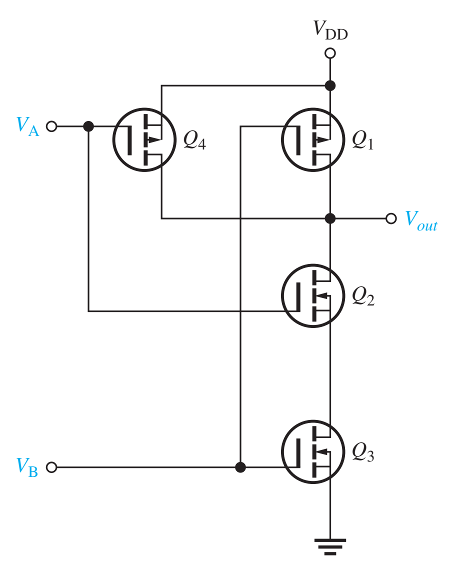
SWITCHED CAPACITOR


Input frequency
V_A
V_B
C

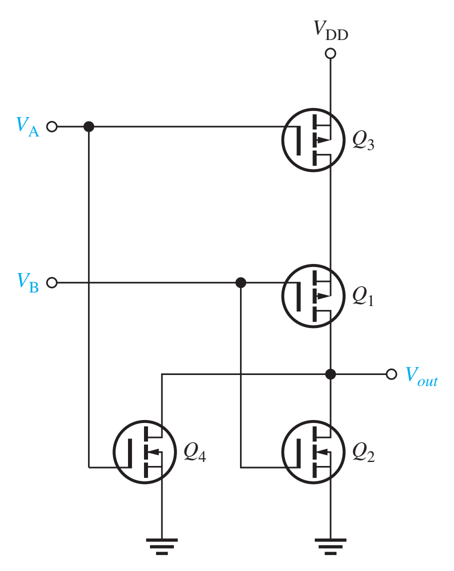
CMOS INVERTER


V_{DD}
Q_1
V_{in}
V_{out}
Q_2

CMOS NAND GATE


V_{DD}
V_A
Q_4
Q_1
V_{out}
Q_2
V_B
Q_3

CMOS NOR GATE


V_{DD}
V_A
Q_3
V_B
Q_1
V_{out}
Q_4
Q_2

SUMMARY

Section 9–1

- The transconductance, g_m, of a FET relates the output current, I_d, to the input voltage, V_{gs}.
- The voltage gain of a common-source amplifier is determined largely by the transconductance, g_m, and the drain resistance, R_d.
- The internal drain-to-source resistance, r'_{ds}, of a FET influences (reduces) the gain if it is not sufficiently greater than R_d so that it can be neglected.
- An unbypassed resistance between source and ground (R_S) reduces the voltage gain of a FET amplifier.
- A load resistance connected to the drain of a common-source amplifier reduces the voltage gain.
- There is a 180° phase inversion between gate and drain voltages.
- The input resistance at the gate of a FET is extremely high.

Section 9–2

- The voltage gain of a common-drain amplifier (source-follower) is always slightly less than 1.
- There is no phase inversion between gate and source in a source-follower.

Section 9–3

- The input resistance of a common-gate amplifier is the reciprocal of g_m.
- The cascode amplifier combines a CS amplifier and a CG amplifier.

Section 9–4

- The class D amplifier is a nonlinear amplifier because the transistors operate as switches.
- The class D amplifier uses pulse-width modulation (PWM) to represent the input signal.
- A low-pass filter converts the PWM signal back to the original input signal.
- The efficiency of a class D amplifier approaches 100%.

Section 9–5

- An analog switch passes or blocks an analog signal when turned *on* or *off* by a digital control input.
- A sampling circuit is an analog switch that is turned *on* for short time intervals to allow a sufficient number of discrete input signal values to appear on the output so that the input signal can be accurately represented by those discrete values.
- An analog multiplexer consists of two or more analog switches that connect sampled portions of their analog input signals to a single output in a time sequence.
- Switched-capacitors are used to emulate resistance in programmable IC analog arrays.

Section 9–6

- Complementary MOS (CMOS) is used in low-power digital switching circuits.
- CMOS uses an *n*-channel MOSFET and a *p*-channel MOSFET connected in series.
- The inverter, NAND gate, and NOR gate are examples of digital logic circuits.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Analog switch A device that switches an analog signal on and off.

Class D A nonlinear amplifier in which the transistors are operated as switches.

CMOS Complementary MOS.

Common-drain A FET amplifier configuration in which the drain is the grounded terminal.

Common-gate A FET amplifier configuration in which the gate is the grounded terminal.

Common-source A FET amplifier configuration in which the source is the grounded terminal.

Pulse-width modulation A process in which a signal is converted to a series of pulses with widths that vary proportionally to the signal amplitude.

Source-follower The common-drain amplifier.

KEY FORMULAS

Common-Source Amplifier

9–1	$A_v = g_m R_d$	Voltage gain with source grounded or R_s bypassed
9–2	$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$	Self-biased JFET current

9–3	$A_v = g_m R_d$	Voltage gain
9–4	$R_{in} = R_G \parallel \left(\frac{V_{GS}}{I_{GSS}}\right)$	Input resistance, self-bias and zero-bias
9–5	$R_{in} = R_1 \parallel R_2 \parallel R_{IN(gate)}$	Input resistance, voltage-divider bias

Common-Drain Amplifier

9–6	$A_v = \frac{g_m R_s}{1 + g_m R_s}$	Voltage gain
9–7	$R_{in} = R_G \parallel R_{IN(gate)}$	Input resistance

Common-Gate Amplifier

9–8	$A_v = g_m R_d$	Voltage gain
9–9	$R_{in(source)} = \frac{1}{g_m}$	Input resistance

MOSFET Analog Switching

9–10	$R = \frac{1}{fC}$	Emulated resistance

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. A common-source (CS) amplifier has a very high input resistance.
2. The drain current in a CS amplifier can be calculated using a quadratic formula.
3. The voltage gain of a CS amplifier is the transconductance times the source resistance.
4. There is no phase inversion in a CS amplifier.
5. A CS amplifier using a D-MOSFET can operate with both positive and negative input voltages.
6. A common-drain (CD) amplifier is called a *drain-follower.*
7. The input resistance of a CD amplifier is very low.
8. The input resistance of a common-gate (CG) amplifier is very low.
9. A cascode amplifier uses both a CS and a CG amplifier.
10. The class D amplifier always operates in the linear region.
11. The class D amplifier uses pulse-width modulation.
12. An analog switch is controlled by a digital input.
13. The purpose of a switched-capacitor circuit is to emulate resistance.
14. CMOS is a device used in linear amplifiers.
15. CMOS utilizes a *pnp* MOSFET and an *npn* MOSFET connected together.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the drain current is increased in Figure 9–9, V_{GS} will
   (a) increase **(b)** decrease **(c)** not change
2. If the JFET in Figure 9–9 is substituted with one having a lower value of I_{DSS}, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
3. If the JFET in Figure 9–9 is substituted with one having a lower value of $V_{GS(off)}$, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
4. If the value of R_G in Figure 9–9 is increased, V_{GS} will
   (a) increase **(b)** decrease **(c)** not change

5. If the value of R_G in Figure 9–11 is increased, the input resistance seen by the signal source will

   (a) increase **(b)** decrease **(c)** not change

6. If the value of R_1 in Figure 9–17 is increased, V_{GS} will

   (a) increase **(b)** decrease **(c)** not change

7. If the value of R_L in Figure 9–17 is decreased, the voltage gain will

   (a) increase **(b)** decrease **(c)** not change

8. If the value of R_S in Figure 9–20 is increased, the voltage gain will

   (a) increase **(b)** decrease **(c)** not change

9. If C_4 in Figure 9–46 opens, the output signal voltage will

   (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 9–1

1. In a common-source amplifier, the output voltage is

   (a) 180° out of phase with the input **(b)** in phase with the input
   (c) taken at the source **(d)** taken at the drain
   (e) answers (a) and (c) **(f)** answers (a) and (d)

2. In a certain common-source (CS) amplifier, $V_{ds} = 3.2$ V rms and $V_{gs} = 280$ mV rms. The voltage gain is

   (a) 1 **(b)** 11.4 **(c)** 8.75 **(d)** 3.2

3. In a certain CS amplifier, $R_D = 1.0\text{ k}\Omega$, $R_S = 560\ \Omega$, $V_{DD} = 10$ V, and $g_m = 4500\ \mu\text{S}$. If the source resistor is completely bypassed, the voltage gain is

   (a) 450 **(b)** 45 **(c)** 4.5 **(d)** 2.52

4. Ideally, the equivalent circuit of a FET contains

   (a) a current source in series with a resistance
   (b) a resistance between drain and source terminals
   (c) a current source between gate and source terminals
   (d) a current source between drain and source terminals

5. The value of the current source in Question 4 is dependent on the

   (a) transconductance and gate-to-source voltage
   (b) dc supply voltage
   (c) external drain resistance
   (d) answers (b) and (c)

6. A certain common-source amplifier has a voltage gain of 10. If the source bypass capacitor is removed,

   (a) the voltage gain will increase
   (b) the transconductance will increase
   (c) the voltage gain will decrease
   (d) the Q-point will shift

7. A CS amplifier has a load resistance of $10\text{ k}\Omega$ and $R_D = 820\ \Omega$. If $g_m = 5$ mS and $V_{in} = 500$ mV, the output signal voltage is

   (a) 1.89 V **(b)** 2.05 V **(c)** 25 V **(d)** 0.5 V

8. If the load resistance in Question 7 is removed, the output voltage will

   (a) stay the same **(b)** decrease **(c)** increase **(d)** be zero

Section 9–2

9. A certain common-drain (CD) amplifier with $R_S = 1.0\text{ k}\Omega$ has a transconductance of $6000\ \mu\text{S}$. The voltage gain is

   (a) 1 **(b)** 0.86 **(c)** 0.98 **(d)** 6

10. The datasheet for the transistor used in a CD amplifier specifies $I_{GSS} = 5$ nA at $V_{GS} = 10$ V. If the resistor from gate to ground, R_G, is 50 MΩ, the total input resistance is approximately

(a) 50 MΩ **(b)** 200 MΩ **(c)** 40 MΩ **(d)** 20.5 MΩ

Section 9–3

11. The common-gate (CG) amplifier differs from both the CS and CD configurations in that it has a

(a) much higher voltage gain **(b)** much lower voltage gain

(c) much higher input resistance **(d)** much lower input resistance

12. If you are looking for both good voltage gain and high input resistance, you must use a

(a) CS amplifier **(b)** CD amplifier **(c)** CG amplifier

13. A cascode amplifier consists of

(a) a CD and a CS amplifier **(b)** a CS and a CG amplifier

(c) a CG and a CD amplifier **(d)** two CG amplifiers

Section 9–4

14. The class D amplifier is similar to

(a) class C **(b)** class B **(c)** class A **(d)** none of these

15. The class D amplifier uses

(a) frequency modulation **(b)** amplitude modulation

(c) pulse-width modulation **(d)** duty cycle modulation

Section 9–5

16. E-MOSFETs are generally used for switching applications because of their

(a) threshold characteristic **(b)** high input resistance

(c) linearity **(d)** high gain

17. A sampling circuit must sample a signal at a minimum of

(a) one time per cycle **(b)** the signal frequency

(c) twice the signal frequency **(d)** alternate cycles

18. The value of resistance emulated by a switched-capacitor circuit is a function of

(a) voltage and capacitance **(b)** frequency and capacitance

(c) gain and transconductance **(d)** frequency and transconductance

Section 9–6

19. A basic CMOS circuit uses a combination of

(a) *n*-channel MOSFETs **(b)** *p*-channel MOSFETs

(c) *pnp* and *npn* BJTs **(d)** an *n*-channel and a *p*-channel MOSFET

20. CMOS is commonly used in

(a) digital circuits **(b)** linear circuits **(c)** RF circuits **(d)** power circuits

Section 9–7

21. If there is an internal open between the drain and source in a CS amplifier, the drain voltage is equal to

(a) 0 V **(b)** V_{DD} **(c)** V_{GS} **(d)** V_{GD}

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 9–1

The Common-Source Amplifier

1. A FET has a $g_m = 6000\ \mu$S. Determine the rms drain current for each of the following rms values of V_{gs}.

(a) 10 mV **(b)** 150 mV **(c)** 0.6 V **(d)** 1 V

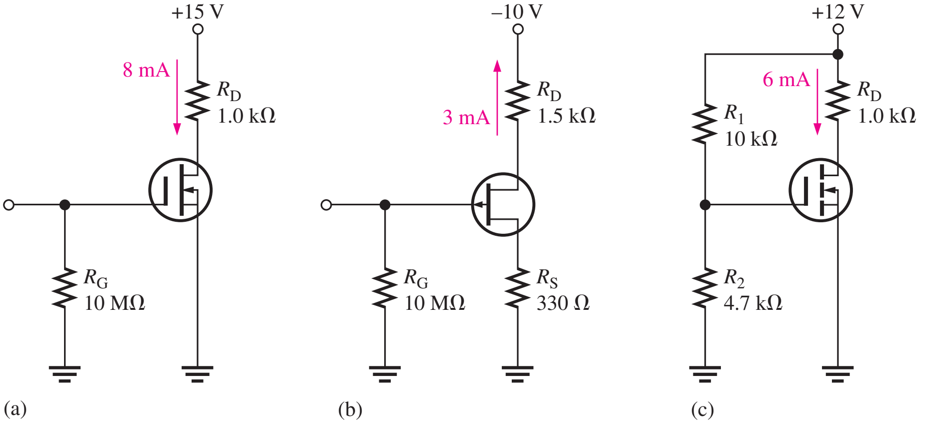
2. The gain of a certain JFET amplifier with a source resistance of zero is 20. Determine the drain resistance if the g_m is 3500 μS.

3. A certain FET amplifier has a g_m of 4.2 mS, $r'_{ds} = 12$ kΩ, and $R_D = 4.7$ kΩ. What is the voltage gain? Assume the source resistance is 0 Ω.

4. What is the gain for the amplifier in Problem 3 if the source resistance is 1.0 kΩ?

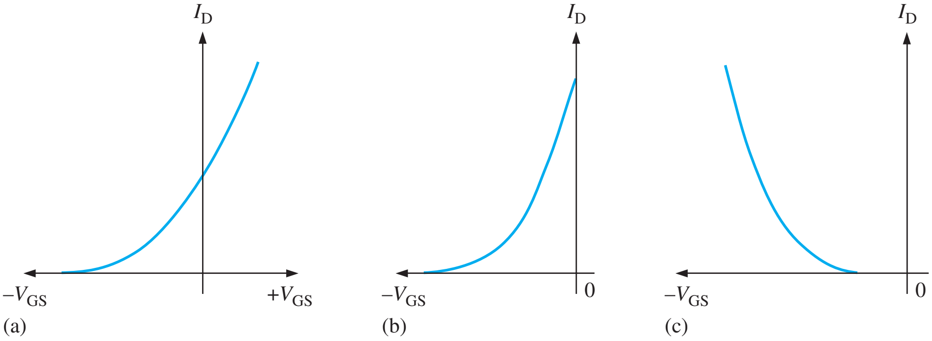
5. Identify the type of FET and its bias arrangement in Figure 9–54. Ideally, what is V_{GS}?
6. Calculate the dc voltages from each terminal to ground for the FETs in Figure 9–54.

▶ FIGURE 9–54


+15 V
8 mA
R_D
1.0 kΩ
R_G
10 MΩ
(a)
−10 V
3 mA
R_D
1.5 kΩ
R_G
10 MΩ
R_S
330 Ω
(b)
+12 V
6 mA
R_1
10 kΩ
R_D
1.0 kΩ
R_2
4.7 kΩ
(c)

7. Identify each characteristic curve in Figure 9–55 by the type of FET that it represents.

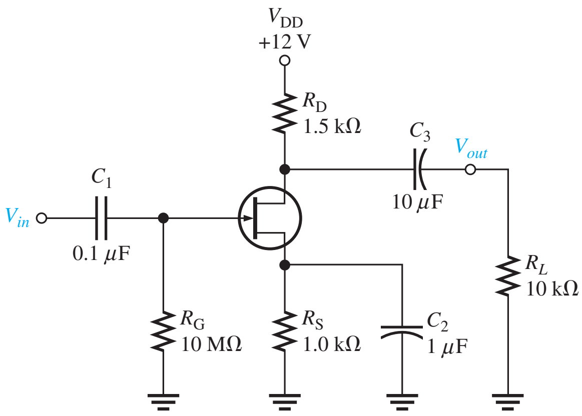
▶ FIGURE 9–55



8. Refer to the JFET transfer characteristic curve in Figure 9–16(a) and determine the peak-to-peak value of I_d when V_{gs} is varied ±1.5 V about its Q-point value.
9. Repeat Problem 8 for the curves in Figure 9–16(b) and Figure 9–16(c).
10. Given that $I_D = 2.83$ mA in Figure 9–56, find V_{DS} and V_{GS}. $V_{GS(off)} = -7$ V and $I_{DSS} = 8$ mA.
11. If a 50 mV rms input signal is applied to the amplifier in Figure 9–56, what is the peak-to-peak output voltage? $g_m = 5000\ \mu S$.
12. If a 1500 Ω load is ac coupled to the output in Figure 9–56, what is the resulting output voltage (rms) when a 50 mV rms input is applied? $g_m = 5000\ \mu S$.

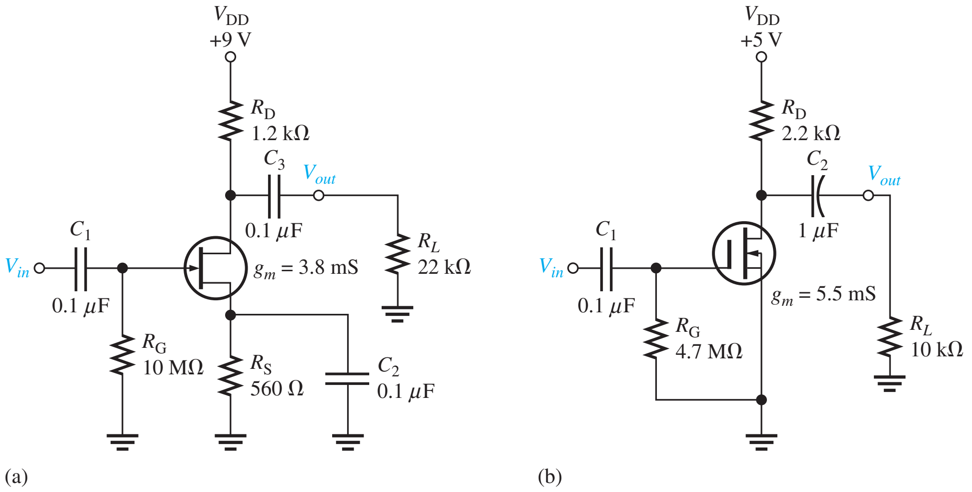
▶ FIGURE 9–56

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F09-56).


V_{DD}
+12 V
R_D
1.5 kΩ
C_3
V_{out}
10 μF
C_1
V_{in}
0.1 μF
R_L
10 kΩ
R_G
10 MΩ
R_S
1.0 kΩ
C_2
1 μF

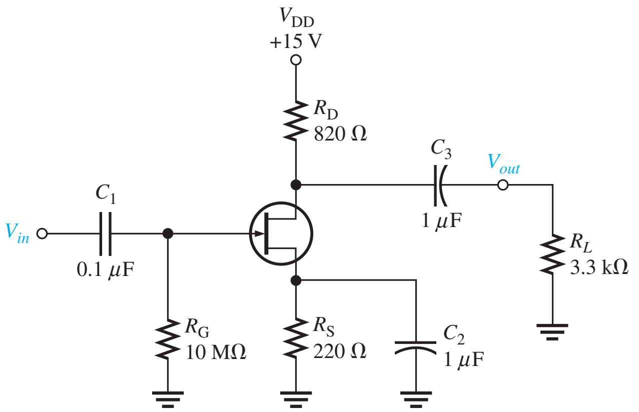
13. Determine the voltage gain of each common-source amplifier in Figure 9–57.

FIGURE 9–57


V_{DD}
+9 V
R_D
1.2 kΩ
C_3
V_{out}
0.1 μF
C_1
V_{in}
0.1 μF
g_m = 3.8 mS
R_L
22 kΩ
R_G
10 MΩ
R_S
560 Ω
C_2
0.1 μF
(a)
V_{DD}
+5 V
R_D
2.2 kΩ
C_2
V_{out}
1 μF
C_1
V_{in}
0.1 μF
g_m = 5.5 mS
R_G
4.7 MΩ
R_L
10 kΩ
(b)

14. Draw the dc and ac equivalent circuits for the amplifier in Figure 9–58.

FIGURE 9–58


V_{DD}
+15 V
R_D
820 Ω
C_3
V_{out}
1 μF
C_1
V_{in}
0.1 μF
R_L
3.3 kΩ
R_G
10 MΩ
R_S
220 Ω
C_2
1 μF

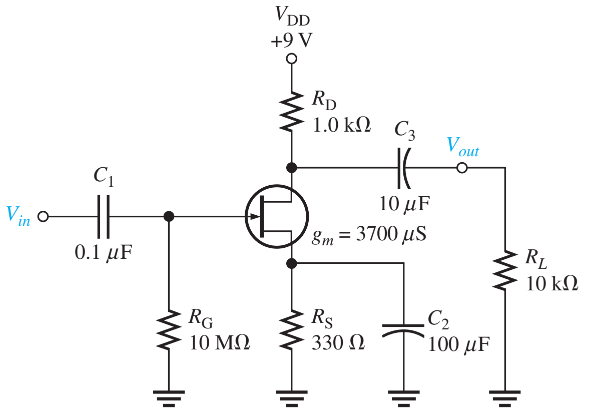
15. Determine the drain current in Figure 9–58 given that $I_{DSS} = 15$ mA and $V_{GS(off)} = -4$ V. The Q-point is centered.

16. What is the gain of the amplifier in Figure 9–58 if C_2 is removed?

17. A 4.7 kΩ resistor is connected in parallel with R_L in Figure 9–58. What is the voltage gain?

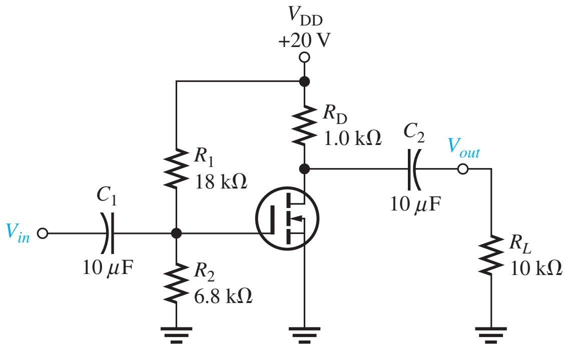
18. For the common-source amplifier in Figure 9–59, determine I_D, V_{GS}, and V_{DS} for a centered *Q*-point. $I_{DSS} = 9$ mA, and $V_{GS(off)} = -3$ V.

FIGURE 9–59


V_{DD}
+9 V
R_D
1.0 kΩ
C_3
V_{out}
10 μF
C_1
V_{in}
0.1 μF
g_m = 3700 μS
R_L
10 kΩ
R_G
10 MΩ
R_S
330 Ω
C_2
100 μF

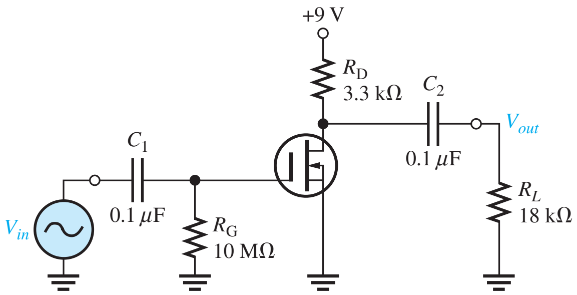
19. If a 10 mV rms signal is applied to the input of the amplifier in Figure 9–59, what is the rms value of the output signal?

20. Determine V_{GS}, I_D, and V_{DS} for the amplifier in Figure 9–60. $I_{D(on)} = 18$ mA at $V_{GS} = 10$ V, $V_{GS(th)} = 2.5$ V, and $g_m = 3000\ \mu S$.


V_{DD}
+20 V
R_D
1.0 kΩ
C_2
V_{out}
10 μF
R_1
18 kΩ
C_1
V_{in}
10 μF
R_2
6.8 kΩ
R_L
10 kΩ

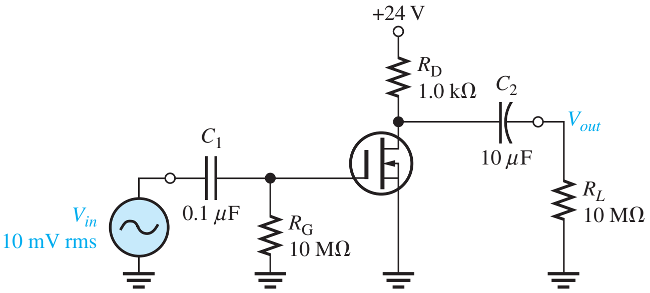
▲ FIGURE 9–60

21. Determine R_{in} seen by the signal source in Figure 9–61. $I_{GSS} = 25$ nA at $V_{GS} = -15$ V.


+9 V
R_D
3.3 kΩ
C_2
V_{out}
0.1 μF
C_1
V_{in}
0.1 μF
R_G
10 MΩ
R_L
18 kΩ

▲ FIGURE 9–61

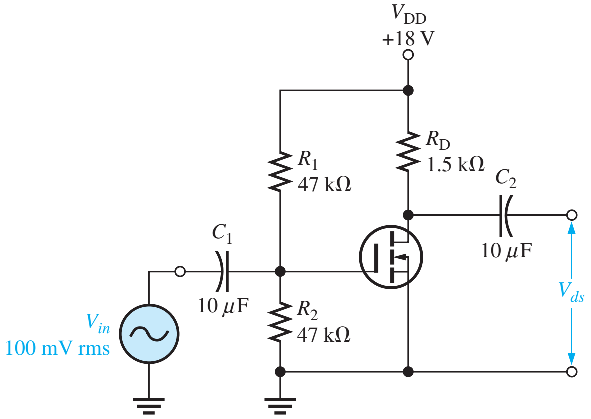
22. Determine the total drain voltage waveform (dc and ac) and the V_{out} waveform in Figure 9–62. $g_m = 4.8$ mS and $I_{DSS} = 15$ mA. Observe that $V_{GS} = 0$.


+24 V
R_D
1.0 kΩ
C_2
V_{out}
10 μF
C_1
0.1 μF
V_{in}
10 mV rms
R_G
10 MΩ
R_L
10 MΩ

▲ FIGURE 9–62

23. For the unloaded amplifier in Figure 9–63, find V_{GS}, I_D, V_{DS}, and the rms output voltage V_{ds}. $I_{D(on)} = 8$ mA at $V_{GS} = 12$ V, $V_{GS(th)} = 4$ V, and $g_m = 4500$ S.

▶ FIGURE 9–63

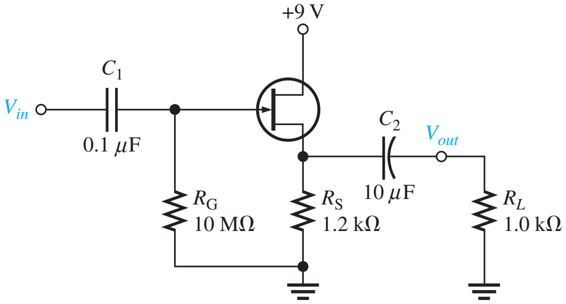


V_{DD}
+18 V
R_1
47 kΩ
R_D
1.5 kΩ
C_2
10 μF
C_1
10 μF
V_{ds}
V_{in}
100 mV rms
R_2
47 kΩ

Section 9–2 The Common-Drain Amplifier

24. For the source-follower in Figure 9–64, determine the voltage gain and input resistance. $I_{GSS} = 50$ pA at $V_{GS} = -15$ V and $g_m = 5500$ μS.

▶ FIGURE 9–64

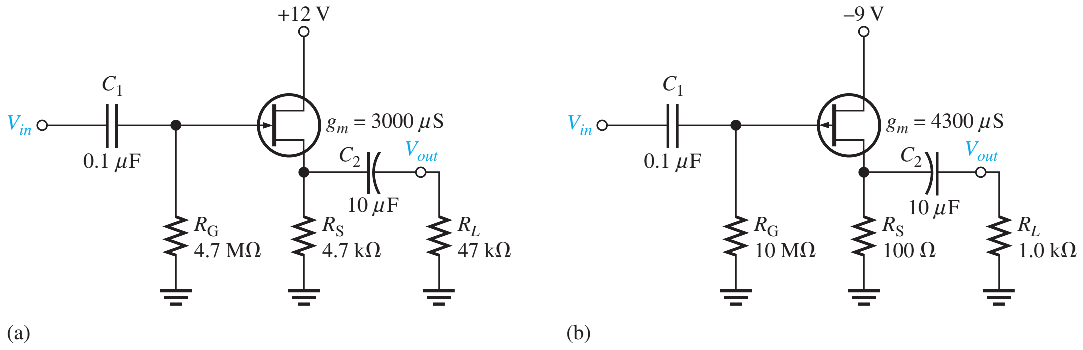


+9 V
C_1
V_{in}
0.1 μF
C_2
V_{out}
R_G
10 MΩ
R_S
1.2 kΩ
10 μF
R_L
1.0 kΩ

25. If the JFET in Figure 9–64 is replaced with one having a g_m of 3000 μS, what are the gain and the input resistance with all other conditions the same?

26. Find the gain of each amplifier in Figure 9–65.

27. Determine the voltage gain of each amplifier in Figure 9–65 when the capacitively coupled load is changed to 10 kΩ.



+12 V
C_1
V_{in}
0.1 μF
$g_m = 3000$ μS
C_2
V_{out}
10 μF
R_G
4.7 MΩ
R_S
4.7 kΩ
R_L
47 kΩ
(a)
–9 V
C_1
V_{in}
0.1 μF
$g_m = 4300$ μS
C_2
V_{out}
10 μF
R_G
10 MΩ
R_S
100 Ω
R_L
1.0 kΩ
(b)

▲ FIGURE 9–65

Section 9–3 The Common-Gate Amplifier

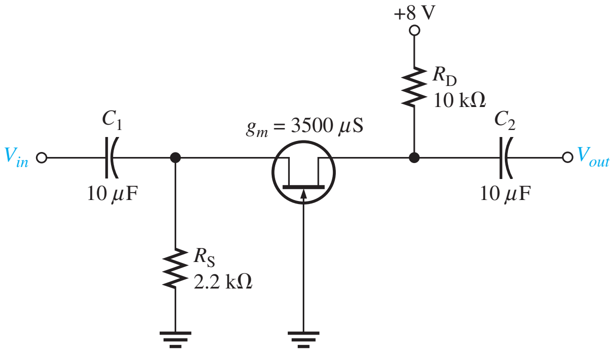
28. A common-gate amplifier has a $g_m = 4000\ \mu\text{S}$ and $R_d = 1.5\ \text{k}\Omega$. What is its gain?

29. What is the input resistance of the amplifier in Problem 28?

30. Determine the voltage gain and input resistance of the common-gate amplifier in Figure 9–66.

31. For a cascode amplifier like shown in Figure 9–24, $g_m = 2800\ \mu\text{S}$, $I_{GSS} = 2$ nA at $V_{GS} = 15$ V. If $R_3 = 15\ \text{M}\Omega$ and $L = 1.5$ mH, determine the voltage gain and the input impedance at $f = 100$ MHz.

▶ FIGURE 9–66



Section 9–4 The Class D Amplifier

32. A class D amplifier has an output of ±9 V. If the input signal is 5 mV, what is the voltage gain?

33. A certain class D amplifier dissipates an internal power of 140 mW in the comparator and the triangular wave generator. Each complementary MOSFET has 0.25 V drop in the *on* state. The amplifier operates from ±12 Vdc sources and provides 0.35 A to a load. Determine the efficiency.

Section 9–5 MOSFET Analog Switching

34. An analog switch uses an *n*-channel MOSFET with $V_{GS(th)} = 4$ V. A voltage of +8 V is applied to the gate. Determine the maximum peak-to-peak input signal that can be applied if the drain-to-source voltage drop is neglected.

35. An analog switch is used to sample a signal with a maximum frequency of 15 kHz. Determine the minimum frequency of the pulses applied to the MOSFET gate.

36. A switched-capacitor circuit uses a 10 pF capacitor. Determine the frequency required to emulate a 10 kΩ resistor.

37. For a frequency of 25 kHz, what is the emulated resistance in a switched-capacitor circuit if $C = 0.001\ \mu\text{F}$?

Section 9–6 MOSFET Digital Switching

38. What is the output voltage of a CMOS inverter that operates with $V_{DD} = +5$ V, when the input is 0 V? When the input is +5 V?

39. For each of the following input combinations, determine the output of a CMOS NAND gate that operates with $V_{DD} = +3.3$ V.

(a) $V_A = 0$ V, $V_B = 0$ V

(b) $V_A = +3.3$ V, $V_B = 0$ V

(c) $V_A = 0$ V, $V_B = +3.3$ V

(d) $V_A = +3.3$ V, $V_B = +3.3$ V

40. Repeat Problem 39 for a CMOS NOR gate.

41. List two advantages of the MOSFET over the BJT in power switching.

Section 9–7 Troubleshooting

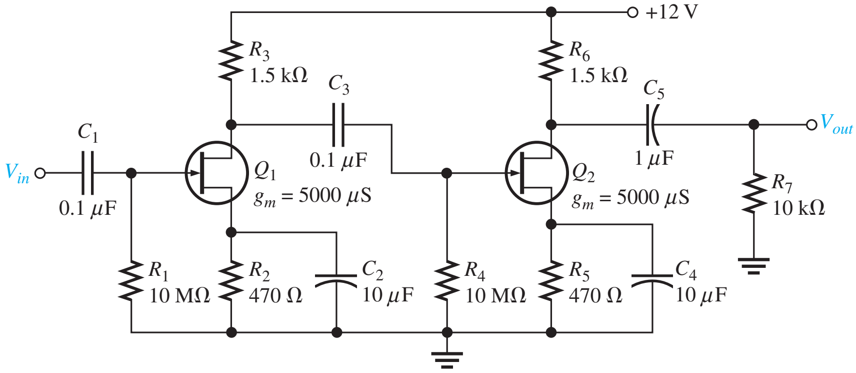
42. What symptom(s) would indicate each of the following failures when a signal voltage is applied to the input in Figure 9–67?

- **(a)** Q_1 open from drain to source
- **(b)** R_3 open
- **(c)** C_2 shorted
- **(d)** C_3 open
- **(e)** Q_2 open from drain to source

43. If $V_{in} = 10$ mV rms in Figure 9–67, what is V_{out} for each of the following faults?

- **(a)** C_1 open
- **(b)** C_4 open
- **(c)** a short from the source of Q_2 to ground
- **(d)** Q_2 has an open gate

▶ FIGURE 9–67



DATASHEET PROBLEMS

44. What type of FET is the 2N3796?

45. Referring to the datasheet in Figure 9–68, determine the following:

- **(a)** typical $V_{GS(off)}$ for the 2N3796
- **(b)** maximum drain-to-source voltage for the 2N3797
- **(c)** maximum power dissipation for the 2N3797 at an ambient temperature of 25°C
- **(d)** maximum gate-to-source voltage for the 2N3797

46. Referring to Figure 9–68, determine the maximum power dissipation for a 2N3796 at an ambient temperature of 55°C.

47. Referring to Figure 9–68, determine the minimum g_{m0} for the 2N3796 at a frequency of 1 kHz.

48. What is the drain current when $V_{GS} = +3.5$ V for the 2N3797?

49. Typically, what is the drain current for a zero-biased 2N3796?

50. What is the maximum possible voltage gain for a 2N3796 common-source amplifier with $R_d = 2.2\text{ k}\Omega$?

ADVANCED PROBLEMS

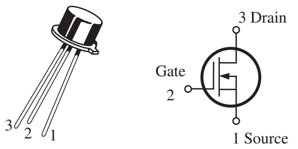
51. The MOSFET in a certain single-stage common-source amplifier has a range of forward transconductance values from 2.5 mS to 7.5 mS. If the amplifier is capacitively coupled to a variable load that ranges from 4 kΩ to 10 kΩ and the dc drain resistance is 1.0 kΩ, determine the minimum and maximum voltage gains.

52. Design an amplifier using a 2N3797 that operates from a 24 V supply voltage. The typical dc drain-to-source voltage should be approximately 12 V and the typical voltage gain should be approximately 9.

53. Modify the amplifier you designed in Problem 52 so that the voltage gain can be set at 9 for any randomly selected 2N3797.

2N3796
2N3797

Case 22-03, Style 2
TO-18 (TO-206AA)



MOSFETs
Low Power Audio
***N*-channel — Depletion**

Maximim Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage 2N3796 2N3797	V_{DS}	 25 20	V dc
Gate-Source voltage	V_{GS}	±10	V dc
Drain current	I_D	20	mA dc
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction temperature	T_J	+175	°C
Storage channel temperature range	T_{stg}	– 65 to + 200	°C

Electrical Characteristics (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF Characteristics						
Drain-Source breakdown voltage ($V_{GS} = -4.0$ V, $I_D = 5.0\ \mu$A) ($V_{GS} = -7.0$ V, $I_D = 5.0\ \mu$A)	 2N3796 2N3797	$V_{(BR)DSX}$	 25 20	 30 25	 – –	V dc
Gate reverse current ($V_{GS} = -10$ V, $V_{DS} = 0$) ($V_{GS} = -10$ V, $V_{DS} = 0$, $T_A = 150°C$)		I_{GSS}	 – –	 – –	 1.0 200	pA dc
Gate-Source cutoff voltage ($I_D = 0.5\ \mu$A, $V_{DS} = 10$ V) ($I_D = 2.0\ \mu$A, $V_{DS} = 10$ V)	2N3796 2N3797	$V_{GS(off)}$	 – –	 – 3.0 – 5.0	 – 4.0 – 7.0	V dc
Drain-Gate reverse current ($V_{DG} = 10$ V, $I_S = 0$)		I_{DGO}	–	–	1.0	pA dc
ON Characteristics						
Zero-gate-voltage drain current ($V_{DS} = 10$ V, $V_{GS} = 0$)	 2N3796 2N3797	I_{DSS}	 0.5 2.0	 1.5 2.9	 3.0 6.0	mA dc
On-State drain current ($V_{DS} = 10$ V, $V_{GS} = +3.5$ V)	2N3796 2N3797	$I_{D(on)}$	 7.0 9.0	 8.3 14	 14 18	mA dc
Small-Signal Characteristics						
Forward transfer admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz)	 2N3796 2N3797	$\lvert Y_{fs} \rvert$	 900 1500	 1200 2300	 1800 3000	μmhos or μS
($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	2N3796 2N3797		900 1500	– –	– –	
Output admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz)	 2N3796 2N3797	$\lvert Y_{os} \rvert$	 – –	 12 27	 25 60	μmhos or μS
Input capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	 2N3796 2N3797	C_{iss}	 – –	 5.0 6.0	 7.0 8.0	pF
Reverse transfer capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz)		C_{rss}	–	0.5	0.8	pF

▲ FIGURE 9–68

Partial datasheet for the 2N3796 and 2N3797 D-MOSFETs.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

54. Open file TSP09-54 and determine the fault.

55. Open file TSP09-55 and determine the fault.

56. Open file TSP09-56 and determine the fault.

57. Open file TSP09-57 and determine the fault.

58. Open file TSP09-58 and determine the fault.

59. Open file TSP09-59 and determine the fault.

60. Open file TSP09-60 and determine the fault.

61. Open file TSP09-61 and determine the fault.

62. Open file TSP09-62 and determine the fault.

AMPLIFIER FREQUENCY RESPONSE

10

CHAPTER OUTLINE

10–1 Basic Concepts
10–2 The Decibel
10–3 Low-Frequency Amplifier Response
10–4 High-Frequency Amplifier Response
10–5 Total Amplifier Frequency Response
10–6 Frequency Response of Multistage Amplifiers
10–7 Frequency Response Measurements
Application Activity

CHAPTER OBJECTIVES

- Explain how circuit capacitances affect the frequency response of an amplifier
- Use the decibel (dB) to express amplifier gain
- Analyze the low-frequency response of an amplifier
- Analyze the high-frequency response of an amplifier
- Analyze an amplifier for total frequency response
- Analyze multistage amplifiers for frequency response
- Measure the frequency response of an amplifier

KEY TERMS

- Decibel
- Midrange gain
- Critical frequency
- Roll-off
- Decade
- Bode Plot
- Bandwidth

APPLICATION ACTIVITY PREVIEW

In the Application Activity, you will modify the PA system preamp from Chapter 6 to increase the low-frequency response to reduce the effects of 60 Hz interference.

VISIT THE COMPANION WEBSITE

Study aids and all Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In the previous chapters on amplifiers, the effects of the input frequency on an amplifier's operation due to capacitive elements in the circuit were neglected in order to focus on other concepts. The coupling and bypass capacitors were considered to be ideal shorts and the internal transistor capacitances were considered to be ideal opens. This treatment is valid when the frequency is in an amplifier's midrange.

As you know, capacitive reactance decreases with increasing frequency and vice versa. When the frequency is low enough, the coupling and bypass capacitors can no longer be considered as shorts because their reactances are large enough to have a significant effect. Also, when the frequency is high enough, the internal transistor capacitances can no longer be considered as opens because their reactances become small enough to have a significant effect on the amplifier operation. A complete picture of an amplifier's response must take into account the full range of frequencies over which the amplifier can operate.

In this chapter, you will study the frequency effects on amplifier gain and phase shift. The coverage applies to both BJT and FET amplifiers, and a mix of both are included to illustrate the concepts.

10–1 BASIC CONCEPTS

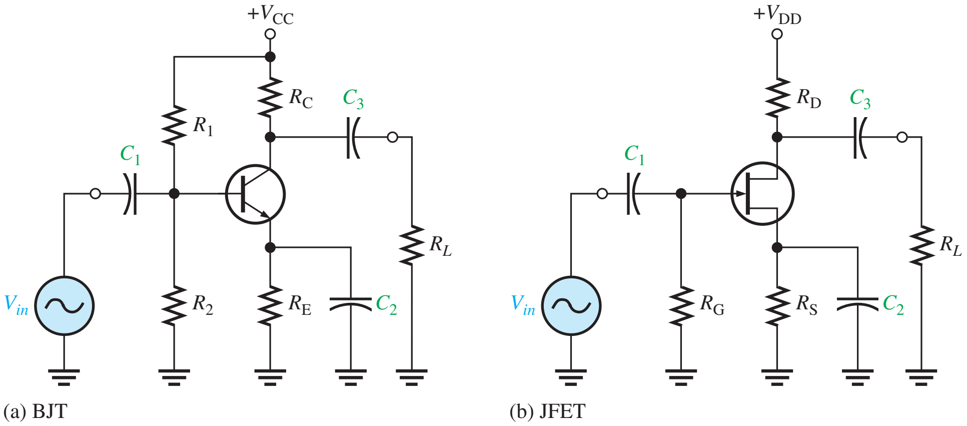
In amplifiers, the coupling and bypass capacitors appear to be shorts to ac at the midband frequencies. At low frequencies the capacitive reactance of these capacitors affect the gain and phase shift of signals, so they must be taken into account. The **frequency response** of an amplifier is the change in gain or phase shift over a specified range of input signal frequencies.

After completing this section, you should be able to

- ❑ **Explain how circuit capacitances affect the frequency response of an amplifier**
    - ◆ Define frequency response
- ❑ Discuss the effect of coupling capacitors
    - ◆ Recall the formula for capacitive reactance
- ❑ Discuss the effect of bypass capacitors
- ❑ Describe the effect of internal transistor capacitances
    - ◆ Identify the internal capacitance in BJTs and JFETs
- ❑ Explain Miller's theorem
    - ◆ Calculate the Miller input and output capacitances

Effect of Coupling Capacitors

Recall from basic circuit theory that $X_C = 1/(2\pi fC)$. This formula shows that the capacitive reactance varies inversely with frequency. At lower frequencies the reactance is greater, and it decreases as the frequency increases. At lower frequencies—for example, audio frequencies below 10 Hz—capacitively coupled amplifiers such as those in Figure 10–1 have less voltage gain than they have at higher frequencies. The reason is that at lower frequencies more signal voltage is dropped across C_1 and C_3 because their reactances are higher. This higher signal voltage drop at lower frequencies reduces the voltage gain. Also, a phase shift is introduced by the coupling capacitors because C_1 forms a lead circuit with the R_{in} of the amplifier and C_3 forms a lead circuit with R_L in series with R_C or R_D. Recall that a *lead circuit* is an RC circuit in which the output voltage across R leads the input voltage in phase.



(a) BJT (b) JFET

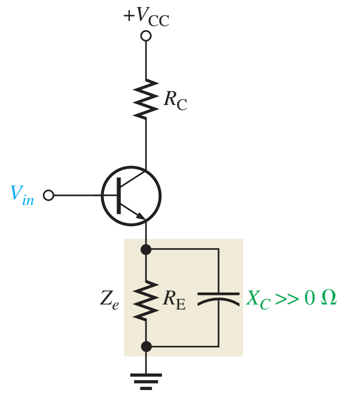
▲ FIGURE 10–1

Examples of capacitively coupled BJT and FET amplifiers.

Effect of Bypass Capacitors

At lower frequencies, the reactance of the bypass capacitor, C_2 in Figure 10–1, becomes significant and the emitter (or FET source terminal) is no longer at ac ground. The capacitive reactance X_{C2} in parallel with R_E (or R_S) creates an impedance that reduces the gain. This is illustrated in Figure 10–2.

For example, when the frequency is sufficiently high, $X_C \cong 0\ \Omega$ and the voltage gain of the CE amplifier is $A_v = R_C/r'_e$. At lower frequencies, $X_C \gg 0\ \Omega$ and the voltage gain is $A_v = R_C/(r'_e + Z_e)$.



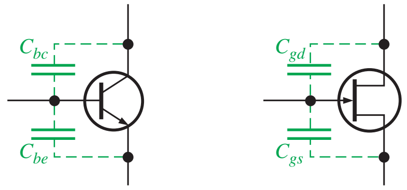
▲ **FIGURE 10–2**

Nonzero reactance of the bypass capacitor in parallel with R_E creates an emitter impedance, (Z_e), which reduces the voltage gain.

Effect of Internal Transistor Capacitances

At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances, however, do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases.

Figure 10–3 shows the internal *pn* junction capacitances for both a bipolar junction transistor and a JFET. In the case of the BJT, C_{be} is the base-emitter junction capacitance and C_{bc} is the base-collector junction capacitance. In the case of the JFET, C_{gs} is the capacitance between gate and source and C_{gd} is the capacitance between gate and drain.



(a) BJT

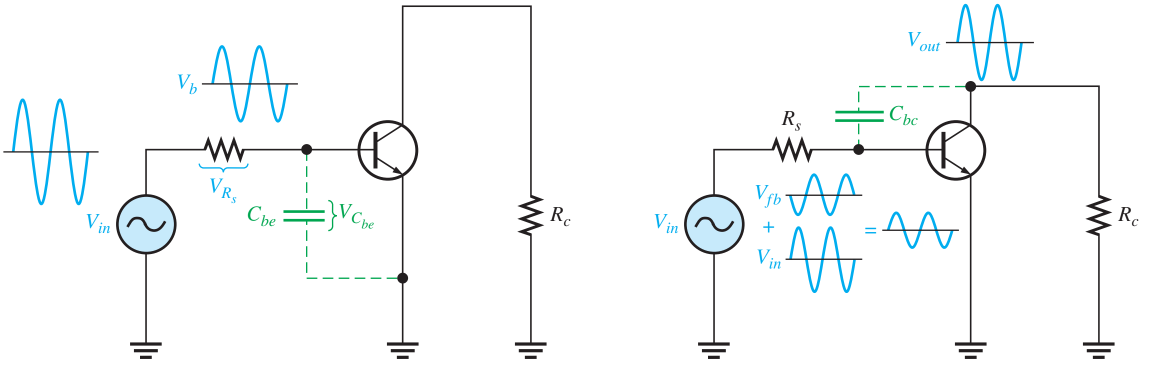
(b) JFET

▲ **FIGURE 10–3**

Internal transistor capacitances.

Datasheets often refer to the BJT capacitance C_{bc} as the output capacitance, often designated C_{ob}. The capacitance C_{be} is often designated as the input capacitance C_{ib}. Datasheets for FETs normally specify input capacitance C_{iss} and reverse transfer capacitance C_{rss}. From these, C_{gs} and C_{gd} can be calculated, as you will see in Section 10–4.

At lower frequencies, the internal capacitances have a very high reactance because of their low capacitance value (usually only a few picofarads) and the low frequency value. Therefore, they look like opens and have no effect on the transistor's performance. As the frequency goes up, the internal capacitive reactances go down, and at some point they begin to have a significant effect on the transistor's gain. When the reactance of C_{be} (or C_{gs}) becomes small enough, a significant amount of the signal voltage is lost due to a voltage-divider effect of the signal source resistance and the reactance of C_{be}, as illustrated in Figure 10–4(a). When the



(a) Effect of C_{be}, where V_b is reduced by the voltage-divider action of R_s and $X_{C_{be}}$.

(b) Effect of C_{bc}, where part of V_{out} (V_{fb}) goes back through C_{bc} to the base and reduces the input signal because it is approximately 180° out of phase with V_{in}.

▲ **FIGURE 10–4**

AC equivalent circuit for a BJT amplifier showing effects of the internal capacitances C_{be} and C_{bc}.

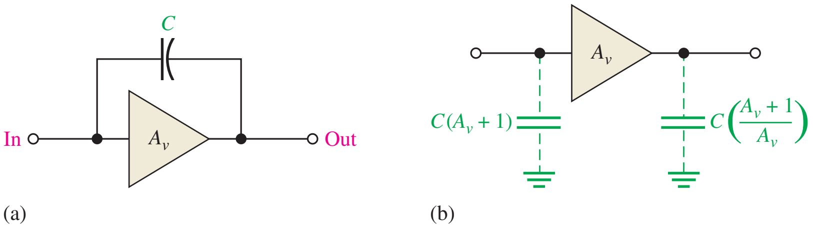
reactance of C_{bc} (or C_{gd}) becomes small enough, a significant amount of output signal voltage is fed back out of phase with the input (negative feedback), thus effectively reducing the voltage gain. This is illustrated in Figure 10–4(b).

Miller's Theorem

Miller's theorem is used to simplify the analysis of inverting amplifiers at high frequencies where the internal transistor capacitances are important. The capacitance C_{bc} in BJTs (C_{gd} in FETs) between the input (base or gate) and the output (collector or drain) is shown in Figure 10–5(a) in a generalized form. A_v is the absolute voltage gain of the inverting amplifier at midrange frequencies, and C represents either C_{bc} or C_{gd}.

▶ FIGURE 10–5

General case of Miller input and output capacitances. C represents C_{bc} or C_{gd}.

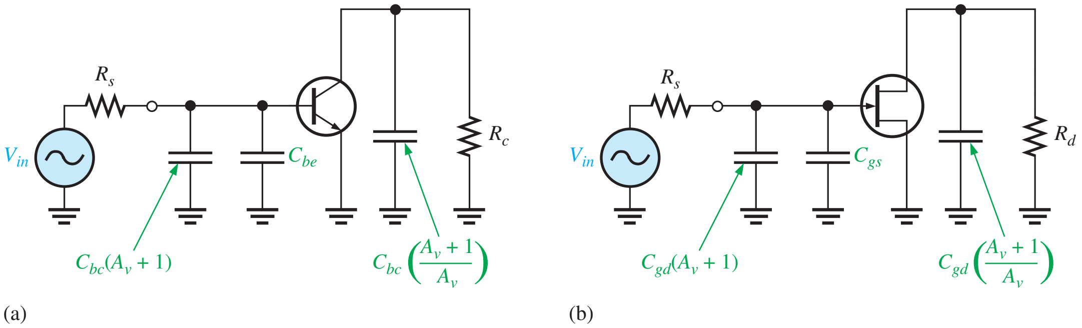


Miller's theorem states that C effectively appears as a capacitance from input to ground, as shown in Figure 10–5(b), that can be expressed as follows:

Equation 10–1

$$C_{in(Miller)} = C(A_v + 1)$$

This formula shows that C_{bc} (or C_{gd}) has a much greater impact on input capacitance than its actual value. For example, if $C_{bc} = 6$ pF and the amplifier gain is 50, then $C_{in(Miller)} =$ 306 pF. Figure 10–6 shows how this effective input capacitance appears in the actual ac equivalent circuit in parallel with C_{be} (or C_{gs}).



▲ FIGURE 10–6

Amplifier ac equivalent circuits showing internal capacitances and effective Miller capacitances.

Miller's theorem also states that C effectively appears as a capacitance from output to ground, as shown in Figure 10–5(b), that can be expressed as follows:

Equation 10–2

$$C_{out(Miller)} = C\left(\frac{A_v + 1}{A_v}\right)$$

This formula indicates that if the voltage gain is 10 or greater, $C_{out(Miller)}$ is approximately equal to C_{bc} or C_{gd} because $(A_v + 1)/A_v$ is approximately equal to 1. Figure 10–6 also shows how this effective output capacitance appears in the ac equivalent circuit for BJTs and FETs. Equations 10–1 and 10–2 are derived in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

SECTION 10–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. In an ac amplifier, which capacitors affect the low-frequency gain?
2. How is the high-frequency gain of an amplifier limited?
3. When can coupling and bypass capacitors be neglected?
4. Determine $C_{in(Miller)}$ if $A_v = -50$ and $C_{bc} = 5$ pF.
5. Determine $C_{out(Miller)}$ if $A_v = -25$ and $C_{bc} = 3$ pF.

10–2 THE DECIBEL

The decibel is a unit of logarithmic gain measurement and is commonly used to express amplifier response.

After completing this section, you should be able to

- ❑ **Use the decibel (dB) to express amplifier gain**
  - ◆ Express power gain and voltage gain in dB
- ❑ Discuss the 0 dB reference
  - ◆ Define *midrange gain*
- ❑ Define and discuss the critical frequency
- ❑ Discuss power measurement in dBm
  - ◆ Identify the internal capacitance in BJTs and JFETs
- ❑ Explain Miller's theorem
  - ◆ Calculate the Miller input and output capacitances

The use of decibels to express gain was introduced in Chapter 6. The decibel unit is important in amplifier measurements. The basis for the decibel unit stems from the logarithmic response of the human ear to the intensity of sound. The **decibel** is a logarithmic measurement of the ratio of one power to another or one voltage to another. Power gain is expressed in decibels (dB) by the following formula:

$$A_{p(\mathrm{dB})} = 10 \log A_p$$

Equation 10–3

where A_p is the actual power gain, P_{out}/P_{in}. Voltage gain is expressed in decibels by the following formula:

$$A_{v(\mathrm{dB})} = 20 \log A_v$$

Equation 10–4

If A_v is greater than 1, the dB gain is positive. If A_v is less than 1, the dB gain is negative and is usually called *attenuation.* You can use the LOG key on your calculator when working with these formulas.

EXAMPLE 10–1

Express each of the following ratios in dB:

(a) $\dfrac{P_{out}}{P_{in}} = 250$ **(b)** $\dfrac{P_{out}}{P_{in}} = 100$ **(c)** $A_v = 10$

(d) $A_p = 0.5$ **(e)** $\dfrac{V_{out}}{V_{in}} = 0.707$

Solution

(a) $A_{p(\mathrm{dB})} = 10 \log (250) = \mathbf{24\ dB}$

(b) $A_{p(\mathrm{dB})} = 10 \log (100) = \mathbf{20\ dB}$

(c) $A_{v(\text{dB})} = 20 \log (10) = \mathbf{20\ dB}$

(d) $A_{p(\text{dB})} = 10 \log (0.5) = \mathbf{-3\ dB}$

(e) $A_{v(\text{dB})} = 20 \log (0.707) = \mathbf{-3\ dB}$

*Related Problem** Express each of the following gains in dB: **(a)** $A_v = 1200$, **(b)** $A_p = 50$, **(c)** $A_v = 125{,}000$.

***Answers can be found at www.pearsonhighered.com/floyd.**

FYI

The factor of 20 in Equation 10–4 is because power is proportional to voltage squared. Technically, the equation should be applied only when the voltages are measured in the same impedance. This is the case for many communication systems, such as in television or microwave systems.

0 dB Reference

It is often convenient in amplifiers to assign a certain value of gain as the 0 dB reference. This does not mean that the actual voltage gain is 1 (which is 0 dB); it means that the reference gain, no matter what its actual value, is used as a reference with which to compare other values of gain and is therefore assigned a 0 dB value.

Many amplifiers exhibit a maximum gain over a certain range of frequencies and a reduced gain at frequencies below and above this range. The maximum gain occurs for the range of frequencies between the upper and lower critical frequencies and is called the **midrange gain**, which is assigned a 0 dB value. Any value of gain below midrange can be referenced to 0 dB and expressed as a negative dB value. For example, if the midrange voltage gain of a certain amplifier is 100 and the gain at a certain frequency below midrange is 50, then this reduced voltage gain can be expressed as $20 \log (50/100) = 20 \log (0.5) = -6$ dB. This indicates that it is 6 dB *below* the 0 dB reference. Halving the output voltage for a steady input voltage is always a 6 dB *reduction* in the gain. Correspondingly, a doubling of the output voltage is always a 6 dB *increase* in the gain. Figure 10–7 illustrates a normalized gain-versus-frequency curve showing several dB points. The term *normalized* means that the midrange voltage gain is assigned a value of 1 or 0 dB.

FIGURE 10–7

Normalized voltage gain versus frequency curve.

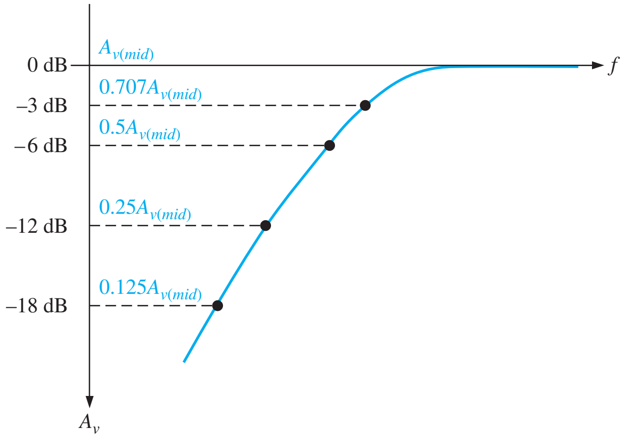


Table 10–1 shows how doubling or halving voltage gains translates into decibel values. Notice in the table that every time the voltage gain is doubled, the decibel value increases by 6 dB, and every time the gain is halved, the dB value decreases by 6 dB.

Critical Frequency

A **critical frequency** (also known as **cutoff frequency** or *corner frequency*) is a frequency at which the output power drops to one-half of its midrange value. This corresponds to a 3 dB reduction in the power gain, as expressed in dB by the following formula:

$$A_{p(\text{dB})} = 10 \log (0.5) = -3 \text{ dB}$$

TABLE 10–1

Decibel values corresponding to doubling and halving of the voltage gain.

VOLTAGE GAIN (A_v)	DECIBEL VALUE*
32	$20 \log (32) = 30$ dB
16	$20 \log (16) = 24$ dB
8	$20 \log (8) = 18$ dB
4	$20 \log (4) = 12$ dB
2	$20 \log (2) = 6$ dB
1	$20 \log (1) = 0$ dB
0.707	$20 \log (0.707) = -3$ dB
0.5	$20 \log (0.5) = -6$ dB
0.25	$20 \log (0.25) = -12$ dB
0.125	$20 \log (0.125) = -18$ dB
0.0625	$20 \log (0.0625) = -24$ dB
0.03125	$20 \log (0.03125) = -30$ dB

*Decibel values are with respect to zero reference.

Also, at the critical frequencies the voltage gain is 70.7% of its midrange value and is expressed in dB as

$$\mathbf{A_{v(dB)} = 20 \log (0.707) = -3 \text{ dB}}$$

EXAMPLE 10–2

A certain amplifier has a midrange rms output voltage of 10 V. What is the rms output voltage for each of the following dB gain reductions with a constant rms input voltage?

(a) −3 dB **(b)** −6 dB **(c)** −12 dB **(d)** −24 dB

Solution Multiply the midrange output voltage by the voltage gain corresponding to the specified decibel value in Table 10–1.

(a) At −3 dB, $V_{out} = 0.707(10 \text{ V}) = \mathbf{7.07 \text{ V}}$

(b) At −6 dB, $V_{out} = 0.5(10 \text{ V}) = \mathbf{5 \text{ V}}$

(c) At −12 dB, $V_{out} = 0.25(10 \text{ V}) = \mathbf{2.5 \text{ V}}$

(d) At −24 dB, $V_{out} = 0.0625(10 \text{ V}) = \mathbf{0.625 \text{ V}}$

Related Problem Determine the output voltage at the following decibel levels for a midrange value of 50 V:

(a) 0 dB **(b)** −18 dB **(c)** −30 dB

Power Measurement in dBm

The **dBm** is a unit for measuring power levels referenced to 1 mW. Positive dBm values represent power levels above 1 mW, and negative dBm values represent power levels below 1 mW.

Because the decibel (dB) can be used to represent only power *ratios,* not actual power, the dBm provides a convenient way to express actual power output of an amplifier or other device. Each 3 dBm increase corresponds to a doubling of the power, and a 3 dBm decrease corresponds to a halving of the power.

To state that an amplifier has a 3 dB power gain indicates only that the output power is twice the input power and nothing about the actual output power. To indicate actual output

FYI

The unit of dBmV is used in some applications such as cable TV where the reference level is 1 mV, which corresponds to 0 dB. Just as the dBm is used to indicate actual power, the dBmV unit is used to indicate actual voltage.

TABLE 10–2

Power in terms of dBm.

POWER	dBm
32 mW	15 dBm
16 mW	12 dBm
8 mW	9 dBm
4 mW	6 dBm
2 mW	3 dBm
1 mW	0 dBm
0.5 mW	−3 dBm
0.25 mW	−6 dBm
0.125 mW	−9 dBm
0.0625 mW	−12 dBm
0.03125 mW	−15 dBm

power, the dBm can be used. For example, 3 dBm is equivalent to 2 mW because 2 mW is twice the 1 mW reference. 6 dBm is equivalent to 4 mW, and so on. Likewise, −3 dBm is the same as 0.5 mW. Table 10–2 shows several values of power in terms of dBm.

SECTION 10–2 CHECKUP

1. How much increase in actual voltage gain corresponds to +12 dB?
2. Convert a power gain of 25 to decibels.
3. What power corresponds to 0 dBm?

10–3 LOW-FREQUENCY AMPLIFIER RESPONSE

The voltage gain and phase shift of capacitively coupled amplifiers are affected when the signal frequency is below a critical value. At low frequencies, the reactance of the coupling capacitors becomes significant, resulting in a reduction in voltage gain and an increase in phase shift. Frequency responses of both BJT and FET capacitively coupled amplifiers are discussed.

After completing this section, you should be able to

- ☐ **Analyze the low-frequency response of an amplifier**
- ☐ Analyze a BJT amplifier
  - ◆ Calculate the midrange voltage gain ◆ Identify the parts of the amplifier that affect low-frequency response
- ☐ Identify and analyze the BJT amplifier's input *RC* circuit
  - ◆ Calculate the lower critical frequency and gain roll-off ◆ Sketch a Bode plot ◆ Define *decade* and *octave* ◆ Determine the phase shift
- ☐ Identify and analyze the BJT amplifier's output *RC* circuit
  - ◆ Calculate the lower critical frequency ◆ Determine the phase shift
- ☐ Identify and analyze the BJT amplifier's bypass *RC* circuit
  - ◆ Calculate the lower critical frequency ◆ Explain the effect of a swamping resistor
- ☐ Analyze a FET amplifier
- ☐ Identify and analyze the D-MOSFET amplifier's input *RC* circuit
  - ◆ Calculate the lower critical frequency ◆ Determine the phase shift
- ☐ Identify and analyze the D-MOSFET amplifier's output *RC* circuit
  - ◆ Calculate the lower critical frequency ◆ Determine the phase shift

- ❑ Explain the total low-frequency response of an amplifier
    - ◆ Illustrate the response with Bode plots
- ❑ Simulate the frequency response using Multisim
    - ◆ Calculate the lower critical frequency ◆ Determine the phase shift

BJT Amplifiers

A typical capacitively coupled common-emitter amplifier is shown in Figure 10–8. Assuming that the coupling and bypass capacitors are ideal shorts at the midrange signal frequency, you can determine the midrange voltage gain using Equation 10–5, where $R_c = R_C \| R_L$.

$$\boldsymbol{A_{v(mid)} = \frac{R_c}{r'_e}}$$

Equation 10–5

If a swamping resistor (R_{E1}) is used, it appears in series with r'_e and the equation becomes

$$A_{v(mid)} = \frac{R_c}{r'_e + R_{E1}}$$

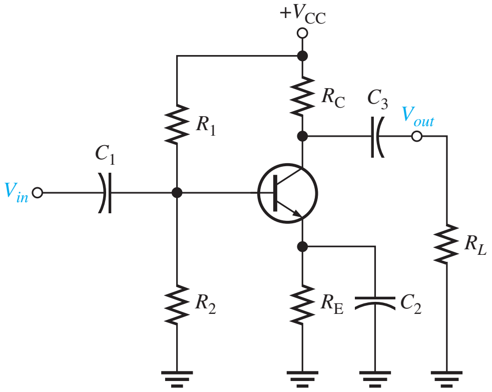


FIGURE 10–8

A capacitively coupled BJT amplifier.

The BJT amplifier in Figure 10–8 has three high-pass *RC* circuits that affect its gain as the frequency is reduced below midrange. These are shown in the low-frequency ac equivalent circuit in Figure 10–9. Unlike the ac equivalent circuit used in previous chapters, which represented midrange response ($X_C \cong 0\ \Omega$), the low-frequency equivalent circuit retains the coupling and bypass capacitors because X_C is not small enough to neglect when the signal frequency is sufficiently low.

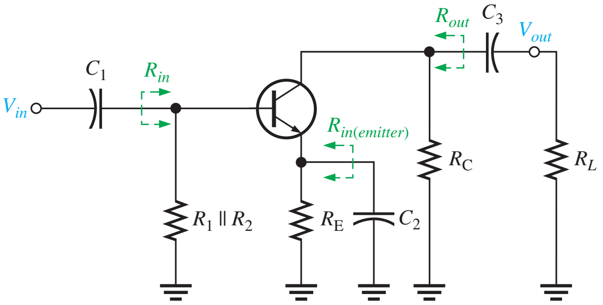


FIGURE 10–9

The low-frequency ac equivalent circuit of the amplifier in Figure 10–8 consists of three high-pass *RC* circuits.

One *RC* circuit is formed by the input coupling capacitor C_1 and the input resistance of the amplifier. The second *RC* circuit is formed by the output coupling capacitor C_3, the resistance looking in at the collector (R_{out}), and the load resistance. The third *RC* circuit that affects the low-frequency response is formed by the emitter-bypass capacitor C_2 and the resistance looking in at the emitter.

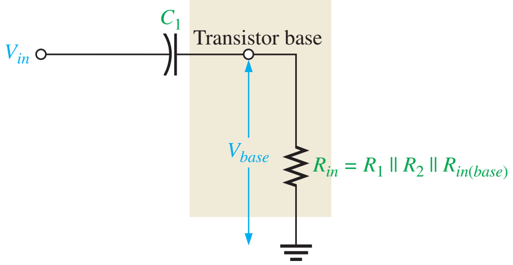
The Input *RC* Circuit

The input *RC* circuit for the BJT amplifier in Figure 10–8 is formed by C_1 and the amplifier's input resistance and is shown in Figure 10–10. (Input resistance was discussed in Chapter 6.) As the signal frequency decreases, X_{C1} increases. This causes less voltage across the input resistance of the amplifier at the base because more voltage is dropped across C_1 and because of this, the overall voltage gain of the amplifier is reduced. The base voltage for the input *RC* circuit in Figure 10–10 (neglecting the internal resistance of the input signal source) can be stated as

$$V_{base} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}}\right)V_{in}$$

► FIGURE 10–10

Input *RC* circuit formed by the input coupling capacitor and the amplifier's input resistance.



As previously mentioned, a critical point in the amplifier's response occurs when the output voltage is 70.7% of its midrange value. This condition occurs in the input *RC* circuit when $X_{C1} = R_{in}$.

$$V_{base} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + R_{in}^2}}\right)V_{in} = \left(\frac{R_{in}}{\sqrt{2R_{in}^2}}\right)V_{in} = \left(\frac{R_{in}}{\sqrt{2}R_{in}}\right)V_{in} = \left(\frac{1}{\sqrt{2}}\right)V_{in} = 0.707V_{in}$$

In terms of measurement in decibels,

$$20 \log\left(\frac{V_{base}}{V_{in}}\right) = 20 \log (0.707) = -3 \text{ dB}$$

Lower Critical Frequency The condition where the gain is down 3 dB is logically called the −3 *dB point* of the amplifier response; the overall gain is 3 dB less than at midrange frequencies because of the attenuation (gain less than 1) of the input *RC* circuit. The frequency, f_{cl}, at which this condition occurs is called the *lower critical frequency* (also known as the *lower cutoff frequency, lower corner frequency,* or *lower break frequency*) and can be calculated as follows:

$$X_{C1} = \frac{1}{2\pi f_{cl(input)}C_1} = R_{in}$$

Equation 10–6

$$\boldsymbol{f_{cl(input)} = \frac{1}{2\pi R_{in}C_1}}$$

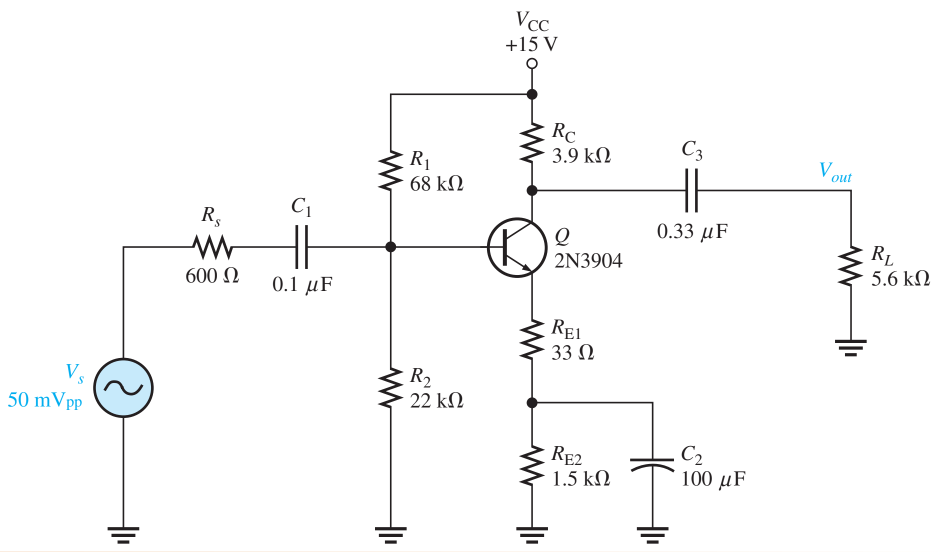
If the resistance of the input source is taken into account, Equation 10–6 becomes

$$f_{cl(input)} = \frac{1}{2\pi(R_s + R_{in})C_1}$$

EXAMPLE 10–3

For the circuit in Figure 10–11, calculate the lower critical frequency due to the input *RC* circuit. Assumed $r'_e = 9.6\ \Omega$ and $\beta = 200$. Notice that a swamping resistor, R_{E1}, is used.

▶ **FIGURE 10–11**



Solution The input resistance is

$$R_{in} = R_1 \| R_2 \| (\beta(r'_e + R_{E1})) = 68\text{ k}\Omega \| 22\text{ k}\Omega \| (200(9.6\ \Omega + 33\ \Omega)) = 5.63\text{ k}\Omega$$

The lower critical frequency is

$$f_{cl(input)} = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(5.63\text{ k}\Omega)(0.1\ \mu\text{F})} = \mathbf{282\ Hz}$$

Related Problem What value of input capacitor will move the lower cutoff frequency to 130 Hz?

Open the Multisim file E10-03 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. The Bode plotter is not an actual instrument available, but allows the user to see the response of a circuit in the frequency domain (frequency is the independent variable). Notice that C_2 and C_3 are taken out of the calculation by making their value huge (1 F!). While this is unrealistic, it works nicely for the computer simulation to isolate the input response.

Voltage Gain Roll-Off at Low Frequencies As you have seen, the input *RC* circuit reduces the overall voltage gain of an amplifier by 3 dB when the frequency is reduced to the critical value f_c. As the frequency continues to decrease below f_c, the overall voltage gain also continues to decrease. The rate of decrease in voltage gain with frequency is called **roll-off**. For each ten times reduction in frequency below f_c, *there is a 20 dB reduction in voltage gain.*

Let's consider a frequency that is one-tenth of the critical frequency ($f = 0.1f_c$). Since $X_{C1} = R_{in}$ at f_c, then $X_{C1} = 10R_{in}$ at $0.1f_c$ because of the inverse relationship of X_{C1} and f. The attenuation of the input *RC* circuit is, therefore,

$$\text{Attenuation} = \frac{V_{base}}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + (10R_{in})^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + 100R_{in}^2}}$$

$$= \frac{R_{in}}{\sqrt{R_{in}^2(1 + 100)}} = \frac{R_{in}}{R_{in}\sqrt{101}} = \frac{1}{\sqrt{101}} \cong \frac{1}{10} = 0.1$$

HISTORY NOTE

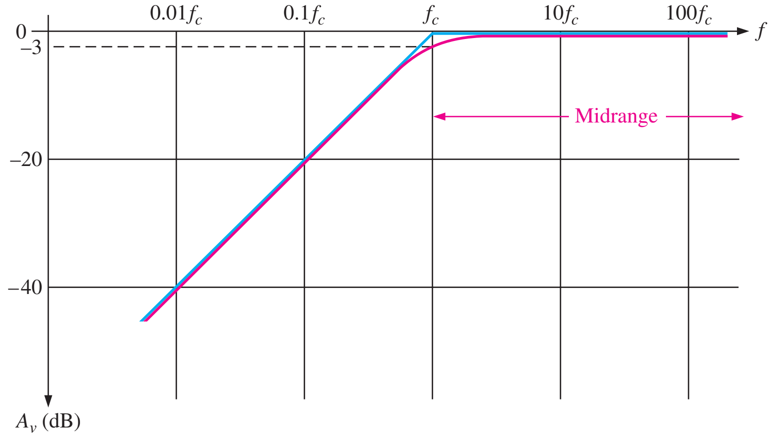
Hendrik Wade Bode pronounced *Boh-dee* (1905–1982) was born in Madison, Wisconsin. He received his B.A. degree in 1924, at the age of 19, from Ohio State University and his M.A. degree in 1926, both in Mathematics. He was hired by Bell Labs and completed his Ph.D. in Physics in 1935. In 1938 he developed his now well-known magnitude and phase plots. His work on automatic control systems introduced innovative methods to the study of system stability.

The dB attenuation is

$$20\log\left(\frac{V_{base}}{V_{in}}\right) = 20\log(0.1) = -20\text{ dB}$$

The Bode Plot A ten-times change in frequency is called a **decade**. So, for the input *RC* circuit, the attenuation is reduced by 20 dB for each decade that the frequency decreases below the critical frequency. This causes the overall voltage gain to drop 20 dB per decade.

A plot of dB voltage gain versus frequency on semilog graph paper (logarithmic horizontal axis scale and a linear vertical axis scale) is called a **Bode plot**. A generalized Bode plot for an input *RC* circuit appears in Figure 10–12. The ideal response curve is shown in blue. Notice that it is flat (0 dB) down to the critical frequency, at which point the gain drops at −20 dB/decade as shown. Above f_c are the midrange frequencies. The actual response curve is shown in red. Notice that it decreases gradually beginning in midrange and is down to −3 dB at the critical frequency. Often, the ideal response is used to simplify amplifier analysis. As previously mentioned, the critical frequency at which the curve "breaks" into a −20 dB/decade drop is sometimes called the *lower break frequency.*



▲ FIGURE 10–12

Bode plot. (Blue is ideal; red is actual.)

Sometimes, the voltage gain roll-off of an amplifier is expressed in dB/octave rather than dB/decade. An **octave** corresponds to a doubling or halving of the frequency. For example, an increase in frequency from 100 Hz to 200 Hz is an octave. Likewise, a decrease in frequency from 100 kHz to 50 kHz is also an octave. A rate of −20 dB/decade is approximately equivalent to −6 dB/octave, a rate of −40 dB/decade is approximately equivalent to −12 dB/octave, and so on.

EXAMPLE 10–4

The midrange voltage gain of a certain amplifier is 100. The input *RC* circuit has a lower critical frequency of 1 kHz. Determine the actual voltage gain at $f = 1$ kHz, $f = 100$ Hz, and $f = 10$ Hz.

Solution When $f = 1$ kHz, the voltage gain is 3 dB less than at midrange. At −3 dB, the voltage gain is reduced by a factor of 0.707.

$$A_v = (0.707)(100) = \mathbf{70.7}$$

When $f = 100\text{ Hz} = 0.1f_c$, the voltage gain is 20 dB less than at f_c. The voltage gain at −20 dB is one-tenth of that at the midrange frequencies.

$$A_v = (0.1)(100) = \mathbf{10}$$

When $f = 10\text{ Hz} = 0.01f_c$, the voltage gain is 20 dB less than at $f = 0.1f_c$ or -40 dB. The voltage gain at -40 dB is one-tenth of that at -20 dB or one-hundredth that at the midrange frequencies.

$$A_v = (0.01)(100) = \mathbf{1}$$

Related Problem The midrange voltage gain of an amplifier is 300. The lower critical frequency of the input *RC* circuit is 400 Hz. Determine the actual voltage gain at 400 Hz, 40 Hz, and 4 Hz.

Phase Shift in the Input RC Circuit In addition to reducing the voltage gain, the input *RC* circuit also causes an increasing phase shift through an amplifier as the frequency decreases. At midrange frequencies, the phase shift through the input *RC* circuit is approximately zero because the capacitive reactance, X_{C1}, is approximately 0 Ω. At lower frequencies, higher values of X_{C1} cause a phase shift to be introduced, and the output voltage of the *RC* circuit leads the input voltage. As you learned in ac circuit theory, the phase angle in an input *RC* circuit is expressed as

$$\boldsymbol{\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)}$$

Equation 10–7

For midrange frequencies, $X_{C1} \cong 0\ \Omega$, so

$$\theta = \tan^{-1}\left(\frac{0\ \Omega}{R_{in}}\right) = \tan^{-1}(0) = 0°$$

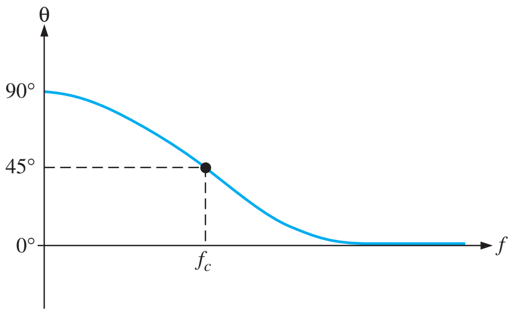
At the critical frequency, $X_{C1} = R_{in}$, so

$$\theta = \tan^{-1}\left(\frac{R_{in}}{R_{in}}\right) = \tan^{-1}(1) = 45°$$

At a decade below the critical frequency, $X_{C1} = 10R_{in}$, so

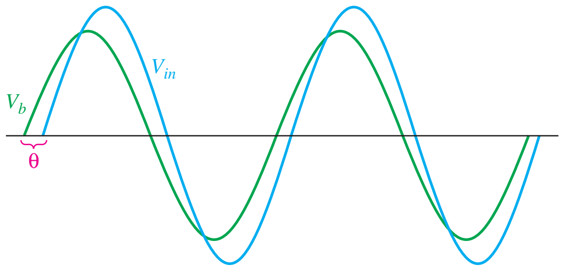
$$\theta = \tan^{-1}\left(\frac{10R_{in}}{R_{in}}\right) = \tan^{-1}(10) = 84.3°$$

A continuation of this analysis will show that the phase shift through the input *RC* circuit approaches 90° as the frequency approaches zero. A plot of phase angle versus frequency is shown in Figure 10–13. The result is that the voltage at the base of the transistor *leads* the input signal voltage in phase below midrange, as shown in Figure 10–14.



▲ FIGURE 10–13

Phase angle versus frequency for the input *RC* circuit.



▲ FIGURE 10–14

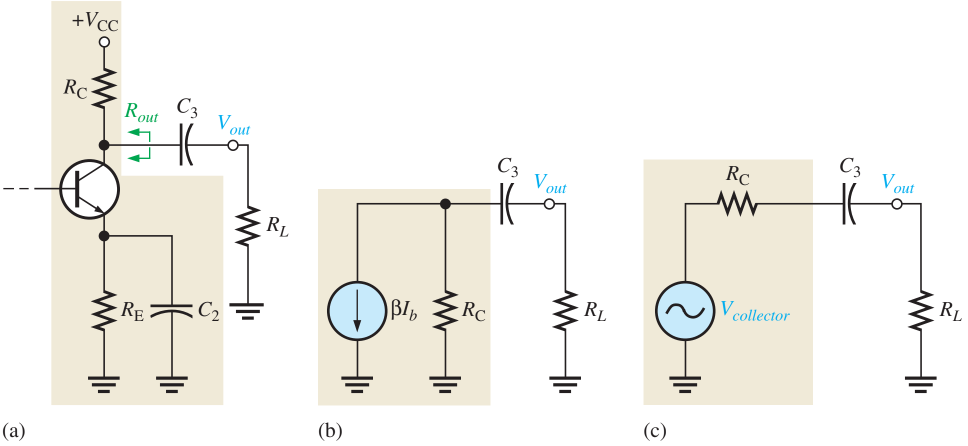
The input *RC* circuit causes the base voltage to lead the input voltage below midrange by an amount equal to the circuit phase angle, θ.

The Output *RC* Circuit

The second high-pass *RC* circuit in the BJT amplifier of Figure 10–8 is formed by the coupling capacitor C_3, the resistance looking in at the collector, and the load resistance R_L, as shown in Figure 10–15(a). In determining the output resistance, looking in at the collector, the transistor is treated as an ideal current source (with infinite internal resistance), and the upper end of R_C is effectively at ac ground, as shown in Figure 10–15(b). Therefore, thevenizing the circuit to the left of capacitor C_3 produces an equivalent voltage source equal to the collector voltage and a series resistance equal to R_C, as shown in Figure 10–15(c). The lower critical frequency of this output *RC* circuit is

Equation 10–8

$$f_{cl(output)} = \frac{1}{2\pi(R_C + R_L)C_3}$$



▲ FIGURE 10–15

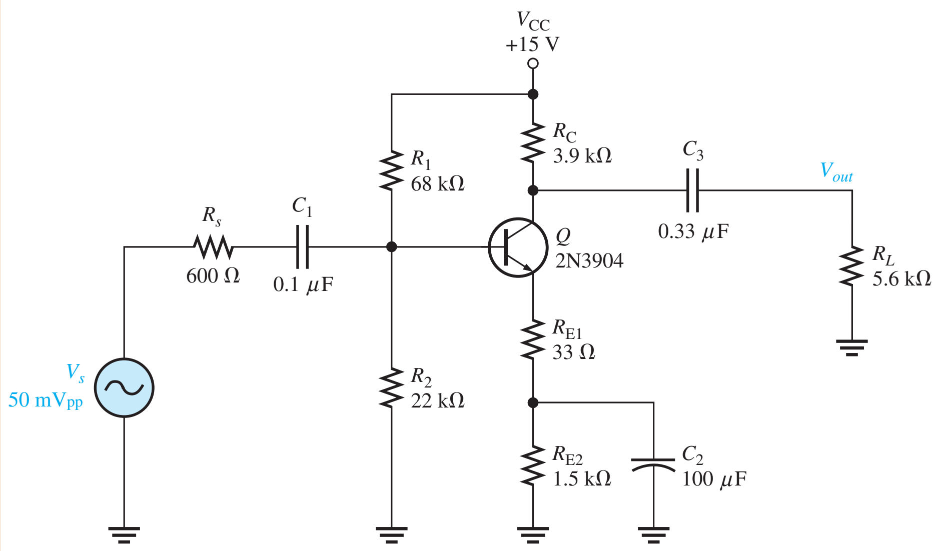
Development of the equivalent low-frequency output *RC* circuit.

The effect of the output *RC* circuit on the amplifier voltage gain is similar to that of the input *RC* circuit. As the signal frequency decreases, X_{C3} increases. This causes less voltage across the load resistance because more voltage is dropped across C_3. The signal voltage is reduced by a factor of 0.707 when frequency is reduced to the lower critical value, f_{cl}, for the circuit. This corresponds to a 3 dB reduction in voltage gain.

EXAMPLE 10–5

For the circuit from Example 10–3 and shown in Figure 10–16, calculate the lower critical frequency due to the output *RC* circuit.

▶ **FIGURE 10–16**



Solution The resistance in the output *RC* circuit is

$$R_C + R_L = 3.9\,\text{k}\Omega + 5.6\,\text{k}\Omega = 9.5\,\text{k}\Omega$$

The lower critical frequency is

$$f_{cl(output)} = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(9.5\,\text{k}\Omega)(0.33\,\mu\text{F})} = \mathbf{50.8\ Hz}$$

Related Problem What effect does a larger load resistor have on the gain and the lower cutoff frequency?

Open the Multisim file E10-05 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. Notice that C_1 and C_2 are taken out of the calculation by making their value huge as explained in Example 10–3.

Phase Shift in the Output RC Circuit The phase angle in the output *RC* circuit is

$$\boldsymbol{\theta = \tan^{-1}\left(\frac{X_{C3}}{R_C + R_L}\right)}$$

Equation 10–9

$\theta \cong 0°$ for the midrange frequencies and approaches 90° as the frequency approaches zero (X_{C3} approaches infinity). At the critical frequency f_c, the phase shift is 45°.

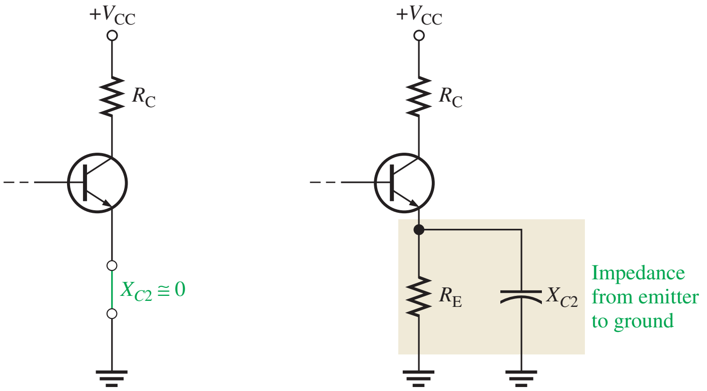
The Bypass *RC* Circuit

The third *RC* circuit that affects the low-frequency gain of the BJT amplifier in Figure 10–8 includes the bypass capacitor C_2. As illustrated in Figure 10–17(a) for midrange frequencies, it is assumed that $X_{C2} \cong 0\,\Omega$, effectively shorting the emitter to ground so that the amplifier gain is R_c/r'_e, as you already know. As the frequency is reduced, X_{C2} increases and no longer provides a sufficiently low reactance to effectively place the emitter at ac ground, as shown in part (b). Because the impedance from emitter to ground increases, the gain decreases. In this case, R_e in the formula, $A_v = R_c/(r'_e + R_e)$, is replaced by an impedance formed by R_E in parallel with X_{C2}.

The bypass *RC* circuit is formed by C_2 and the resistance looking in at the emitter, $R_{in(emitter)}$, as shown in Figure 10–18(a). The resistance looking in at the emitter is derived

▶ FIGURE 10–17

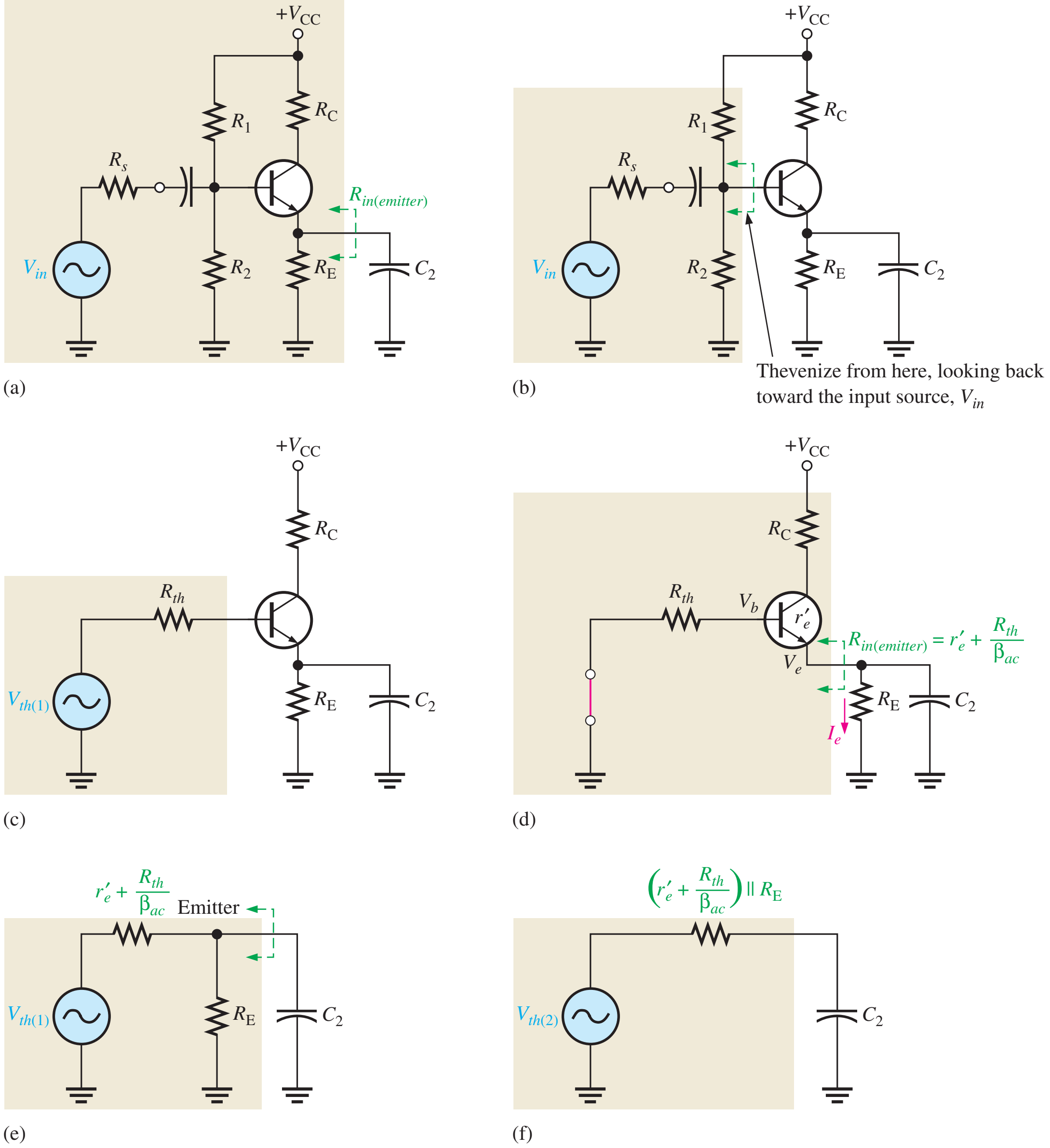
At low frequencies, X_{C2} in parallel with R_E creates an impedance that reduces the voltage gain.



$+V_{CC}$
R_C
$X_{C2} \cong 0$
$+V_{CC}$
R_C
R_E
X_{C2}
Impedance from emitter to ground

(a) For midrange frequencies, C_2 effectively shorts the emitter to ground.

(b) Below f_c, X_{C2} and R_E form an impedance between the emitter and ground.



$+V_{CC}$
R_1
R_C
R_s
$R_{in(emitter)}$
V_{in}
R_2
R_E
C_2
(a)
$+V_{CC}$
R_C
R_1
R_s
V_{in}
R_2
R_E
C_2
(b)
$+V_{CC}$
R_C
R_{th}
$V_{th(1)}$
R_E
C_2
(c)
$+V_{CC}$
R_C
R_{th}
V_b
r'_e
$R_{in(emitter)} = r'_e + \frac{R_{th}}{\beta_{ac}}$
V_e
R_E
C_2
I_e
(d)
$r'_e + \frac{R_{th}}{\beta_{ac}}$
Emitter
$V_{th(1)}$
R_E
C_2
(e)
$\left(r'_e + \frac{R_{th}}{\beta_{ac}}\right) \parallel R_E$
$V_{th(2)}$
C_2
(f)

Thevenize from here, looking back toward the input source, V_{in}

▲ FIGURE 10–18

Development of the equivalent bypass *RC* circuit.

as follows. First, Thevenin's theorem is applied looking from the base of the transistor toward the input source V_{in}, as shown in Figure 10–18(b). This results in an equivalent resistance (R_{th}) and an equivalent voltage source ($V_{th(1)}$) in series with the base, as shown in Figure 10–18(c). The resistance looking in at the emitter is determined with the equivalent input source shorted, as shown in Figure 10–18(d), and is expressed as follows:

$$R_{in(emitter)} = r'_e + \frac{V_e}{I_e} \cong r'_e + \frac{V_b}{\beta_{ac} I_b} = r'_e + \frac{I_b R_{th}}{\beta_{ac} I_b}$$

$$\boldsymbol{R_{in(emitter)} = r'_e + \frac{R_{th}}{\beta_{ac}}}$$

Equation 10–10

Looking from the capacitor C_2, $r'_e + R_{th}/\beta_{ac}$ is in parallel with R_E, as shown in Figure 10–18(e). Thevenizing again, we get the equivalent *RC* circuit shown in Figure 10–18(f). The lower critical frequency for this equivalent bypass *RC* circuit is

$$\boldsymbol{f_{cl(bypass)} = \frac{1}{2\pi[(r'_e + R_{th}/\beta_{ac}) \parallel R_E]C_2}}$$

Equation 10–11

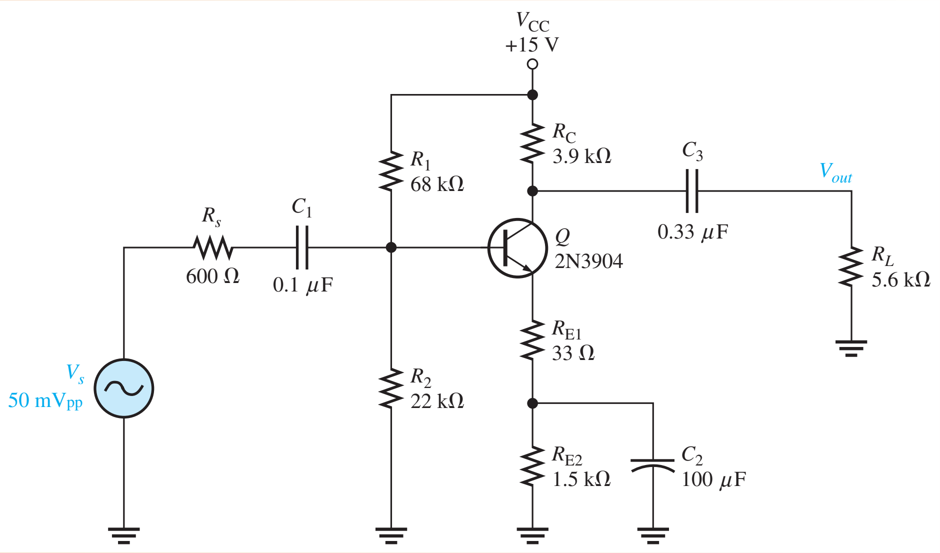
If a swamping resistor is used, the equation for $R_{in(emitter)}$ becomes

$$R_{in(emitter)} = r'_e + R_{E1} + \frac{R_{th}}{\beta_{ac}}$$

EXAMPLE 10–6

For the circuit from Example 10–3 and shown in Figure 10–19, calculate the lower critical frequency due to the bypass *RC* circuit. Assume $r'_e = 9.6\ \Omega$ and $\beta = 200$.

► FIGURE 10–19



Solution The resistance in the emitter bypass circuit is

$$R_{in(emitter)} = r'_e + R_{E1} + \frac{R_{th}}{\beta_{ac}} = 9.6\ \Omega + 33\ \Omega + \frac{68\text{ k}\Omega \parallel 22\text{ k}\Omega \parallel 600\ \Omega}{200} = 45.5\ \Omega$$

The lower critical frequency is

$$f_{cl(bypass)} = \frac{1}{2\pi(R_{in(emitter)} \parallel R_{E2})C_2} = \frac{1}{2\pi(45.5\ \Omega \parallel 1.5\text{ k}\Omega)(100\ \mu\text{F})} = \mathbf{36.0\ Hz}$$

Related Problem Explain why C_2 is larger than C_1 or C_3.

Open the Multisim file E10-06 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. Notice that C_1 and C_3 are taken out of the calculation by making their value huge as before (1 F!).

FET Amplifiers

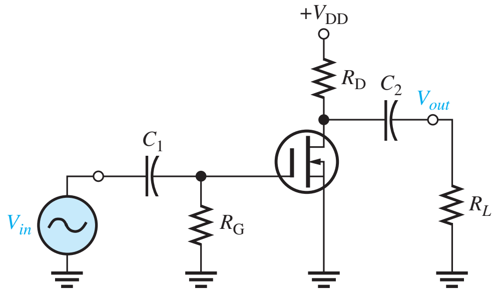
A zero-biased D-MOSFET amplifier with capacitive coupling on the input and output is shown in Figure 10–20. As you learned in Chapter 9, the midrange voltage gain of a zero-biased amplifier is

$$A_{v(mid)} = g_m R_d$$

This is the gain at frequencies high enough so that the capacitive reactances are approximately zero.

FIGURE 10–20

Zero-biased D-MOSFET amplifier.



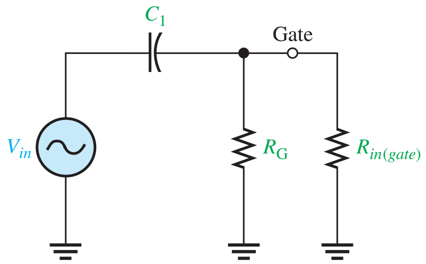
The amplifier in Figure 10–20 has only two high-pass *RC* circuits that influence its low-frequency response. One *RC* circuit is formed by the input coupling capacitor C_1 and the input resistance. The other circuit is formed by the output coupling capacitor C_2 and the output resistance looking in at the drain.

The Input *RC* Circuit

The input *RC* circuit for the FET amplifier in Figure 10–20 is shown in Figure 10–21. As in the case for the BJT amplifier, the reactance of the input coupling capacitor increases as the frequency decreases. When $X_{C1} = R_{in}$, the gain is down 3 dB below its midrange value.

FIGURE 10–21

Input *RC* circuit.



The lower critical frequency is

$$f_{cl(input)} = \frac{1}{2\pi R_{in} C_1}$$

The input resistance is

$$R_{in} = R_G \| R_{in(gate)}$$

where $R_{in(gate)}$ is determined from datasheet information as

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

Therefore, the lower critical frequency is

$$\boldsymbol{f_{cl(input)} = \frac{1}{2\pi(R_G \parallel R_{in(gate)})C_1}}$$

Equation 10–12

For practical work, the value of $R_{in(gate)}$ is so large it can be ignored, as will be illustrated in Example 10–7.

The gain rolls off below f_c at 20 dB/decade, as previously shown. The phase angle in the low-frequency input *RC* circuit is

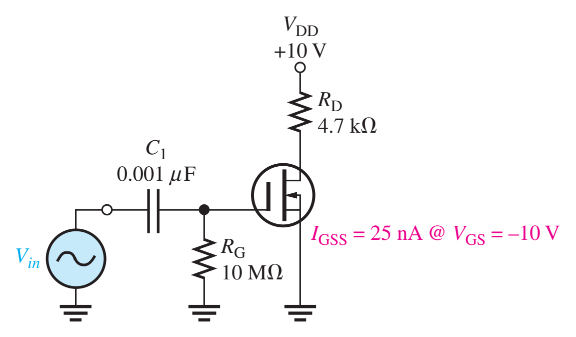
$$\boldsymbol{\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)}$$

Equation 10–13

EXAMPLE 10–7

What is the lower critical frequency of the input *RC* circuit in the FET amplifier of Figure 10–22?

▶ FIGURE 10–22



Solution First determine R_{in} and then calculate f_c.

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{10\text{ V}}{25\text{ nA}} = 400\text{ M}\Omega$$

$$R_{in} = R_G \parallel R_{in(gate)} = 10\text{ M}\Omega \parallel 400\text{ M}\Omega = 9.8\text{ M}\Omega$$

$$f_{cl(input)} = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(9.8\text{ M}\Omega)(0.001\ \mu\text{F})} = \mathbf{16.2\ Hz}$$

For all practical purposes,

$$R_{in} \cong R_G = 10\text{ M}\Omega$$

and

$$f_{cl(input)} = \frac{1}{2\pi R_G C_1} = \frac{1}{2\pi(10\text{ M}\Omega)(0.001\ \mu\text{F})} \cong 15.9\text{ Hz}$$

There is very little difference in the two results.

The critical frequency of the input *RC* circuit of a FET amplifier is usually very low because of the very high input resistance and the high value of R_G.

Related Problem How much does the lower critical frequency of the input *RC* circuit change if the FET in Figure 10–22 is replaced by one with $I_{GSS} = 10\text{ nA} @ V_{GS} = -8\text{ V}$?

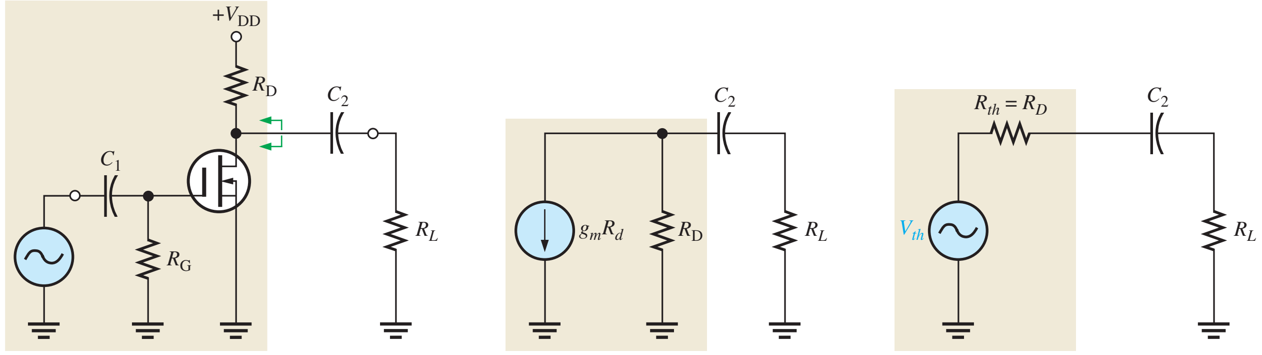
Open the Multisim file E10-07 in the Examples folder on the companion website and measure the low critical frequency for the input circuit. Compare to the calculated results.

The Output *RC* Circuit

The second *RC* circuit that affects the low-frequency response of the FET amplifier in Figure 10–20 is formed by a coupling capacitor C_2 and the output resistance looking in at the drain, as shown in Figure 10–23(a). The load resistor, R_L, is also included. As in the case of the BJT, the FET is treated as a current source, and the upper end of R_D is effectively ac ground, as shown in Figure 10–23(b). The Thevenin equivalent of the circuit to the left of C_2 is shown in Figure 10–23(c). The lower critical frequency for this *RC* circuit is

Equation 10–14

$$f_{cl(output)} = \frac{1}{2\pi(R_D + R_L)C_2}$$



(a) (b) (c)

▲ **FIGURE 10–23**

Development of the equivalent low-frequency output *RC* circuit.

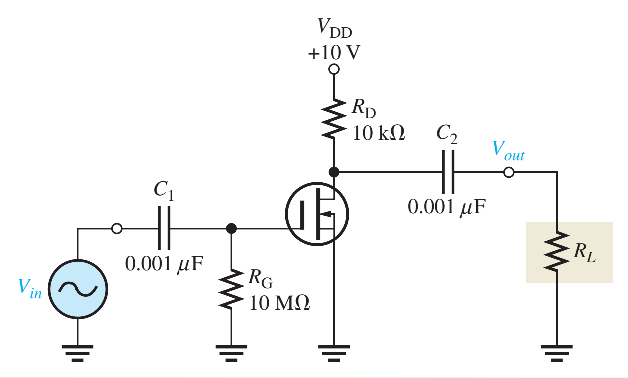
The effect of the output *RC* circuit on the amplifier's voltage gain below the midrange is similar to that of the input *RC* circuit. The circuit with the highest critical frequency dominates because it is the one that first causes the gain to roll off as the frequency drops below its midrange values. The phase angle in the low-frequency output *RC* circuit is

Equation 10–15

$$\theta = \tan^{-1}\left(\frac{X_{C2}}{R_D + R_L}\right)$$

Again, at the critical frequency, the phase angle is 45° and approaches 90° as the frequency approaches zero. However, starting at the critical frequency, the phase angle decreases from 45° and becomes very small as the frequency goes higher.

EXAMPLE 10–8 Determine the lower critical frequencies for the FET amplifier in Figure 10–24. Assume that the load is another identical amplifier with the same R_{in}. The datasheet shows $I_{GSS} = 100\text{ nA}$ at $V_{GS} = -12\text{ V}$.



▲ **FIGURE 10–24**

Solution First, find the lower critical frequency for the input *RC* circuit.

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{12\text{ V}}{100\text{ nA}} = 120\text{ M}\Omega$$

$$R_{in} = R_G \parallel R_{in(gate)} = 10\text{ M}\Omega \parallel 120\text{ M}\Omega = 9.2\text{ M}\Omega$$

$$f_{cl(input)} = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(9.2\text{ M}\Omega)(0.001\ \mu\text{F})} = \mathbf{17.3\ Hz}$$

The output *RC* circuit has a lower critical frequency of

$$f_{cl(output)} = \frac{1}{2\pi(R_D + R_L)C_2} = \frac{1}{2\pi(9.21\text{ M}\Omega)(0.001\ \mu\text{F})} \cong \mathbf{17.3\ Hz}$$

Related Problem If the circuit in Figure 10–24 were operated with no load, how is the low-frequency response affected?

Open the Multisim file E10-08 in the Examples folder on the companion website. Determine the total low-frequency response of the amplifier.

Total Low-Frequency Response of an Amplifier

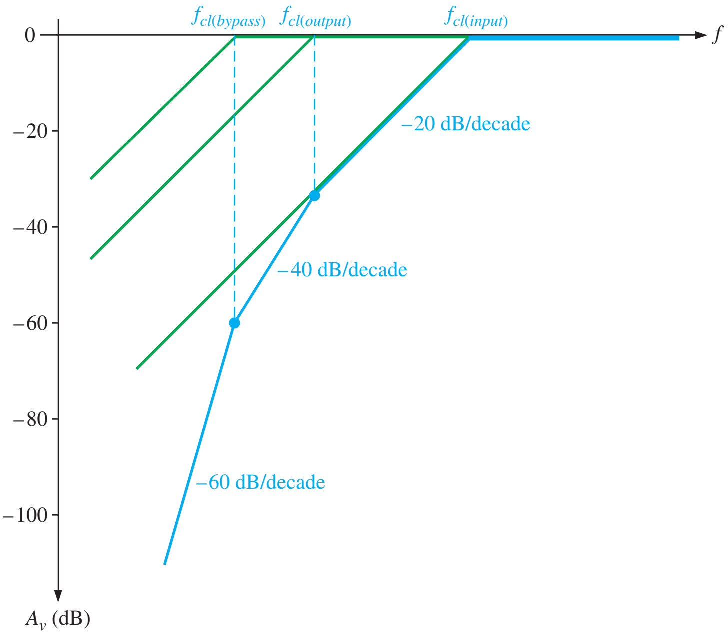
Now that we have individually examined the high-pass *RC* circuits that affect a BJT or FET amplifier's voltage gain at low frequencies, let's look at the combined effect of the three *RC* circuits in a BJT amplifier. Each circuit has a critical frequency determined by the *R* and *C* values. The critical frequencies of the three *RC* circuits are not necessarily all equal. If one of the *RC* circuits has a critical (break) frequency higher than the other two, then it is the *dominant RC* circuit. The dominant circuit determines the frequency at which the overall voltage gain of the amplifier begins to drop at −20 dB/decade. The other circuits each cause an additional −20 dB/decade roll-off below their respective critical (break) frequencies.

To get a better picture of what happens at low frequencies, refer to the Bode plot in Figure 10–25, which shows the superimposed ideal responses for the three *RC* circuits (green lines) of a BJT amplifier. In this example, each *RC* circuit has a different critical frequency. The input *RC* circuit is dominant (highest f_c) in this case, and the bypass *RC* circuit has the lowest f_c. The ideal overall response is shown as the blue line.

Here is what happens. As the frequency is reduced from midrange, the first "break point" occurs at the critical frequency of the input *RC* circuit, $f_{cl(input)}$, and the gain begins to drop at −20 dB/decade. This constant roll-off rate continues until the critical frequency of the output *RC* circuit, $f_{cl(output)}$, is reached. At this break point, the output *RC* circuit adds another −20 dB/decade to make a total roll-off of −40 dB/decade. This constant

FIGURE 10–25

Composite Bode plot of a BJT amplifier response for three low-frequency *RC* circuits with different critical frequencies. Total response is shown by the blue curve.

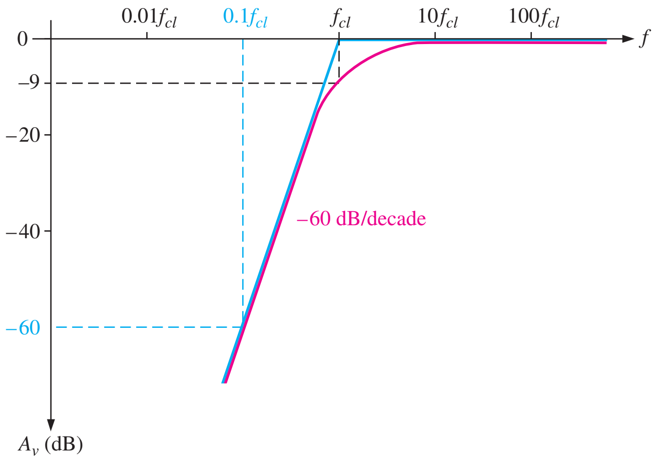


−40 dB/decade roll-off continues until the critical frequency of the bypass *RC* circuit, $f_{cl(bypass)}$, is reached. The bypass *RC* circuit adds still another −20 dB/decade at this break point, making the gain roll-off at −60 dB/decade.

If all *RC* circuits have the same critical frequency, the response curve has one break point at that value of f_{cl}, and the voltage gain rolls off at −60 dB/decade below that value, as shown by the ideal curve (blue) in Figure 10–26. Actually, the midrange voltage gain does not extend down to the dominant critical frequency but is really at −9 dB below the midrange voltage gain at that point (−3 dB for each *RC* circuit), as shown by the red curve.

FIGURE 10–26

Composite Bode plot of an amplifier response where all *RC* circuits have the same f_{cl}. (Blue is ideal; red is actual.)

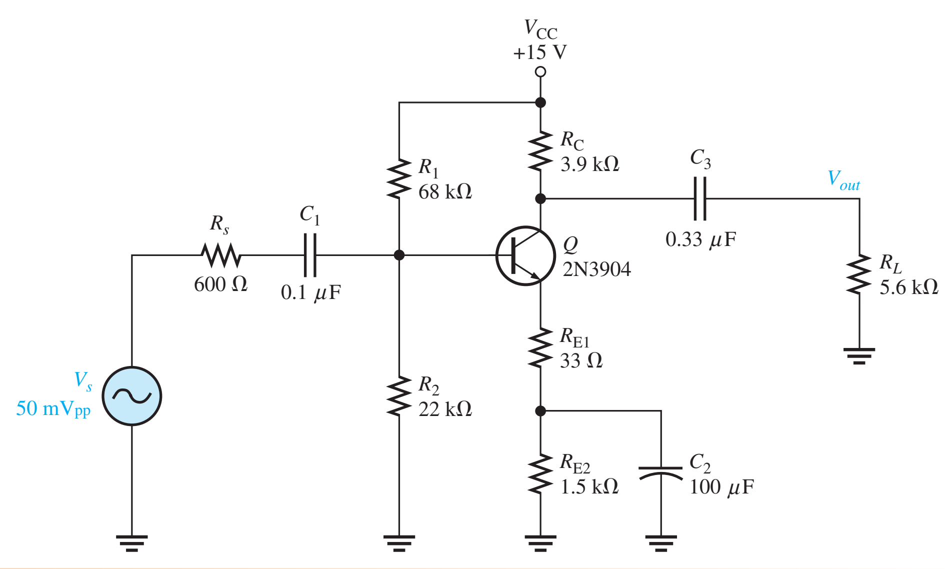


EXAMPLE 10–9

For the circuit from Example 10–3 and shown in Figure 10–27, determine the midband gain in decibels and draw the Bode plot, showing each of the lower critical frequencies. Assume $r'_e = 9.6\ \Omega$.

Solution The midband gain is

$$A_v = \frac{R_C R_L}{r'_e + R_{E1}} = \frac{(3.9\ \text{k}\Omega)(5.6\ \text{k}\Omega)}{9.6\ \Omega + 33\ \Omega} = 54.0$$


V_{CC}
+15 V
R_C
3.9 kΩ
C_3
0.33 μF
V_{out}
R_1
68 kΩ
R_s
600 Ω
C_1
0.1 μF
Q
2N3904
R_L
5.6 kΩ
R_{E1}
33 Ω
V_s
50 mVpp
R_2
22 kΩ
R_{E2}
1.5 kΩ
C_2
100 μF

▲ FIGURE 10–27

In decibels,

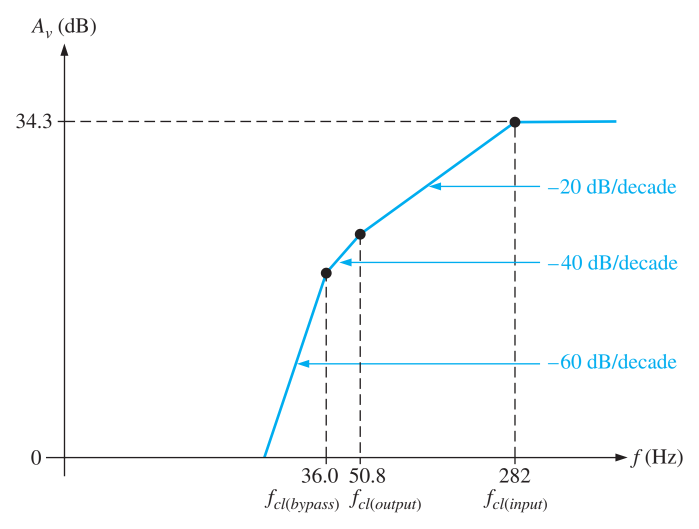
$$A_v = 20 \log (54.0) = \mathbf{34.3\ dB}$$

The critical frequency for the input circuit was found in Example 10–3 and is 282 Hz. The critical frequency for the output circuit was found in Example 10–5 and is 50.8 Hz. The critical frequency for the emitter bypass circuit was found in Example 10–6 and is 36.0 Hz.

The overall response is shown in the Bode plot of Figure 10–28. The lower critical frequency of the input circuit has the highest value and is therefore the overall or dominant critical frequency because the response first begins to roll off at this frequency.

▶ FIGURE 10–28

Ideal Bode plot for the overall low-frequency response of the amplifier in Figure 10–27.



Related Problem If the overall gain of the amplifier is reduced by increasing R_{E1}, how will the lower critical frequency be affected?

Computer Simulation of Frequency Response

As you saw in the previous example, the calculation of multiple critical frequencies is involved and each critical frequency contributes to the overall response. The ideal response shown in Example 10–9 is an excellent first approximation, but when more accuracy is required, a computer simulation is used. The computer takes into account all of the parameters for the particular device including effects such as internal capacitances that are usually ignored in manual calculations, and it can calculate in detail the interactions that occur when there are multiple breakpoints as in Example 10–9.

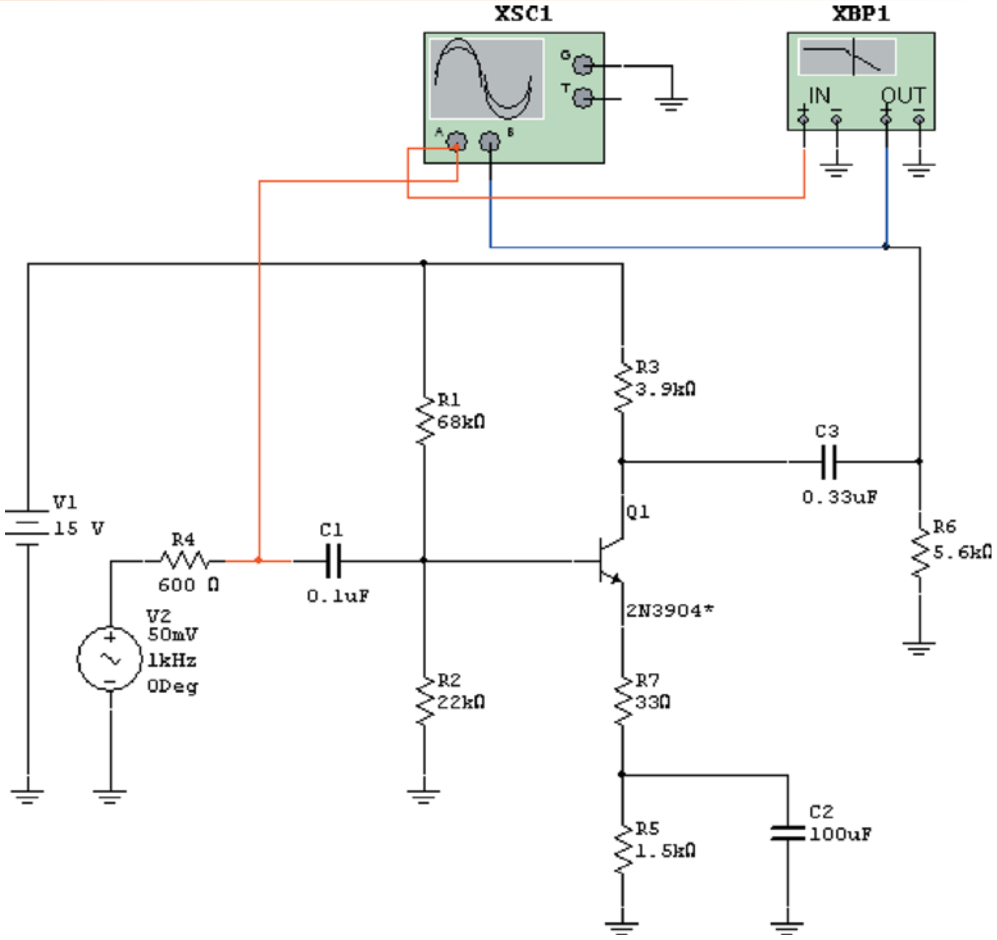
Multisim is based on SPICE models that can show the frequency response of circuits on the Bode plotter. As mentioned earlier, the Bode plotter is not a real instrument. It performs the same function as an instrument called the spectrum analyzer, which can also plot the frequency response of a circuit. Example 10–10 illustrates the application of computer analysis to the circuit in the previous example.

F Y I

SPICE was one of the first computer programs that could simulate electronic circuits. Its origins can be traced to a program called CANCER (Computer Analysis of Nonlinear Circuits, Excluding Radiation) at the University of California. It was developed as a computer aid for designing integrated circuits in the 1960s. SPICE is an acronym for Simulation Program with Integrated Circuit Emphasis. Over the years, SPICE has been revised many times but is still the underlying software for many of today's simulations.

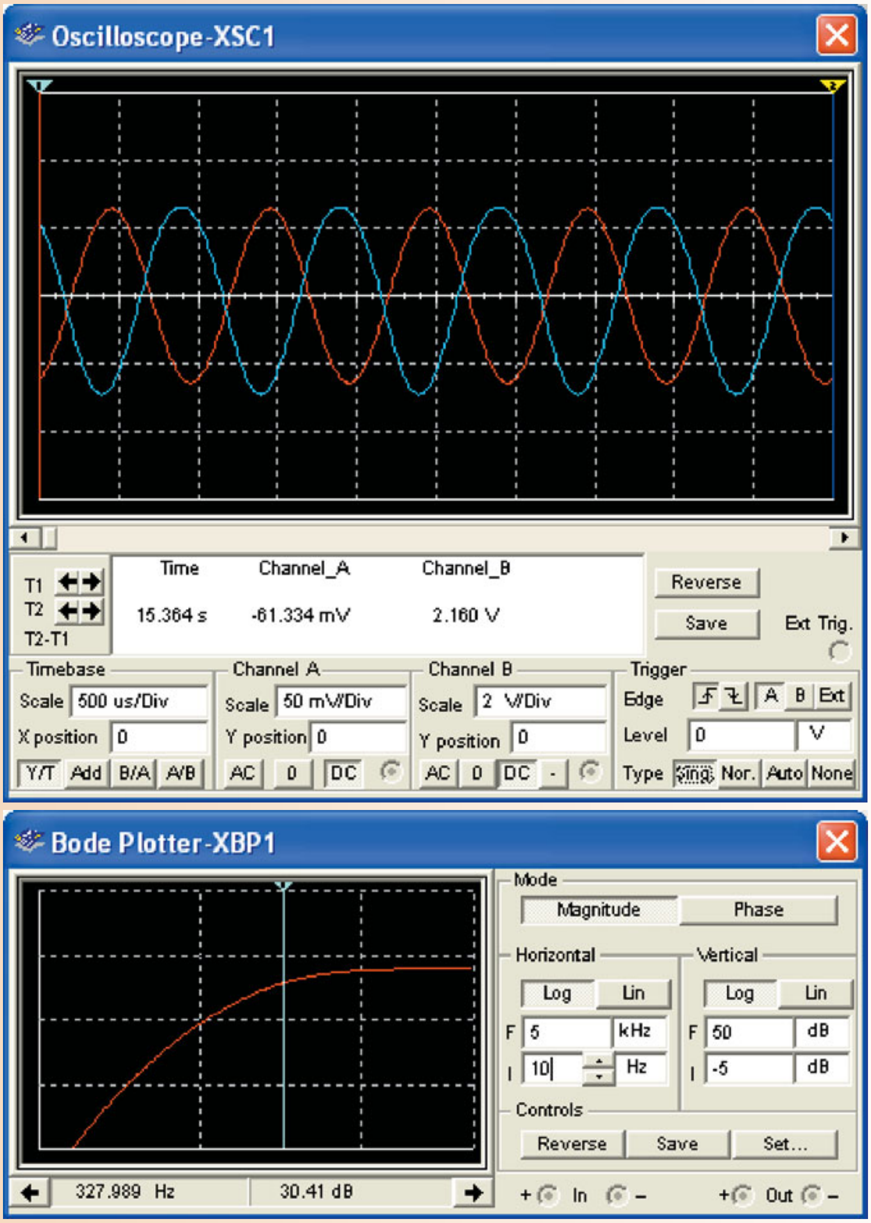
EXAMPLE 10–10 Use Multisim to show the overall low-frequency response of the circuit in Example 10–9.

Solution Figure 10–29 shows the circuit in Multisim with an oscilloscope display and Bode plotter. The cursor is set to the critical frequency on the Bode plotter so that the



▲ FIGURE 10–29

frequency can be read directly. The result in Figure 10–30 indicates the overall critical frequency is 328 Hz.


Oscilloscope-XSC1
T1
T2
T2-T1
Reverse
Save
Ext Trig.
Timebase
Channel A
Channel B
Trigger
Edge
A
B
Ext
Y/T
Add
B/A
A/B
AC
0
DC
-
Type
Sing.
Nor.
Auto
None
Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Vertical
Log
Lin
Controls
Reverse
Save
Set...
+ In –
+ Out –

Time	Channel_A	Channel_B
15.364 s	-61.334 mV	2.160 V

Timebase: Scale 500 us/Div; X position 0

Channel A: Scale 50 mV/Div; Y position 0

Channel B: Scale 2 V/Div; Y position 0

Trigger: Level 0 V

Horizontal: F 5 kHz; I 10 Hz

Vertical: F 50 dB; I -5 dB

327.989 Hz 30.41 dB

▲ FIGURE 10–30

Related Problem What change would you make to reduce the lower critical frequency to 100 Hz?

SECTION 10–3 CHECKUP

1. A certain BJT amplifier exhibits three critical frequencies in its low-frequency response: $f_{cl1} = 130$ Hz, $f_{cl2} = 167$ Hz, and $f_{cl3} = 75$ Hz. Which is the dominant critical frequency?
2. If the midrange voltage gain of the amplifier in Question 1 is 50 dB, what is the gain at the dominant f_{cl}?

3. A certain RC circuit has an $f_{cl} = 235$ Hz, above which the attenuation is 0 dB. What is the dB attenuation at 23.5 Hz?
4. What is the amount of phase shift contributed by an input circuit when $X_C = 0.5R_{in}$ at a certain frequency below f_{cl1}?
5. What is the critical frequency when $R_D = 1.5\ \text{k}\Omega$, $R_L = 5\ \text{k}\Omega$, and $C_2 = 0.0022\ \mu\text{F}$ in a circuit like Figure 10–24?

10–4 HIGH-FREQUENCY AMPLIFIER RESPONSE

You have seen how the coupling and bypass capacitors affect the voltage gain of an amplifier at lower frequencies where the reactances of the coupling and bypass capacitors are significant. In the midrange of an amplifier, the effects of the capacitors are minimal and can be neglected. If the frequency is increased sufficiently, a point is reached where the transistor's internal capacitances begin to have a significant effect on the gain. The basic differences between BJTs and FETs are the specifications of the internal capacitances and the input resistance.

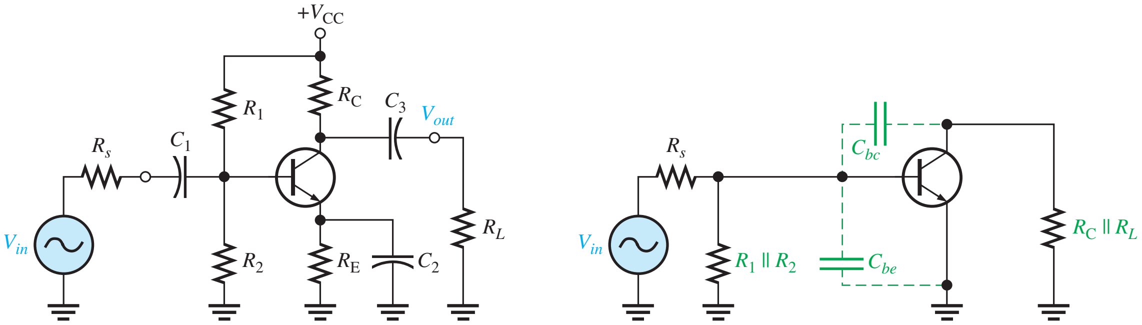
After completing this section, you should be able to

- ☐ **Analyze the high-frequency response of an amplifier**
- ☐ Analyze a BJT amplifier
  - ◆ Apply Miller's theorem
- ☐ Identify and analyze the BJT amplifier's input RC circuit
  - ◆ Calculate the upper critical frequency and gain roll-off ◆ Determine the phase shift
- ☐ Identify and analyze the BJT amplifier's output RC circuit
  - ◆ Calculate the upper critical frequency ◆ Determine the phase shift
- ☐ Analyze a FET amplifier
- ☐ Identify and analyze a JFET amplifier
  - ◆ Determine internal capacitances on a datasheet ◆ Apply Miller's theorem
- ☐ Identify and analyze the JFET amplifier's input RC circuit
  - ◆ Calculate the upper critical frequency ◆ Determine the phase shift
- ☐ Identify and analyze the JFET amplifier's output RC circuit
  - ◆ Calculate the upper critical frequency ◆ Determine the phase shift
- ☐ Discuss the total high-frequency response of an amplifier
  - ◆ Use Bode plots to illustrate the high-frequency response

BJT Amplifiers

A high-frequency ac equivalent circuit for the BJT amplifier in Figure 10–31(a) is shown in Figure 10–31(b). Notice that the coupling and bypass capacitors are treated as effective shorts and do not appear in the equivalent circuit. The internal capacitances, C_{be} and C_{bc}, which are significant only at high frequencies, do appear in the diagram. As previously mentioned. C_{be} is sometimes called the input capacitance C_{ib}, and C_{bc} is sometimes called the output capacitance C_{ob}. C_{be} is specified on datasheets at a certain value of V_{BE}. Often, a datasheet will list C_{ib} as C_{ibo} and C_{ob} as C_{obo}. The o as the last letter in the subscript indicates the capacitance is measured with the base open. For example, a 2N2222A transistor has a C_{be} of 25 pF at $V_{\text{BE}} = 0.5$ V dc, $I_C = 0$, and $f = 1$ MHz. Also, C_{bc} is specified at a certain value of V_{BC}. The 2N2222A has a maximum C_{bc} of 8 pF at $V_{\text{BC}} = 10$ V dc.

Miller's Theorem in High-Frequency Analysis By applying Miller's theorem to the inverting amplifier in Figure 10–31(b) and using the midrange voltage gain, you have a circuit



(a) Capacitively coupled amplifier (b) High-frequency equivalent circuit

▲ FIGURE 10–31

Capacitively coupled amplifier and its high-frequency equivalent circuit.

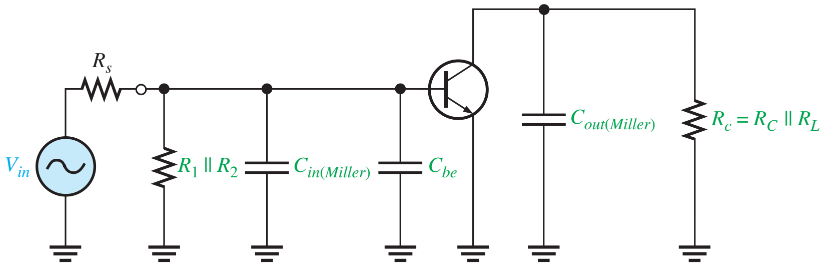
that can be analyzed for high-frequency response. Looking in from the signal source, the capacitance C_{bc} appears in the Miller input capacitance from base to ground.

$$C_{in(Miller)} = C_{bc}(A_v + 1)$$

C_{be} simply appears as a capacitance to ac ground, as shown in Figure 10–32, in parallel with $C_{in(Miller)}$. Looking in at the collector, C_{bc} appears in the Miller output capacitance from collector to ground. As shown in Figure 10–32, the Miller output capacitance appears in parallel with R_c.

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

These two Miller capacitances create a high-frequency input *RC* circuit and a high-frequency output *RC* circuit. These two circuits differ from the low-frequency input and output circuits, which act as high-pass filters, because the capacitances go to ground and therefore act as low-pass filters. The equivalent circuit in Figure 10–32 is an ideal model because stray capacitances that are due to circuit interconnections are neglected.



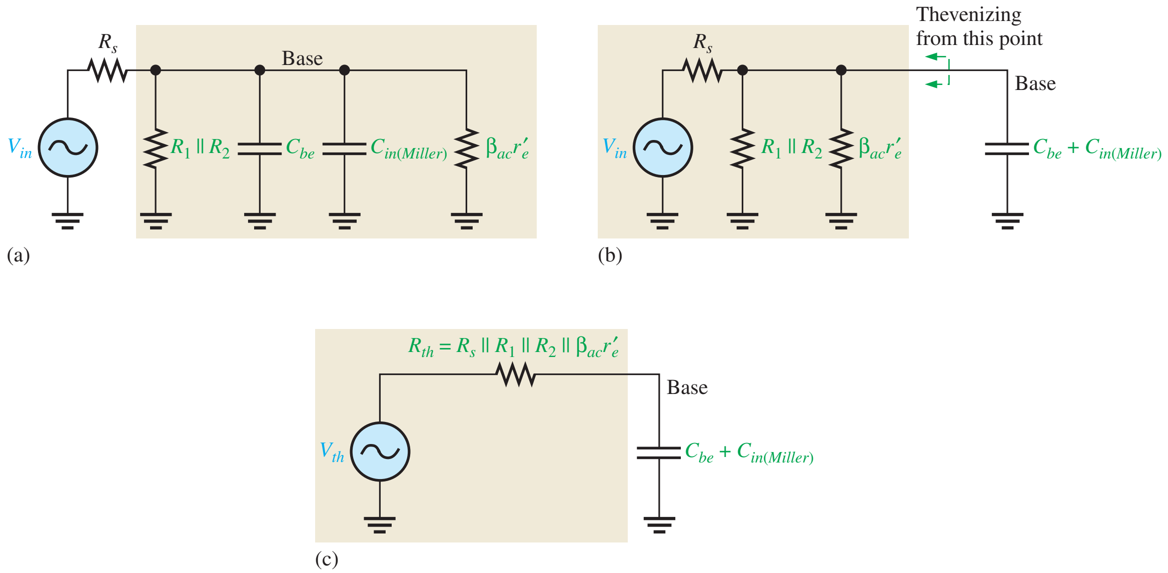
◀ FIGURE 10–32

High-frequency equivalent circuit after applying Miller's theorem.

The Input *RC* Circuit

At high frequencies, the input circuit is as shown in Figure 10–33(a), where $\beta_{ac}r'_e$ is the input resistance at the base of the transistor because the bypass capacitor effectively shorts the emitter to ground. By combining C_{be} and $C_{in(Miller)}$ in parallel and repositioning, you get the simplified circuit shown in Figure 10–33(b). Next, by thevenizing the circuit to the left of the capacitor, as indicated, the input *RC* circuit is reduced to the equivalent form shown in Figure 10–33(c).

As the frequency increases, the capacitive reactance becomes smaller. This causes the signal voltage at the base to decrease, so the amplifier's voltage gain decreases. The reason for this is that the capacitance and resistance act as a voltage divider and, as the frequency increases, more voltage is dropped across the resistance and less across the capacitance. At the critical frequency, the gain is 3 dB less than its midrange value. The upper critical high


R_s
Base
V_{in}
$R_1 \parallel R_2$
C_{be}
$C_{in(Miller)}$
$\beta_{ac}r'_e$
(a)
Thevenizing
from this point
R_s
Base
V_{in}
$R_1 \parallel R_2$
$\beta_{ac}r'_e$
$C_{be} + C_{in(Miller)}$
(b)
$R_{th} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac}r'_e$
Base
V_{th}
$C_{be} + C_{in(Miller)}$
(c)

▲ **FIGURE 10–33**

Development of the equivalent high-frequency input *RC* circuit.

frequency of the input circuit, $f_{cu(input)}$, is the frequency at which the capacitive reactance is equal to the total resistance.

$$X_{C_{tot}} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac}r'_e$$

Therefore,

$$\frac{1}{2\pi f_{cu(input)}C_{tot}} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac}r'_e$$

and

Equation 10–16

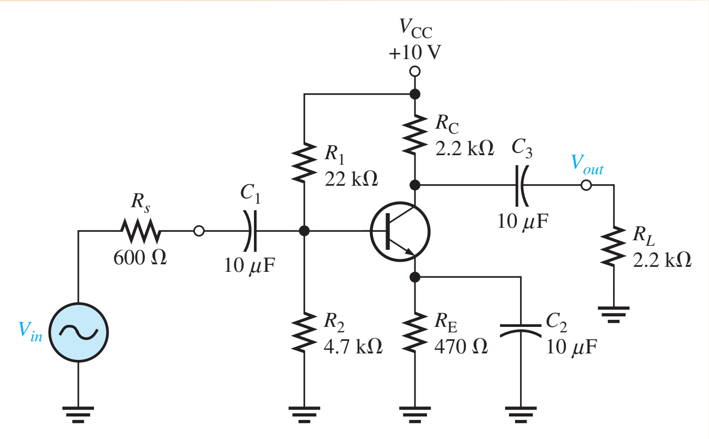
$$\boldsymbol{f_{cu(input)} = \frac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac}r'_e)C_{tot}}}$$

where R_s is the resistance of the signal source and $C_{tot} = C_{be} + C_{in(Miller)}$. As the frequency goes above $f_{cu(input)}$, the input *RC* circuit causes the gain to roll off at a rate of -20 dB/decade just as with the low-frequency response.

EXAMPLE 10–11

Derive the equivalent high-frequency input *RC* circuit for the BJT amplifier in Figure 10–34. Use this to determine the upper critical frequency due to the input

▶ **FIGURE 10–34**


V_{CC}
+10 V
R_C
2.2 kΩ
C_3
V_{out}
R_1
22 kΩ
10 μF
R_s
C_1
600 Ω
10 μF
R_L
2.2 kΩ
V_{in}
R_2
4.7 kΩ
R_E
470 Ω
C_2
10 μF

circuit. The transistor's datasheet provides the following: $\beta_{ac} = 125$, $C_{be} = 20$ pF, and $C_{bc} = 2.4$ pF.

Solution First, find r'_e as follows:

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{4.7\text{ k}\Omega}{26.7\text{ k}\Omega}\right)10\text{ V} = 1.76\text{ V}$$

$$V_E = V_B - 0.7\text{ V} = 1.06\text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.06\text{ V}}{470\ \Omega} = 2.26\text{ mA}$$

$$r'_e = \frac{25\text{ mV}}{I_E} = 11.1\ \Omega$$

The total resistance of the input circuit is

$$R_{in(tot)} = R_s \| R_1 \| R_2 \| \beta_{ac}r'_e = 600\ \Omega \| 22\text{ k}\Omega \| 4.7\text{ k}\Omega \| 125(11.1\ \Omega) = 378\ \Omega$$

Next, in order to determine the capacitance, you must calculate the midrange gain of the amplifier so that you can apply Miller's theorem.

$$A_{v(mid)} = \frac{R_c}{r'_e} = \frac{R_C \| R_L}{r'_e} = \frac{1.1\text{ k}\Omega}{11.1\ \Omega} = 99$$

Apply Miller's theorem.

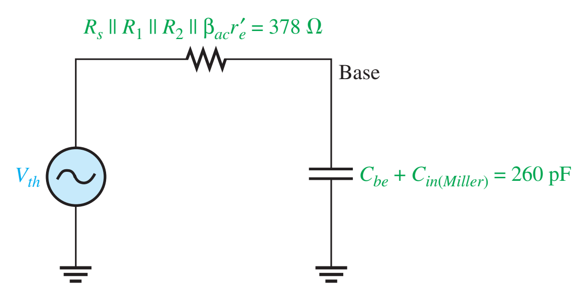
$$C_{in(Miller)} = C_{bc}(A_{v(mid)} + 1) = (2.4\text{ pF})(100) = 240\text{ pF}$$

The total input capacitance is $C_{in(Miller)}$ in parallel with C_{be}.

$$C_{in(tot)} = C_{in(Miller)} + C_{be} = 240\text{ pF} + 20\text{ pF} = 260\text{ pF}$$

The resulting high-frequency input RC circuit is shown in Figure 10–35. The upper critical frequency is

$$f_{cu(input)} = \frac{1}{2\pi(R_{in(tot)})(C_{in(tot)})} = \frac{1}{2\pi(378\ \Omega)(260\text{ pF})} = \mathbf{1.62\ MHz}$$


$R_s \| R_1 \| R_2 \| \beta_{ac}r'_e = 378\ \Omega$
Base
V_{th}
$C_{be} + C_{in(Miller)} = 260$ pF

▲ **FIGURE 10–35**

High-frequency equivalent input *RC* circuit for the amplifier in Figure 10–34.

Related Problem Determine the input RC circuit for Figure 10–34 and find its upper critical frequency if a transistor with the following specifications is used: $\beta_{ac} = 75$, $C_{be} = 15$ pF, $C_{bc} = 2$ pF.

Open the Multisim file E10-11 in the Examples folder on the companion website. Measure the critical frequency for the amplifier's high-frequency response and compare to the calculated result.

Phase Shift of the Input RC Circuit Because the output voltage of a high-frequency input *RC* circuit is across the capacitor, the output of the circuit lags the input. The phase angle is expressed as

Equation 10–17

$$\theta = \tan^{-1}\left(\frac{R_s \| R_1 \| R_2 \| \beta_{ac} r'_e}{X_{C_{(tot)}}}\right)$$

At the critical frequency, the phase angle is 45° with the signal voltage at the base of the transistor lagging the input signal. As the frequency increases above f_c, the phase angle increases above 45° and approaches 90° when the frequency is sufficiently high.

The Output *RC* Circuit

The high-frequency output *RC* circuit is formed by the Miller output capacitance and the resistance looking in at the collector, as shown in Figure 10–36(a). In determining the output resistance, the transistor is treated as a current source (open) and one end of R_C is effectively ac ground, as shown in Figure 10–36(b). By rearranging the position of the capacitance in the diagram and thevenizing the circuit to the left, as shown in Figure 10–36(c), you get the equivalent circuit in Figure 10–36(d). The equivalent output *RC* circuit consists of a resistance equal to the parallel combination of R_C and R_L in series with a capacitance that is determined by the following Miller formula:

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

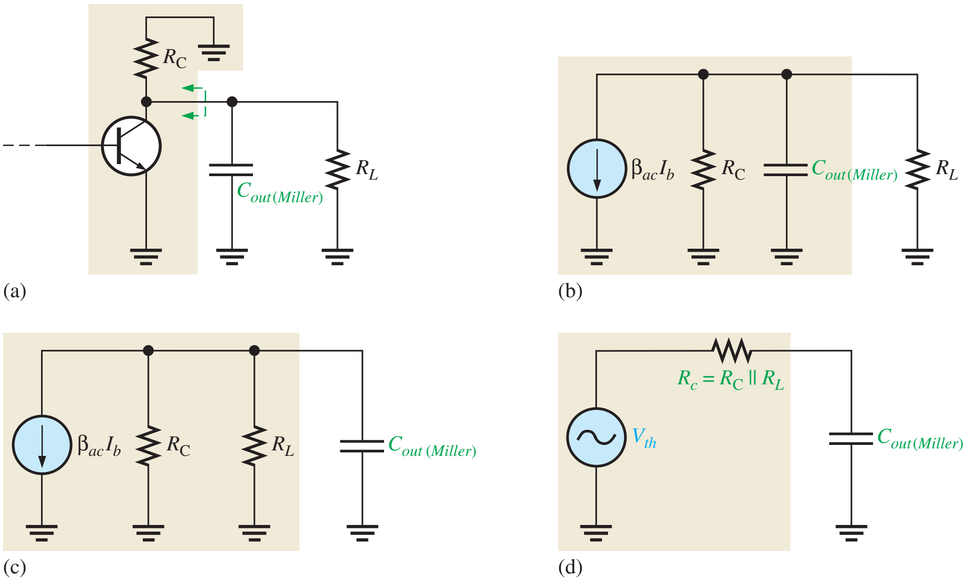
If the voltage gain is at least 10, this formula can be approximated as

$$C_{out(Miller)} \cong C_{bc}$$

The upper critical frequency for the output circuit is determined with the following equation, where $R_c = R_C \| R_L$.

Equation 10–18

$$f_{cu(output)} = \frac{1}{2\pi R_c C_{out(Miller)}}$$



▲ FIGURE 10–36

Development of the equivalent high-frequency output *RC* circuit.

Just as in the input *RC* circuit, the output *RC* circuit reduces the gain by 3 dB at the critical frequency. When the frequency goes above the critical value, the gain drops at a −20 dB/decade rate. The phase angle introduced by the output *RC* circuit is

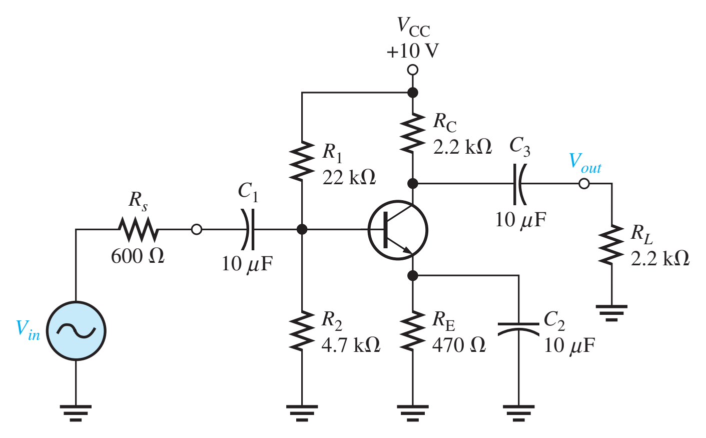
$$\boldsymbol{\theta = \tan^{-1}\left(\frac{R_c}{X_{C_{out(Miller)}}}\right)}$$

Equation 10–19

EXAMPLE 10–12

Determine the upper critical frequency of the amplifier in Example 10–11 shown in Figure 10–37 due to its output *RC* circuit.

▶ FIGURE 10–37



Solution Calculate the Miller output capacitance.

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right) = (2.4\text{ pF})\left(\frac{99 + 1}{99}\right) \cong 2.4\text{ pF}$$

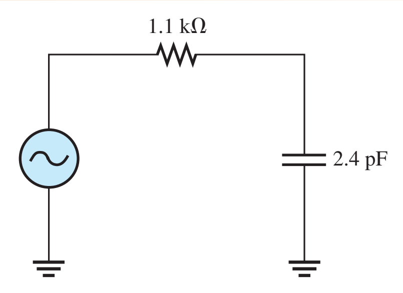
The equivalent resistance is

$$R_c = R_C \| R_L = 2.2\text{ k}\Omega \| 2.2\text{ k}\Omega = 1.1\text{ k}\Omega$$

The equivalent output *RC* circuit is shown in Figure 10–38. Determine the upper critical frequency as follows ($C_{out(Miller)} \cong C_{bc}$):

$$f_{cu(output)} = \frac{1}{2\pi R_c C_{bc}} = \frac{1}{2\pi(1.1\text{ k}\Omega)(2.4\text{ pF})} = \mathbf{60.3\text{ MHz}}$$

▶ FIGURE 10–38

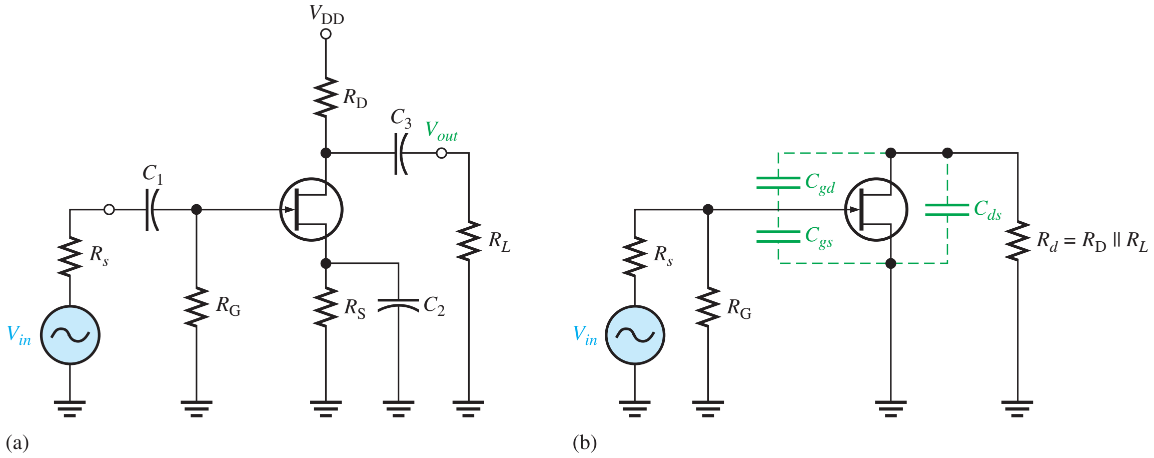


Related Problem If another transistor with $C_{bc} = 5$ pF is used in the amplifier, what is $f_{cu(output)}$?

FET Amplifiers

The approach to the high-frequency analysis of a FET amplifier is similar to that of a BJT amplifier. The basic differences are the specifications of the internal FET capacitances and the determination of the input resistance.

Figure 10–39(a) shows a JFET common-source amplifier that will be used to illustrate high-frequency analysis. A high-frequency equivalent circuit for the amplifier is shown in Figure 10–39(b). Notice that the coupling and bypass capacitors are assumed to have negligible reactances and are considered to be shorts. The internal capacitances C_{gs} and C_{gd} appear in the equivalent circuit because their reactances are significant at high frequencies.



▲ FIGURE 10–39

Example of a JFET amplifier and its high-frequency equivalent circuit.

Values of C_{gs}, C_{gd}, and C_{ds} FET datasheets do not normally provide values for C_{gs}, C_{gd}, or C_{ds}. Instead, three other values are usually specified because they are easier to measure. These are C_{iss}, the input capacitance; C_{rss}, the reverse transfer capacitance; and C_{oss}, the output capacitance. Because of the manufacturer's method of measurement, the following relationships allow you to determine the capacitor values needed for analysis.

Equation 10–20
$$C_{gd} = C_{rss}$$

Equation 10–21
$$C_{gs} = C_{iss} - C_{rss}$$

Equation 10–22
$$C_{ds} = C_{oss} - C_{rss}$$

C_{oss} is not specified as often as the other values on datasheets. Sometimes, it is designated as $C_{d(sub)}$, the drain-to-substrate capacitance. In cases where a value is not available, you must either assume a value or neglect C_{ds}.

EXAMPLE 10–13

The datasheet for a 2N3823 JFET gives $C_{iss} = 6$ pF and $C_{rss} = 2$ pF. Determine C_{gd} and C_{gs}.

Solution

$$C_{gd} = C_{rss} = \mathbf{2\,pF}$$
$$C_{gs} = C_{iss} - C_{rss} = 6\,\text{pF} - 2\,\text{pF} = \mathbf{4\,pF}$$

Related Problem Although C_{oss} is not specified on the datasheet for the 2N3823 JFET, assume a value of 3 pF and determine C_{ds}.

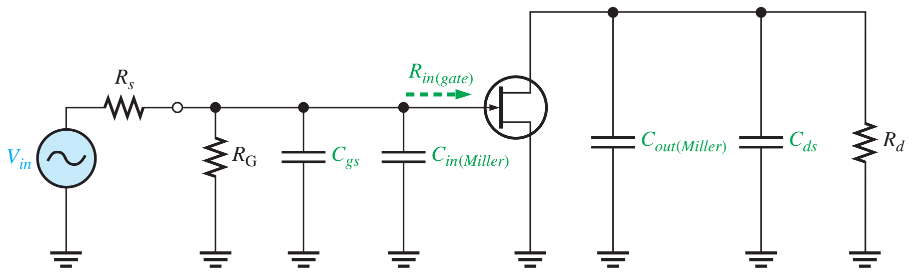
Using Miller's Theorem Miller's theorem is applied the same way in FET inverting amplifier high-frequency analysis as was done in BJT amplifiers. Looking in from the signal source in Figure 10–39(b), C_{gd} effectively appears in the Miller input capacitance, which was given in Equation 10–1, as follows:

$$C_{in(Miller)} = C_{gd}(A_v + 1)$$

C_{gs} simply appears as a capacitance to ac ground in parallel with $C_{in(Miller)}$, as shown in Figure 10–40. Looking in at the drain, C_{gd} effectively appears in the Miller output capacitance (from Equation 10–2) from drain to ground in parallel with R_d, as shown in Figure 10–40.

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right)$$

These two Miller capacitances contribute to a high-frequency input *RC* circuit and a high-frequency output *RC* circuit. Both are low-pass filters, which produce phase lag.



▲ FIGURE 10–40

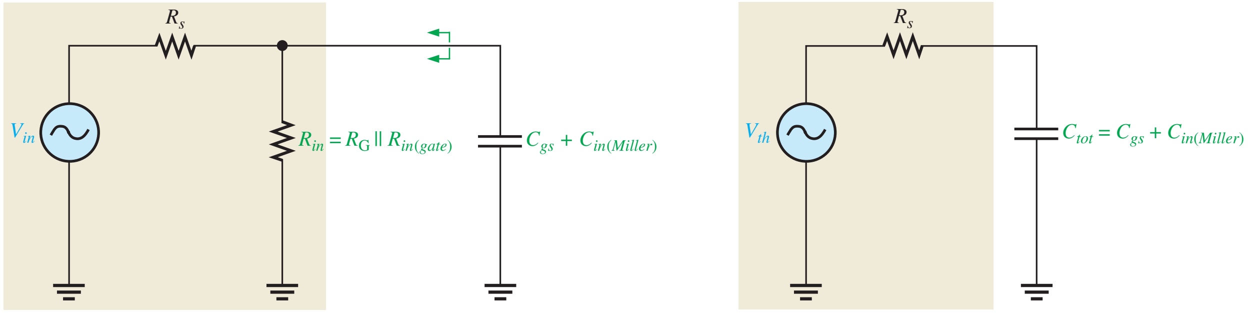
High-frequency equivalent circuit after applying Miller's theorem.

The Input *RC* Circuit

The high-frequency input circuit forms a low-pass type of filter and is shown in Figure 10–41(a). Because both R_G and the input resistance at the gate of FETs are extremely high, the controlling resistance for the input circuit is the resistance of the input source as long as $R_s \ll R_{in}$. This is because R_s appears in parallel with R_{in} when Thevenin's theorem is applied. The simplified input *RC* circuit appears in Figure 10–41(b). The upper critical frequency for the input circuit is

$$f_{cu(input)} = \frac{1}{2\pi R_s C_{tot}}$$

Equation 10–23


R_s
V_{in}
$R_{in} = R_G \parallel R_{in(gate)}$
$C_{gs} + C_{in(Miller)}$
R_s
V_{th}
$C_{tot} = C_{gs} + C_{in(Miller)}$

(a) Thevenizing

(b) Thevenin equivalent input circuit, neglecting R_{in}

▲ FIGURE 10–41

Input *RC* circuit.

where $C_{tot} = C_{gs} + C_{in(Miller)}$. The input RC circuit produces a phase angle of

Equation 10–24

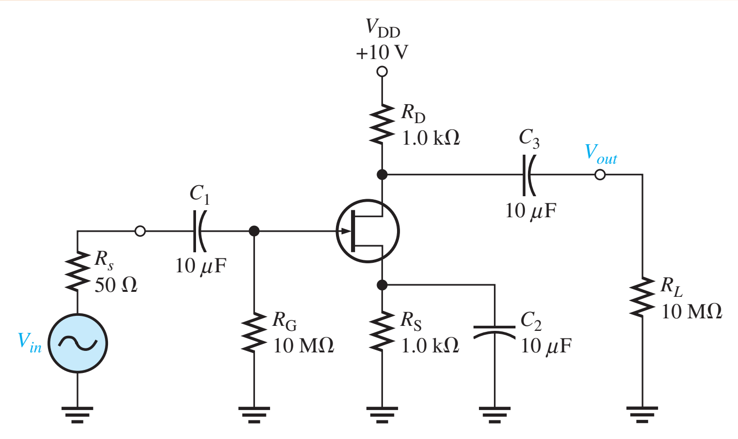
$$\boldsymbol{\theta = \tan^{-1}\left(\frac{R_s}{X_{C_{tot}}}\right)}$$

The effect of the input RC circuit is to reduce the midrange gain of the amplifier by 3 dB at the critical frequency and to cause the gain to decrease at −20 dB/decade above f_c.

EXAMPLE 10–14

Find the upper critical frequency of the input RC circuit for the FET amplifier in Figure 10–42. $C_{iss} = 8$ pF, $C_{rss} = 3$ pF, and $g_m = 6500\ \mu$S.

▶ FIGURE 10–42



Solution Determine C_{gd} and C_{gs}.

$$C_{gd} = C_{rss} = 3\text{ pF}$$
$$C_{gs} = C_{iss} - C_{rss} = 8\text{ pF} - 3\text{ pF} = 5\text{ pF}$$

Determine the upper critical frequency for the input RC circuit as follows:

$$A_v = g_m R_d = g_m(R_D \| R_L) \cong (6500\ \mu\text{S})(1\text{ k}\Omega) = 6.5$$
$$C_{in(Miller)} = C_{gd}(A_v + 1) = (3\text{ pF})(7.5) = 22.5\text{ pF}$$

The total input capacitance is

$$C_{in(tot)} = C_{gs} + C_{in(Miller)} = 5\text{ pF} + 22.5\text{ pF} = 27.5\text{ pF}$$

The upper critical frequency is

$$f_{cu(input)} = \frac{1}{2\pi R_s C_{in(tot)}} = \frac{1}{2\pi(50\ \Omega)(27.5\text{ pF})} = \mathbf{116\ MHz}$$

Related Problem If the gain of the amplifier in Figure 10–42 is increased to 10, what happens to f_c?

The Output *RC* Circuit

The high-frequency output RC circuit is formed by the Miller output capacitance and the output resistance looking in at the drain, as shown in Figure 10–43(a). As in the case of the BJT, the FET is treated as a current source. When you apply Thevenin's theorem, you get an equivalent output RC circuit consisting of R_D in parallel with R_L and an equivalent output capacitance.

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right)$$

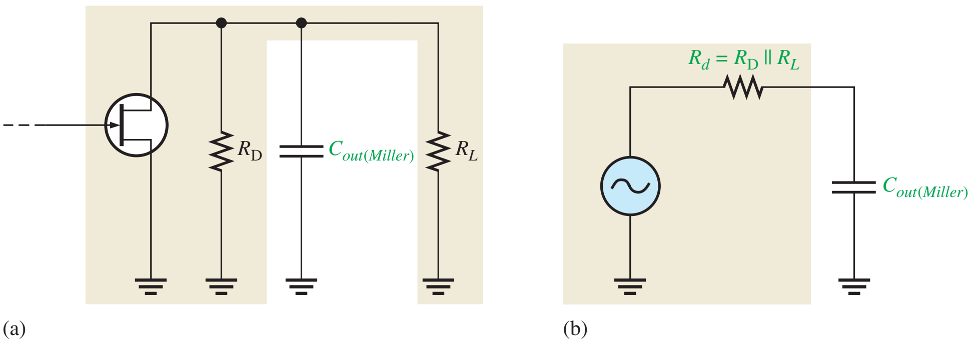


FIGURE 10–43

Output *RC* circuit.

This equivalent output circuit is shown in Figure 10–43(b). The critical frequency of the output *RC* lag circuit is

$$f_{cu(output)} = \frac{1}{2\pi R_d C_{out(Miller)}}$$

Equation 10–25

The output circuit produces a phase shift of

$$\theta = \tan^{-1}\left(\frac{R_d}{X_{C_{out(Miller)}}}\right)$$

Equation 10–26

EXAMPLE 10–15

Determine the upper critical frequency of the output *RC* circuit for the FET amplifier in Figure 10–42. What is the phase shift introduced by this circuit at the critical frequency? Which *RC* circuit is dominant, that is, which one has the lower value of upper critical frequency?

Solution Since R_L is very large compared to R_D, it can be neglected, and the equivalent output resistance is

$$R_d \cong R_D = 1.0\ \text{k}\Omega$$

The equivalent output capacitance is

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right) = (3\ \text{pF})\left(\frac{7.5}{6.5}\right) = 3.46\ \text{pF}$$

Therefore, the upper critical frequency is

$$f_{cu(output)} = \frac{1}{2\pi R_d C_{out(Miller)}} = \frac{1}{2\pi(1.0\ \text{k}\Omega)(3.46\ \text{pF})} = \mathbf{46\ MHz}$$

Although it has been neglected, any stray wiring capacitance could significantly affect the frequency response because $C_{out(Miller)}$ is very small.

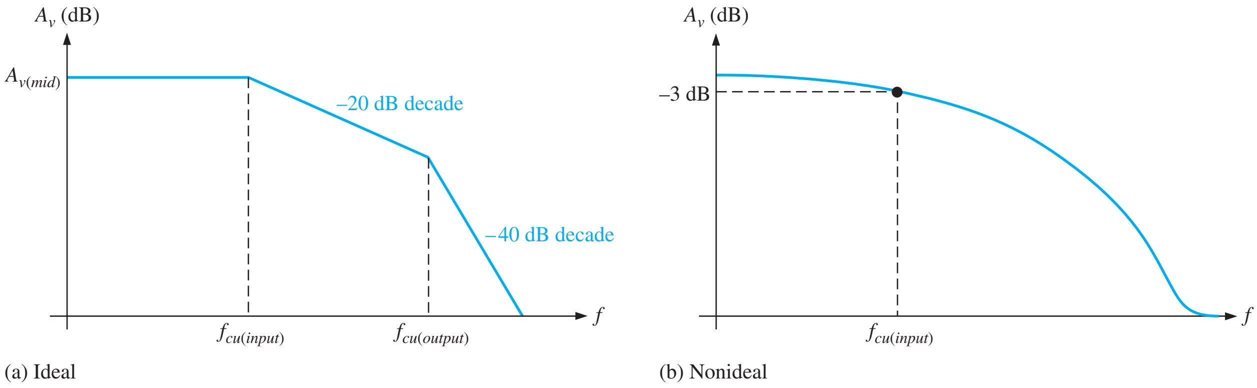
The phase angle is always **45°** at f_c for an *RC* circuit and the output lags.

In Example 10–14, the upper critical frequency of the input *RC* circuit was found to be 116 MHz. Therefore, the upper critical frequency for the output circuit is dominant because it is the lower of the two.

Related Problem If A_v of the amplifier in Figure 10–42 is increased to 10, what is the upper critical frequency of the output circuit?

Total High-Frequency Response of an Amplifier

As you have seen, the two *RC* circuits created by the internal transistor capacitances influence the high-frequency response of both BJT and FET amplifiers. As the frequency increases and reaches the high end of its midrange values, one of the *RC* circuits will cause the amplifier's gain to begin dropping off. The frequency at which this occurs is the dominant upper critical frequency; it is the lower of the two upper critical high frequencies. An ideal high-frequency Bode plot is shown in Figure 10–44(a). It shows the first break point at $f_{cu(input)}$ where the voltage gain begins to roll off at −20 dB/decade. At $f_{cu(output)}$, the gain begins dropping at −40 dB/decade because each *RC* circuit is providing a −20 dB/decade roll-off. Figure 10–44(b) shows a nonideal Bode plot where the voltage gain is actually −3 dB/decade below midrange at $f_{cu(input)}$. Other possibilities are that the output *RC* circuit is dominant or that both circuits have the same critical frequency.



(a) Ideal

(b) Nonideal

▲ **FIGURE 10–44**

High-frequency Bode plots.

SECTION 10–4 CHECKUP

1. What determines the high-frequency response of an amplifier?
2. If an amplifier has a midrange voltage gain of 80, the transistor's C_{bc} is 4 pF, and C_{be} = 8 pF, what is the total input capacitance?
3. A certain amplifier has $f_{cu(input)}$ = 3.5 MHz and $f_{cu(output)}$ = 8.2 MHz. Which circuit dominates the high-frequency response?
4. What are the capacitances that are usually specified on a FET datasheet?
5. If C_{gs} = 4 pF and C_{gd} = 3 pF, what is the total input capacitance of a FET amplifier whose voltage gain is 25?

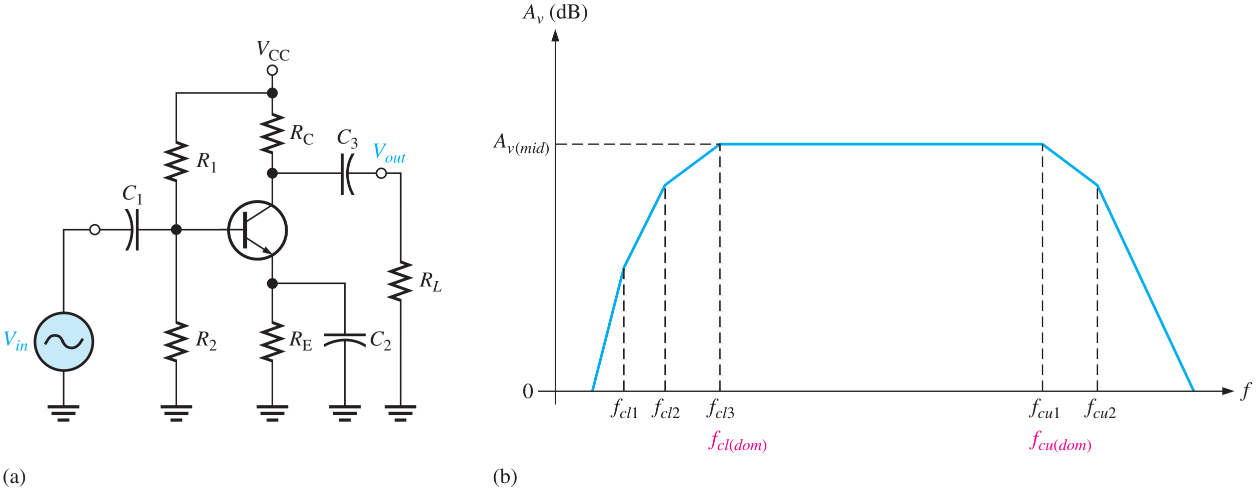
10–5 TOTAL AMPLIFIER FREQUENCY RESPONSE

In the previous sections, you learned how each *RC* circuit in an amplifier affects the frequency response. In this section, we will bring these concepts together and examine the total response of typical amplifiers and the specifications relating to their performance.

After completing this section, you should be able to

- ❑ **Analyze an amplifier for total frequency response**
- ❑ Discuss bandwidth
  - ◆ Define the dominant critical frequencies
- ❑ Explain gain-bandwidth product
  - ◆ Define *unity-gain frequency*

Figure 10–45(b) shows a generalized ideal response curve (Bode plot) for the BJT amplifier shown in Figure 10–45(a). As previously discussed, the three break points at the lower critical frequencies (f_{cl1}, f_{cl2}, and f_{cl3}) are produced by the three low-frequency *RC* circuits formed by the coupling and bypass capacitors. The break points at the upper critical frequencies, f_{cu1} and f_{cu2}, are produced by the two high-frequency *RC* circuits formed by the transistor's internal capacitances.



(a) (b)

▲ FIGURE 10–45

A BJT amplifier and its generalized ideal response curve (Bode plot).

Of particular interest are the two dominant critical frequencies, f_{cl3} and f_{cu1}, in Figure 10–45(b). These two frequencies are where the voltage gain of the amplifier is 3 dB below its midrange value. These dominant frequencies are designated $f_{cl(dom)}$ and $f_{cu(dom)}$.

The upper and lower dominant critical frequencies are sometimes called the *half-power frequencies.* This term is derived from the fact that the output power of an amplifier at its critical frequencies is one-half of its midrange power, as previously mentioned. This can be shown as follows, starting with the fact that the output voltage is 0.707 of its midrange value at the dominant critical frequencies.

$$V_{out(f_c)} = 0.707V_{out(mid)}$$

$$P_{out(f_c)} = \frac{V^2_{out(f_c)}}{R_{out}} = \frac{(0.707V_{out(mid)})^2}{R_{out}} = \frac{0.5V^2_{out(mid)}}{R_{out}} = 0.5P_{out(mid)}$$

Bandwidth

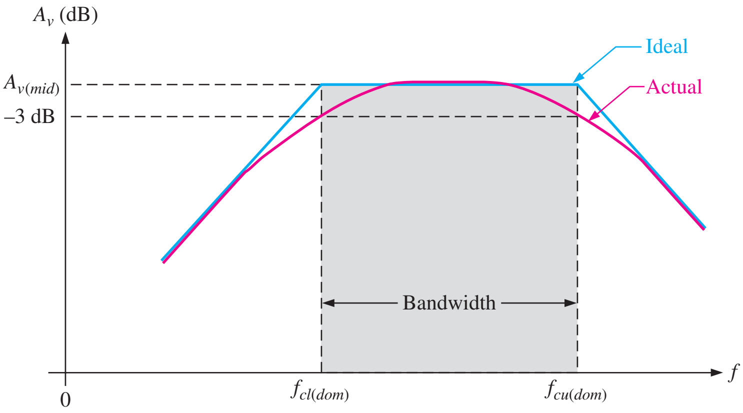
An amplifier normally operates with signal frequencies between $f_{cl(dom)}$ and $f_{cu(dom)}$. As you know, when the input signal frequency is at $f_{cl(dom)}$ or $f_{cu(dom)}$, the output signal voltage level is 70.7% of its midrange value or −3 dB. If the signal frequency drops below $f_{cl(dom)}$, the gain and thus the output signal level drops at 20 dB/decade until the next critical frequency is reached. The same occurs when the signal frequency goes above $f_{cu(dom)}$.

The range (band) of frequencies lying between $f_{cl(dom)}$ and $f_{cu(dom)}$ is defined as the **bandwidth** of the amplifier, as illustrated in Figure 10–46. Only the dominant critical frequencies appear in the response curve because they determine the bandwidth. Also, sometimes the other critical frequencies are far enough away from the dominant frequencies that they play no significant role in the total amplifier response and can be neglected. The amplifier's bandwidth is expressed in units of hertz as

$$BW = f_{cu(dom)} - f_{cl(dom)} \qquad \text{Equation 10–27}$$

FIGURE 10–46

Response curve illustrating the bandwidth of an amplifier.



Ideally, all signal frequencies lying in an amplifier's bandwidth are amplified equally. For example, if a 10 mV rms signal is applied to an amplifier with a voltage gain of 20, it is amplified to 200 mV rms for all frequencies in the bandwidth. Actually, the gain is down 3 dB at $f_{cl(dom)}$ and $f_{cu(dom)}$.

EXAMPLE 10–16

What is the bandwidth of an amplifier having an $f_{cl(dom)}$ of 200 Hz and an $f_{cu(dom)}$ of 2 kHz?

Solution

$$BW = f_{cu(dom)} - f_{cl(dom)} = 2000\text{ Hz} - 200\text{ Hz} = \mathbf{1800\text{ Hz}}$$

Notice that bandwidth has the unit of hertz.

Related Problem

If $f_{cl(dom)}$ is increased, does the bandwidth increase or decrease? If $f_{cu(dom)}$ is increased, does the bandwidth increase or decrease?

Gain-Bandwidth Product

One characteristic of amplifiers is that the product of the voltage gain and the bandwidth is always constant when the roll-off is −20 dB/decade. This characteristic is called the **gain-bandwidth product.** Let's assume that the dominant lower critical frequency of a particular amplifier is much less than the dominant upper critical frequency.

$$f_{cl(dom)} \ll f_{cu(dom)}$$

The bandwidth can then be approximated as

$$BW = f_{cu(dom)} - f_{cl(dom)} \cong f_{cu}$$

Unity-Gain Frequency The simplified Bode plot for this condition is shown in Figure 10–47. Notice that $f_{cl(dom)}$ is neglected because it is so much smaller than $f_{cu(dom)}$, and the bandwidth approximately equals $f_{cu(dom)}$. Beginning at $f_{cu(dom)}$, the gain rolls off until unity gain (0 dB) is reached. The frequency at which the amplifier's gain is 1 is called the *unity-gain frequency*, f_T. The significance of f_T is that it always equals the midrange voltage gain times the bandwidth and is constant for a given transistor.

Equation 10–28

$$f_T = A_{v(mid)}BW$$

For the case shown in Figure 10–47, $f_T = A_{v(mid)}f_{cu(dom)}$. For example, if a transistor datasheet specifies $f_T = 100$ MHz, this means that the transistor is capable of producing a voltage gain of 1 up to 100 MHz, or a gain of 100 up to 1 MHz, or any combination of gain and bandwidth that produces a product of 100 MHz.

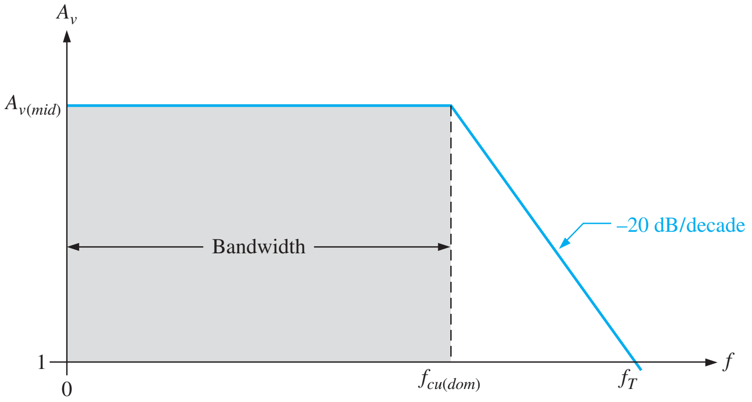


FIGURE 10–47

Simplified response curve where $f_{cl(dom)}$ is negligible (assumed to be zero) compared to $f_{cu(dom)}$.

EXAMPLE 10–17

A certain transistor has an f_T of 175 MHz. When this transistor is used in an amplifier with a midrange voltage gain of 50, what bandwidth can be achieved ideally?

Solution

$$f_T = A_{v(mid)}BW$$

$$BW = \frac{f_T}{A_{v(mid)}} = \frac{175\text{ MHz}}{50} = \mathbf{3.5\text{ MHz}}$$

Related Problem An amplifier has a midrange voltage gain of 20 and a bandwidth of 1 MHz. What is the f_T of the transistor?

SECTION 10–5 CHECKUP

1. What is the voltage gain of an amplifier at f_T?
2. What is the bandwidth of an amplifier when $f_{cu(dom)} = 25$ kHz and $f_{cl(dom)} = 100$ Hz?
3. The f_T of a certain transistor is 130 MHz. What voltage gain can be achieved with a bandwidth of 50 MHz?

10–6 FREQUENCY RESPONSE OF MULTISTAGE AMPLIFIERS

To this point, you have seen how the voltage gain of a single-stage amplifier changes over frequency. When two or more stages are cascaded to form a multistage amplifier, the overall frequency response is determined by the frequency response of each stage depending on the relationships of the critical frequencies.

After completing this section, you should be able to

- ❑ **Analyze multistage amplifiers for frequency response**
- ❑ Analyze the case where the stages have different critical frequencies
  - ◆ Determine the overall bandwidth
- ❑ Analyze the case where the stages have equal critical frequencies
  - ◆ Determine the overall bandwidth
- ❑ Simulate a two-stage amplifier using Multisim

When amplifier stages are cascaded to form a multistage amplifier, the dominant frequency response is determined by the responses of the individual stages. There are two cases to consider:

1. Each stage has a different dominant lower critical frequency and a different dominant upper critical frequency.

2. Each stage has the same dominant lower critical frequency and the same dominant upper critical frequency.

Different Critical Frequencies

Ideally, when the dominant lower critical frequency, $f_{cl(dom)}$, of each amplifier stage is different from the other stages, the overall dominant lower critical frequency, $f'_{cl(dom)}$, equals the dominant critical frequency of the stage with the highest $f_{cl(dom)}$.

Ideally, when the dominant upper critical frequency, $f_{cu(dom)}$, of each amplifier stage is different from the other stages, the overall dominant upper critical frequency, $f'_{cu(dom)}$, equals the dominant critical frequency of the stage with the lowest $f_{cu(dom)}$.

In practice, the critical frequencies interact, so these calculated values should be considered approximations that are useful for troubleshooting or estimating the response. When more accuracy is required, a computer simulation is the best solution.

Overall Bandwidth The bandwidth of a multistage amplifier is the difference between the overall dominant lower critical frequency and the overall dominant upper critical frequency.

$$BW = f'_{cu(dom)} - f'_{cl(dom)}$$

EXAMPLE 10–18

In a certain 2-stage amplifier, one stage has a dominant lower critical frequency of 850 Hz and a dominant upper critical frequency of 100 kHz. The other has a dominant lower critical frequency of 1 kHz and a dominant upper critical frequency of 230 kHz. Determine the overall bandwidth of the 2-stage amplifier.

Solution

$$f'_{cl(dom)} = 1\text{ kHz}$$
$$f'_{cu(dom)} = 100\text{ kHz}$$
$$BW = f'_{cu(dom)} - f'_{cl(dom)} = 100\text{ kHz} - 1\text{ kHz} = \mathbf{99\text{ kHz}}$$

Related Problem A certain 3-stage amplifier has the following dominant lower critical frequencies for each stage: $f_{cl(dom)(1)} = 500$ Hz, $f_{cl(dom)(2)} = 980$ Hz, and $f_{cl(dom)(3)} = 130$ Hz. What is the overall dominant lower critical frequency?

Equal Critical Frequencies

When each amplifier stage in a multistage arrangement has equal dominant critical frequencies, you may think that the overall dominant critical frequency is equal to the critical frequency of each stage. This is not the case, however.

When the dominant lower critical frequencies of each stage in a multistage amplifier are all the same, the overall dominant lower critical frequency is increased by a factor of $1/\sqrt{2^{1/n} - 1}$ as shown by the following formula (n is the number of stages in the multistage amplifier):

Equation 10–29

$$\mathbf{f'_{cl(dom)} = \frac{f_{cl(dom)}}{\sqrt{2^{1/n} - 1}}}$$

When the dominant upper critical frequencies of each stage are all the same, the overall dominant upper critical frequency is reduced by a factor of $\sqrt{2^{1/n} - 1}$.

Equation 10–30

$$\mathbf{f'_{cu(dom)} = f_{cu(dom)}\sqrt{2^{1/n} - 1}}$$

The proofs of these formulas are given in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

EXAMPLE 10–19

Both stages in a 2-stage amplifier have a dominant lower critical frequency of 500 Hz and a dominant upper critical frequency of 80 kHz. Determine the overall bandwidth.

Solution

$$f'_{cl(dom)} = \frac{f_{cl(dom)}}{\sqrt{2^{1/n} - 1}} = \frac{500\text{ Hz}}{\sqrt{2^{0.5} - 1}} = \frac{500\text{ Hz}}{0.644} = 776\text{ Hz}$$

$$f'_{cu(dom)} = f_{cu(dom)}\sqrt{2^{1/n} - 1} = (80\text{ kHz})(0.644) = 51.5\text{ kHz}$$

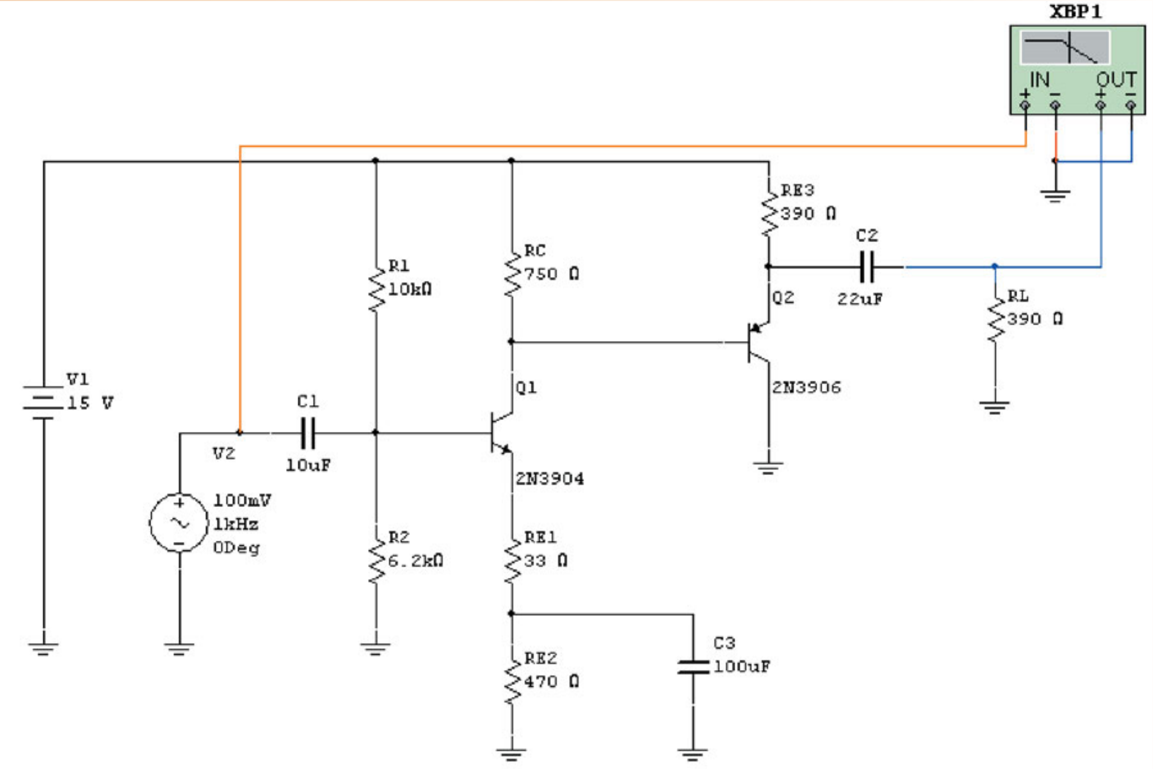
$$BW = f'_{cu(dom)} - f'_{cl(dom)} = 51.5\text{ kHz} - 776\text{ Hz} = \mathbf{50.7\text{ kHz}}$$

Related Problem If a third identical stage is connected in cascade to the 2-stage amplifier in this example, what is the resulting overall bandwidth?

Computer Simulation for Multistage Amplifiers

With multistage amplifiers, the detailed calculation of the frequency response is greatly simplified by computer simulation. There are several interactions within each stage and other interactions between the stages that affect the overall response. When you need more accuracy, a computer simulation is used. This is particularly useful in design work because you can change a component and see the effect immediately on the frequency response. The following example illustrates the application of computer analysis to a multistage amplifier.

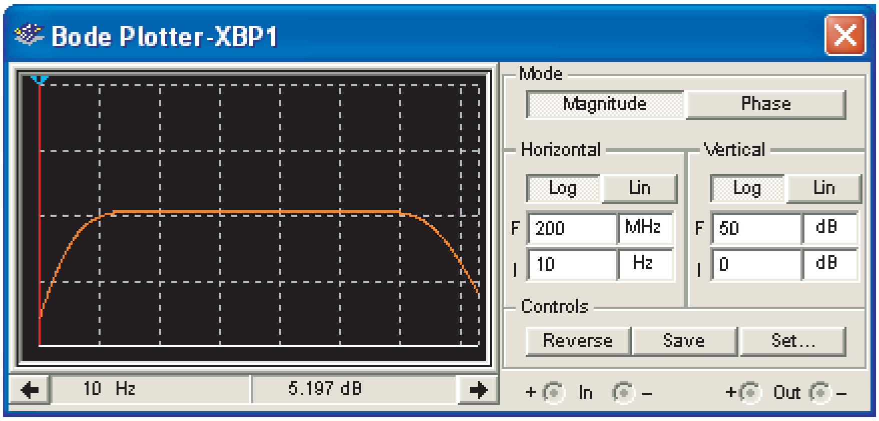
EXAMPLE 10–20 A dc coupled two-stage amplifier is simulated with Multisim in Figure 10–48 to determine the overall frequency response.



▲ FIGURE 10–48

Solution The circuit was constructed in Multisim by dragging the parts needed onto the simulated workbench and connecting them. Connect the Bode plotter and adjust it to show the complete response curve with upper and lower critical frequencies. Figure 10–49 shows the display. When the cursor is moved to the lower critical frequency (3 dB

▶ FIGURE 10–49



Horizontal: F 200 MHz; I 10 Hz

Vertical: F 50 dB; I 0 dB

10 Hz 5.197 dB

below midrange), a reading of approximately 56 Hz is observed. When the cursor is moved to the upper critical frequency, a reading of approximately 34 MHz is observed.

Related Problem Determine the gain of the amplifier in Figure 10–48.

SECTION 10–6 CHECKUP

1. One stage in an amplifier has $f_{cl} = 1$ kHz and the other stage has $f_{cl} = 325$ Hz. What is the dominant lower critical frequency?
2. In a certain 3-stage amplifier $f_{cu(1)} = 50$ kHz, $f_{cu(2)} = 55$ kHz, and $f_{cu(3)} = 49$ kHz. What is the dominant upper critical frequency?
3. When more identical stages are added to a multistage amplifier with each stage having the same critical frequency, does the bandwidth increase or decrease?

10–7 Frequency Response Measurements

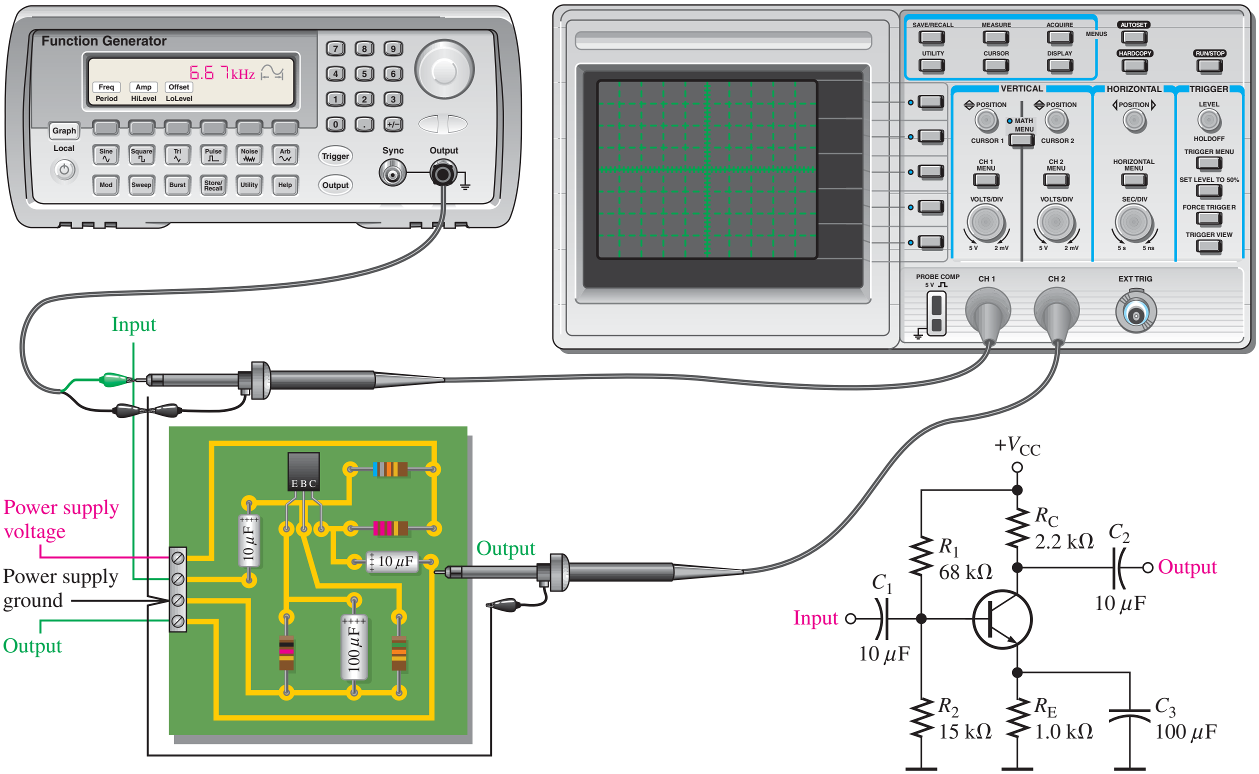
Two basic methods are used to measure the frequency response of an amplifier. The methods apply to both BJT and FET amplifiers although a BJT amplifier is used as an example. You will concentrate on determining the two dominant critical frequencies. From these values, you can get the bandwidth.

After completing this section, you should be able to

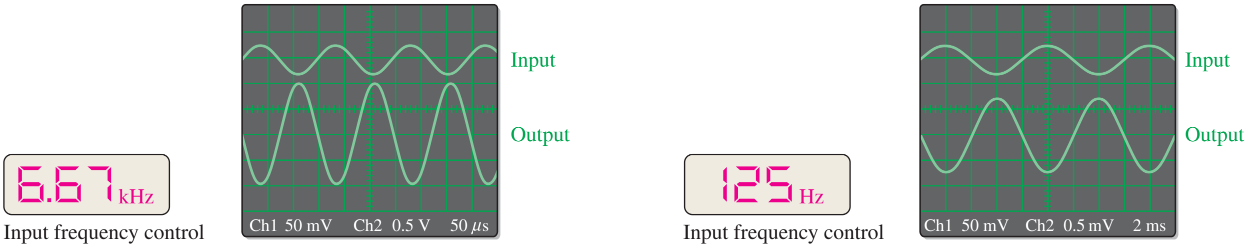
- **Measure the frequency response of an amplifier**
- Analyze the case where the stages have different critical frequencies
    - Determine the overall bandwidth
- Analyze the case where the stages have equal critical frequencies
    - Determine the overall bandwidth
- Simulate a two-stage amplifier using Multisim
- Measure the frequency response of an amplifier
    - Describe a general measurement procedure
- Apply frequency/amplitude measurement to determine critical frequencies
- Use step-response measurement
    - Determine the upper critical frequency
    - Determine the lower critical frequency

Frequency/Amplitude Measurement

Figure 10–50(a) shows the test setup for an amplifier circuit board. The schematic for the circuit board is also shown. The amplifier is driven by a sinusoidal voltage source with a


Function Generator
6.67 kHz
Freq Period
Amp HiLevel
Offset LoLevel
Graph
Local
Sine
Square
Tri
Pulse
Noise
Arb
Trigger
Sync
Output
Mod
Sweep
Burst
Store/Recall
Utility
Help
Output
SAVE/RECALL
MEASURE
ACQUIRE
AUTOSET
MENUS
UTILITY
CURSOR
DISPLAY
HARDCOPY
RUN/STOP
VERTICAL
HORIZONTAL
TRIGGER
POSITION
POSITION
POSITION
LEVEL
MATH MENU
CURSOR 1
CURSOR 2
HOLDOFF
CH 1 MENU
CH 2 MENU
HORIZONTAL MENU
TRIGGER MENU
SET LEVEL TO 50%
VOLTS/DIV
VOLTS/DIV
SEC/DIV
FORCE TRIGGER
TRIGGER VIEW
PROBE COMP 5 V
CH 1
CH 2
EXT TRIG
Input
Power supply voltage
Power supply ground
Output
E B C
10 μF
10 μF
100 μF
Output
+V_CC
R_C 2.2 kΩ
R_1 68 kΩ
C_2
Output
10 μF
Input
C_1
10 μF
R_2 15 kΩ
R_E 1.0 kΩ
C_3 100 μF

(a) Circuit and test setup for measuring the frequency response of an amplifier


6.67 kHz
Input
Output
Ch1 50 mV Ch2 0.5 V 50 μs
125 Hz
Input
Output
Ch1 50 mV Ch2 0.5 mV 2 ms

Input frequency control on function generator

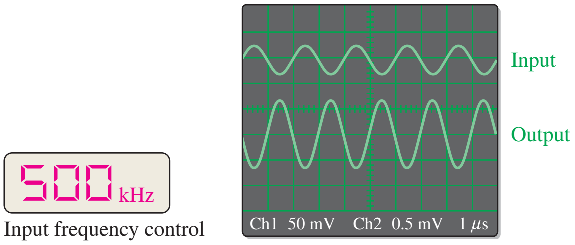
Amplifier input and output voltages

Input frequency control on function generator

Amplifier input and output voltages

(b) Frequency is set to a midrange value (6.67 kHz in this case). Input voltage adjusted for an output of 1 V peak.

(c) Frequency is reduced until the output is 0.707 V peak. This is the lower critical frequency.


500 kHz
Input
Output
Ch1 50 mV Ch2 0.5 mV 1 μs

Input frequency control on function generator

Amplifier input and output voltages

(d) Frequency is increased until the output is again 0.707 V peak. This is the upper critical frequency.

▲ FIGURE 10–50

A general procedure for measuring an amplifier's frequency response.

dual-channel oscilloscope connected to the input and to the output. The input frequency is set to a midrange value, and its amplitude is adjusted to establish an output signal reference level, as shown in Figure 10–50(b). This output voltage reference level for midrange should be set at a convenient value within the linear operation of the amplifier: for example, 100 mV, 1 V, 10 V, and so on. In this case, set the output signal to a peak value of 1 V.

Next, the frequency of the input voltage is decreased until the peak value of the output drops to 0.707 V. The amplitude of the input voltage must be kept constant as the frequency is reduced. Readjustment may be necessary because of changes in loading of the voltage source with frequency. When the output is 0.707 V, the frequency is measured, and you have the value for f_{cl} as indicated in Figure 10–50(c).

Next, the input frequency is increased back up through midrange and beyond until the peak value of the output voltage again drops to 0.707 V. Again, the amplitude of the input must be kept constant as the frequency is increased. When the output is 0.707 V, the frequency is measured and you have the value for f_{cu} as indicated in Figure 10–50(d). From these two frequency measurements, you can find the bandwidth by the formula $BW = f_{cu} - f_{cl}$.

Step-Response Measurement

The lower and upper critical frequencies of an amplifier can be determined using the *step-response method* by applying a voltage step to the input of the amplifier and measuring the rise and fall times of the resulting output voltage. The basic test setup shown in Figure 10–50(a) is used except that the pulse output of the function generator is selected. The input step is created by the rising edge of a pulse that has a long duration compared to the rise and fall times to be measured. The rise time of the input pulse must be fast compared to the rise time you measure from the amplifier.

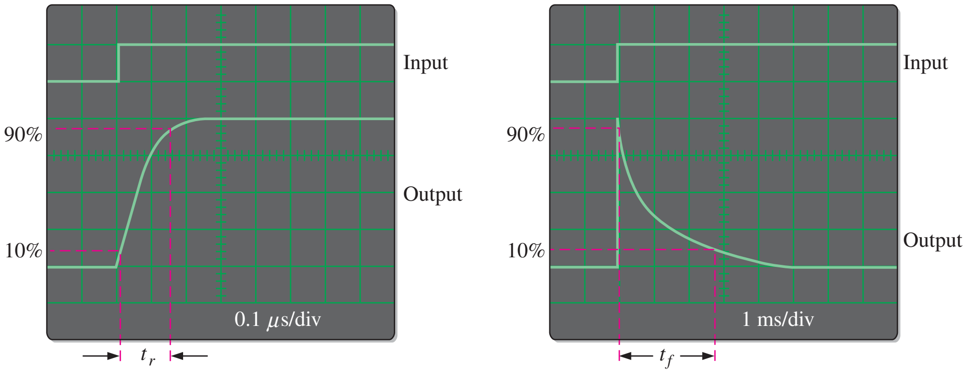
High-Frequency Measurement When a step input is applied, the amplifier's high-frequency *RC* circuits (internal capacitances) prevent the output from responding immediately to the step input. As a result, the output voltage has a rise time (t_r) associated with it, as shown in Figure 10–51(a). In fact, the rise time is inversely related to the upper critical frequency (f_{cu}) of the amplifier. As f_{cu} becomes lower, the rise time of the output becomes greater. The oscilloscope display illustrates how the rise time is measured from the 10% amplitude point to the 90% amplitude point. The scope must be set on a short time base so the relatively short interval of the rise time can be accurately observed. Once this measurement is made, f_{cu} can be calculated with the following formula:

Equation 10–31

$$f_{cu} = \frac{0.35}{t_r}$$

▶ **FIGURE 10–51**

Measurement of the rise and fall times associated with the amplifier's step response. The outputs are inverted.



(a) Measurement of output rise time to determine the upper critical frequency

(b) Measurement of output fall time to determine the lower critical frequency

Low-Frequency Measurement To determine the lower critical frequency (f_{cl}) of the amplifier, the step input must be of sufficiently long duration to observe the full charging time of the low-frequency *RC* circuits (coupling capacitances), which cause the "sloping" of the output and which we will refer to as the fall time (t_f). This is illustrated in Figure 10–51(b). The fall time is inversely related to the low critical frequency of the amplifier. As f_{cl} becomes higher, the fall time of the output becomes less. The scope display illustrates how the fall time is measured from the 90% point to the 10% point. The scope must be set on a long time base so the complete interval of the fall time can be observed. Once this measurement is made, f_{cl} can be determined with the following formula.

$$f_{cl} = \frac{0.35}{t_f}$$

Equation 10–32

The derivations of Equations 10–31 and 10–32 are in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

SECTION 10–7 CHECKUP

1. In Figure 10–50, what are the lower and upper critical frequencies?
2. The rise time and the fall time of an amplifier's output voltage are measured between what two points on the voltage transition?
3. In Figure 10–51, what is the rise time?
4. In Figure 10–51, what is the fall time?
5. What is the bandwidth of the amplifier whose step response is measured in Figure 10–51?

Application Activity: *Frequency Analysis of Audio Amplifier*

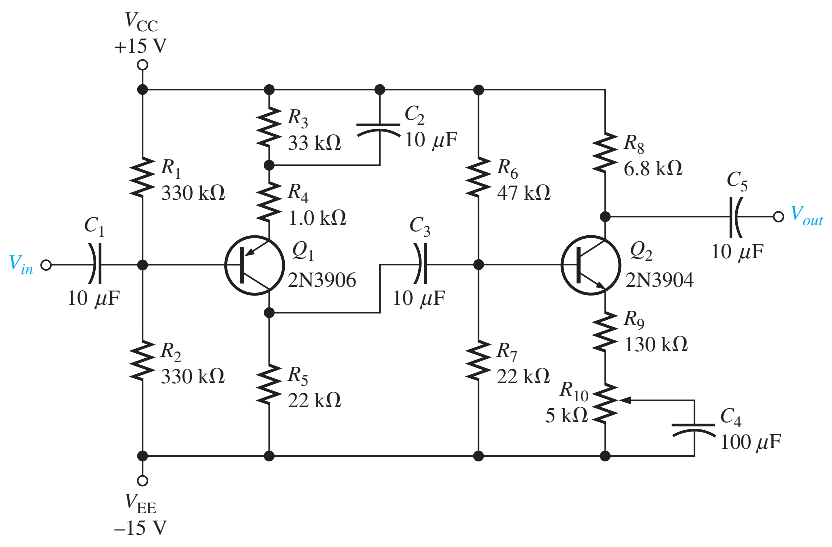
A utility company is interested in purchasing a large quantity of the PA systems that were developed in the Application Activities in Chapters 6 and 7. Because the company frequently works near high-voltage power lines, where 60 Hz interference is common, it has requested that the PA systems be designed to minimize pickup from power lines. You have been assigned to analyze the frequency response of the PA system and determine the best way to avoid the 60 Hz interference. The modified PA system will be marketed only for voice communication.

The audio frequency spectrum is defined to be the range of frequencies from 20 Hz to 20 kHz. However, the range of frequencies of the human voice is generally accepted to be between 300 Hz and 3 kHz. Based on this, the audio amplifier is to be redesigned for a 300 Hz ± 10% cutoff (critical) frequency in order to minimize the 60 Hz interference. The utility company has requested that the gain at 60 Hz should be down by a minimum of −20 dB from the midrange gain for the units it is purchasing. The high-frequency response of the amplifier is no concern at this point, as long as it is greater than approximately 3 kHz.

The original audio amplifier, shown in Figure 10–52 and in the simulation of Figure 10–53, has a dominant lower critical frequency of 16 Hz as indicated on the Bode plotter in Figure 10–53(c). In order to meet the new specification for a lower critical frequency of 300 Hz, the amplifier must be modified with lower capacitance values.

▶ FIGURE 10–52

The audio preamplifier with original capacitor values.



A frequency analysis of the original amplifier is as follows. For the Q_1 stage, the *input circuit* consists of C_1 and $R_1 \| R_2 \| \beta_{ac}R_4$. r'_e is neglected. The critical frequency is (assuming $\beta_{ac} = 100$)

$$f_{cl(input)} = \frac{1}{2\pi(R_1 \| R_2 \| \beta_{ac}R_4)C_1} = \frac{1}{2\pi(62.3\text{ k}\Omega)10\ \mu\text{F}} = 0.255\text{ Hz}$$

The *bypass circuit* consists of C_2 and

$$\left(R_4 + \left(\frac{R_1 \| R_2 \| R_{source}}{\beta_{ac}}\right)\right) \| R_3 \cong R_4$$

The expression reduces to approximately R_4 because R_{source} is assumed to be 300 Ω (microphone impedance) and R_3 is much greater than R_4.

$$f_{cl(bypass)} = \frac{1}{2\pi R_4 C_2} = \frac{1}{2\pi(1\text{ k}\Omega)10\ \mu\text{F}} = 15.9\text{ Hz}$$

The *output circuit* consists of C_3 and $R_5 + R_6 \| R_7 \| \beta_{ac}(R_9 + R_{10})$. r'_e is neglected. Assuming that R_{10} is set at 1 kΩ,

$$f_{cl(output)} = \frac{1}{2\pi(R_5 + R_6 \| R_7 \| \beta_{ac}(R_9 + R_{10}))C_3} = \frac{1}{2\pi(35.2\text{ k}\Omega)10\ \mu\text{F}} = 0.452\text{ Hz}$$

For the Q_2 stage, the *input circuit* is the same as the output circuit of the Q_1 stage.

$$f_{cl(input)} = \frac{1}{2\pi(R_5 + R_6 \| R_7 \| \beta_{ac}(R_9 + R_{10}))C_3} = \frac{1}{2\pi(35.2\text{ k}\Omega)10\ \mu\text{F}} = 0.452\text{ Hz}$$

The *bypass circuit* consists of C_4 and approximately $R_9 + R_{10} + (R_6 \| R_7)/\beta_{ac}$. The resistance is partially dependent on the setting of R_{10}. We will assume that the gain setting is such that R_{10} has negligible effect on the frequency.

$$f_{cl(bypass)} = \frac{1}{2\pi\left(R_9 + \dfrac{R_6 \| R_7}{\beta_{ac}}\right)C_4} = \frac{1}{2\pi(280\ \Omega)100\ \mu\text{F}} = 5.68\text{ Hz}$$

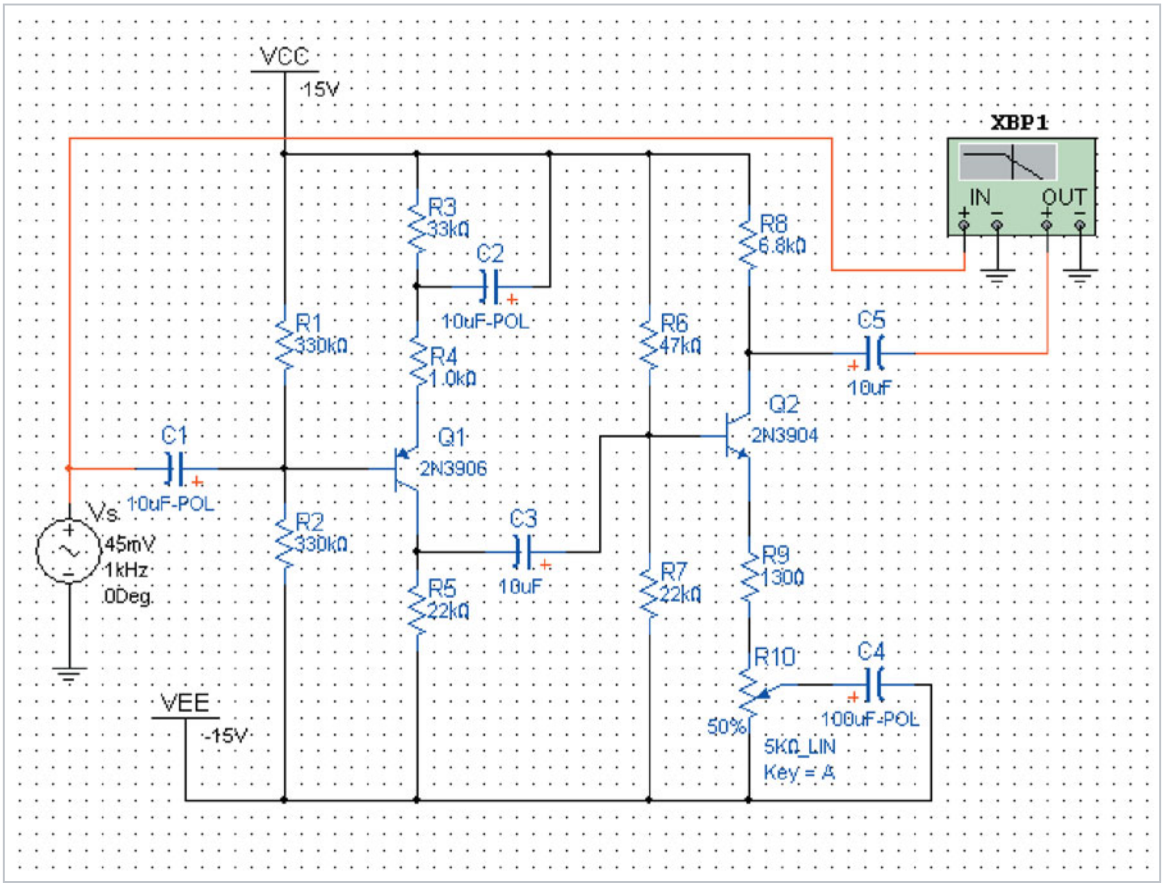
The *output circuit* consists of C_5 and $R_8 + R_L$. The load is the 29 kΩ input resistance of the power amplifier.

$$f_{cl(output)} = \frac{1}{2\pi(R_8 + R_L)C_5} = \frac{1}{2\pi(35.8\text{ k}\Omega)10\ \mu\text{F}} = 0.445\text{ Hz}$$

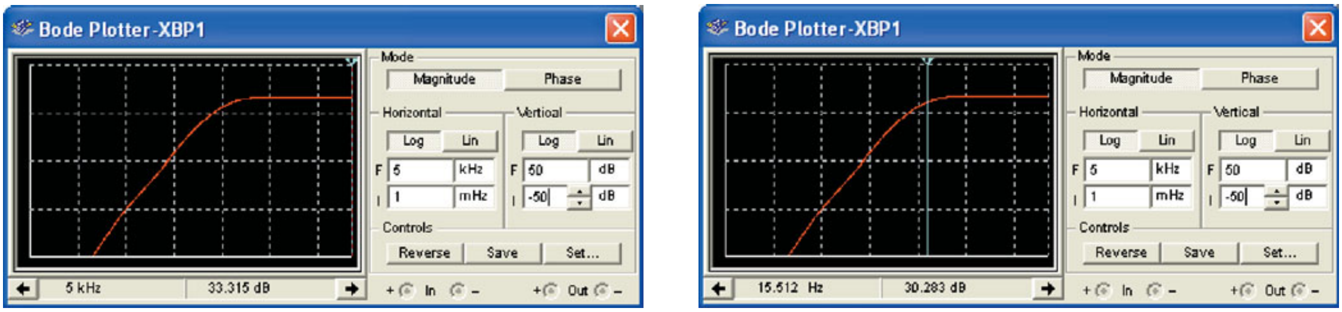
The dominant critical frequency of the amplifier is established by the Q_1 stage bypass circuit and is $f_{cl(bypass)} = 15.9$ Hz, which is in very close agreement with the simulation.

Simulation of Original Circuit

The Multisim preamp with the original capacitor values is shown in Figure 10–53(a). A Bode plotter is connected to measure the frequency response. Figure 10–53(b) shows the logarithmic response curve with a midrange gain at 5 kHz of 33.3 dB.


VCC
15V
XBP1
IN
OUT
R3
33kΩ
C2
10uF-POL
R8
6.8kΩ
R1
330kΩ
R4
1.0kΩ
R6
47kΩ
C5
10uF
Q2
2N3904
C1
Q1
2N3906
Vs
45mV
1kHz
0Deg
10uF-POL
R2
330kΩ
C3
10uF
R5
22kΩ
R7
22kΩ
R9
130Ω
R10
C4
50%
100uF-POL
5KΩ_LIN
Key = A
VEE
-15V

(a) Circuit screen with original capacitor values


Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Log
Lin
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out
Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Log
Lin
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out

Horizontal: F 5 kHz, I 1 mHz; Vertical: F 50 dB, I -50 dB

5 kHz 33.315 dB

Horizontal: F 5 kHz, I 1 mHz; Vertical: F 50 dB, I -50 dB

15.512 Hz 30.283 dB

(b) At 5 kHz gain is 33.3 dB

(c) Approximate f_c is 16 Hz at 30.3 dB (down 3 dB)

▲ FIGURE 10–53

Preamp frequency response with original capacitor values.

Moving the Bode plotter cursor down until the gain is approximately 3 dB below midrange, or 30.3 dB, results in a lower critical frequency of 16 Hz at this gain setting (note that there is a small effect on the response for different gains due to a different path for C_4 to charge and discharge). This verifies that the response of the preamp includes the potentially troublesome 60 Hz interference.

Modification to Increase the Overall Lower Critical Frequency

Capacitor values must be reduced to achieve a critical frequency of 300 Hz ± 10%. The approach, in this case, will be to use C_1 and C_3 to set the new dominant critical frequency. C_2 and C_5 will be used to produce a faster roll-off below 60 Hz. C_4 will be left at 100 μF to avoid a change in frequency response when the gain is changed.

C_1 is part of the stage 1 input circuit, and C_3 is part of the stage 2 input circuit. These capacitor values will determine the proper dominant lower critical frequencies required to achieve an overall dominant critical frequency of 300 Hz.

Multistage Frequency Response When the lower critical frequencies of each stage are equal, Equation 10–29 applies. The overall dominant lower critical frequency, $f'_{cl(dom)}$, is 300 Hz. Solving the equation for the dominant lower critical frequency of each stage, $f_{cl(dom)}$, you get

$$f_{cl(dom)} = f'_{cl(dom)}\sqrt{(2^{1/2} - 1)} = 300\text{ Hz}\sqrt{(1.414 - 1)} = 300\text{ Hz}(0.643) = 193\text{ Hz}$$

Setting the dominant critical frequency of both stages of the amplifier to 193 Hz will produce an overall dominant lower critical frequency of 300 Hz. Using the frequency analysis that was done for the original circuit as a guide, do the following calculations.

1. Calculate the value of C_1 to produce a lower critical frequency of 193 Hz.
2. Calculate the value of C_3 to produce a lower critical frequency of 193 Hz.

The results of your calculation should agree with the values shown in Figure 10–54. The value for C_2 is the next lower available value in Multisim.

The Multisim circuit with reduced capacitor values is shown in Figure 10–54(a). As you can see in part (c), the new critical frequency is 276.604 Hz, which is within the specified 10% tolerance of 300 Hz. The gain is 9.744 dB for a frequency near 60 Hz with the volume setting at 85%, as shown in part (d).

3. From the Bode plots in Figure 10–54, determine how much the gain at 60 Hz is down from the midrange gain.

Simulate the preamp circuit using your Multisim software. Observe the operation with the Bode plotter.

Prototyping and Testing

Now that the revised circuit has been simulated and its operation verified, the modifications are made to the circuit and it is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

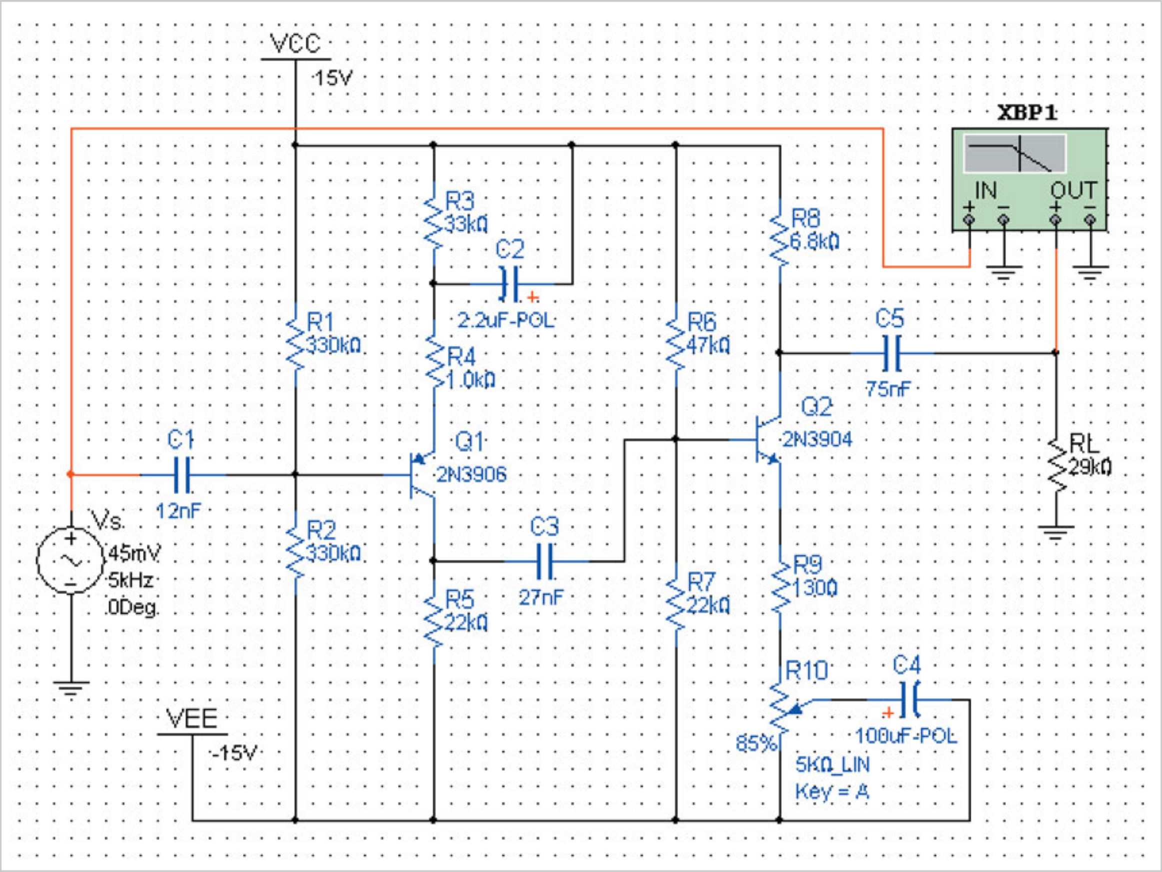
Lab Experiment

To build and test a similar circuit, go to Experiment 10 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

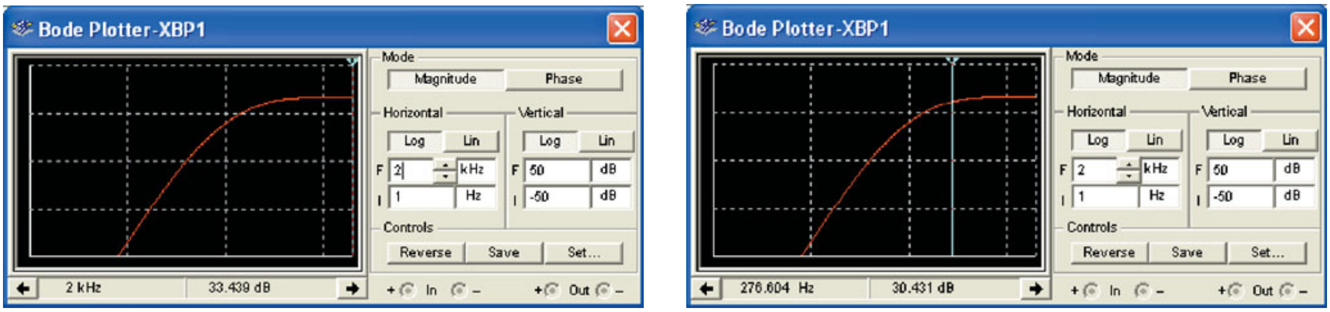
Circuit Board

The capacitor values on the preamp circuit board are changed and the board is tested at 5 kHz and at 60 Hz using an oscilloscope, as shown in Figure 10–55.

4. What is the measured rms output voltage at 5 kHz in Figure 10–55?
5. What is the measured rms output voltage at 60 Hz in Figure 10–55?


VCC
15V
XBP1
IN
OUT
R3
33kΩ
C2
2.2uF-POL
R1
330kΩ
R4
1.0kΩ
R6
47kΩ
R8
6.8kΩ
C5
75nF
Q2
2N3904
RL
29kΩ
C1
12nF
Q1
2N3906
Vs
45mV
5kHz
0Deg
R2
330kΩ
C3
27nF
R5
22kΩ
R7
22kΩ
R9
130Ω
R10
C4
100uF-POL
85%
5KΩ_LIN
Key = A
VEE
-15V

(a) Circuit screen with reduced capacitor values


Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out

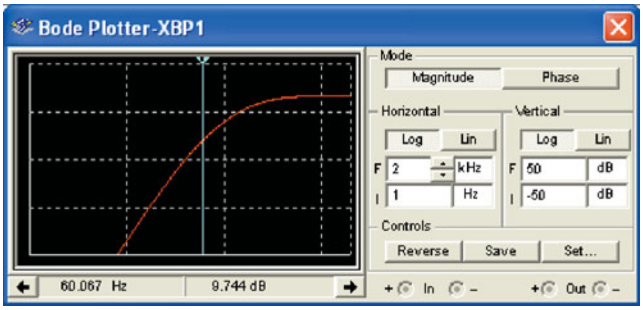
Horizontal: F 2 kHz, I 1 Hz; Vertical: F 50 dB, I -50 dB

2 kHz 33.439 dB

276.604 Hz 30.431 dB

(b) Midrange gain is 33.439 Hz

(c) f_c is 276.604 Hz at 30.431 dB (-3 dB)


Bode Plotter-XBP1
Mode
Magnitude
Phase
Horizontal
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out

Horizontal: F 2 kHz, I 1 Hz; Vertical: F 50 dB, I -50 dB

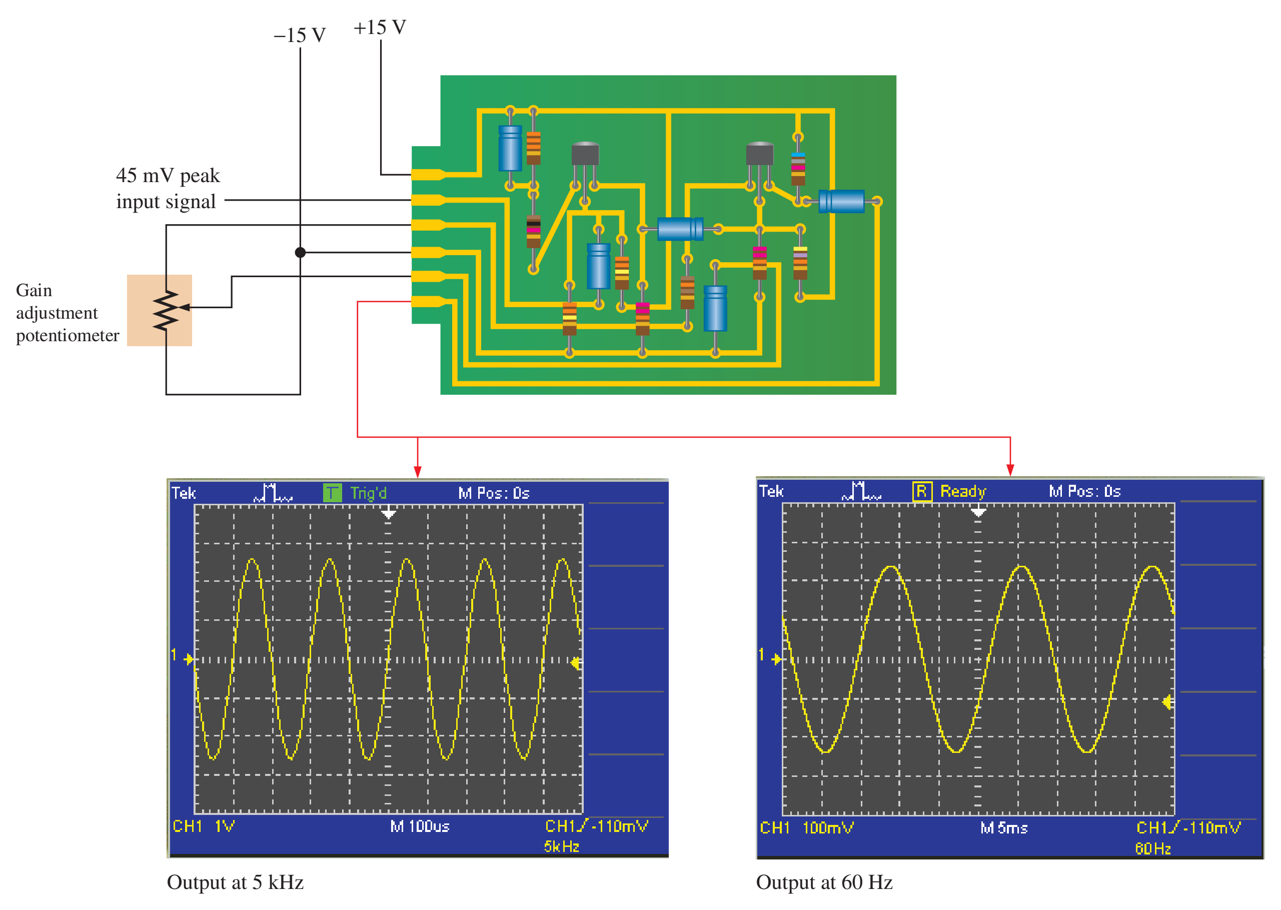
60.067 Hz 9.744 dB

(d) At 60.067 Hz the gain is 9.744 dB (down 23.7 dB)

▲ **FIGURE 10–54**

Preamp frequency response with reduced capacitor values.

6. What would be the approximate rms amplitude of the output waveform at 300 Hz?
7. Based on the oscilloscope measurement in Figure 10–55, express the voltage gain at 5 kHz in dB.
8. Based on the oscilloscope measurement in Figure 10–55, express the voltage gain at 60 Hz in dB.


−15 V
+15 V
45 mV peak input signal
Gain adjustment potentiometer
Tek
Trig'd
M Pos: 0s
1
CH1 1V
M 100us
CH1 ∕ -110mV
5kHz
Tek
Ready
M Pos: 0s
1
CH1 100mV
M 5ms
CH1 ∕ -110mV
60Hz

Output at 5 kHz

Output at 60 Hz

▲ **FIGURE 10–55**

Frequency test of new preamp board using an oscilloscope.

SUMMARY

Section 10–1
- The coupling and bypass capacitors of an amplifier affect the low-frequency response.
- The internal transistor capacitances affect the high-frequency response.

Section 10–2
- The decibel is a logarithmic unit of measurement for power gain and voltage gain.
- A decrease in voltage gain to 70.7% of midrange value is a reduction of 3 dB.
- A halving of the voltage gain corresponds to a reduction of 6 dB.
- The dBm is a unit for measuring power levels referenced to 1 mW.

- Critical frequencies are values of frequency at which the *RC* circuits reduce the voltage gain to 70.7% of its midrange value.

Section 10–3

- Each *RC* circuit causes the gain to drop at a rate of 20 dB/decade.
- For the low-frequency *RC* circuits, the *highest* critical frequency is the dominant critical frequency.
- A decade of frequency change is a ten-times change (increase or decrease).
- An octave of frequency change is a two-times change (increase or decrease).

Section 10–4

- For the high-frequency *RC* circuits, the *lowest* critical frequency is the dominant critical frequency.

Section 10–5

- The bandwidth of an amplifier is the range of frequencies between the dominant lower critical frequency and the dominant upper critical frequency.
- The gain-bandwidth product is a transistor parameter that is constant and equal to the unity-gain frequency.

Section 10–6

- The dominant critical frequencies of a multistage amplifier establish the bandwidth.

Section 10–7

- Two frequency response measurement methods are frequency/amplitude and step.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Bandwidth The characteristic of certain types of electronic circuits that specifies the usable range of frequencies that pass from input to output.

Bode plot An idealized graph of the gain in dB versus frequency used to graphically illustrate the response of an amplifier or filter.

Critical frequency The frequency at which the response of an amplifier or filter is 3 dB less than at midrange.

Decade A ten-times increase or decrease in the value of a quantity such as frequency.

Decibel A logarithmic measure of the ratio of one power to another or one voltage to another.

Midrange gain The gain that occurs for the range of frequencies between the lower and upper critical frequencies.

Roll-off The rate of decrease in the gain of an amplifier above or below the critical frequencies.

KEY FORMULAS

Miller's Theorem

10–1	$C_{in(Miller)} = C(A_v + 1)$	Miller input capacitance, where $C = C_{bc}$ or C_{gd}
10–2	$C_{out(Miller)} = C\left(\dfrac{A_v + 1}{A_v}\right)$	Miller output capacitance, where $C = C_{bc}$ or C_{gd}

The Decibel

10–3	$A_{p(\mathrm{dB})} = 10 \log A_p$	Power gain in decibels
10–4	$A_{v(\mathrm{dB})} = 20 \log A_v$	Voltage gain in decibels

BJT Amplifier Low-Frequency Response

10–5	$A_{v(mid)} = \dfrac{R_c}{r'_e}$	Midrange voltage gain
10–6	$f_{cl(input)} = \dfrac{1}{2\pi R_{in} C_1}$	Lower critical frequency, input *RC* circuit
10–7	$\theta = \tan^{-1}\left(\dfrac{X_{C1}}{R_{in}}\right)$	Phase angle, input *RC* circuit
10–8	$f_{cl(output)} = \dfrac{1}{2\pi(R_C + R_L)C_3}$	Lower critical frequency, output *RC* circuit

10–9	$\theta = \tan^{-1}\left(\dfrac{X_{C3}}{R_C + R_L}\right)$	Phase angle, output *RC* circuit
10–10	$R_{in(emitter)} = r'_e + \dfrac{R_{th}}{\beta_{ac}}$	Resistance looking in at emitter
10–11	$f_{cl(bypass)} = \dfrac{1}{2\pi[(r'_e + R_{th}/\beta_{ac}) \parallel R_E]C_2}$	Lower critical frequency, bypass *RC* circuit

FET Amplifier Low-Frequency Response

10–12	$f_{cl(input)} = \dfrac{1}{2\pi(R_G \parallel R_{in(gate)})C_1}$	Lower critical frequency, input *RC* circuit
10–13	$\theta = \tan^{-1}\left(\dfrac{X_{C1}}{R_{in}}\right)$	Phase angle, input *RC* circuit
10–14	$f_{cl(output)} = \dfrac{1}{2\pi(R_D + R_L)C_2}$	Lower critical frequency, output *RC* circuit
10–15	$\theta = \tan^{-1}\left(\dfrac{X_{C2}}{R_D + R_L}\right)$	Phase angle, output *RC* circuit

BJT Amplifier High-Frequency Response

10–16	$f_{cu(input)} = \dfrac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r'_e)C_{tot}}$	Upper critical frequency, input *RC* circuit
10–17	$\theta = \tan^{-1}\left(\dfrac{R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r'_e}{X_{C_{tot}}}\right)$	Phase angle, input *RC* circuit
10–18	$f_{cu(output)} = \dfrac{1}{2\pi R_c C_{out(Miller)}}$	Upper critical frequency, output *RC* circuit
10–19	$\theta = \tan^{-1}\left(\dfrac{R_c}{X_{C_{out(Miller)}}}\right)$	Phase angle, output *RC* circuit

FET Amplifier High-Frequency Response

10–20	$C_{gd} = C_{rss}$	Gate-to-drain capacitance
10–21	$C_{gs} = C_{iss} - C_{rss}$	Gate-to-source capacitance
10–22	$C_{ds} = C_{oss} - C_{rss}$	Drain-to-source capacitance
10–23	$f_{cu(input)} = \dfrac{1}{2\pi R_s C_{tot}}$	Upper critical frequency, input *RC* circuit
10–24	$\theta = \tan^{-1}\left(\dfrac{R_s}{X_{C_{tot}}}\right)$	Phase angle, input *RC* circuit
10–25	$f_{cu(output)} = \dfrac{1}{2\pi R_d C_{out(Miller)}}$	Upper critical frequency, output *RC* circuit
10–26	$\theta = \tan^{-1}\left(\dfrac{R_d}{X_{C_{out(Miller)}}}\right)$	Phase angle, output *RC* circuit

Total Response

10–27	$BW = f_{cu} - f_{cl}$	Bandwidth
10–28	$f_T = A_{v(mid)}BW$	Unity-gain bandwidth

Multistage Response

10–29	$f'_{cl(dom)} = \dfrac{f_{cl(dom)}}{\sqrt{2^{1/n} - 1}}$	Overall dominant lower critical frequency for case of equal dominant critical frequencies

10–30	$f'_{cu(dom)} = f_{cu(dom)}\sqrt{2^{1/n} - 1}$	Overall dominant upper critical frequency for case of equal dominant critical frequencies

Measurement Techniques

10–31	$f_{cu} = \dfrac{0.35}{t_r}$	Upper critical frequency
10–32	$f_{cl} = \dfrac{0.35}{t_f}$	Lower critical frequency

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. Coupling capacitors in an amplifier determine the low-frequency response.
2. Bypass capacitors in an amplifier determine the high-frequency response.
3. Internal transistor capacitance has no effect on an amplifier's frequency response.
4. Miller's theorem states that both gain and internal capacitances influence high-frequency response.
5. The midrange gain is between the upper and lower critical frequencies.
6. The critical frequency is where the gain is 6 dB less than the midrange gain.
7. dBm is a unit for measuring power levels.
8. A ten-times change in frequency is called a decade.
9. An octave corresponds to a doubling or halving of the frequency.
10. The input and output *RC* circuits have no effect on the frequency response.
11. A Bode plot shows the voltage gain versus frequency on a logarithmic scale.
12. Phase shift is part of an amplifier's frequency response.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the value of R_1 in Figure 10–8 is increased, the signal voltage at the base will
   (a) increase **(b)** decrease **(c)** not change
2. If the value of C_1 in Figure 10–27 is decreased, the critical frequency associated with the input circuit will
   (a) increase **(b)** decrease **(c)** not change
3. If the value of R_L in Figure 10–27 is increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
4. If the value of R_C in Figure 10–27 is decreased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
5. If V_{CC} in Figure 10–34 is increased, the dc emitter voltage will
   (a) increase **(b)** decrease **(c)** not change
6. If the transistor in Figure 10–34 is replaced with one having a higher β_{ac}, the critical frequency will
   (a) increase **(b)** decrease **(c)** not change
7. If the transistor in Figure 10–34 is replaced with one having a lower β_{ac}, the midrange voltage gain will
   (a) increase **(b)** decrease **(c)** not change
8. If the value of R_D in Figure 10–42 is increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
9. If the value of R_L in Figure 10–42 is increased, the critical frequency will
   (a) increase **(b)** decrease **(c)** not change
10. If the FET in Figure 10–42 is replaced with one having a higher g_m, the critical frequency will
    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 10–1

1. The low-frequency response of an amplifier is determined in part by

(a) the voltage gain **(b)** the type of transistor
(c) the supply voltage **(d)** the coupling capacitors

2. The high-frequency response of an amplifier is determined in part by

(a) the gain-bandwidth product **(b)** the bypass capacitor
(c) the internal transistor capacitances **(d)** the roll-off

3. The Miller input capacitance of an amplifier is dependent, in part, on

(a) the input coupling capacitor **(b)** the voltage gain
(c) the bypass capacitor **(d)** none of these

Section 10–2

4. The decibel is used to express

(a) power gain **(b)** voltage gain **(c)** attenuation **(d)** all of these

5. When the voltage gain is 70.7% of its midrange value, it is said to be

(a) attenuated **(b)** down 6 dB **(c)** down 3 dB **(d)** down 1 dB

6. In an amplifier, the gain that occurs between the lower and upper critical frequencies is called the

(a) critical gain **(b)** midrange gain **(c)** bandwidth gain **(d)** decibel gain

7. A certain amplifier has a voltage gain of 100 at midrange. If the gain decreases by 6 dB, it is equal to

(a) 50 **(b)** 70.7 **(c)** 0 **(d)** 20

Section 10–3

8. The gain of a certain amplifier decreases by 6 dB when the frequency is reduced from 1 kHz to 10 Hz. The roll-off is

(a) −3 dB/decade **(b)** −6 dB/decade **(c)** −3 dB/octave **(d)** −6 dB/octave

9. The gain of a particular amplifier at a given frequency decreases by 6 dB when the frequency is doubled. The roll-off is

(a) −12 dB/decade **(b)** −20 dB/decade **(c)** −6 dB/octave **(d)** answers (b) and (c)

10. The lower critical frequency of a direct-coupled amplifier with no bypass capacitor is

(a) variable **(b)** 0 Hz **(c)** dependent on the bias **(d)** none of these

Section 10–4

11. At the upper critical frequency, the peak output voltage of a certain amplifier is 10 V. The peak voltage in the midrange of the amplifier is

(a) 7.07 V **(b)** 6.37 V **(c)** 14.14 V **(d)** 10 V

12. The high-frequency response of an amplifier is determined by the

(a) coupling capacitors **(b)** bias circuit
(c) transistor capacitances **(d)** all of these

13. The Miller input and output capacitances for a BJT inverting amplifier depend on

(a) C_{bc} **(b)** β_{ac} **(c)** A_v **(d)** answers (a) and (c)

Section 10–5

14. The bandwidth of an amplifier is determined by

(a) the midrange gain **(b)** the critical frequencies
(c) the roll-off rate **(d)** the input capacitance

15. An amplifier has the following critical frequencies: 1.2 kHz, 950 Hz, 8 kHz, and 8.5 kHz. The bandwidth is

(a) 7550 Hz **(b)** 7300 Hz **(c)** 6800 Hz **(d)** 7050 Hz

16. Ideally, the midrange gain of an amplifier

(a) increases with frequency
(b) decreases with frequency
(c) remains constant with frequency
(d) depends on the coupling capacitors

17. The frequency at which an amplifier's gain is 1 is called the

(a) unity-gain frequency **(b)** midrange frequency

(c) corner frequency **(d)** break frequency

18. When the voltage gain of an amplifier is increased, the bandwidth

(a) is not affected **(b)** increases **(c)** decreases **(d)** becomes distorted

19. If the f_T of the transistor used in a certain amplifier is 75 MHz and the bandwidth is 10 MHz, the voltage gain must be

(a) 750 **(b)** 7.5 **(c)** 10 **(d)** 1

20. In the midrange of an amplifier's bandwidth, the peak output voltage is 6 V. At the lower critical frequency, the peak output voltage is

(a) 3 V **(b)** 3.82 V **(c)** 8.48 V **(d)** 4.24 V

Section 10–6

21. The dominant lower critical frequency of a multistage amplifier is the

(a) lowest f_{cl} **(b)** highest f_{cl} **(c)** average of all the f_{cl}'s **(d)** none of these

22. When the critical frequencies of all of the stages are the same, the dominant critical frequency is

(a) higher than any individual f_{cl} **(b)** lower than any individual f_{cl}

(c) equal to the individual f_{cl}'s **(d)** the sum of all individual f_{cl}'s

Section 10–7

23. In the step response of a noninverting amplifier, a longer rise time means

(a) a narrower bandwidth **(b)** a lower f_{cl}

(c) a higher f_{cu} **(d)** answers (a) and (b)

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 10–1

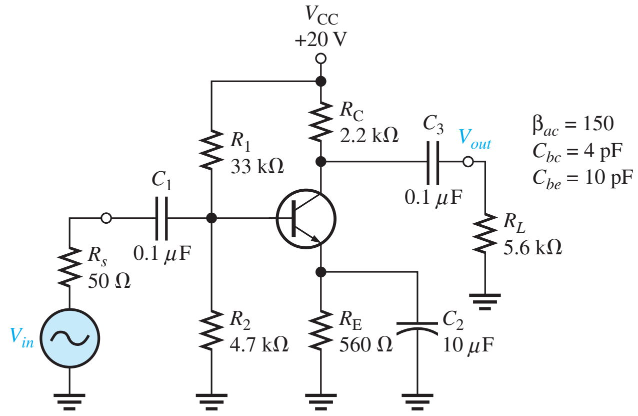
Basic Concepts

1. In a capacitively coupled amplifier, the input coupling capacitor and the output coupling capacitor form two of the circuits (along with the respective resistances) that determine the low- frequency response. Assuming that the input and output impedances are the same and neglecting the bypass circuit, which circuit will first cause the gain to drop from its midrange value as the frequency is lowered?

2. Explain why the coupling capacitors do not have a significant effect on gain at sufficiently high-signal frequencies.

3. List the capacitances that affect high-frequency gain in both BJT and FET amplifiers.

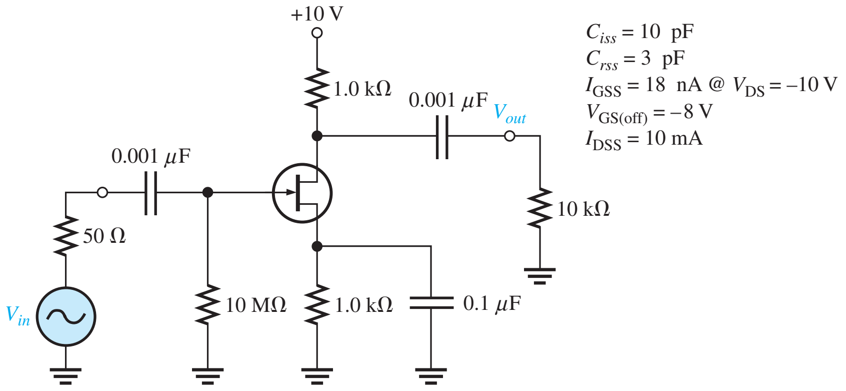
4. In the amplifier of Figure 10–56, list the capacitances that affect the low-frequency response of the amplifier and those that affect the high-frequency response.



▶ **FIGURE 10–56**

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F10-56).

5. Determine the Miller input capacitance in Figure 10–56.
6. Determine the Miller output capacitance in Figure 10–56.
7. Determine the Miller input and output capacitances for the amplifier in Figure 10–57.



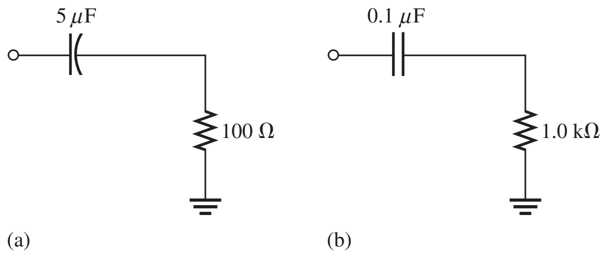
▲ FIGURE 10–57

Section 10–2 The Decibel

8. A certain amplifier exhibits an output power of 5 W with an input power of 0.5 W. What is the power gain in dB?
9. If the output voltage of an amplifier is 1.2 V rms and its voltage gain is 50, what is the rms input voltage? What is the gain in dB?
10. The midrange voltage gain of a certain amplifier is 65. At a certain frequency beyond midrange, the gain drops to 25. What is the gain reduction in dB?
11. What are the dBm values corresponding to the following power values?
    (a) 2 mW **(b)** 1 mW **(c)** 4 mW **(d)** 0.25 mW
12. Express the midrange voltage gain of the amplifier in Figure 10–56 in decibels. Also express the voltage gain in dB for the critical frequencies.

Section 10–3 Low-Frequency Amplifier Response

13. Determine the critical frequencies of each *RC* circuit in Figure 10–58.

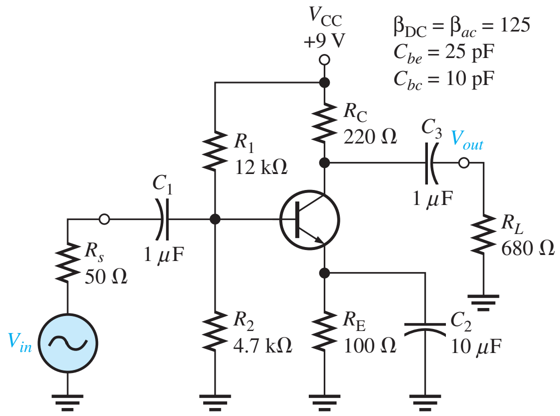


(a) (b)

▲ FIGURE 10–58

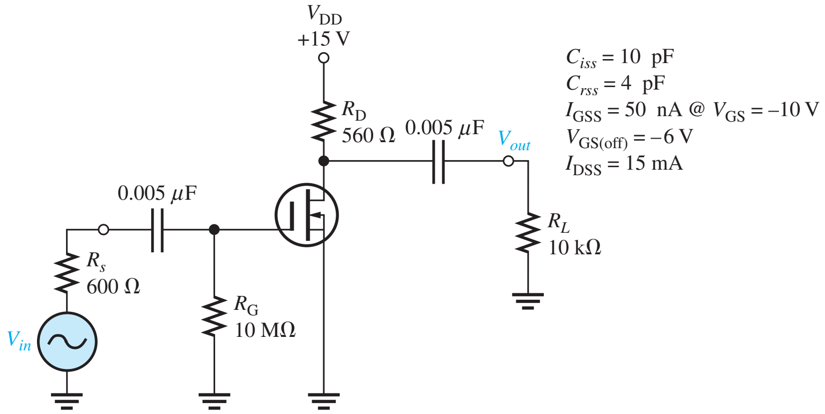
14. Determine the critical frequencies associated with the low-frequency response of the BJT amplifier in Figure 10–59. Which is the dominant critical frequency? Sketch the Bode plot.
15. Determine the voltage gain of the amplifier in Figure 10–59 at one-tenth of the dominant critical frequency, at the dominant critical frequency, and at ten times the dominant critical frequency for the low-frequency response.
16. Determine the phase shift at each of the frequencies used in Problem 15.

▶ FIGURE 10–59


V_{CC}
+9 V
$\beta_{DC} = \beta_{ac} = 125$
$C_{be} = 25$ pF
$C_{bc} = 10$ pF
R_C
220 Ω
R_1
12 kΩ
C_3
V_{out}
1 μF
C_1
R_L
680 Ω
R_s
50 Ω
1 μF
V_{in}
R_2
4.7 kΩ
R_E
100 Ω
C_2
10 μF

17. Determine the critical frequencies associated with the low-frequency response of the FET amplifier in Figure 10–60. Indicate the dominant critical frequency and draw the Bode plot.

18. Find the voltage gain of the amplifier in Figure 10–60 at the following frequencies: f_c, $0.1f_c$, and $10f_c$, where f_c is the dominant critical frequency.


V_{DD}
+15 V
$C_{iss} = 10$ pF
$C_{rss} = 4$ pF
$I_{GSS} = 50$ nA @ $V_{GS} = -10$ V
$V_{GS(off)} = -6$ V
$I_{DSS} = 15$ mA
R_D
560 Ω
0.005 μF
V_{out}
0.005 μF
R_L
10 kΩ
R_s
600 Ω
R_G
10 MΩ
V_{in}

▲ FIGURE 10–60

Section 10–4 High-Frequency Amplifier Response

19. Determine the critical frequencies associated with the high-frequency response of the amplifier in Figure 10–59. Identify the dominant critical frequency and sketch the Bode plot.

20. Determine the voltage gain of the amplifier in Figure 10–59 at the following frequencies: $0.1f_c$, f_c, $10f_c$, and $100f_c$, where f_c is the dominant critical frequency in the high-frequency response.

21. The datasheet for the FET in Figure 10–60 gives $C_{rss} = 4$ pF and $C_{iss} = 10$ pF. Determine the critical frequencies associated with the high-frequency response of the amplifier, and indicate the dominant frequency.

22. Determine the voltage gain in dB and the phase shift at each of the following multiples of the dominant critical frequency in Figure 10–60 for the high-frequency response: $0.1f_c$, f_c, $10f_c$, and $100f_c$.

Section 10–5 Total Amplifier Frequency Response

23. A particular amplifier has the following low critical frequencies: 25 Hz, 42 Hz, and 136 Hz. It also has high critical frequencies of 8 kHz and 20 kHz. Determine the upper and lower critical frequencies.

24. Determine the bandwidth of the amplifier in Figure 10–59.

25. $f_T = 200$ MHz is taken from the datasheet of a transistor used in a certain amplifier. If the midrange gain is determined to be 38 and if f_{cl} is low enough to be neglected compared to f_{cu}, what bandwidth would you expect? What value of f_{cu} would you expect?

26. If the midrange gain of a given amplifier is 50 dB and therefore 47 dB at f_{cu}, how much gain is there at $2f_{cu}$? At $4f_{cu}$? At $10f_{cu}$?

Section 10–6 Frequency Response of Multistage Amplifiers

27. In a certain two-stage amplifier, the first stage has critical frequencies of 230 Hz and 1.2 MHz. The second stage has critical frequencies of 195 Hz and 2 MHz. What are the dominant critical frequencies?

28. What is the bandwidth of the two-stage amplifier in Problem 27?

29. Determine the bandwidth of a two-stage amplifier in which each stage has a lower critical frequency of 400 Hz and an upper critical frequency of 800 kHz.

30. What is the dominant lower critical frequency of a three-stage amplifier in which $f_{cl} = 50$ Hz for each stage.

31. In a certain two-stage amplifier, the lower critical frequencies are $f_{cl(1)} = 125$ Hz and $f_{cl(2)} =$ 125 Hz, and the upper critical frequencies are $f_{cu(1)} = 3$ MHz and $f_{cu(2)} = 2.5$ MHz. Determine the bandwidth.

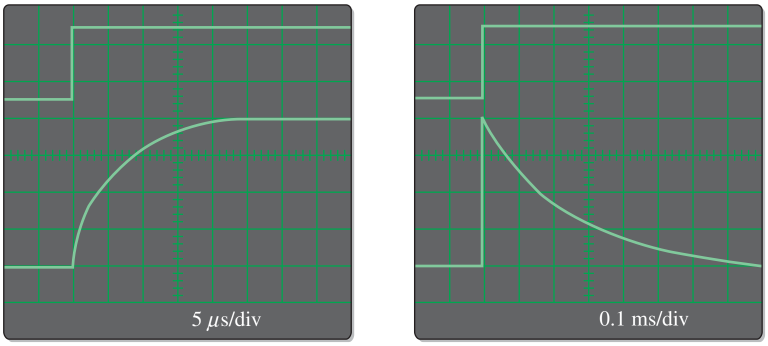
Section 10–7 Frequency Response Measurements

32. In a step-response test of a certain amplifier, $t_r = 20$ ns and $t_f = 1$ ms. Determine f_{cl} and f_{cu}.

33. Suppose you are measuring the frequency response of an amplifier with a signal source and an oscilloscope. Assume that the signal level and frequency are set such that the oscilloscope indicates an output voltage level of 5 V rms in the midrange of the amplifier's response. If you wish to determine the upper critical frequency, indicate what you would do and what scope indication you would look for.

34. Determine the approximate bandwidth of an amplifier from the indicated results of the step-response test in Figure 10–61.

▶ FIGURE 10–61



APPLICATION ACTIVITY PROBLEMS

35. Determine the dominant lower critical frequency for the amplifier in Figure 10–52 if the coupling capacitors are changed to 1 μF. Assume $R_L = 29\ \text{k}\Omega$ and $\beta_{ac} = 100$.

36. Does the change in Problem 35 significantly affect the overall bandwidth?

37. How does a change from 29 kΩ to 100 kΩ in load resistance on the final output of the amplifier in Figure 10–52 affect the dominant lower critical frequency?

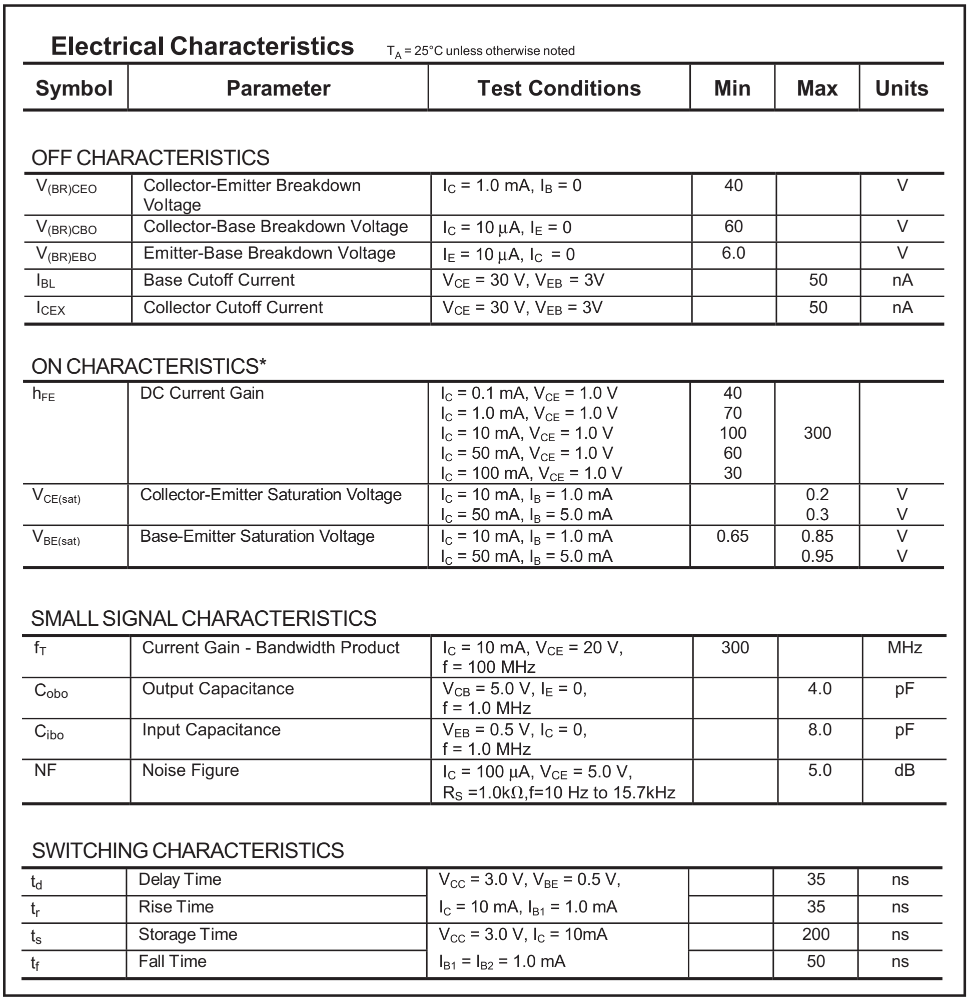
38. If the transistors in the modified preamp in the Application Activity have a β_{ac} of 300, determine the effect on the dominant lower critical frequency.

DATASHEET PROBLEMS

39. Referring to the partial datasheet for a 2N3904 in Figure 10–62, determine the total input capacitance for an amplifier if the voltage gain is 25.

40. A certain amplifier uses a 2N3904 and has a midrange voltage gain of 50. Referring to the partial datasheet in Figure 10–62, determine its minimum bandwidth.

41. The datasheet for a 2N4351 MOSFET specifies the maximum values of internal capacitances as follows: $C_{iss} = 5$ pF, $C_{rss} = 1.3$ pF, and $C_{d(sub)} = 5$ pF. Determine C_{gd}, C_{gs}, and C_{ds}.



Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	6.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V	40		
		I_C = 1.0 mA, V_{CE} = 1.0 V	70		
		I_C = 10 mA, V_{CE} = 1.0 V	100	300	
		I_C = 50 mA, V_{CE} = 1.0 V	60		
		I_C = 100 mA, V_{CE} = 1.0 V	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA		0.2	V
		I_C = 50 mA, I_B = 5.0 mA		0.3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA	0.65	0.85	V
		I_C = 50 mA, I_B = 5.0 mA		0.95	V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz		8.0	pF
NF	Noise Figure	I_C = 100 μA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V,		35	ns
t_r	Rise Time	I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA		200	ns
t_f	Fall Time	I_{B1} = I_{B2} = 1.0 mA		50	ns

▲ FIGURE 10–62

Partial datasheet for the 2N3904. Copyright Fairchild Semiconductor Corporation. Used by permission.

ADVANCED PROBLEMS

42. Two single-stage capacitively coupled amplifiers like the one in Figure 10–56 are connected as a two-stage amplifier (R_L is removed from the first stage). Determine whether or not this configuration will operate as a linear amplifier with an input voltage of 10 mV rms. If not, modify the design to achieve maximum gain without distortion.

43. Two stages of the amplifier in Figure 10–60 are connected in cascade. Determine the overall bandwidth.

44. Redesign the amplifier in Figure 10–52 for an adjustable voltage gain of 50 to 500 and a lower critical frequency of 1 kHz.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

45. Open file TSP10-45 and determine the fault.

46. Open file TSP10-46 and determine the fault.

47. Open file TSP10-47 and determine the fault.

48. Open file TSP10-48 and determine the fault.

11 THYRISTORS

CHAPTER OUTLINE

11–1 The Four-Layer Diode
11–2 The Silicon-Controlled Rectifier (SCR)
11–3 SCR Applications
11–4 The Diac and Triac
11–5 The Silicon-Controlled Switch (SCS)
11–6 The Unijunction Transistor (UJT)
11–7 The Programmable Unijunction Transistor (PUT)
Application Activity

CHAPTER OBJECTIVES

- Describe the basic structure and operation of a 4-layer diode
- Describe the basic structure and operation of an SCR
- Discuss several SCR applications
- Describe the basic structure and operation of the diac and triac
- Describe a silicon-controlled switch (SCS)
- Describe the basic structure and operation of the unijunction transistor
- Describe the basic structure and operation of the programmable UJT

KEY TERMS

- 4-layer diode
- Thyristor
- Forward-breakover voltage ($V_{BR(F)}$)
- Holding current (I_H)
- SCR
- LASCR
- Diac
- Triac
- SCS
- UJT
- Standoff ratio
- PUT

APPLICATION ACTIVITY PREVIEW

The Application Activity in this chapter is a motor speed-control system for a production line conveyor. The system senses the number of parts passing a point in a specified period of time and adjusts the rate of movement of the conveyor belt to achieve a desired rate of flow of the parts. The focus is on the conveyor motor speed-control circuit.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In this chapter, several types of semiconductor devices are introduced. A family of devices known as thyristors are constructed of four semiconductor layers (*pnpn*). Thyristors include the 4-layer diode, the silicon-controlled rectifier (SCR), the diac, the triac, and the silicon-controlled switch (SCS). These types of thyristors share certain common characteristics in addition to their four-layer construction. They act as open circuits capable of withstanding a certain rated voltage until they are triggered. When triggered, they turn on and become low-resistance current paths and remain so, even after the trigger is removed, until the current is reduced to a certain level or until they are triggered off, depending on the type of device. Thyristors can be used to control the amount of ac power to a load and are used in lamp dimmers, motor speed controls, ignition systems, and charging circuits, to name a few.

Other devices described in this chapter include the unijunction transistor (UJT) and the programmable unijunction transistor (PUT). UJTs and PUTs are used as trigger devices for thyristors and also in oscillators and timing circuits.

11–1 THE FOUR-LAYER DIODE

The basic thyristor is a 4-layer device with two terminals, the anode and the cathode. It is constructed of four semiconductor layers that form a *pnpn* structure. The device acts as a switch and remains off until the forward voltage reaches a certain value; then it turns on and conducts. Conduction continues until the current is reduced below a specified value. Although the 4-layer diode is seldom used in new designs, the principles form the basis of other thyristors that you will study.

After completing this section, you should be able to

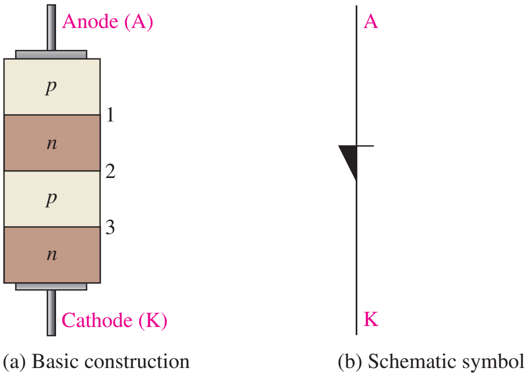
- **Describe the basic structure and operation of a 4-layer diode**
- Discuss the Shockley diode
  ◆ Identify the schematic symbol ◆ Explain the operation based on the equivalent circuit ◆ Explain the forward-breakover voltage ◆ Define *holding current* ◆ Define *switching current* ◆ Describe an application

Shockley Diode

The **4-layer diode** (also known as Shockley diode and SUS) is a type of **thyristor**, which is a class of devices constructed of four semiconductor layers. The basic construction of a 4-layer diode and its schematic symbol are shown in Figure 11–1.

The *pnpn* structure can be represented by an equivalent circuit consisting of a *pnp* transistor and an *npn* transistor, as shown in Figure 11–2(a). The upper *pnp* layers form Q_1 and the lower *npn* layers form Q_2, with the two middle layers shared by both equivalent transistors. Notice that the base-emitter junction of Q_1 corresponds to *pn* junction 1 in Figure 11–1, the base-emitter junction of Q_2 corresponds to *pn* junction 3, and the base-collector junctions of both Q_1 and Q_2 correspond to *pn* junction 2.

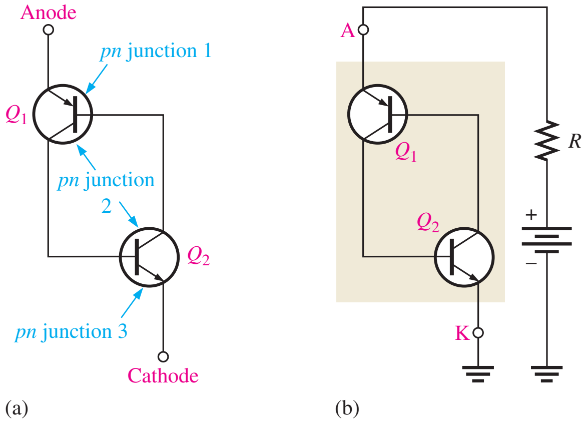
When a positive bias voltage is applied to the anode with respect to the cathode, as shown in Figure 11–2(b), the base-emitter junctions of Q_1 and Q_2 (*pn* junctions 1 and 3 in Figure 11–1(a)) are forward-biased, and the common base-collector junction (*pn* junction 2 in Figure 11–1(a)) is reverse-biased.



(a) Basic construction (b) Schematic symbol

▲ FIGURE 11–1

The 4-layer diode.



(a) (b)

▲ FIGURE 11–2

A 4-layer diode equivalent circuit.

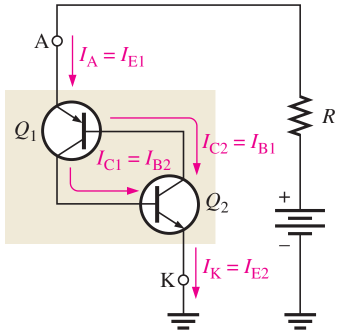
HISTORY NOTE

The four-layer diode (also called a Shockley diode) was invented by William Shockley while he was at Bell Labs. Shockley believed the four-layer diode would revolutionize telephone switching circuits because it could replace the mechanical switches used by the telephone equipment of the time. In the mid-1950s, Shockley founded Shockley Semiconductor Labs with the intent of constructing silicon transistors but soon changed the emphasis of his company to the four-layer diode. It was difficult to manufacture with the technology of the time, and Shockley's company never managed to turn a profit. The four-layer diode eventually evolved into the SCR, which is essentially a four-layer diode with an added control gate.

The currents in a 4-layer diode are shown in the equivalent circuit in Figure 11–3. At low-bias levels, there is very little anode current, and thus it is in the *off* state or forward-blocking region.

▶ FIGURE 11–3

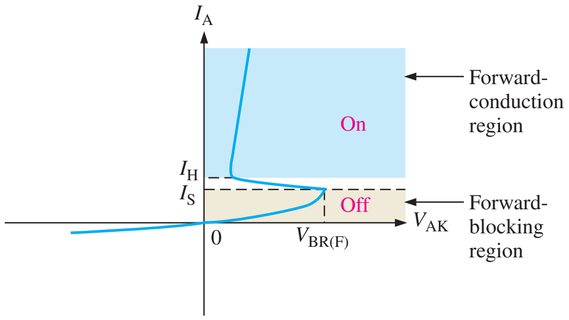
Currents in a 4-layer diode equivalent circuit.



Forward-Breakover Voltage The operation of the 4-layer diode may seem unusual because when it is forward-biased, it can act essentially as an open switch. There is a region of forward bias, called the *forward-blocking region,* in which the device has a very high forward resistance (ideally an open) and is in the *off* state. The forward-blocking region exists from $V_{AK} = 0$ V up to a value of V_{AK} called the **forward-breakover voltage, $V_{BR(F)}$**. This is indicated on the 4-layer diode characteristic curve in Figure 11–4.

▶ FIGURE 11–4

A 4-layer diode characteristic curve.



As V_{AK} is increased from 0, the anode current, I_A, gradually increases, as shown on the graph. As I_A increases, a point is reached where $I_A = I_S$, the switching current. At this point, $V_{AK} = V_{BR(F)}$, and the internal transistor structures become saturated. When this happens, the forward voltage drop, V_{AK}, suddenly decreases to a low value, and the 4-layer diode enters the *forward-conduction region* as indicated in Figure 11–4. Now, the device is in the *on* state and acts as a closed switch. When the anode current drops back below the holding value, I_H, the device turns off.

Holding Current Once the 4-layer diode is conducting (in the *on* state), it will continue to conduct until the anode current is reduced below a specified level, called the **holding current, I_H**. This parameter is also indicated on the characteristic curve in Figure 11–4. When I_A falls below I_H, the device rapidly switches back to the *off* state and enters the forward-blocking region.

Switching Current The value of the anode current at the point where the device switches from the forward-blocking region (off) to the forward-conduction region (on) is called the **switching current, I_S**. This value of current is always less than the holding current, I_H.

EXAMPLE 11–1 A certain 4-layer diode is biased in the forward-blocking region with an anode-to-cathode voltage of 20 V. Under this bias condition, the anode current is 1 μA. Determine the resistance of the diode in the forward-blocking region.

Solution The resistance is

$$R_{\text{AK}} = \frac{V_{\text{AK}}}{I_{\text{A}}} = \frac{20\ \text{V}}{1\ \mu\text{A}} = \mathbf{20\ M\Omega}$$

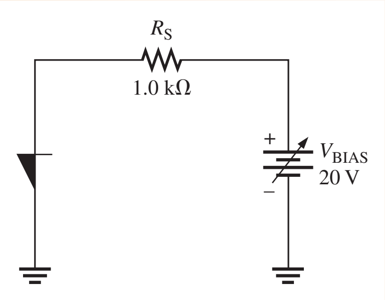
Related Problem[*] If the anode current is 2 μA and $V_{\text{AK}} = 20$ V, what is the 4-layer diode's resistance in the forward-blocking region?

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

EXAMPLE 11–2 Determine the value of anode current in Figure 11–5 when the device is on. $V_{\text{BR(F)}} =$ 10 V. Assume the forward voltage drop is 0.9 V.

▶ FIGURE 11–5



Solution The voltage at the anode, V_{A}, is 0.9. The voltage across R_{S} is

$$V_{R_{\text{S}}} = V_{\text{BIAS}} - V_{\text{A}} = 20\ \text{V} - 0.9\ \text{V} = 19.1\ \text{V}$$

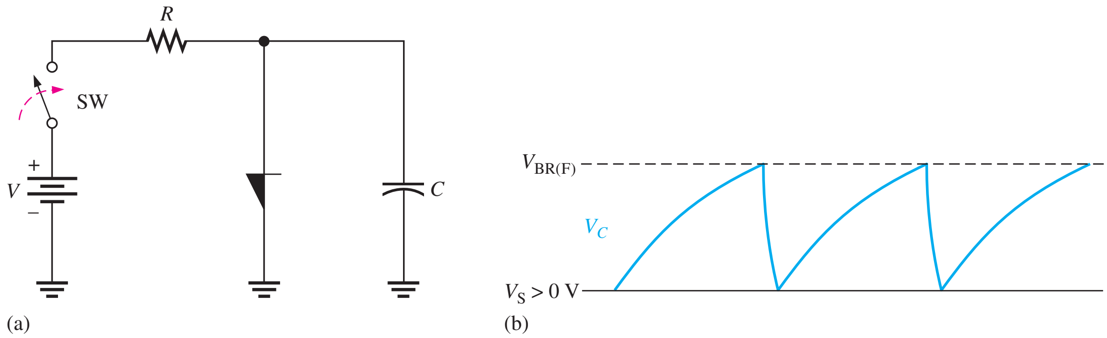
The anode current is

$$I_{\text{A}} = \frac{V_{R_{\text{S}}}}{R_{\text{S}}} = \frac{19.1\ \text{V}}{1.0\ \text{k}\Omega} = \mathbf{19.1\ mA}$$

Related Problem What is the resistance in the forward-conduction region of the 4-layer diode in Figure 11–5?

An Application

The circuit in Figure 11–6(a) is a **relaxation oscillator.** The operation is as follows. When the switch is closed, the capacitor charges through R until its voltage reaches the forward-breakover voltage of the 4-layer diode. At this point the diode switches into conduction, and the capacitor rapidly discharges through the diode. Discharging continues until the current through the diode falls below the holding value. At this point, the diode switches



▲ **FIGURE 11–6**

A 4-layer diode relaxation oscillator.

back to the *off* state, and the capacitor begins to charge again. The result of this action is a voltage waveform across *C* like that shown in Figure 11–6(b).

SECTION 11–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. Why is the 4-layer diode classified as a thyristor?
2. What is the forward-blocking region?
3. What happens when the anode-to-cathode voltage exceeds the forward-breakover voltage?
4. Once it is on, how can the 4-layer diode be turned off?

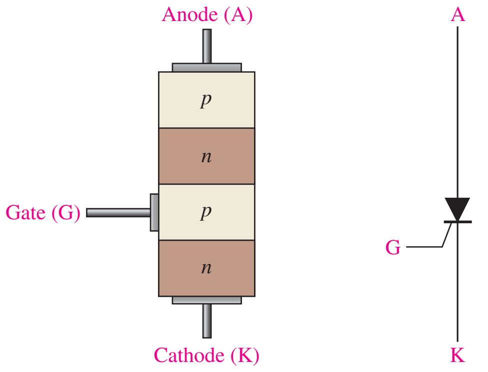
11–2 THE SILICON-CONTROLLED RECTIFIER (SCR)

Like the 4-layer diode, the SCR has two possible states of operation. In the *off* state, it acts ideally as an open circuit between the anode and the cathode; actually, rather than an open, there is a very high resistance. In the *on* state, the SCR acts ideally as a short from the anode to the cathode; actually, there is a small *on* (forward) resistance. The LASCR operates as an SCR except it is triggered by light.

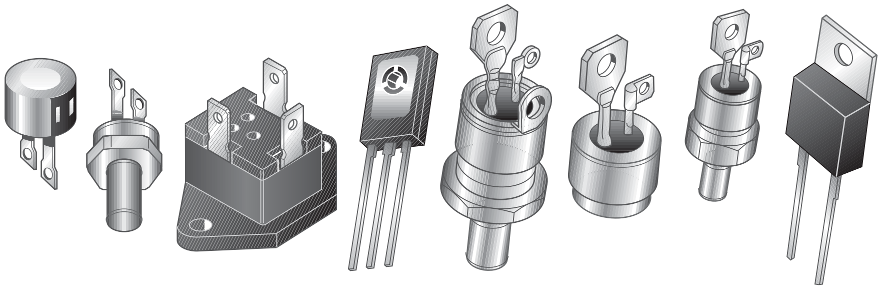
After completing this section, you should be able to

- ❑ **Describe the basic structure and operation of an SCR**
  - ◆ Identify the schematic symbol
- ❑ Draw the SCR equivalent circuit
- ❑ Explain how an SCR is turned on
  - ◆ Describe the characteristic curve
- ❑ Explain how an SCR is turned off
- ❑ Discuss and define SCR characteristics and ratings
- ❑ Describe the light-activated SCR and show a simple application

An **SCR** (silicon-controlled rectifier) is a 4-layer *pnpn* device similar to the 4-layer diode except with three terminals: anode, cathode, and gate. The basic structure of an SCR is shown in Figure 11–7(a), and the schematic symbol is shown in Figure 11–7(b). Typical SCR packages are shown in Figure 11–7(c). Other types of thyristors are found in the same or similar packages.



(a) Basic construction (b) Schematic symbol



(c) Typical packages

FIGURE 11–7

The silicon-controlled rectifier (SCR).

SCR Equivalent Circuit

Like the 4-layer diode operation, the SCR operation can best be understood by thinking of its internal *pnpn* structure as a two-transistor arrangement, as shown in Figure 11–8. This structure is like that of the 4-layer diode except for the gate connection. The upper *pnp* layers act as a transistor, Q_1, and the lower *npn* layers act as a transistor, Q_2. Again, notice that the two middle layers are "shared."

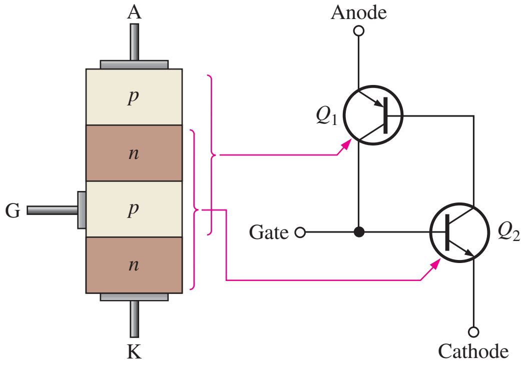
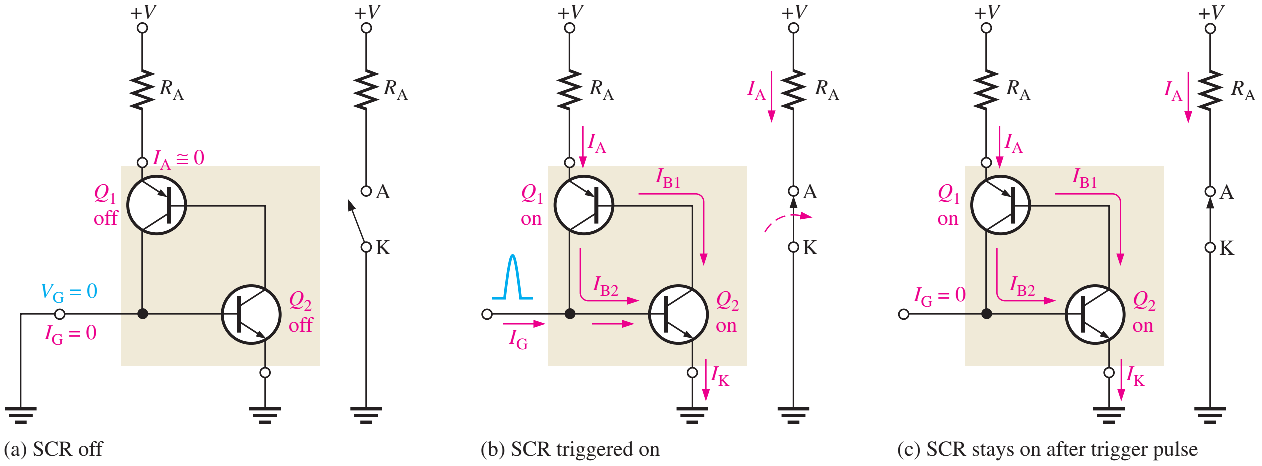


FIGURE 11–8

SCR equivalent circuit.

Turning the SCR On

When the gate current, I_G, is zero, as shown in Figure 11–9(a), the device acts as a 4-layer diode in the *off* state. In this state, the very high resistance between the anode and cathode can be approximated by an open switch, as indicated. When a positive pulse of current (**trigger**) is applied to the gate, both transistors turn on (the anode must be more positive than the cathode). This action is shown in Figure 11–9(b). I_{B2} turns on Q_2, providing a path for I_{B1} into the Q_2 collector, thus turning on Q_1. The collector current of Q_1 provides



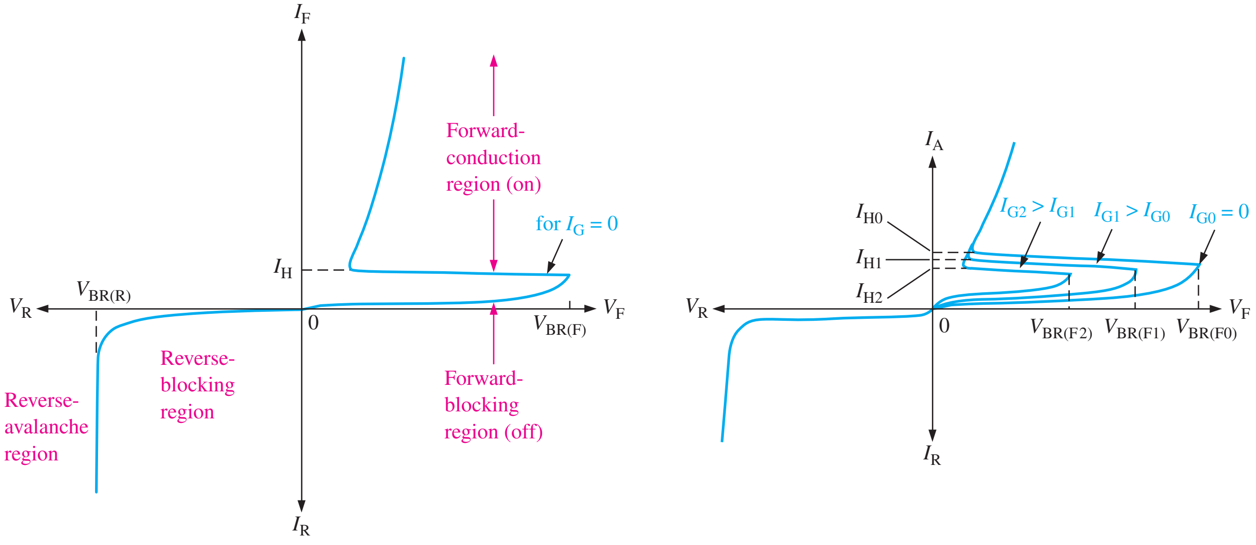
(a) SCR off
(b) SCR triggered on
(c) SCR stays on after trigger pulse

▲ **FIGURE 11–9**

The SCR turn-on process with the switch equivalents shown.

additional base current for Q_2 so that Q_2 stays in conduction after the trigger pulse is removed from the gate. By this regenerative action, Q_2 sustains the saturated conduction of Q_1 by providing a path for I_{B1}; in turn, Q_1 sustains the saturated conduction of Q_2 by providing I_{B2}. Thus, the device stays on (latches) once it is triggered on, as shown in Figure 11–9(c). In this state, the very low resistance between the anode and cathode can be approximated by a closed switch, as indicated.

Like the 4-layer diode, an SCR can also be turned on without gate triggering by increasing the anode-to-cathode voltage to a value exceeding the forward-breakover voltage $V_{BR(F)}$, as shown on the characteristic curve in Figure 11–10(a). The forward-breakover voltage decreases as I_G is increased above 0 V, as shown by the set of curves in Figure 11–10(b). Eventually, a value of I_G is reached at which the SCR turns on at a very low anode-to-cathode voltage. So, as you can see, the gate current controls the value of forward breakover voltage, $V_{BR(F)}$, required for turn-on.



(a) For $I_G = 0$
(b) For various I_G values

▲ **FIGURE 11–10**

SCR characteristic curves.

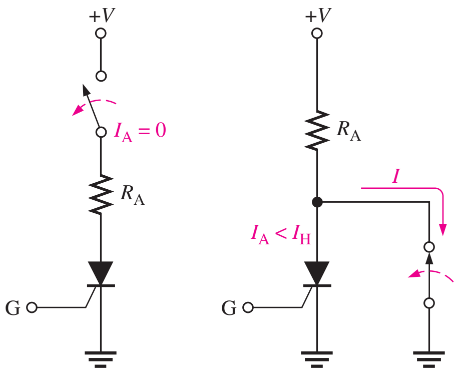
Although anode-to-cathode voltages in excess of $V_{BR(F)}$ will not damage the device if current is limited, this situation should be avoided because the normal control of the SCR is lost. It should normally be triggered on only with a pulse at the gate.

Turning the SCR Off

When the gate returns to 0 V after the trigger pulse is removed, the SCR cannot turn off; it stays in the forward-conduction region. The anode current must drop below the value of the holding current, I_H, in order for turn-off to occur. The holding current is indicated in Figure 11–10.

There are two basic methods for turning off an SCR: *anode current interruption* and *forced commutation.* The anode current can be interrupted by either a momentary series or parallel switching arrangement, as shown in Figure 11–11. The series switch in part (a) simply reduces the anode current to zero and causes the SCR to turn off. The parallel switch in part (b) routes part of the total current away from the SCR, thereby reducing the anode current to a value less than I_H.

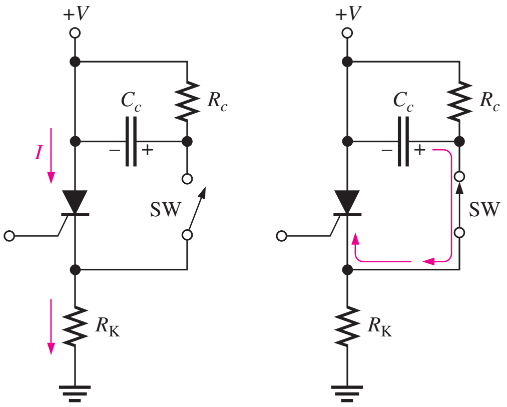
The **forced commutation** method basically requires momentarily forcing current through the SCR in the direction opposite to the forward conduction so that the net forward current is reduced below the holding value. The basic circuit, as shown in Figure 11–12, consists of a switch (normally a transistor switch) and a capacitor. While the SCR is conducting, the switch is open and C_c is charged to the supply voltage through R_c, as shown in part (a). To turn off the SCR, the switch is closed, placing the capacitor across the SCR and forcing current through it opposite to the forward current, as shown in part (b). Typically, turn-off times for SCRs range from a few microseconds up to about 30 μs.



(a) (b)

▲ FIGURE 11–11

SCR turn-off by anode current interruption.



(a) On (b) Off

▲ FIGURE 11–12

SCR turn-off by forced commutation.

SCR Characteristics and Ratings

Several of the most important SCR characteristics and ratings are defined as follows. Use the curve in Figure 11–10(a) for reference where appropriate.

Forward-breakover voltage, $V_{BR(F)}$ This is the voltage at which the SCR enters the forward-conduction region. The value of $V_{BR(F)}$ is maximum when $I_G = 0$ and is designated $V_{BR(F0)}$. When the gate current in increased, $V_{BR(F)}$ decreases and is designated $V_{BR(F1)}$, $V_{BR(F2)}$, and so on, for increasing steps in gate current (I_{G1}, I_{G2}, and so on).

Holding current, I_H This is the value of anode current below which the SCR switches from the forward-conduction region to the forward-blocking region. The value increases with decreasing values of I_G and is maximum for $I_G = 0$.

Gate trigger current, I_{GT} This is the value of gate current necessary to switch the SCR from the forward-blocking region to the forward-conduction region under specified conditions.

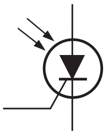
Average forward current, $I_{F(avg)}$ This is the maximum continuous anode current (dc) that the device can withstand in the conduction state under specified conditions.

Forward-conduction region This region corresponds to the *on* condition of the SCR where there is forward current from anode to cathode through the very low resistance (approximate short) of the SCR.

Forward-blocking and reverse-blocking regions These regions correspond to the *off* condition of the SCR where the forward current from anode to cathode is blocked by the effective open circuit of the SCR.

Reverse-breakdown voltage, $V_{BR(R)}$ This parameter specifies the value of reverse voltage from cathode to anode at which the device breaks into the avalanche region and begins to conduct heavily (the same as in a *pn* junction diode).

The Light-Activated SCR (LASCR)

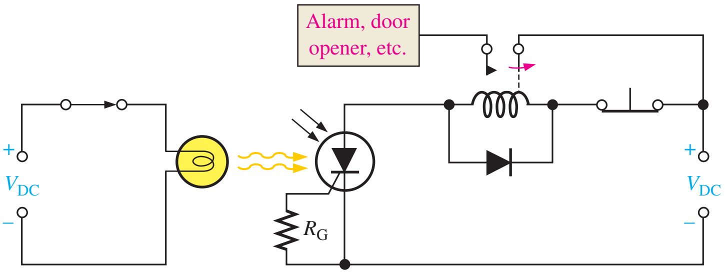


▲ FIGURE 11–13

LASCR symbol.

The light-activated silicon-controlled rectifier (**LASCR**) is a four-layer semiconductor device (thyristor) that operates essentially as does the conventional SCR except that it can also be light-triggered. The LASCR conducts current in one direction when activated by a sufficient amount of light and continues to conduct until the current falls below a specified value. Figure 11–13 shows a LASCR schematic symbol. The LASCR is most sensitive to light when the gate terminal is open. If necessary, a resistor from the gate to the cathode can be used to reduce the sensitivity.

Figure 11–14 shows a LASCR used to energize a latching relay. The input source turns on the lamp; the resulting incident light triggers the LASCR. The anode current energizes the relay and closes the contact. Notice that the input source is electrically isolated from the rest of the circuit.



▲ FIGURE 11–14

A LASCR circuit.

SECTION 11–2 CHECKUP

1. What is an SCR?
2. Name the SCR terminals.
3. How can an SCR be turned on (made to conduct)?
4. How can an SCR be turned off?
5. What is required in Figure 11–14 to turn off the LASCR and de-energize the relay?

11–3 SCR APPLICATIONS

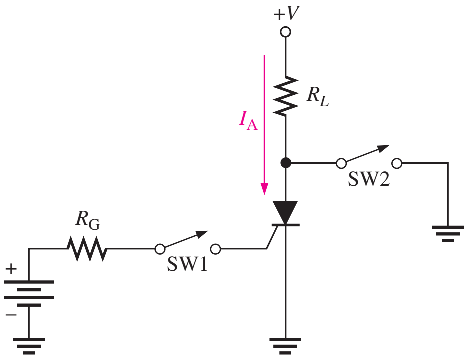
The SCR is used in many applications, including motor controls, time-delay circuits, heater controls, phase controls, relay controls, and sawtooth generators.

After completing this section, you should be able to

- ❑ **Discuss several SCR applications**
- ❑ Explain the operation of an on-off control current
- ❑ Describe half-wave power control
- ❑ Explain how a backup lighting circuit works
- ❑ Discuss an over-voltage protection circuit
- ❑ Explain the operation of a sawtooth generator

On-Off Control of Current

Figure 11–15 shows an SCR circuit that permits current to be switched to a load by the momentary closure of switch SW1 and removed from the load by the momentary closure of switch SW2.



◀ FIGURE 11–15

On-Off SCR control circuit.

Assuming the SCR is initially off, momentary closure of SW1 provides a pulse of current into the gate, thus triggering the SCR on so that it conducts current through R_L. The SCR remains in conduction even after the momentary contact of SW1 is removed if the anode current is equal to or greater than the holding current, I_H. When SW2 is momentarily closed, current is shunted around the SCR, thus reducing its anode current below the holding value, I_H. This turns the SCR off and reduces the load current to zero.

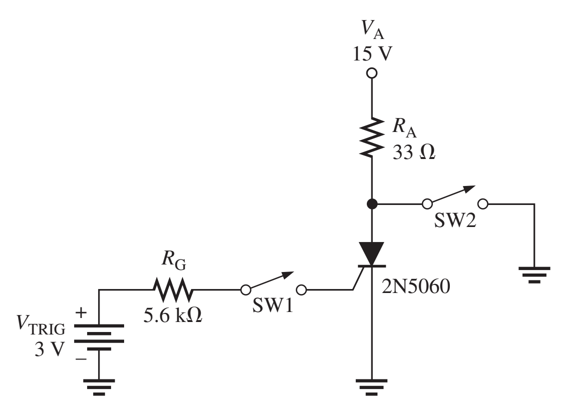
EXAMPLE 11–3 Determine the gate trigger current and the anode current when the switch, SW1, is momentarily closed in Figure 11–16. Assume $V_{AK} = 0.2\text{ V}$, $V_{GK} = 0.7\text{ V}$, and $I_H = 5\text{ mA}$.

Solution

$$I_G = \frac{V_{TRIG} - V_{GK}}{R_G} = \frac{3\text{ V} - 0.7\text{ V}}{5.6\text{ k}\Omega} = \mathbf{410\ \mu A}$$

$$I_A = \frac{V_A - V_{AK}}{R_A} = \frac{15\text{ V} - 0.2\text{ V}}{33\ \Omega} = \mathbf{448\text{ mA}}$$

▶ FIGURE 11–16



Related Problem Will the SCR turn on if V_A is reduced to 12 V? Explain.

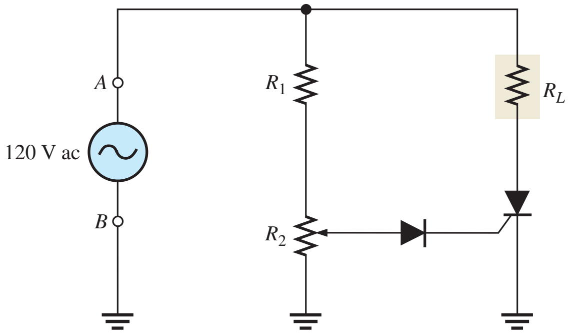
Open the Multisim file E11-03 in the Examples folder on the companion website. With SW2 open, momentarily close SW1. Compare the measured anode current with the calculated value. Notice that the anode current continues even after SW1 is opened. Close SW2 and observe the anode current. Explain your observation.

Half-Wave Power Control

A common application of SCRs is in the control of ac power for lamp dimmers, electric heaters, and electric motors. A half-wave, variable-resistance, phase-control circuit is shown in Figure 11–17; 120 V ac are applied across terminals *A* and *B*; R_L represents the resistance of the load (for example, a heating element or lamp filament). Resistor R_1 limits the current, and potentiometer R_2 sets the trigger level for the SCR.

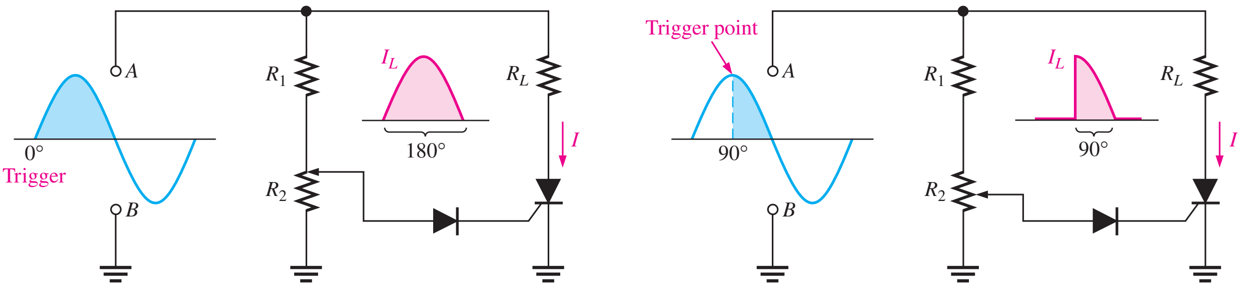
▶ FIGURE 11–17

Half-wave, variable-resistance, phase-control circuit.



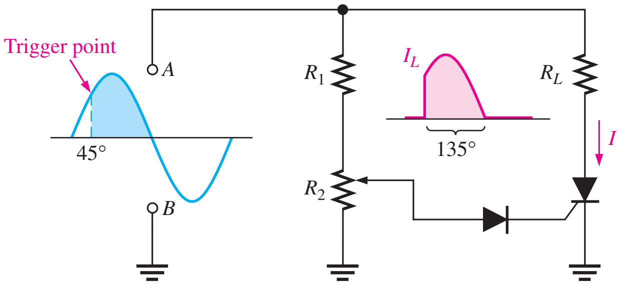
By adjusting R_2, the SCR can be made to trigger at any point on the positive half-cycle of the ac waveform between 0° and 90°, as shown in Figure 11–18.

When the SCR triggers near the beginning of the cycle (approximately 0°), as in Figure 11–18(a), it conducts for approximately 180° and maximum power is delivered to the load. When it triggers near the peak of the positive half-cycle (90°), as in Figure 11–18(b), the SCR conducts for approximately 90° and less power is delivered to the load. By adjusting R_2, triggering can be made to occur anywhere between these two extremes, and therefore, a variable amount of power can be delivered to the load. Figure 11–18(c) shows triggering at the 45° point as an example. When the ac input goes negative, the SCR turns off and does not conduct again until the trigger point on the next positive half-cycle. The diode prevents the negative ac voltage from being applied to the gate of the SCR.


0°
Trigger
A
B
R_1
R_2
I_L
180°
R_L
I
Trigger point
A
B
90°
R_1
R_2
I_L
90°
R_L
I

(a) 180° conduction

(b) 90° conduction


Trigger point
A
B
45°
R_1
R_2
I_L
135°
R_L
I

(c) 135° conduction

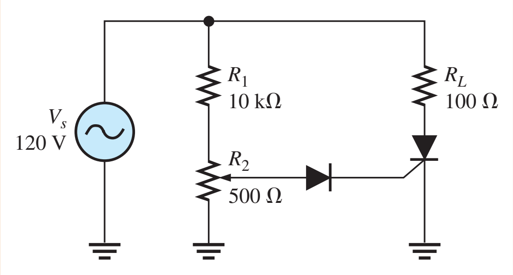
▲ **FIGURE 11–18**

Operation of the phase-control circuit.

EXAMPLE 11–4

Show the voltage waveform across the SCR in Figure 11–19 from anode to cathode (ground) in relation to the load current for 180°, 45°, and 90° conduction. Assume an ideal SCR.

▶ **FIGURE 11–19**

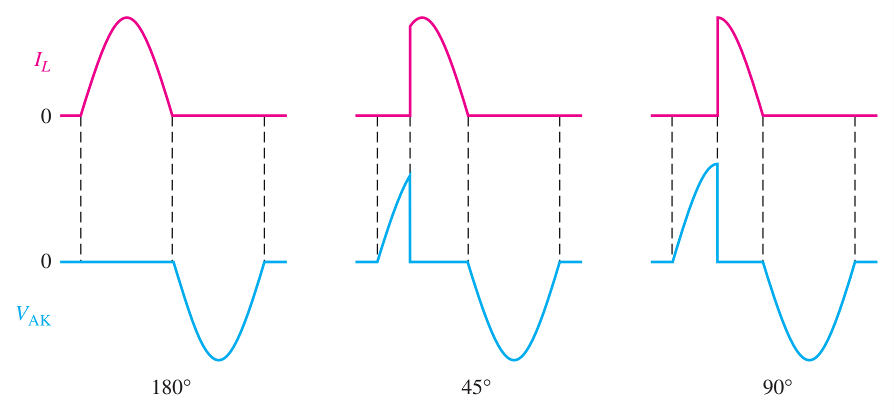

R_1
10 kΩ
R_L
100 Ω
V_s
120 V
R_2
500 Ω

Solution When there is load current, the SCR is conducting and the voltage across it is ideally zero. When there is no load current, the voltage across the SCR is the same as the applied voltage. The waveforms are shown in Figure 11–20.

Related Problem What is the voltage across the SCR if it is never triggered?

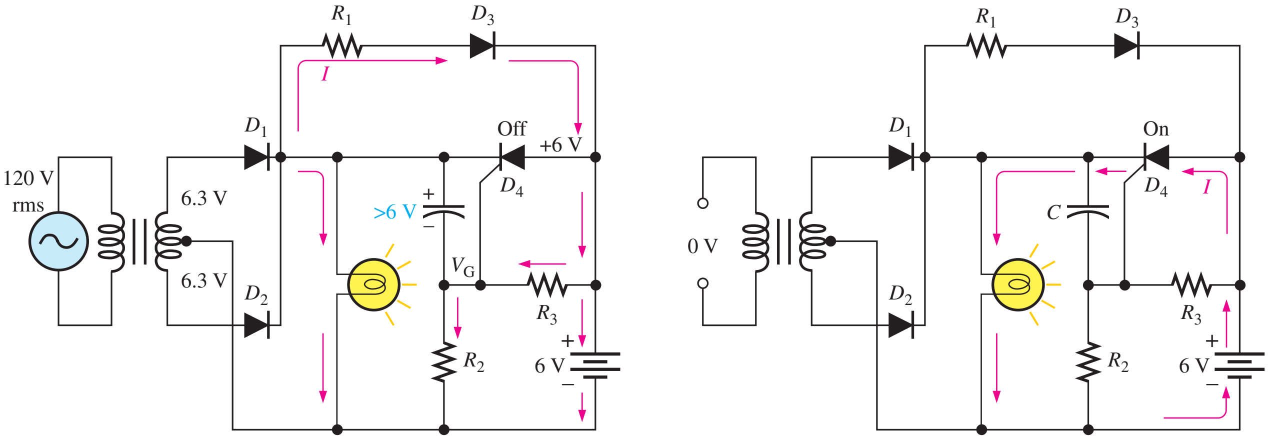
Open the Multisim file E11-04 in the Examples folder on the companion website. View the voltage across the SCR with the oscilloscope. Vary the potentiometer setting and observe how V_{AK} changes.

▶ FIGURE 11–20



Backup Lighting for Power Interruptions

As another example of SCR applications, let's examine a circuit that will maintain lighting by using a backup battery when there is an ac power failure. Figure 11–21 shows a center-tapped full-wave rectifier used for providing ac power to a low-voltage lamp. As long as the ac power is available, the battery charges through diode D_3 and R_1.



(a) ac power on

(b) Backup battery power (ac power off)

▲ FIGURE 11–21

Automatic backup lighting circuit.

The SCR's cathode voltage is established when the capacitor charges to the peak value of the full-wave rectified ac (6.3 V rms less the drops across R_2 and D_1). The anode is at the 6 V battery voltage, making it less positive than the cathode, thus preventing conduction. The SCR's gate is at a voltage established by the voltage divider made up of R_2 and R_3. Under these conditions the lamp is illuminated by the ac input power and the SCR is off, as shown in Figure 11–21(a).

When there is an interruption of ac power, the capacitor discharges through the closed path R_1, D_3, and R_3, making the cathode less positive than the anode or the gate. This action establishes a triggering condition, and the SCR begins to conduct. Current from the battery is through the SCR and the lamp, thus maintaining illumination, as shown in Figure 11–21(b). When ac power is restored, the capacitor recharges and the SCR turns off. The battery begins recharging.

An Over-Voltage Protection Circuit

Figure 11–22 shows a simple over-voltage protection circuit, sometimes called a "crowbar" circuit, in a dc power supply. The dc output voltage from the regulator is monitored by the zener diode (D_1) and the resistive voltage divider (R_1 and R_2). The upper limit of the output voltage is set by the zener voltage. If this voltage is exceeded, the zener conducts and the voltage divider produces an SCR trigger voltage. The trigger voltage turns on the SCR, which is connected across the line voltage. The SCR current causes the fuse to blow, thus disconnecting the line voltage from the power supply.

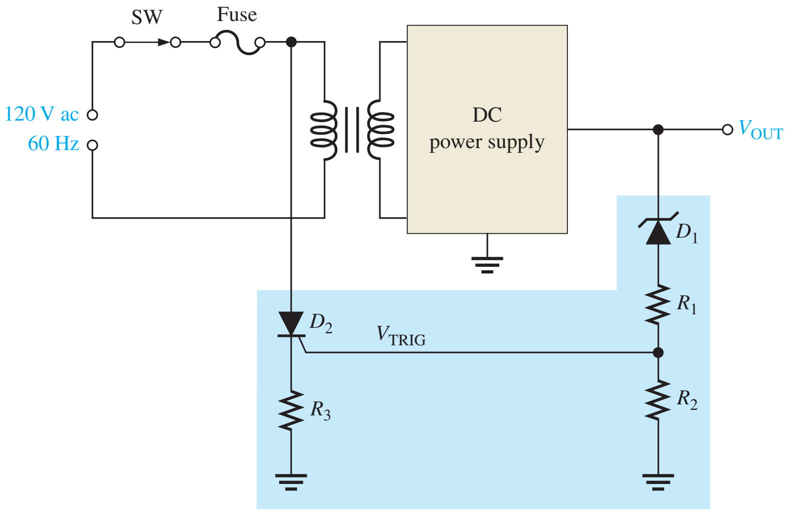


FIGURE 11–22

A basic SCR over-voltage protection circuit (shown in blue).

Sawtooth Generator

The SCR can be used in conjunction with an RC circuit to produce a repetitive sawtooth waveform. The circuit is shown in Figure 11–23. The time constant is set by R_1 and C_1, and the voltage at which the SCR triggers on is determined by the variable voltage-divider formed by R_2 and R_3. When the switch is closed, the capacitor begins charging and turns on the SCR. When the SCR turns on, the capacitor quickly discharges through it; the anode current then decreases below the holding value, causing the SCR to turn off. As soon as the SCR is off, the capacitor starts charging again and the cycle is repeated. By adjusting the potentiometer, the frequency of the sawtooth waveform can be changed.

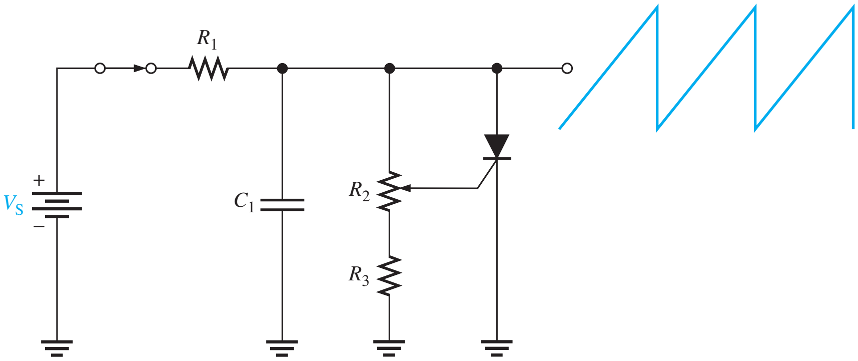


FIGURE 11–23

SECTION 11–3 CHECKUP

1. If the potentiometer in Figure 11–18 is set at its midpoint, during what part of the input cycle will the SCR conduct?
2. In Figure 11–21, what is the purpose of diode D_3?

11–4 THE DIAC AND TRIAC

Both the diac and the triac are types of thyristors that can conduct current in both directions (bilateral). The difference between the two devices is that a diac has two terminals, while a triac has a third terminal, which is the gate for triggering. The diac functions basically like two parallel 4-layer diodes turned in opposite directions. The triac functions basically like two parallel SCRs turned in opposite directions with a common gate terminal.

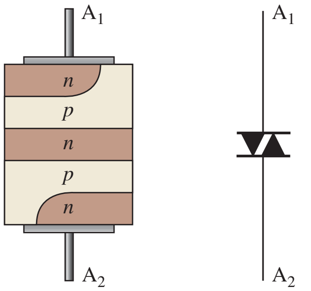
After completing this section, you should be able to

- **Describe the basic structure and operation of the diac and triac**
- Explain the operation of the diac
  - Identify the schematic symbol
  - Describe the characteristic curve
  - Discuss the equivalent circuit
- Explain the operation of the triac
  - Identify the schematic symbol
  - Describe the characteristic curve
  - Discuss the equivalent circuit
- Describe an application of the triac

The Diac

A **diac** is a two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction when activated. The basic construction and schematic symbol for a diac are shown in Figure 11–24. Notice that there are two terminals, labelled A_1 and A_2. The top and bottom layers contain both *n* and *p* materials. The right side of the stack can be regarded as a *pnpn* structure with the same characteristics as a four-layer diode, while the left side is an inverted four-layer diode having an *npnp* structure.

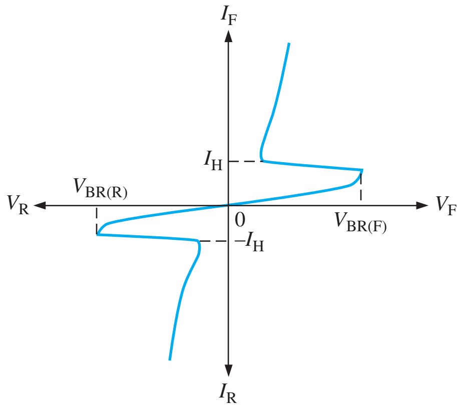
Conduction occurs in a diac when the breakover voltage is reached with either polarity across the two terminals. The curve in Figure 11–25 illustrates this characteristic. Once breakover occurs, current is in a direction depending on the polarity of the voltage across the terminals. The device turns off when the current drops below the holding value.



(a) Basic construction (b) Symbol

▲ FIGURE 11–24

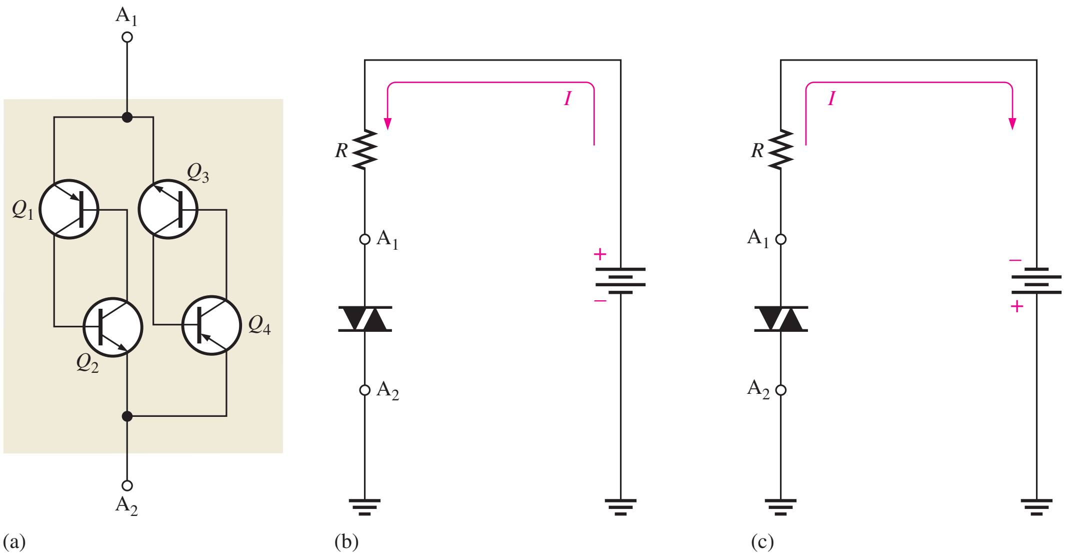
The diac.



▲ FIGURE 11–25

Diac characteristic curve.

The equivalent circuit of a diac consists of four transistors arranged as shown in Figure 11–26(a). When the diac is biased as in Figure 11–26(b), the *pnpn* structure from A_1 to A_2 provides the same operation as was described for the 4-layer diode. In the equivalent circuit, Q_1 and Q_2 are forward-biased, and Q_3 and Q_4 are reverse-biased. The device operates on the upper right portion of the characteristic curve in Figure 11–25 under this bias



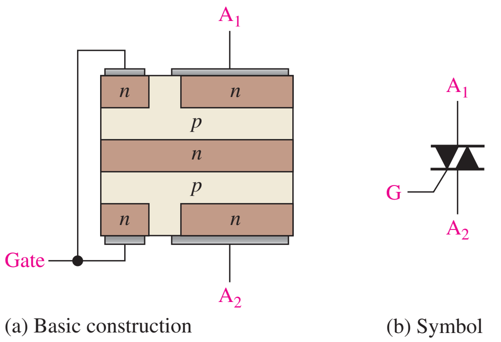
▲ FIGURE 11–26

Diac equivalent circuit and bias conditions.

condition. When the diac is biased as shown in Figure 11–26(c), the *pnpn* structure from A_2 and A_1 is used. In the equivalent circuit, Q_3 and Q_4 are forward-biased, and Q_1 and Q_2 are reverse-biased. Under this bias condition, the device operates on the lower left portion of the characteristic curve, as shown in Figure 11–25.

The Triac

A **triac** is like a diac with a gate terminal. A triac can be turned on by a pulse of gate current and does not require the breakover voltage to initiate conduction, as does the diac. Basically, a triac can be thought of simply as two SCRs connected in parallel and in opposite directions with a common gate terminal. Unlike the SCR, the triac can conduct current in either direction when it is triggered on, depending on the polarity of the voltage across its A_1 and A_2 terminals. Figure 11–27 shows the basic construction and schematic symbol for a triac.



(a) Basic construction

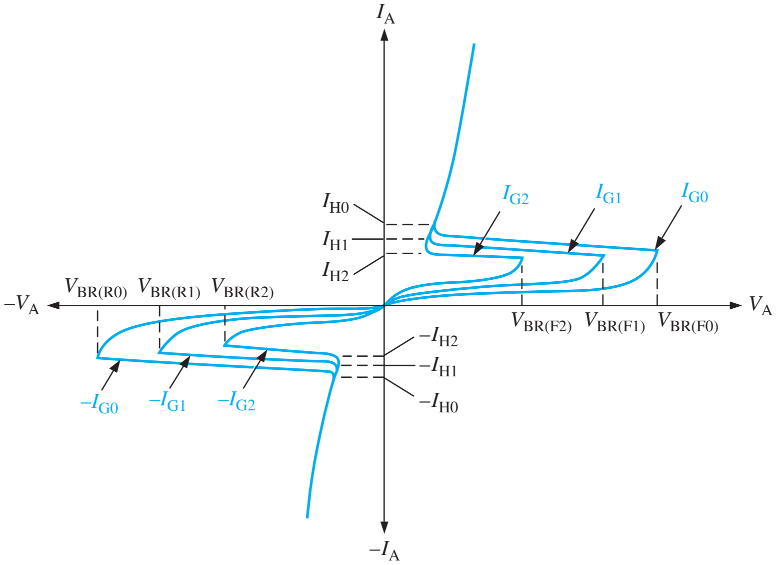
(b) Symbol

◀ FIGURE 11–27

The triac.

The characteristic curve is shown in Figure 11–28. Notice that the breakover potential decreases as the gate current increases, just as with the SCR. As with other thyristors, the triac ceases to conduct when the anode current drops below the specified value of the holding current, I_H. The only way to turn off the triac is to reduce the current to a sufficiently low level.

Figure 11–29 shows the triac being triggered into both directions of conduction. In part (a), terminal A_1 is biased positive with respect to A_2, so the triac conducts as shown when

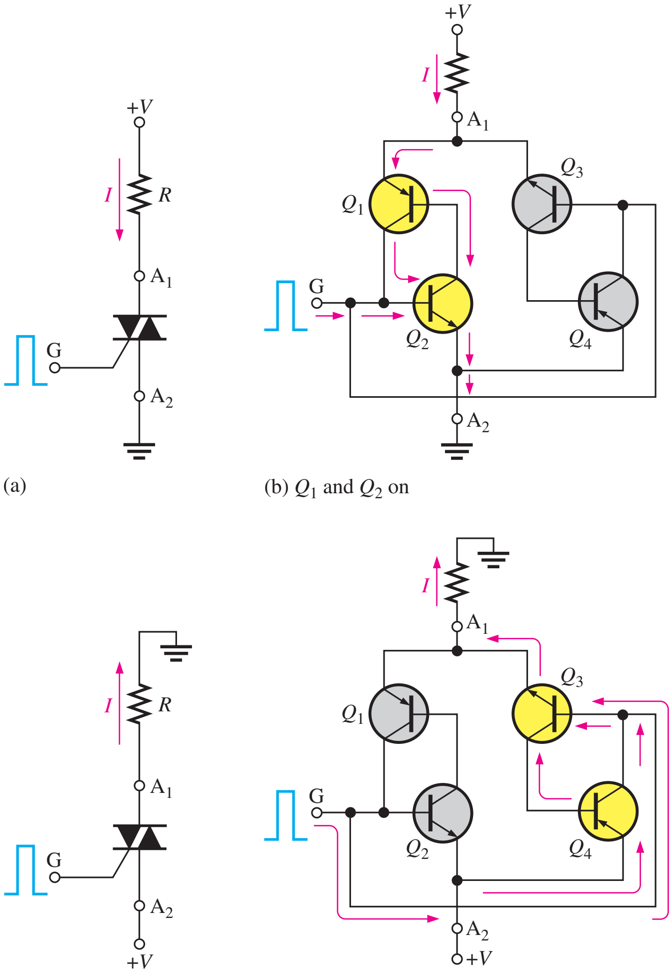


▲ **FIGURE 11–28**

Triac characteristic curves.

▶ **FIGURE 11–29**

Bilateral operation of a triac.


+V
I
R
A1
G
A2
Q1
Q2
Q3
Q4
+V

(a) (b) Q_1 and Q_2 on

(c) (d) Q_3 and Q_4 on

triggered by a positive pulse at the gate terminal. The transistor equivalent circuit in part (b) shows that Q_1 and Q_2 conduct when a positive trigger pulse is applied. In part (c), terminal A_2 is biased positive with respect to A_1, so the triac conducts as shown. In this case, Q_3 and Q_4 conduct as indicated in part (d) upon application of a positive trigger pulse.

Applications

Like the SCR, triacs are also used to control average power to a load by the method of phase control. The triac can be triggered such that the ac power is supplied to the load for a controlled portion of each half-cycle. During each positive half-cycle of the ac, the triac is off for a certain interval, called the *delay angle* (measured in degrees), and then it is triggered on and conducts current through the load for the remaining portion of the positive half-cycle, called the *conduction angle.* Similar action occurs on the negative half-cycle except that, of course, current is conducted in the opposite direction through the load. Figure 11–30 illustrates this action.

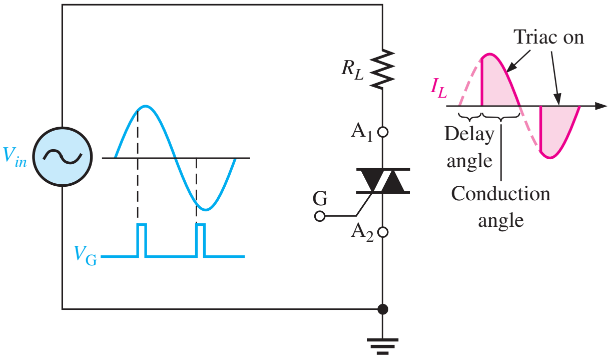
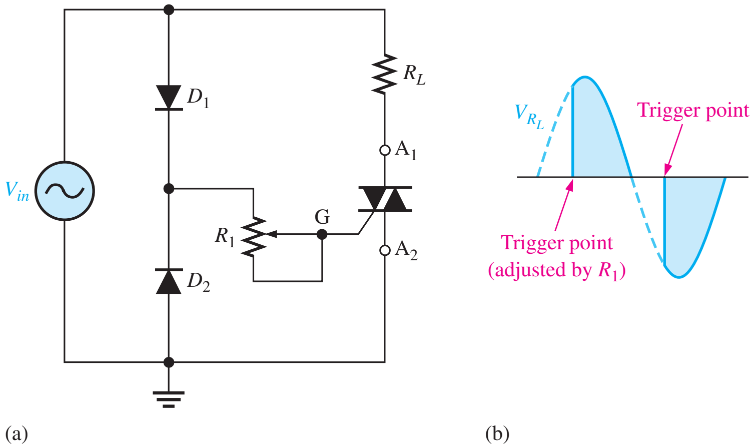


FIGURE 11–30

Basic triac phase control.

One example of phase control using a triac is illustrated in Figure 11–31(a). Diodes are used to provide trigger pulses to the gate of the triac. Diode D_1 conducts during the positive half-cycle. The value of R_1 sets the point on the positive half-cycle at which the triac triggers. Notice that during this portion of the ac cycle, A_1 and G are positive with respect to A_2.



(a) (b)

FIGURE 11–31

Triac phase-control circuit.

Diode D_2 conducts during the negative half-cycle, and R_1 sets the trigger point. Notice that during this portion of the ac cycle, A_2 and G are positive with respect to A_1. The resulting waveform across R_L is shown in Figure 11–31(b).

In the phase-control circuit, it is necessary that the triac turn off at the end of each positive and each negative alternation of the ac. Figure 11–32 illustrates that there is an interval near each 0 crossing where the triac current drops below the holding value, thus turning the device off.

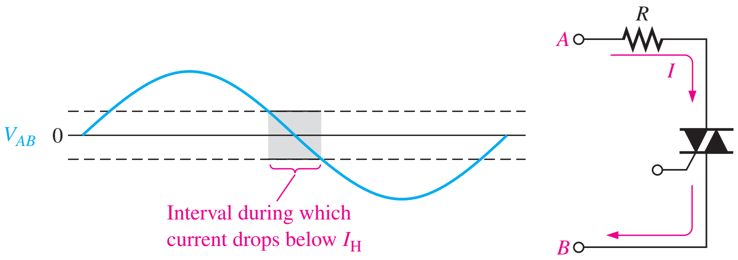


FIGURE 11–32

Triac turn-off interval.

SECTION 11–4 CHECKUP

1. Compare the diac to the 4-layer diode in terms of basic operation.
2. Compare the triac with the SCR in terms of basic operation.
3. How does a triac differ from a diac?

11–5 The Silicon-Controlled Switch (SCS)

The silicon-controlled switch (SCS) is similar in construction to the SCR. The SCS, however, has two gate terminals, the cathode gate and the anode gate. The SCS can be turned on and off using either gate terminal. Remember that the SCR can be only turned on using its gate terminal. Normally, the SCS is available in power ratings lower than those of the SCR.

After completing this section, you should be able to

- **Describe a silicon-controlled switch (SCS)**
- Explain the basic operation
    - Identify the schematic symbol
    - Discuss the equivalent circuit
- Discuss SCS applications

Basic Operation

An **SCS** (silicon-controlled switch) is a four-terminal thyristor that has two gate terminals that are used to trigger the device on and off. The symbol and terminal identification for an SCS are shown in Figure 11–33.

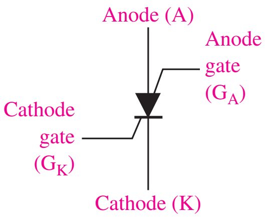


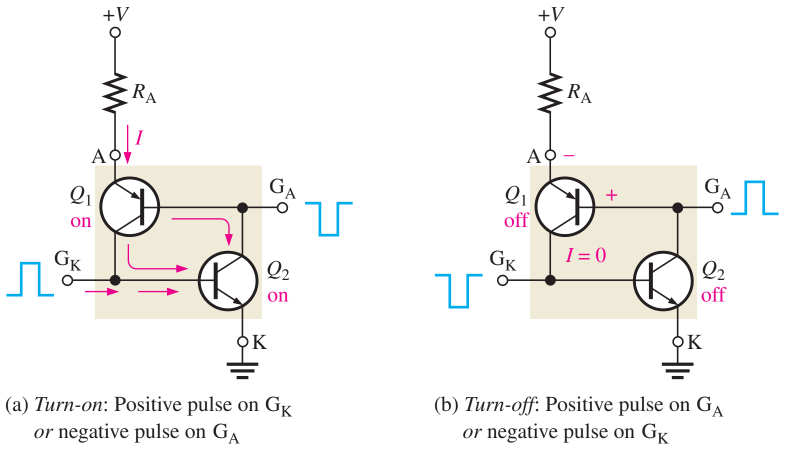
FIGURE 11–33

The silicon-controlled switch (SCS).

As with the previous thyristors, the basic operation of the SCS can be understood by referring to the transistor equivalent, shown in Figure 11–34. To start, assume that both Q_1 and Q_2 are off, and therefore that the SCS is not conducting. A positive pulse on the cathode gate drives Q_2 into conduction and thus provides a path for Q_1 base current. When Q_1 turns on, its collector current provides base current for Q_2, thus sustaining the *on* state of the device. This regenerative action is the same as in the turn-on process of the SCR and the 4-layer diode and is illustrated in Figure 11–34(a).

The SCS can also be turned on with a negative pulse on the anode gate, as indicated in Figure 11–34(a). This drives Q_1 into conduction which, in turn, provides base current for Q_2. Once Q_2 is on, it provides a path for Q_1 base current, thus sustaining the *on* state.

To turn the SCS off, a positive pulse is applied to the anode gate. This reverse-biases the base-emitter junction of Q_1 and turns it off. Q_2, in turn, cuts off and the SCS ceases conduction, as shown in Figure 11–34(b). The device can also be turned off with a negative pulse on the cathode gate, as indicated in part (b). The SCS typically has a faster turn-off time than the SCR.



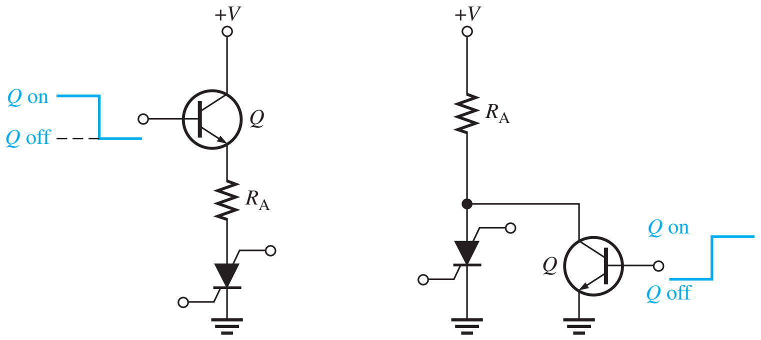
(a) *Turn-on*: Positive pulse on G_K *or* negative pulse on G_A

(b) *Turn-off*: Positive pulse on G_A *or* negative pulse on G_K

FIGURE 11–34

SCS operation.

In addition to the positive pulse on the anode gate or the negative pulse on the cathode gate, there is another method for turning off an SCS. Figure 11–35(a) and (b) shows two switching methods to reduce the anode current below the holding value. In each case, the bipolar junction transistor (BJT) acts as a switch to interrupt the anode current.



(a) Series switch turns off SCS

(b) Shunt switch turns off SCS

FIGURE 11–35

The transistor switch in both series and shunt configurations reduces the anode current below the holding current and turns off the SCS.

Applications

The SCS and SCR are used in similar applications. The SCS has the advantage of faster turn-off with pulses on either gate terminal; however, it is more limited in terms of maximum current and voltage ratings. Also, the SCS is sometimes used in digital applications such as counters, registers, and timing circuits.

SECTION 11–5 CHECKUP

1. Explain the difference between an SCS and an SCR.
2. How can an SCS be turned on?
3. Describe three ways an SCS can be turned off.

11–6 THE UNIJUNCTION TRANSISTOR (UJT)

The unijunction transistor does not belong to the thyristor family because it does not have a four-layer type of construction. The term *unijunction* refers to the fact that the UJT has a single *pn* junction. The UJT is useful in certain oscillator applications and as a triggering device in thyristor circuits.

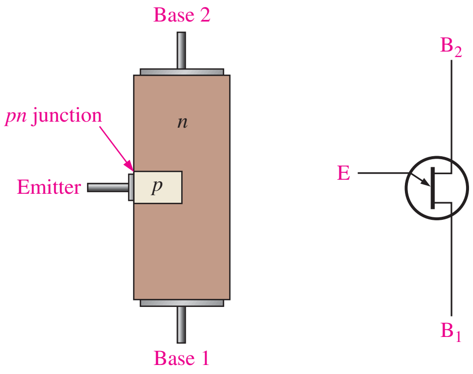
After completing this section, you should be able to

- ❑ **Describe the basic structure and operation of the unijunction transistor**
  - ◆ Identify the schematic symbol
- ❑ Use the equivalent circuit to describe the basic operation
- ❑ Define and discuss the *standoff ratio*
- ❑ Discuss a UJT application

The **UJT** (unijunction transistor) is a three-terminal device whose basic construction is shown in Figure 11–36(a). The schematic symbol appears in Figure 11–36(b). Notice the terminals are labelled Emitter (E), Base 1 (B_1), and Base 2 (B_2). Do not confuse this symbol with that of a JFET; the difference is that the arrow is at an angle for the UJT. The UJT has only one *pn* junction, and therefore, the characteristics of this device are different from those of either the BJT or the FET, as you will see.

▶ **FIGURE 11–36**

The unijunction transistor (UJT).



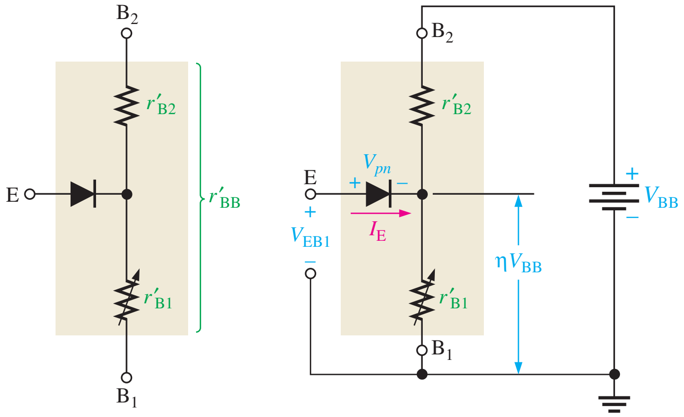
(a) Basic construction (b) Symbol

Equivalent Circuit

The equivalent circuit for the UJT, shown in Figure 11–37(a), will aid in understanding the basic operation. The diode shown in the figure represents the *pn* junction, r'_{B1} represents the internal dynamic resistance of the silicon bar between the emitter and base 1,

▶ **FIGURE 11–37**

UJT equivalent circuit.



(a) (b)

and r'_{B2} represents the dynamic resistance between the emitter and base 2. The total resistance between the base terminals is the sum of r'_{B1} and r'_{B2} and is called the *interbase resistance,* r'_{BB}.

$$r'_{BB} = r'_{B1} + r'_{B2}$$

The value of r'_{B1} varies inversely with emitter current I_E, and therefore, it is shown as a variable resistor. Depending on I_E, the value of r'_{B1} can vary from several thousand ohms down to tens of ohms. The internal resistances r'_{B1} and r'_{B2} form a voltage divider when the device is biased, as shown in Figure 11–37(b). The voltage across the resistance r'_{B1} can be expressed as

$$V_{r'_{B1}} = \left(\frac{r'_{B1}}{r'_{BB}}\right)V_{BB}$$

Standoff Ratio

The ratio r'_{B1}/r'_{BB} is a UJT characteristic called the intrinsic **standoff ratio** and is designated by η (Greek *eta*).

$$\boldsymbol{\eta = \frac{r'_{B1}}{r'_{BB}}}$$

Equation 11–1

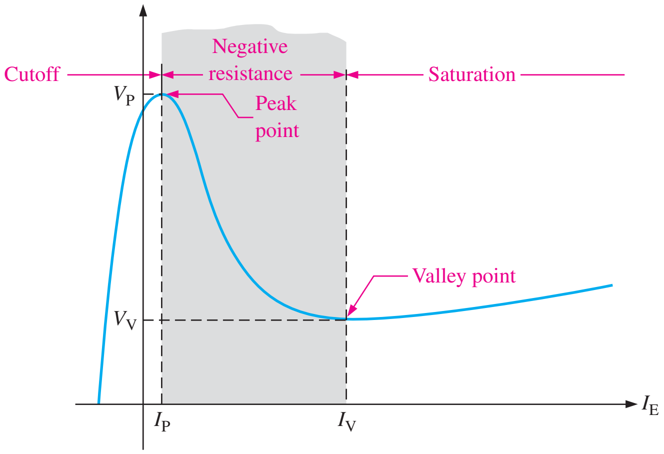
As long as the applied emitter voltage V_{EB1} is less than $V_{r'_{B1}} + V_{pn}$, there is no emitter current because the *pn* junction is not forward-biased (V_{pn} is the barrier potential of the *pn* junction). The value of emitter voltage that causes the *pn* junction to become forward-biased is called V_P (peak-point voltage) and is expressed as

$$\boldsymbol{V_P = \eta V_{BB} + V_{pn}}$$

Equation 11–2

When V_{EB1} reaches V_P, the *pn* junction becomes forward-biased and I_E begins. Holes are injected into the *n*-type bar from the *p*-type emitter. This increase in holes causes an increase in free electrons, thus increasing the conductivity between emitter and B_1 (decreasing r'_{B1}).

After turn-on, the UJT operates in a negative resistance region up to a certain value of I_E, as shown by the characteristic curve in Figure 11–38. As you can see, after the peak point ($V_E = V_P$ and $I_E = I_P$), V_E decreases as I_E continues to increase, thus producing the negative resistance characteristic. Beyond the valley point ($V_E = V_V$ and $I_E = I_V$), the device is in saturation, and V_E increases very little with an increasing I_E.



▲ FIGURE 11–38

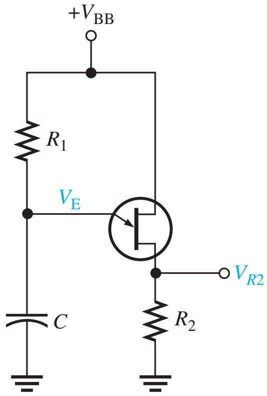
UJT characteristic curve for a fixed value of V_{BB}.

EXAMPLE 11–5 The datasheet of a certain UJT gives $\eta = 0.6$. Determine the peak-point emitter voltage V_P if $V_{BB} = 20\text{ V}$.

Solution

$$V_P = \eta V_{BB} + V_{pn} = 0.6(20\text{ V}) + 0.7\text{ V} = \mathbf{12.7\text{ V}}$$

Related Problem How can the peak-point emitter voltage of a UJT be increased?



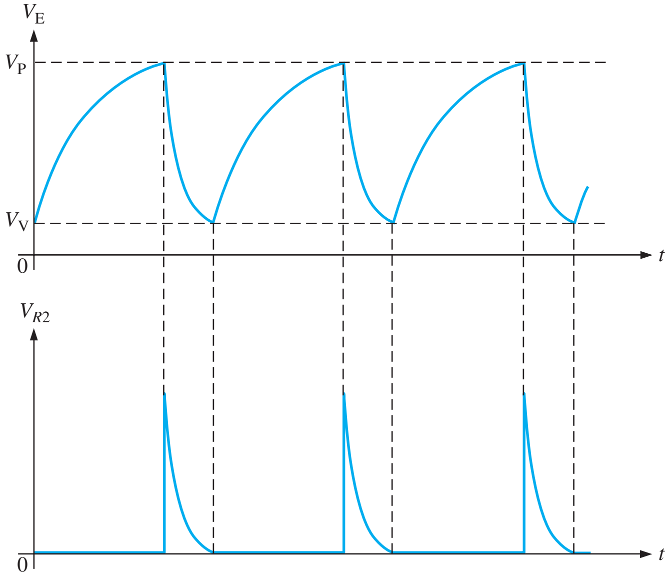
▲ FIGURE 11–39

Relaxation oscillator.

A UJT Application

The UJT can be used as a trigger device for SCRs and triacs. Other applications include nonsinusoidal oscillators, sawtooth generators, phase control, and timing circuits. Figure 11–39 shows a UJT relaxation oscillator as an example of one application.

The operation is as follows. When dc power is applied, the capacitor C charges exponentially through R_1 until it reaches the peak-point voltage V_P. At this point, the *pn* junction becomes forward-biased, and the emitter characteristic goes into the negative resistance region (V_E decreases and I_E increases). The capacitor then quickly discharges through the forward-biased junction, r'_B, and R_2. When the capacitor voltage decreases to the valley-point voltage V_V, the UJT turns off, the capacitor begins to charge again, and the cycle is repeated, as shown in the emitter voltage waveform in Figure 11–40 (top). During the discharge time of the capacitor, the UJT is conducting. Therefore, a voltage is developed across R_2, as shown in the waveform diagram in Figure 11–40 (bottom).



▲ FIGURE 11–40

Waveforms for UJT relaxation oscillator.

Conditions for Turn-On and Turn-Off In the relaxation oscillator of Figure 11–39, certain conditions must be met for the UJT to reliably turn on and turn off. First, to ensure turn-on, R_1 must not limit I_E at the peak point to less than I_P. To ensure this, the voltage drop across R_1 at the peak point should be greater than I_PR_1. Thus, the condition for turn-on is

$$V_{BB} - V_P > I_PR_1$$

or

$$R_1 < \frac{V_{BB} - V_P}{I_P}$$

To ensure turn-off of the UJT at the valley point, R_1 must be large enough that I_E (at the valley point) can decrease below the specified value of I_V. This means that the voltage across R_1 at the valley point must be less than $I_V R_1$. Thus, the condition for turn-off is

$$V_{BB} - V_V < I_V R_1$$

or

$$R_1 > \frac{V_{BB} - V_V}{I_V}$$

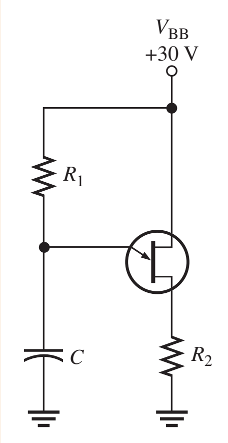
Therefore, for a proper turn-on and turn-off, R_1 must be in the range

$$\frac{V_{BB} - V_P}{I_P} > R_1 > \frac{V_{BB} - V_V}{I_V}$$

EXAMPLE 11–6

Determine a value of R_1 in Figure 11–41 that will ensure proper turn-on and turn-off of the UJT. The characteristic of the UJT exhibits the following values: $\eta = 0.5$, $V_V = 1\text{ V}$, $I_V = 10\text{ mA}$, $I_P = 20\ \mu\text{A}$, and $V_P = 14\text{ V}$.

► FIGURE 11–41



Solution

$$\frac{V_{BB} - V_P}{I_P} > R_1 > \frac{V_{BB} - V_V}{I_V}$$

$$\frac{30\text{ V} - 14\text{ V}}{20\ \mu\text{A}} > R_1 > \frac{30\text{ V} - 1\text{ V}}{10\text{ mA}}$$

$$\mathbf{800\ k\Omega} > R_1 > \mathbf{2.9\ k\Omega}$$

As you can see, R_1 has quite a wide range of possible values that will work.

Related Problem

Determine a value of R_1 in Figure 11–41 that will ensure proper turn-on and turn-off for the following values: $\eta = 0.33$, $V_V = 0.8\text{ V}$, $I_V = 15\text{ mA}$, $I_P = 35\ \mu\text{A}$, and $V_P = 18\text{ V}$.

SECTION 11–6 CHECKUP

1. Name the UJT terminals.
2. What is the intrinsic standoff ratio?
3. In a basic UJT relaxation oscillator such as in Figure 11–39, what three factors determine the period of oscillation?

11–7 THE PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT)

The programmable unijunction transistor (PUT) is actually a type of thyristor and not like the UJT at all in terms of structure. The only similarity to a UJT is that the PUT can be used in some oscillator applications to replace the UJT. The PUT is similar to an SCR except that its anode-to-gate voltage can be used to both turn on and turn off the device.

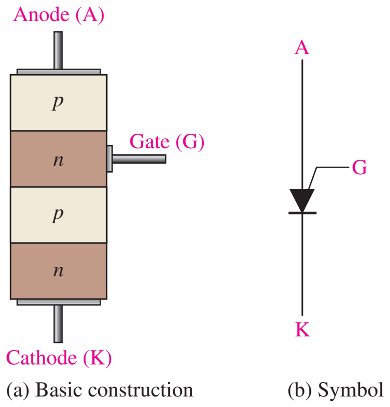
After completing this section, you should be able to

- **Describe the basic structure and operation of the programmable UJT**
  - Identify the schematic symbol
  - Describe how a PUT differs from an SCR
  - Compare a PUT and a UJT
- Explain how to set the trigger voltage
- Discuss a PUT application

A **PUT** (programmable unijunction transistor) is a type of three-terminal thyristor that is triggered into conduction when the voltage at the anode exceeds the voltage at the gate. The structure of the PUT is more similar to that of an SCR (four-layer) than to a UJT. The exception is that the gate is brought out as shown in Figure 11–42. Notice that the gate is connected to the *n* region adjacent to the anode. This *pn* junction controls the *on* and *off* states of the device. The gate is always biased positive with respect to the cathode. When the anode voltage exceeds the gate voltage by approximately 0.7 V, the *pn* junction is forward-biased and the PUT turns on. The PUT stays on until the anode voltage falls back below this level, then the PUT turns off.

FIGURE 11–42

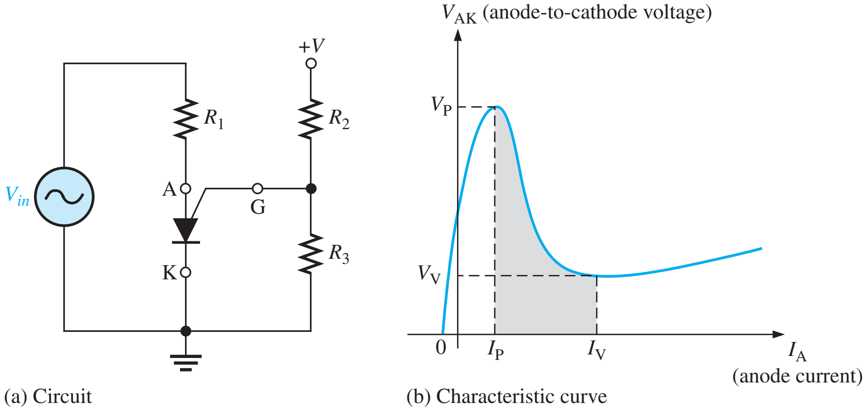
The programmable unijunction transistor (PUT).



(a) Basic construction (b) Symbol

Setting the Trigger Voltage

The gate can be biased to a desired voltage with an external voltage divider, as shown in Figure 11–43(a), so that when the anode voltage exceeds this "programmed" level, the PUT turns on.


V_{AK} (anode-to-cathode voltage)
+V
R_1
R_2
R_3
V_{in}
A
G
K
V_P
V_V
0
I_P
I_V
I_A
(anode current)

(a) Circuit

(b) Characteristic curve

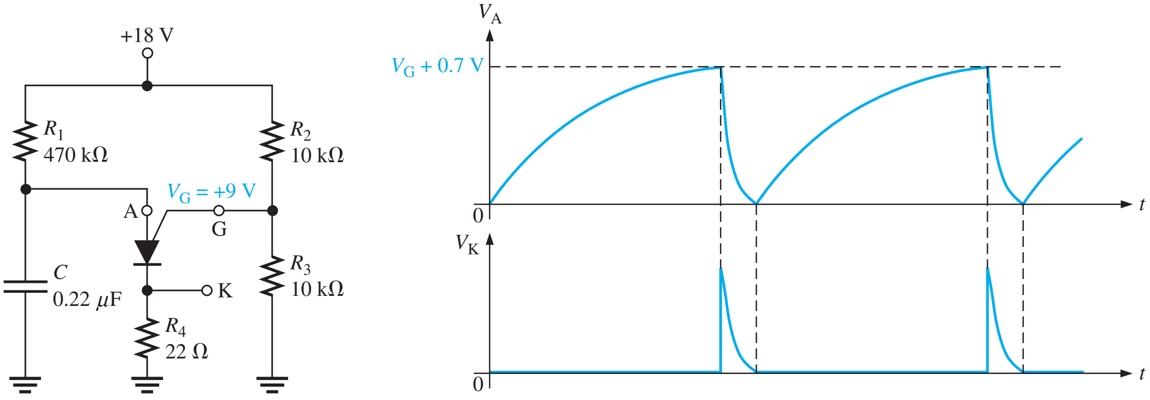
▲ FIGURE 11–43

PUT biasing.

An Application

A plot of the anode-to-cathode voltage, V_{AK}, versus anode current, I_A, in Figure 11–43(b) reveals a characteristic curve similar to that of the UJT. Therefore, the PUT replaces the UJT in many applications. One such application is the relaxation oscillator in Figure 11–44(a).

The basic operation of the PUT is as follows. The gate is biased at +9 V by the voltage divider consisting of resistors R_2 and R_3. When dc power is applied, the PUT is off and the capacitor charges toward +18 V through R_1. When the capacitor reaches $V_G + 0.7$ V, the PUT turns on and the capacitor rapidly discharges through the low *on* resistance of the PUT and R_4. A voltage spike is developed across R_4 during the discharge. As soon as the capacitor discharges, the PUT turns off and the charging cycle starts over, as shown by the waveforms in Figure 11–44(b).


+18 V
R_1
470 kΩ
R_2
10 kΩ
$V_G = +9$ V
A
G
K
C
0.22 μF
R_3
10 kΩ
R_4
22 Ω
V_A
$V_G + 0.7$ V
0
t
V_K
0
t

(a)

(b)

▲ FIGURE 11–44

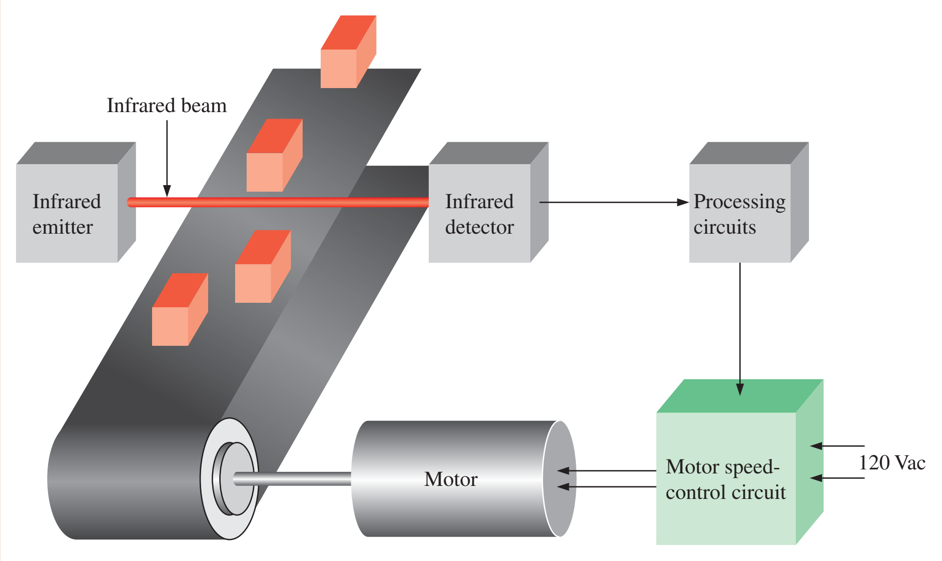
PUT relaxation oscillator.

SECTION 11–7 CHECKUP

1. What does the term *programmable* mean as used in programmable unijunction transistor (PUT)?
2. Compare the structure and the operation of a PUT to those of other devices such as the UJT and SCR.

Application Activity: *Motor Speed Control*

In this application, an SCR and a PUT are used to control the speed of a conveyor belt motor. The circuit controls the speed of the conveyor so that a predetermined average number of randomly spaced parts flow past a point on the production line in a specified period of time. This is to allow an adequate amount of time for the production line workers to perform certain tasks on each part. A basic diagram of the conveyor speed-control system is shown in Figure 11–45.



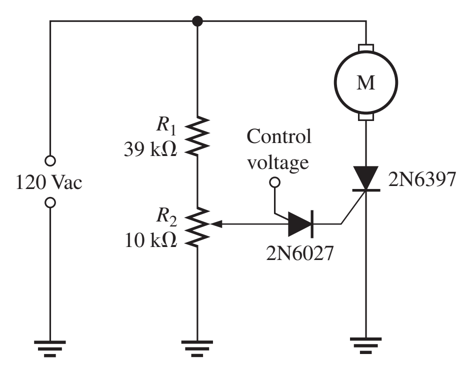
▲ FIGURE 11–45

Block diagram of conveyor speed-control system.

Each time a part on the moving conveyor belt passes the infrared (IR) detector and interrupts the IR beam, a digital counter in the processing circuits is advanced by one. The count of the passing parts is accumulated over a specified period of time and converted to a proportional voltage by the processing circuits. The more parts that pass the IR detector during the specified time, the higher the voltage. The proportional voltage is applied to the motor speed-control circuit which, in turn, adjusts the speed of the electric motor that drives the conveyor belt in order to maintain the desired number of parts in a specified period of time.

The Motor Speed-Control Circuit

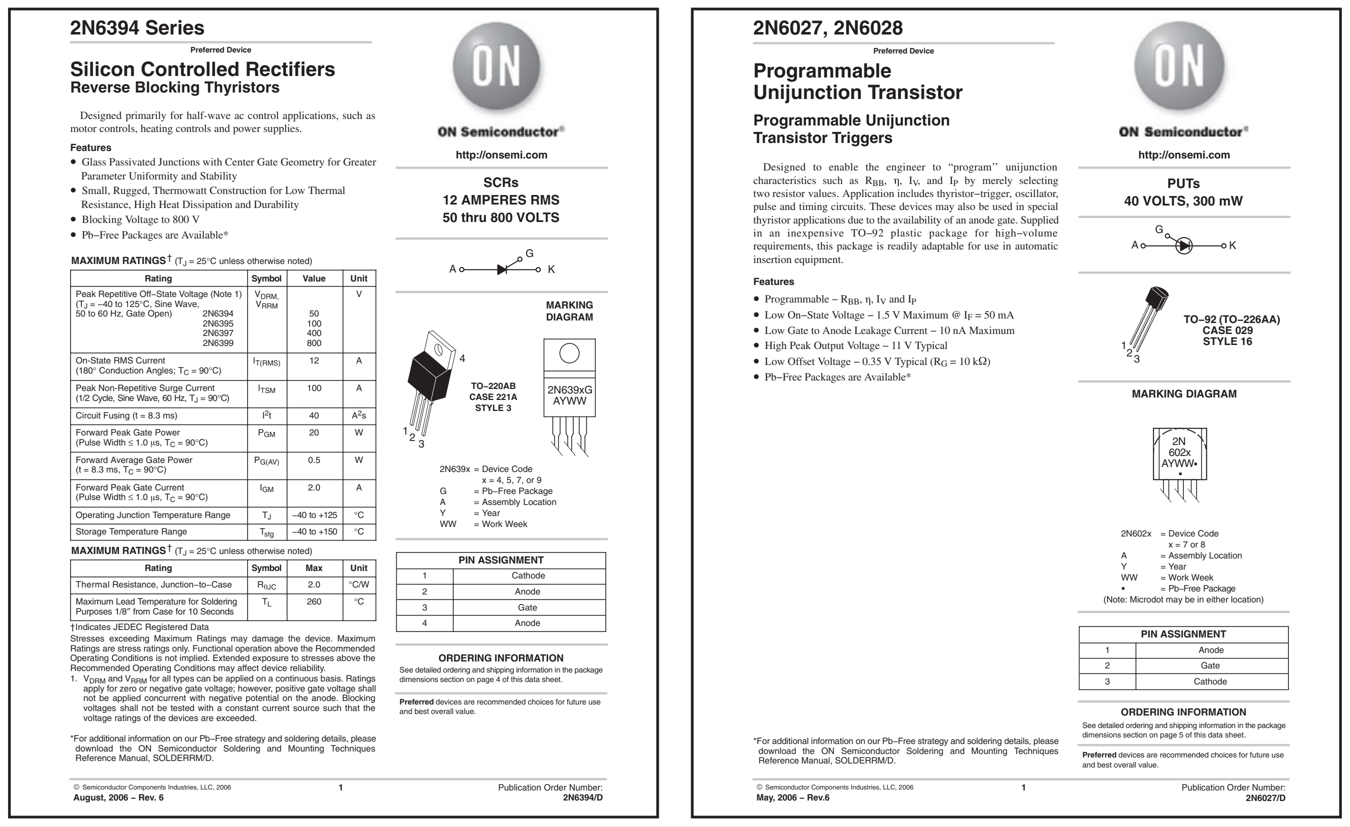
The proportional voltage from the processing circuits is applied to the gate of a PUT. This voltage determines the point in the ac cycle at which the SCR is triggered *on*. For a higher PUT gate voltage, the SCR turns on later in the half-cycle and therefore delivers less average power to the motor to decrease its speed. For a lower PUT gate voltage, the SCR turns on earlier in the half-cycle and delivers more average power to the motor to increase its speed. This process continually adjusts the motor speed to maintain the required number of parts per unit time moving on the conveyor. A potentiometer is used for calibration of the SCR trigger point. The motor speed-control circuit is shown in Figure 11–46.



▶ FIGURE 11–46

Motor speed-control circuit.

The SCR used in the motor speed control is the 2N6397 *n*-channel. The partial datasheet is shown in Figure 11–47. The PUT is the 2N6027 and its partial datasheet is also shown in Figure 11–47.



2N6394 Series

Preferred Device

Silicon Controlled Rectifiers
Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

Features

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 V
- Pb–Free Packages are Available*

MAXIMUM RATINGS† (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Note 1) (T_J = –40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N6394 2N6395 2N6397 2N6399	V_{DRM}, V_{RRM}	 50 100 400 800	V
On-State RMS Current (180° Conduction Angles; T_C = 90°C)	$I_{T(RMS)}$	12	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_J = 90°C)	I_{TSM}	100	A
Circuit Fusing (t = 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 90°C)	P_{GM}	20	W
Forward Average Gate Power (t = 8.3 ms, T_C = 90°C)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T_C = 90°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

MAXIMUM RATINGS† (T_J = 25°C unless otherwise noted)

Rating	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	2.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

†Indicates JEDEC Registered Data

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

SCRs
12 AMPERES RMS
50 thru 800 VOLTS

A K G

MARKING DIAGRAM

4
1 2 3

TO–220AB
CASE 221A
STYLE 3

2N639xG
AYWW

2N639x = Device Code
x = 4, 5, 7, or 9
G = Pb–Free Package
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

© Semiconductor Components Industries, LLC, 2006
August, 2006 – Rev. 6
1
Publication Order Number:
2N6394/D

2N6027, 2N6028

Preferred Device

Programmable Unijunction Transistor
Programmable Unijunction Transistor Triggers

Designed to enable the engineer to "program'' unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor–trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO–92 plastic package for high–volume requirements, this package is readily adaptable for use in automatic insertion equipment.

Features

- Programmable – R_{BB}, η, I_V and I_P
- Low On–State Voltage – 1.5 V Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 V Typical
- Low Offset Voltage – 0.35 V Typical (R_G = 10 kΩ)
- Pb–Free Packages are Available*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

PUTs
40 VOLTS, 300 mW

G A K

1 2 3

TO–92 (TO–226AA)
CASE 029
STYLE 16

MARKING DIAGRAM

2N
602x
AYWW▪
▪

2N602x = Device Code
x = 7 or 8
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT	
1	Anode
2	Gate
3	Cathode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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May, 2006 – Rev.6
1
Publication Order Number:
2N6027/D

▲ FIGURE 11–47

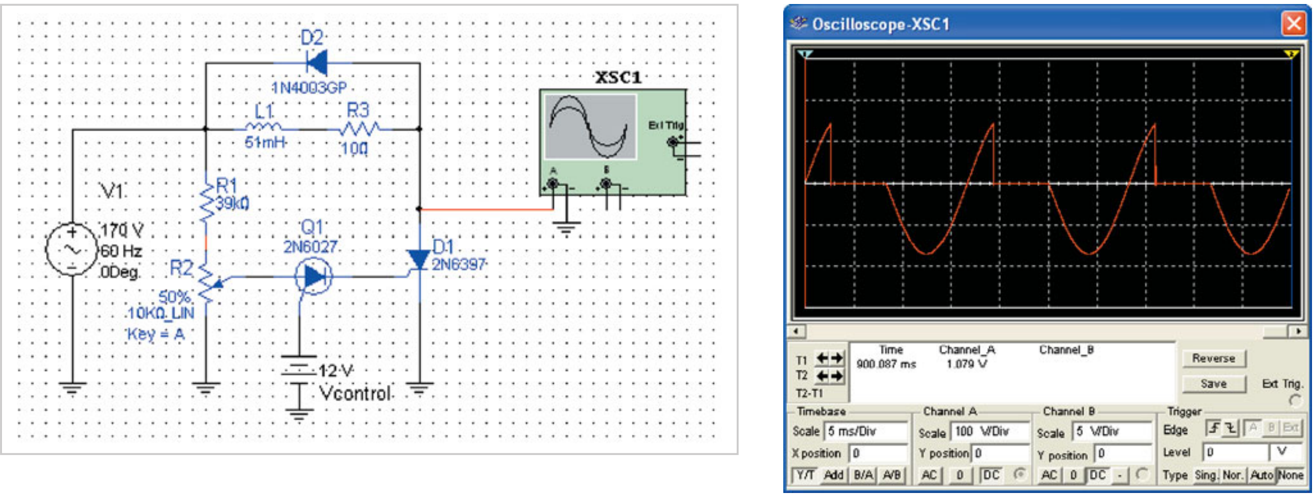
Partial datasheets for the 2N6397 silicon-controlled rectifier and for the 2N6027 programmable unijunction transistor. Copyright of Semiconductor Component Industries, LLC. Used by permission.

Answer the following questions using the partial datasheets in Figure 11–47. If sufficient information doesn't appear on these datasheets, go to *onsemi.com* and download the complete datasheet(s).

1. How much peak voltage can the SCR withstand in the *off* state?
2. What is the maximum SCR current when it is turned on?
3. What is the maximum power dissipation of the PUT?

Simulation

The motor speed-control circuit is simulated in Multisim with a resistive/inductive load in place of the motor and a dc voltage source in place of the input from the processing circuit, as shown in Figure 11–48. The diode is placed across the motor for transient suppression.



Time: 900.087 ms
Channel_A: 1.079 V
Channel_B:
Timebase Scale: 5 ms/Div
X position: 0
Channel A Scale: 100 V/Div
Channel A Y position: 0
Channel B Scale: 5 V/Div
Channel B Y position: 0
Trigger Level: 0 V

(a) Motor speed-control circuit

(b) Voltage across the SCR at $V_{\text{cont}} = 12$ V

▲ FIGURE 11–48

Simulation results for the motor speed-control circuit.

4. On the scope display in Figure 11–48 identify when the SCR is conducting.
5. If the control voltage is reduced, will the SCR conduct more or less?
6. If the control voltage is reduced, will the motor speed increase or decrease?

Figure 11–49 shows the results of varying V_{control}. You can see that as the control voltage is decreased, the SCR conducts for more of the cycle and therefore delivers more power to the motor to increase its speed.

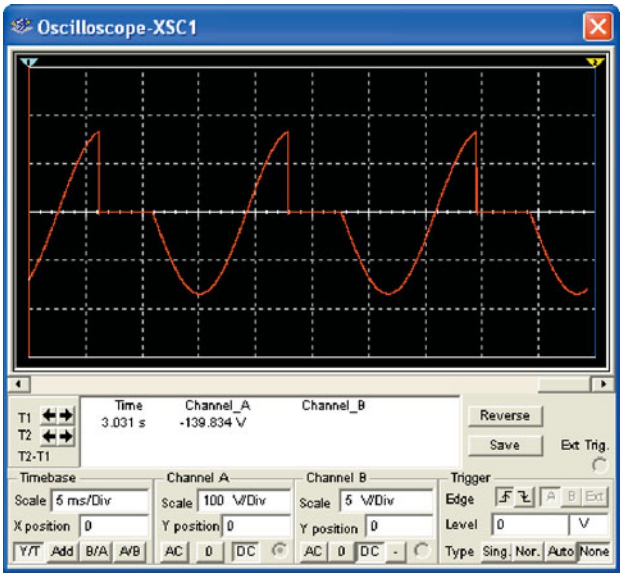
Simulate the motor speed-control circuit using your Multisim software. Observe how the SCR voltage changes with changes in V_{control}.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a similar circuit, go to Experiment 11 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).


Oscilloscope-XSC1
Reverse
Save
Ext Trig.
T1
T2
T2-T1
Y/T
Add
B/A
A/B
AC
0
DC
-
Sing.
Nor.
Auto
None
Oscilloscope-XSC1
Reverse
Save
Ext Trig.
T1
T2
T2-T1
Y/T
Add
B/A
A/B
AC
0
DC
-
Sing.
Nor.
Auto
None

Time 3.031 s
Channel_A -139.834 V
Channel_B
Timebase Scale 5 ms/Div
X position 0
Channel A Scale 100 V/Div
Y position 0
Channel B Scale 5 V/Div
Y position 0
Trigger Edge
Level 0 V
Type

Time 405.042 ms
Channel_A 567.634 mV
Channel_B
Timebase Scale 5 ms/Div
X position 0
Channel A Scale 100 V/Div
Y position 0
Channel B Scale 5 V/Div
Y position 0
Trigger Edge
Level 0 V
Type

(a) Voltage across the SCR at $V_{\text{cont}} = 14.2$ V

(b) Voltage across the SCR at $V_{\text{cont}} = 4$ V

▲ FIGURE 11–49

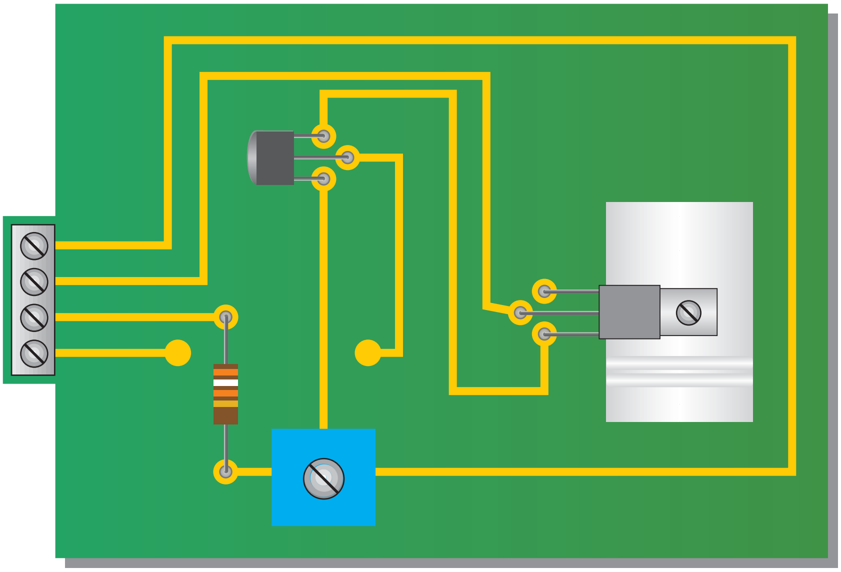
SCR waveforms for two control voltages.

Circuit Board

The motor speed-control circuit board is shown in Figure 11–50. The heat sink is for power dissipation in the SCR.

▶ FIGURE 11–50

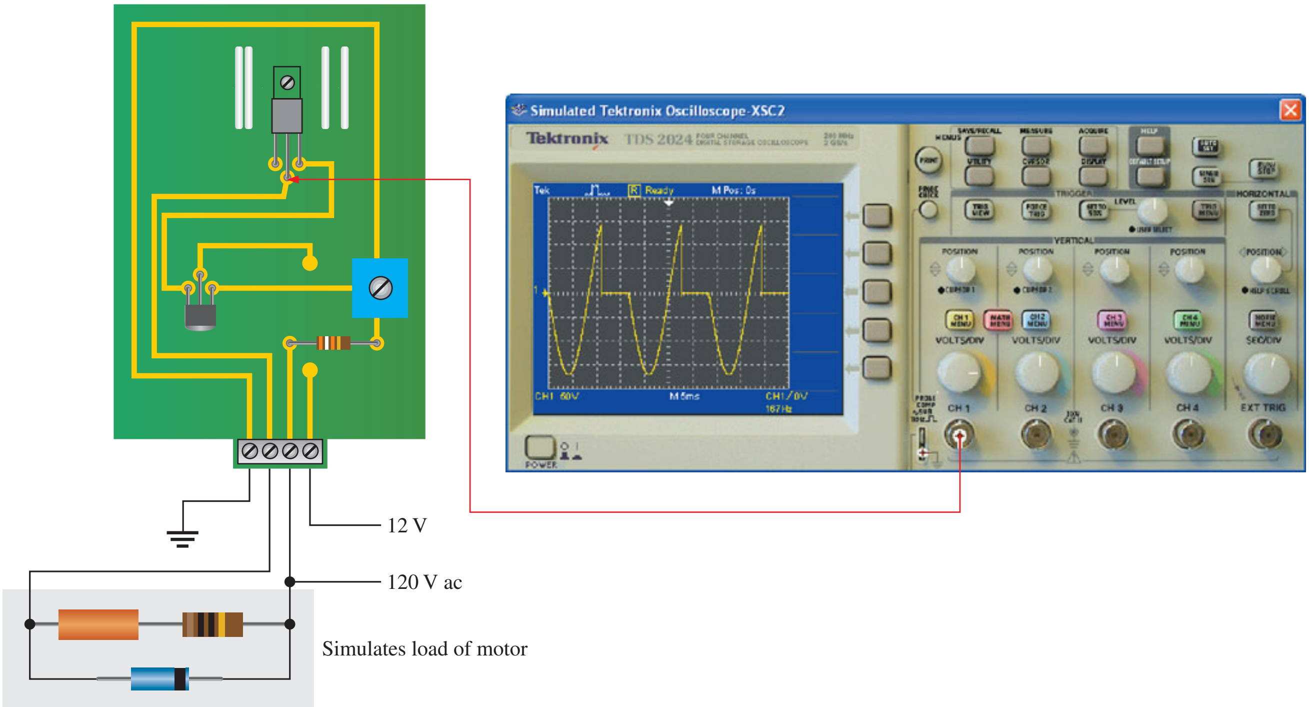
Motor speed-control circuit board.



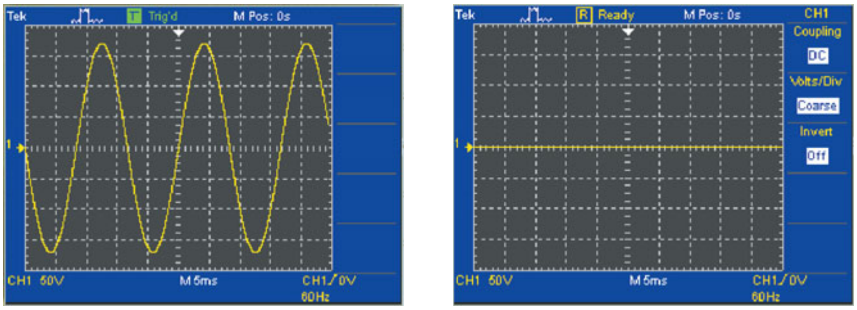
7. Check the printed circuit board for correctness by comparing with the schematic in Figure 11–46.
8. Label each input and output pin according to function.

Troubleshooting

Three circuit boards are tested, and the results are shown in Figure 11–51.


Simulated Tektronix Oscilloscope-XSC2
Tektronix TDS 2024
Tek Ready M Pos: 0s
CH1 50V M 5ms CH1 ∕ 0V 167Hz
12 V
120 V ac
Simulates load of motor

(a) Test of board 1


Tek Trig'd M Pos: 0s
CH1 50V M 5ms CH1 ∕ 0V 60Hz
Tek Ready M Pos: 0s
CH1 Coupling DC Volts/Div Coarse Invert Off
CH1 50V M 5ms CH1 ∕ 0V 60Hz

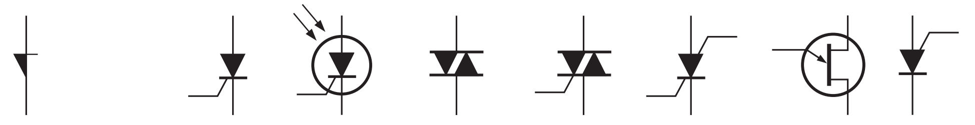
(b) Test of board 2

(c) Test of board 3

▲ **FIGURE 11–51**

9. Determine the problem, if any, in each of the board tests in Figure 11–51.
10. List possible causes of any problem from item 9.?

SUMMARY OF THYRISTOR SYMBOLS



(a) 4-layer diode (b) SCR (c) LASCR (d) Diac (e) Triac (f) SCS (g) UJT (h) PUT

SUMMARY

Section 11–1

- Thyristors are devices constructed with four semiconductor layers (*pnpn*).
- Thyristors include 4-layer diodes, SCRs, LASCRs, diacs, triacs, SCSs, and PUTs.
- The 4-layer diode is a thyristor that conducts when the voltage across its terminals exceeds the breakover potential.

Section 11–2

- The silicon-controlled rectifier (SCR) can be triggered on by a pulse at the gate and turned off by reducing the anode current below the specified holding value.
- Light acts as the trigger source in light-activated SCRs (LASCRs).

Section 11–4

- The diac can conduct current in either direction and is turned on when a breakover voltage is exceeded. It turns off when the current drops below the holding value.
- The triac, like the diac, is a bidirectional device. It can be turned on by a pulse at the gate and conducts in a direction depending on the voltage polarity across the two anode terminals.

Section 11–5

- The silicon-controlled switch (SCS) has two gate terminals and can be turned on by a pulse at the cathode gate and turned off by a pulse at the anode gate.

Section 11–6

- The intrinsic standoff ratio of a unijunction transistor (UJT) determines the voltage at which the device will trigger on.

Section 11–7

- The programmable unijunction transistor (PUT) can be externally programmed to turn on at a desired anode-to-gate voltage level.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Diac A two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction when properly activated.

Forward-breakover voltage ($V_{BR(F)}$) The voltage at which a device enters the forward-blocking region.

4-layer diode The type of two-terminal thyristor that conducts current when the anode-to-cathode voltage reaches a specified "breakover" value.

Holding current (I_H) The value of the anode current below which a device switches from the forward-conduction region to the forward-blocking region.

LASCR Light-activated silicon-controlled rectifier; a four-layer semiconductor device (thyristor) that conducts current in one direction when activated by a sufficient amount of light and continues to conduct until the current falls below a specified value.

PUT Programmable unijunction transistor; a type of three-terminal thyristor (more like an SCR than a UJT) that is triggered into conduction when the voltage at the anode exceeds the voltage at the gate.

SCR Silicon-controlled rectifier; a type of three-terminal thyristor that conducts current when triggered on by a voltage at the single gate terminal and remains on until the anode current falls below a specified value.

SCS Silicon-controlled switch; a type of four-terminal thyristor that has two gate terminals that are used to trigger the device on and off.

Standoff ratio The characteristic of a UJT that determines its turn-on point.

Thyristor A class of four-layer (*pnpn*) semiconductor devices.

Triac A three-terminal thyristor that can conduct current in either direction when properly activated.

UJT Unijunction transistor; a three-terminal single *pn* junction device that exhibits a negative resistance characteristic.

KEY FORMULAS

11–1 $\eta = \dfrac{r'_{B1}}{r'_{BB}}$ UJT intrinsic standoff ratio

11–2 $V_P = \eta V_{BB} + V_{pn}$ UJT peak-point voltage

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. A thyristor is characterized by four semiconductor layers.
2. An SCR is a silicon conduction rectifier.
3. The three terminals of an SCR are the anode, cathode, and gate.
4. One method for turning off an SCR is called forced commutation.
5. The SCR is turned on by a pulse on the anode.
6. A diac can conduct current in two directions.
7. A diac has two terminals.
8. A triac has four terminals.
9. The SCS is a silicon-controlled switch.
10. The UJT is commonly used to trigger thyristors but is not a thyristor itself.
11. The PUT is a three-terminal thyristor that can be turned on and off by a voltage on its gate.
12. PUT stands for positive unijunction transistor.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the potentiometer in Figure 11–19 is adjusted from a setting near the bottom (low resistance from wiper to ground) to a setting near the top (higher resistance from wiper to ground), the average current through R_L will
   (a) increase **(b)** decrease **(c)** not change
2. If the diode in Figure 11–19 opens, the voltage across R_L will
   (a) increase **(b)** decrease **(c)** not change
3. Assume that the battery in Figure 11–21 is fully charged and the ac power goes off. If D_3 opens, the current through the lamp will immediately
   (a) increase **(b)** decrease **(c)** not change
4. If the capacitor in Figure 11–44 shorts to ground, the voltage at the cathode of the PUT will
   (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 11–1

1. A thyristor has
   (a) two *pn* junctions **(b)** three *pn* junctions
   (c) four *pn* junctions **(d)** only two terminals
2. Common types of thyristors include
   (a) BJTs and SCRs **(b)** UJTs and PUTs
   (c) FETs and triacs **(d)** diacs and triacs
3. A 4-layer diode turns on when the anode-to-cathode voltage exceeds
   (a) 0.7 V **(b)** the gate voltage
   (c) the forward-breakover voltage **(d)** the forward-blocking voltage
4. Once it is conducting, a 4-layer diode can be turned off by
   (a) reducing the current below a certain value
   (b) disconnecting the anode voltage
   (c) answers (a) and (b)
   (d) neither answer (a) nor (b)

Section 11–2

5. An SCR differs from the 4-layer diode because
   (a) it has a gate terminal **(b)** it is not a thyristor
   (c) it does not have four layers **(d)** it cannot be turned on and off

6. An SCR can be turned off by

(a) forced commutation **(b)** a negative pulse on the gate

(c) anode current interruption **(d)** answers (a), (b), and (c)

(e) answers (a) and (c)

7. In the forward-blocking region, the SCR is

(a) reverse-biased **(b)** in the *off* state

(c) in the *on* state **(d)** at the point of breakdown

8. The specified value of holding current for an SCR means that

(a) the device will turn on when the anode current exceeds this value

(b) the device will turn off when the anode current falls below this value

(c) the device may be damaged if the anode current exceeds this value

(d) the gate current must equal or exceed this value to turn the device on

Section 11–4

9. The diac is

(a) a thyristor

(b) a bilateral, two-terminal device

(c) like two parallel 4-layer diodes in reverse directions

(d) answers (a), (b), and (c)

10. The triac is

(a) like a bidirectional SCR

(b) a four-terminal device

(c) not a thyristor

(d) answers (a) and (b)

Section 11–5

11. The SCS differs from the SCR because

(a) it does not have a gate terminal

(b) its holding current is less

(c) it can handle much higher currents

(d) it has two gate terminals

12. The SCS can be turned on by

(a) an anode voltage that exceeds forward-breakover voltage

(b) a positive pulse on the cathode gate

(c) a negative pulse on the anode gate

(d) either (b) or (c)

13. The SCS can be turned off by

(a) a negative pulse on the cathode gate and a positive pulse on the anode gate

(b) reducing the anode current to below the holding value

(c) answers (a) and (b)

(d) a positive pulse on the cathode gate and a negative pulse on the anode gate

Section 11–6

14. Which of the following is *not* a characteristic of the UJT?

(a) intrinsic standoff ratio

(b) negative resistance

(c) peak-point voltage

(d) bilateral conduction

Section 11–7

15. The PUT is

(a) much like the UJT

(b) not a thyristor

(c) triggered on and off by the gate-to-anode voltage

(d) not a four-layer device

PROBLEMS

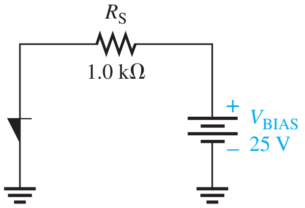
Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 11–1 The Four-Layer Diode

1. The 4-layer diode in Figure 11–52 is biased such that it is in the forward-conduction region. Determine the anode current for $V_{BR(F)} = 20\text{ V}$, $V_{BE} = 0.7\text{ V}$, and $V_{CE(sat)} = 0.2\text{ V}$.

▶ FIGURE 11–52



2. **(a)** Determine the resistance of a certain 4-layer diode in the forward-blocking region if $V_{AK} = 15\text{ V}$ and $I_A = 1\ \mu\text{A}$.

(b) If the forward-breakover voltage is 50 V, how much must V_{AK} be increased to switch the diode into the forward-conduction region?

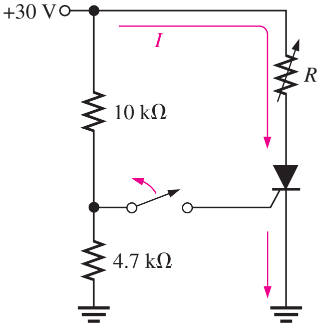
Section 11–2 The Silicon-Controlled Rectifier (SCR)

3. Explain the operation of an SCR in terms of its transistor equivalent.

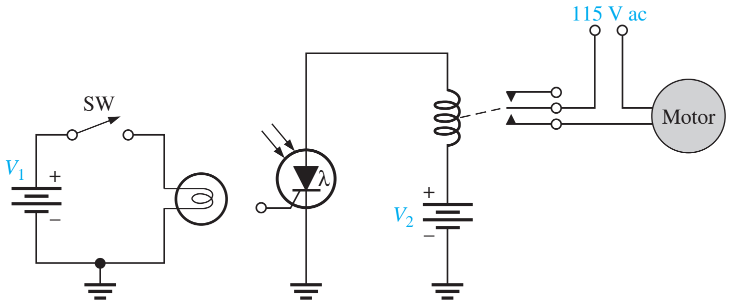
4. To what value must the variable resistor be adjusted in Figure 11–53 in order to turn the SCR off? Assume $I_H = 10\text{ mA}$ and $V_{AK} = 0.7\text{ V}$.

▶ FIGURE 11–53

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F11-53).



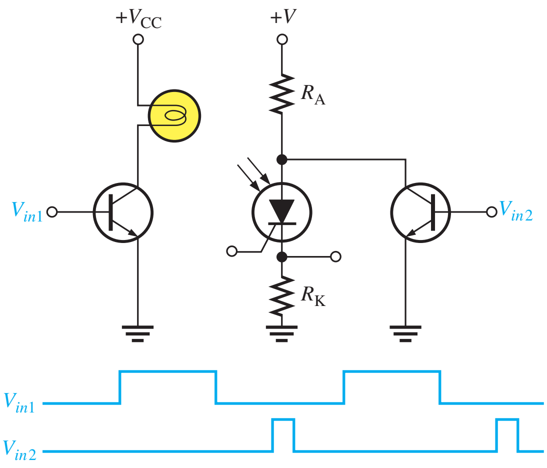
5. By examination of the circuit in Figure 11–54, explain its purpose and basic operation.



▲ FIGURE 11–54

6. Determine the voltage waveform across R_K in Figure 11–55.

▶ **FIGURE 11–55**



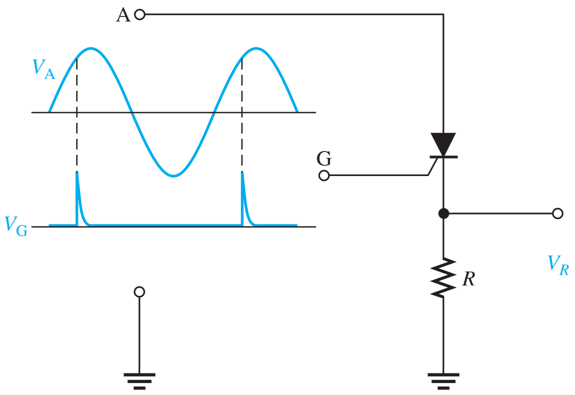
Section 11–3 SCR Applications

7. Describe how you would modify the circuit in Figure 11–17 so that the SCR triggers and conducts on the negative half-cycle of the input.

8. What is the purpose of diodes D_1 and D_2 in Figure 11–21?

9. Sketch the V_R waveform for the circuit in Figure 11–56, given the indicated relationship of the input waveforms.

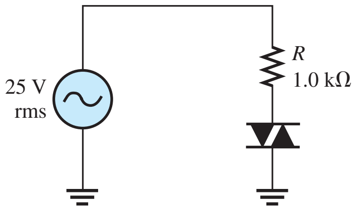
▶ **FIGURE 11–56**



Section 11–4 The Diac and Triac

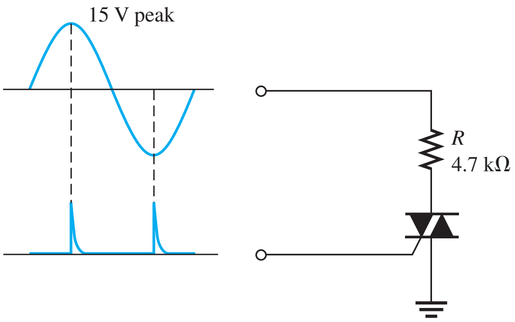
10. Sketch the current waveform for the circuit in Figure 11–57. The diac has a breakover potential of 20 V. $I_H = 20$ mA.

▶ **FIGURE 11–57**



11. Repeat Problem 10 for the triac circuit in Figure 11–58. The breakover potential is 25 V and $I_H = 1$ mA.

▶ FIGURE 11–58



Section 11–5 The Silicon-Controlled Switch (SCS)

12. Explain the turn-on and turn-off operation of an SCS in terms of its transistor equivalent.

13. Name the terminals of an SCS.

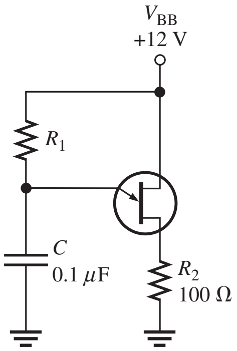
Section 11–6 The Unijunction Transistor (UJT)

14. In a certain UJT, $r'_{B1} = 2.5$ kΩ and $r'_{B2} = 4$ kΩ. What is the intrinsic standoff ratio?

15. Determine the peak-point voltage for the UJT in Problem 14 if $V_{BB} = 15$ V.

16. Find the range of values of R_1 in Figure 11–59 that will ensure proper turn-on and turn-off of the UJT. $\eta = 0.68$, $V_V = 0.8$ V, $I_V = 15$ mA, $I_P = 10\ \mu$A, and $V_P = 10$ V.

▶ FIGURE 11–59

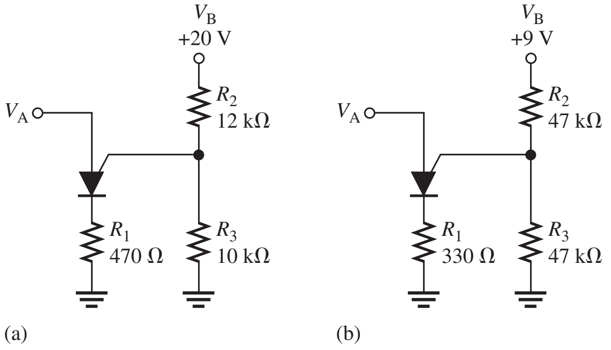


Section 11–7 The Programmable Unijunction Transistor (PUT)

17. At what anode voltage (V_A) will each PUT in Figure 11–60 begin to conduct?

18. Draw the current waveform for each circuit in Figure 11–60 when there is a 10 V peak sinusoidal voltage at the anode. Neglect the forward voltage of the PUT.

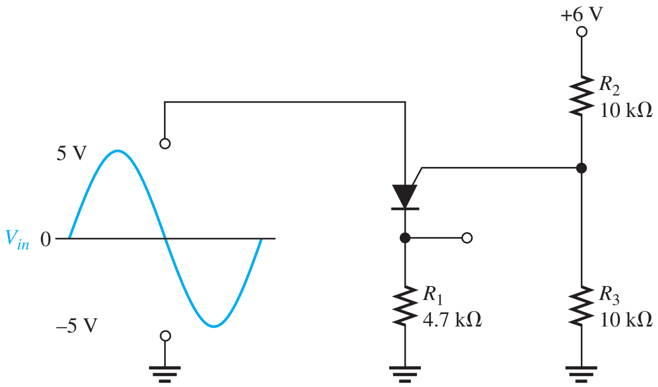
▶ FIGURE 11–60



19. Sketch the voltage waveform across R_1 in Figure 11–61 in relation to the input voltage waveform.

20. Repeat Problem 19 if R_3 is increased to 15 kΩ.

▶ FIGURE 11–61



APPLICATION ACTIVITY PROBLEMS

21. In the motor speed-control circuit of Figure 11–46, at which PUT gate voltage does the electric motor run at the fastest speed: 0 V, 2 V, or 5 V?

22. Does the SCR in the motor speed-control circuit turn on earlier or later in the ac cycle if the resistance of the rheostat is reduced?

23. Describe the SCR action as the PUT gate voltage is increased in the motor speed-control circuit.

ADVANCED PROBLEMS

24. Refer to the SCR over-voltage protection circuit in Figure 11–22. For a +12 V output dc power supply, specify the component values that will provide protection for the circuit if the output voltage exceeds +15 V. Assume the fuse is rated at 1 A.

25. Design an SCR crowbar circuit to protect electronic circuits against a voltage from the power supply in excess of 6.2 V.

26. Design a relaxation oscillator to produce a frequency of 2.5 kHz using a UJT with $\eta = 0.75$ and a valley voltage of 1 V. The circuit must operate from a +12 V dc source. Design values of $I_V = 10$ mA and $I_P = 20\ \mu$A are to be used.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

27. Open file TSP11-27 and determine the fault.

28. Open file TSP11-28 and determine the fault.

29. Open file TSP11-29 and determine the fault.

12

THE OPERATIONAL AMPLIFIER

CHAPTER OUTLINE

12–1 Introduction to Operational Amplifiers
12–2 Op-Amp Input Modes and Parameters
12–3 Negative Feedback
12–4 Op-Amps with Negative Feedback
12–5 Effects of Negative Feedback on Op-Amp Impedances
12–6 Bias Current and Offset Voltage
12–7 Open-Loop Frequency and Phase Responses
12–8 Closed-Loop Frequency Response
12–9 Troubleshooting
Application Activity
Programmable Analog Technology

CHAPTER OBJECTIVES

- Describe the basic operational amplifier and its characteristics
- Discuss op-amp modes and several parameters
- Explain negative feedback in op-amps
- Analyze op-amps with negative feedback
- Describe how negative feedback affects op-amp impedances
- Discuss bias current and offset voltage
- Analyze the open-loop frequency response of an op-amp
- Analyze the closed-loop frequency response of an op-amp
- Troubleshoot op-amp circuits

KEY TERMS

- Operational amplifier (op-amp)
- Differential amplifier
- Differential mode
- Common mode
- CMRR
- Open-loop voltage gain
- Slew rate
- Negative feedback
- Closed-loop voltage gain
- Noninverting amplifier
- Voltage-follower
- Inverting amplifier
- Phase shift
- Gain-bandwidth product

APPLICATION ACTIVITY PREVIEW

For the Application Activity in this chapter, the audio amplifier from the PA system in Chapter 7 is modified. The two-stage preamp portion of the amplifier is replaced by an op-amp circuit. The power amplifier portion is retained in its original configuration with the exception of the drive circuit so that the new design consists of an op-amp driving a push-pull power stage. In the original system there are two PC boards—one for the preamp and one for the power amplifier. The new design will allow both the preamp and the power amplifier to be on a single PC board.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In the previous chapters, you have studied a number of important electronic devices. These devices, such as the diode and the transistor, are separate devices that are individually packaged and interconnected in a circuit with other devices to form a complete, functional unit. Such devices are referred to as *discrete components.*

Now you will begin the study of linear integrated circuits (ICs), where many transistors, diodes, resistors, and capacitors are fabricated on a single tiny chip of semiconductive material and packaged in a single case to form a functional circuit. An integrated circuit, such as an operational amplifier (op-amp), is treated as a single device. This means that you will be concerned with what the circuit does more from an external viewpoint than from an internal, component-level viewpoint.

In this chapter, you will learn the basics of op-amps, which are the most versatile and widely used of all linear integrated circuits. You will also learn about open-loop and closed-loop frequency responses, bandwidth, phase shift, and other frequency-related parameters. The effects of negative feedback will be examined.

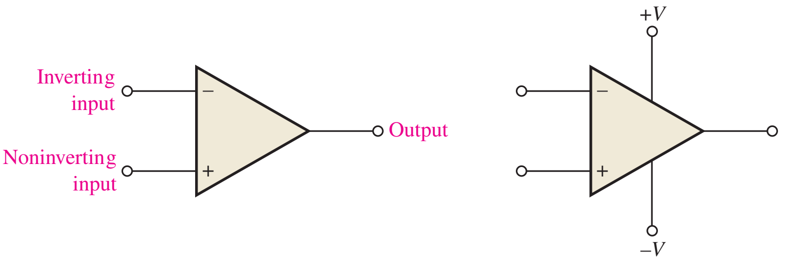
12–1 INTRODUCTION TO OPERATIONAL AMPLIFIERS

Early operational amplifiers (op-amps) were used primarily to perform mathematical operations such as addition, subtraction, integration, and differentiation—thus the term *operational.* These early devices were constructed with vacuum tubes and worked with high voltages. Today's op-amps are linear integrated circuits (ICs) that use relatively low dc supply voltages and are reliable and inexpensive.

After completing this section, you should be able to

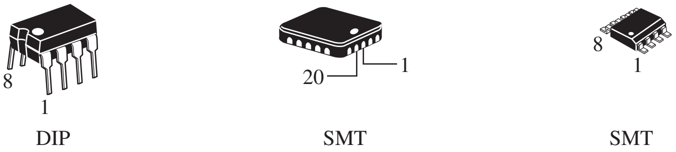
- **Describe the basic operational amplifier and its characteristics**
    - Identify the schematic symbol and IC package terminals
- Discuss the ideal op-amp
- Discuss the practical op-amp
    - Draw the internal block diagram

The standard **operational amplifier (op-amp)** symbol is shown in Figure 12–1(a). It has two input terminals, the inverting (−) input and the noninverting (+) input, and one output terminal. Most op-amps operate with two dc supply voltages, one positive and the other negative, as shown in Figure 12–1(b), although some have a single dc supply. Usually these dc voltage terminals are left off the schematic symbol for simplicity but are understood to be there. Some typical op-amp IC packages are shown in Figure 12–1(c).



(a) Symbol

(b) Symbol with dc supply connections



(c) Typical packages. Pin 1 is indicated by a notch or dot on dual in-line (DIP) and surface-mount technology (SMT) packages, as shown.

FIGURE 12–1

Op-amp symbols and packages.

The Ideal Op-Amp

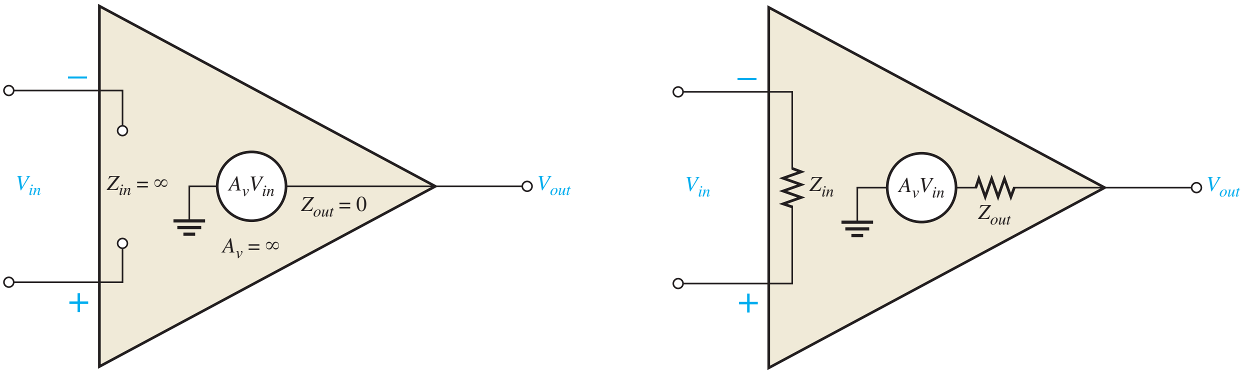
To illustrate what an op-amp is, let's consider its ideal characteristics. A practical op-amp, of course, falls short of these ideal standards, but it is much easier to understand and analyze the device from an ideal point of view.

First, the ideal op-amp has *infinite voltage gain* and *infinite bandwidth.* Also, it has an *infinite input impedance* (open) so that it does not load the driving source. Finally, it has a *zero output impedance.* Op-amp characteristics are illustrated in Figure 12–2(a). The input voltage, V_{in}, appears between the two input terminals, and the output voltage is A_vV_{in}, as indicated by the internal voltage source symbol. The concept of infinite input impedance is

HISTORY NOTE

The operational amplifier concept originated around 1947. It was proposed that such a device would form an extremely useful analog building block. The first commercial op-amps used vacuum tubes, but it was not until the introduction of the integrated circuit did the op-amp start to fulfill its true potential. In 1964, the first integrated circuit op-amp, designated the 702, was developed by Fairchild Semiconductor. This was later followed by the 709 and eventually the 741, which has become an industry standard.

a particularly valuable analysis tool for the various op-amp configurations, which will be discussed in Section 12–4.



(a) Ideal op-amp representation

(b) Practical op-amp representation

▲ FIGURE 12–2

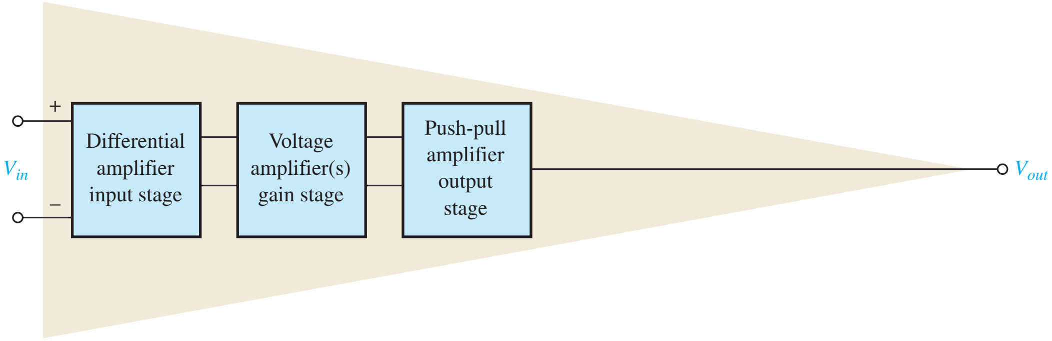
Basic op-amp representations.

The Practical Op-Amp

Although **integrated circuit (IC)** op-amps approach parameter values that can be treated as ideal in many cases, the ideal device can never be made. Any device has limitations, and the IC op-amp is no exception. Op-amps have both voltage and current limitations. Peak-to-peak output voltage, for example, is usually limited to slightly less than the two supply voltages. Output current is also limited by internal restrictions such as power dissipation and component ratings.

Characteristics of a practical op-amp are *very high voltage gain, very high input impedance, and very low output impedance.* These are labelled in Figure 12–2(b). Another practical consideration is that there is always noise generated within the op-amp. **Noise** is an undesired signal that affects the quality of a desired signal. Today, circuit designers are using smaller voltages that require high accuracy, so low-noise components are in greater demand. All circuits generate noise; op-amps are no exception, but the amount can be minimized.

Internal Block Diagram of an Op-Amp A typical op-amp is made up of three types of amplifier circuits: a differential amplifier, a voltage amplifier, and a push-pull amplifier, as shown in Figure 12–3. The **differential amplifier** is the input stage for the op-amp. It provides amplification of the difference voltage between the two inputs. The second stage is usually a class A amplifier that provides additional gain. Some op-amps may have more than one voltage amplifier stage. A push-pull class B amplifier is typically used for the output stage.



+
−
V_{in}
Differential amplifier input stage
Voltage amplifier(s) gain stage
Push-pull amplifier output stage
V_{out}

▲ FIGURE 12–3

Basic internal arrangement of an op-amp.

The differential amplifier was introduced in Chapter 6. The term *differential* comes from the amplifier's ability to amplify the difference of two input signals applied to its inputs. Only the difference in the two signals is amplified; if there is no difference, the output is zero. The differential amplifier exhibits two modes of operation based on the type of input signals. These modes are *differential* and *common,* which are described in the next section. Since the differential amplifier is the input stage of the op-amp, the op-amp exhibits the same modes.

SECTION 12–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What are the connections to a basic op-amp?
2. Describe some of the characteristics of a practical op-amp.
3. List the amplifier stages in a typical op-amp.
4. What does a differential amplifier amplify?

12–2 OP-AMP INPUT MODES AND PARAMETERS

In this section, important op-amp input modes and several parameters are defined. Also several common IC op-amps are compared in terms of these parameters.

After completing this section, you should be able to

- ❑ **Discuss op-amp modes and several parameters**
  - ◆ Identify the schematic symbol and IC package terminals
- ❑ Describe the input signal modes
  - ◆ Explain the differential mode ◆ Explain the common mode
- ❑ Define and discuss op-amp parameters
  - ◆ Define *common-mode rejection ratio (CMRR)* ◆ Calculate the CMRR
  - ◆ Express the CMRR in decibels ◆ Define open-loop voltage gain
  - ◆ Explain maximum output voltage swing ◆ Explain input offset voltage
  - ◆ Explain input bias current ◆ Explain input impedance ◆ Explain input offset current ◆ Explain output impedance ◆ Explain slew rate
  - ◆ Explain frequency response
- ❑ Compare op-amp parameters for several devices

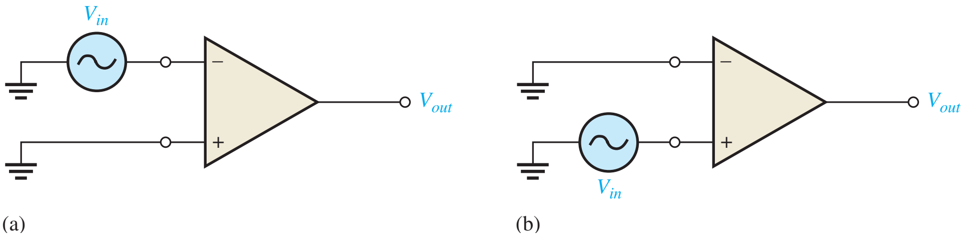
Input Signal Modes

Recall that the input signal modes are determined by the differential amplifier input stage of the op-amp.

Differential Mode In the **differential mode**, either one signal is applied to an input with the other input grounded or two opposite-polarity signals are applied to the inputs. When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input, as shown in Figure 12–4. In the case where the signal voltage is applied to the inverting input as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal is applied to the noninverting input with the inverting input grounded, as in Figure 12–4(b), a noninverted, amplified signal voltage appears at the output.

FIGURE 12–4

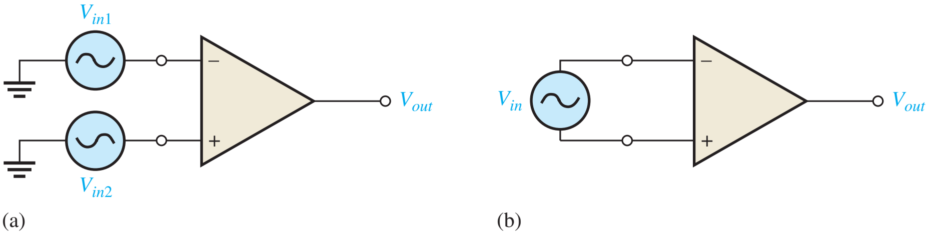
Single-ended differential mode.



In the double-ended differential mode, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 12–5(a). The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source connected between the two inputs, as shown in Figure 12–5(b).

FIGURE 12–5

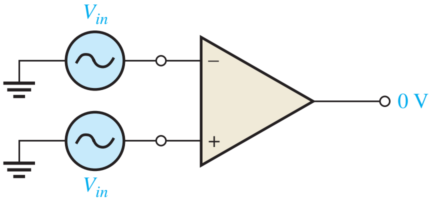
Double-ended differential mode.



Common Mode In the **common mode**, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 12–6. When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage.

FIGURE 12–6

Common-mode operation.



This action is called *common-mode rejection.* Its importance lies in the situation where an unwanted signal appears commonly on both op-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the output and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines, from adjacent lines, the 60 Hz power line, or other sources.

Op-Amp Parameters

Common-Mode Rejection Ratio Desired signals can appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the output as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the op-amp and do not appear on the output. The measure of an amplifier's ability to reject common-mode signals is a parameter called the **CMRR (common-mode rejection ratio)**.

Ideally, an op-amp provides a very high gain for differential-mode signals and zero gain for common-mode signals. Practical op-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high open-loop differential voltage gain (usually several thousand). The higher the open-loop gain with respect to the common-mode gain, the better the performance of the op-amp in terms of rejection of common-mode signals. This suggests that a good measure of the op-amp's performance in rejecting unwanted common-mode signals is the ratio of the open-loop differential voltage gain, A_{ol}, to the common-mode gain, A_{cm}. This ratio is the common-mode rejection ratio, CMRR.

$$\textbf{CMRR} = \frac{A_{ol}}{A_{cm}}$$

Equation 12–1

The higher the CMRR, the better. A very high value of CMRR means that the open-loop gain, A_{ol}, is high and the common-mode gain, A_{cm}, is low.

The CMRR is often expressed in decibels (dB) as

$$\textbf{CMRR} = 20 \log \left(\frac{A_{ol}}{A_{cm}}\right)$$

Equation 12–2

The **open-loop voltage gain**, A_{ol}, of an op-amp is the internal voltage gain of the device and represents the ratio of output voltage to input voltage when there are no external components. The open-loop voltage gain is set entirely by the internal design. Open-loop voltage gain can range up to 200,000 (106 dB) and is not a well-controlled parameter. Datasheets often refer to the open-loop voltage gain as the *large-signal voltage gain.*

A CMRR of 100,000, for example, means that the desired input signal (differential) is amplified 100,000 times more than the unwanted noise (common-mode). If the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the output 100,000 times greater in amplitude than the noise. Thus, the noise or interference has been essentially eliminated.

EXAMPLE 12–1

A certain op-amp has an open-loop differential voltage gain of 100,000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibels.

Solution $A_{ol} = 100{,}000$, and $A_{cm} = 0.2$. Therefore,

$$\text{CMRR} = \frac{A_{ol}}{A_{cm}} = \frac{100{,}000}{0.2} = \mathbf{500{,}000}$$

Expressed in decibels,

$$\text{CMRR} = 20 \log (500{,}000) = \mathbf{114\ dB}$$

Related Problem[*] Determine the CMRR and express it in dB for an op-amp with an open-loop differential voltage gain of 85,000 and a common-mode gain of 0.25.

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[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Maximum Output Voltage Swing ($V_{O(p\text{-}p)}$) With no input signal, the output of an op-amp is ideally 0 V. This is called the *quiescent output voltage.* When an input signal is applied, the ideal limits of the peak-to-peak output signal are $\pm V_{CC}$. In practice, however, this ideal can be approached but never reached. $V_{O(p\text{-}p)}$ varies with the load connected to the op-amp and increases directly with load resistance. For example, the Fairchild KA741 datasheet shows a typical $V_{O(p\text{-}p)}$ of ± 13 V for $V_{CC} = \pm 15$ V when $R_L = 2\ \text{k}\Omega$. $V_{O(p\text{-}p)}$ increases to ± 14 V when $R_L = 10\ \text{k}\Omega$.

Some op-amps do not use both positive and negative supply voltages. One example is when a single dc voltage source is used to power an op-amp that drives an analog-to-digital converter (discussed in Chapter 14). In this case, the op-amp output is designed to operate between ground and a full scale output that is near (or at) the positive supply voltage. Op-amps that operate on a single supply use the terminology V_{OH} and V_{OL} to specify the maximum and minimum output voltage. (Note that these are not the same as the digital definitions of V_{OL} and V_{OH}.)

GREENTECH NOTE

Designers today are "going green" by reducing power in op-amps and applications. To reduce power dissipated by op-amps, lower voltage supplies can be used as well as greater reliance on CMOS. In some cases, CMOS requires only a few picoamps of bias current, which helps designers reduce current in the external circuit.

Input Offset Voltage The ideal op-amp produces zero volts out for zero volts in. In a practical op-amp, however, a small dc voltage, $V_{OUT(error)}$, appears at the output when no differential input voltage is applied. Its primary cause is a slight mismatch of the base-emitter voltages of the differential amplifier input stage of an op-amp.

As specified on an op-amp datasheet, the *input offset voltage,* V_{OS}, is the differential dc voltage required between the inputs to force the output to zero volts. Typical values of input offset voltage are in the range of 2 mV or less. In the ideal case, it is 0 V.

The *input offset voltage drift* is a parameter related to V_{OS} that specifies how much change occurs in the input offset voltage for each degree change in temperature. Typical values range anywhere from about 5 μV per degree Celsius to about 50 μV per degree Celsius. Usually, an op-amp with a higher nominal value of input offset voltage exhibits a higher drift.

Input Bias Current You have seen that the input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents.

The *input bias current* is the dc current required by the inputs of the amplifier to properly operate the first stage. By definition, the input bias current is the *average* of both input currents and is calculated as follows:

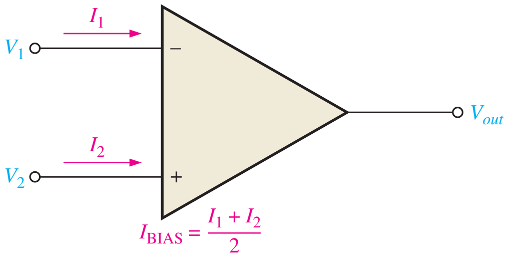
Equation 12–3

$$I_{BIAS} = \frac{I_1 + I_2}{2}$$

The concept of input bias current is illustrated in Figure 12–7.

FIGURE 12–7

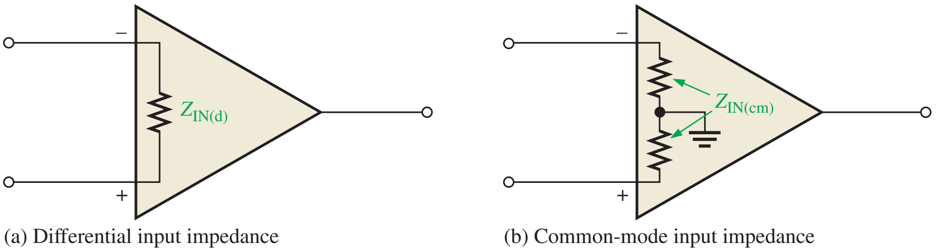
Input bias current is the average of the two op-amp input currents.



Input Impedance Two basic ways of specifying the input impedance of an op-amp are the differential and the common mode. The *differential input impedance* is the total resistance between the inverting and the noninverting inputs, as illustrated in Figure 12–8(a). Differential impedance is measured by determining the change in bias current for a given change in differential input voltage. The *common-mode input impedance* is the resistance between each input and ground and is measured by determining the change in bias current for a given change in common-mode input voltage. It is depicted in Figure 12–8(b).

FIGURE 12–8

Op-amp input impedance.



(a) Differential input impedance

(b) Common-mode input impedance

Input Offset Current Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal.

The *input offset current,* I_{OS}, is the difference of the input bias currents, expressed as an absolute value.

$$I_{OS} = |I_1 - I_2|$$

Equation 12–4

Actual magnitudes of offset current are usually at least an order of magnitude (ten times) less than the bias current. In many applications, the offset current can be neglected. However, high-gain, high-input impedance amplifiers should have as little I_{OS} as possible because the difference in currents through large input resistances develops a substantial offset voltage, as shown in Figure 12–9.

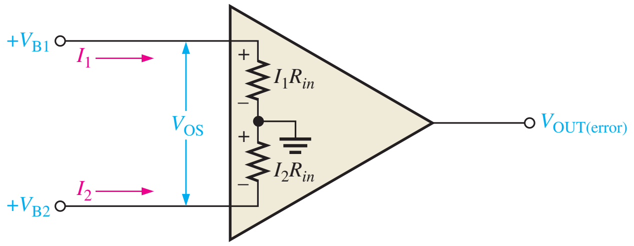


FIGURE 12–9

Effect of input offset current.

The offset voltage developed by the input offset current is

$$V_{OS} = I_1R_{in} - I_2R_{in} = (I_1 - I_2)R_{in}$$

$$V_{OS} = I_{OS}R_{in}$$

Equation 12–5

The error created by I_{OS} is amplified by the gain A_v of the op-amp and appears in the output as

$$V_{OUT(error)} = A_vI_{OS}R_{in}$$

Equation 12–6

A change in offset current with temperature affects the error voltage. Values of temperature coefficient for the offset current in the range of 0.5 nA per degree Celsius are common.

Output Impedance The *output impedance* is the resistance viewed from the output terminal of the op-amp, as indicated in Figure 12–10.

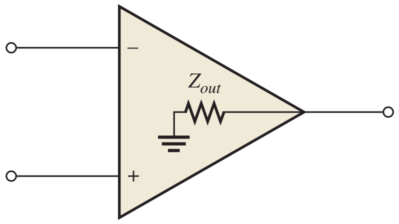


FIGURE 12–10

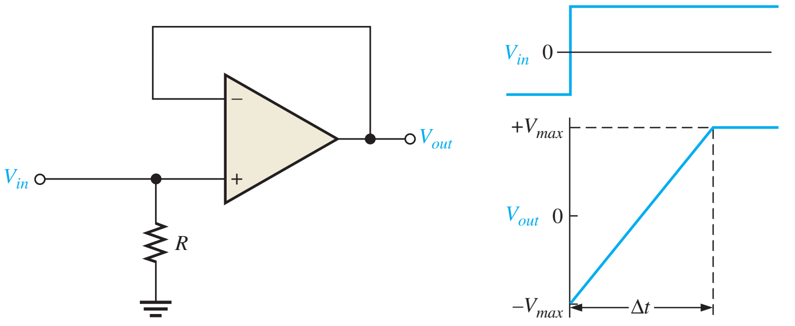
Op-amp output impedance.

Slew Rate The maximum rate of change of the output voltage in response to a step input voltage is the **slew rate** of an op-amp. The slew rate is dependent upon the high-frequency response of the amplifier stages within the op-amp.

Slew rate is measured with an op-amp connected as shown in Figure 12–11(a). This particular op-amp connection is a unity-gain, noninverting configuration that will be discussed in Section 12–4. It gives a worst-case (slowest) slew rate. Recall that the high-frequency components of a voltage step are contained in the rising edge and that the upper critical frequency of an amplifier limits its response to a step input. For a step input, the slope on the output is inversely proportional to the upper critical frequency. Slope increases as upper critical frequency decreases.

▶ FIGURE 12–11

Slew-rate measurement.



(a) Test circuit (b) Step input voltage and the resulting output voltage

A pulse is applied to the input and the resulting ideal output voltage is indicated in Figure 12–11(b). The width of the input pulse must be sufficient to allow the output to "slew" from its lower limit to its upper limit. A certain time interval, Δt, is required for the output voltage to go from its lower limit $-V_{max}$ to its upper limit $+V_{max}$, once the input step is applied. The slew rate is expressed as

Equation 12–7

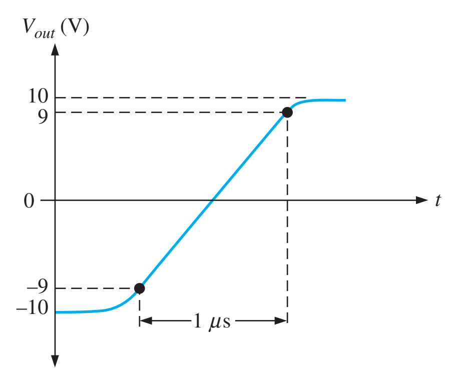
$$\textbf{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

where $\Delta V_{out} = +V_{max} - (-V_{max})$. The unit of slew rate is volts per microsecond (V/μs).

EXAMPLE 12–2

The output voltage of a certain op-amp appears as shown in Figure 12–12 in response to a step input. Determine the slew rate.

▶ FIGURE 12–12



Solution The output goes from the lower to the upper limit in 1 μs. Since this response is not ideal, the limits are taken at the 90% points, as indicated. So, the upper limit is +9 V and the lower limit is −9 V. The slew rate is

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t} = \frac{+9\text{ V} - (-9\text{ V})}{1\ \mu\text{s}} = \mathbf{18\ V/\mu s}$$

Related Problem When a pulse is applied to an op-amp, the output voltage goes from −8 V to +7 V in 0.75 μs. What is the slew rate?

Frequency Response The internal amplifier stages that make up an op-amp have voltage gains limited by junction capacitances, as discussed in Chapter 10. Although the differential amplifiers used in op-amps are somewhat different from the basic amplifiers discussed earlier, the same principles apply. An op-amp has no internal coupling capacitors, however; therefore, the low-frequency response extends down to dc (0 Hz).

Noise Specification Noise has become a more important issue in new circuit designs because of the requirement to run at lower voltages and with greater accuracy than in the past. As little as two or three microvolts can create errors in analog-to-digital conversion. Many sensors produce only tiny voltages that can be masked by noise. As a result, unwanted noise from op-amps and components can degrade the performance of circuits.

Noise is defined as an unwanted signal that affects the quality of a desired signal. While interference from an external source (such as a nearby power line) qualifies as noise, for the purpose of op-amp specifications, interference is not included. Only noise generated within the op-amp is considered in the noise specification. When the op-amp is added to a circuit, additional noise contributions are added from other circuit elements, such as the feedback resistors or any sensors. For example, all resistors generate thermal noise—even one sitting in the parts bin. The circuit designer must consider all sources within the circuit, but the concern here is the op-amp specification for noise, which only considers the op-amp.

There are two basic forms of noise. At low frequencies, noise is inversely proportional to the frequency; this is called $1/f$ noise or "pink noise". Above a critical noise frequency, the noise becomes flat and is spread out equally across the frequency spectrum; this is called "white noise". The power distribution of noise is measured in watts per hertz (W/Hz). Power is proportional to the square of the voltage, so noise voltage (density) is found by taking the square root of the noise power density, resulting in units of volts per square root hertz ($\text{V}/\sqrt{\text{Hz}}$). For operational amplifiers, noise level is normally shown with units of $\text{nV}/\sqrt{\text{Hz}}$ and is specified relative to the input at a specific frequency above the noise critical frequency. For example, a noise level graph for a very low-noise op-amp is shown in Figure 12–13; the specification for this op-amp will indicate that the input voltage noise density at 1 kHz is $1.1\ \text{nV}/\sqrt{\text{Hz}}$. At low frequencies, the noise level is higher than this due to the $1/f$ noise contribution as you can see from the graph.

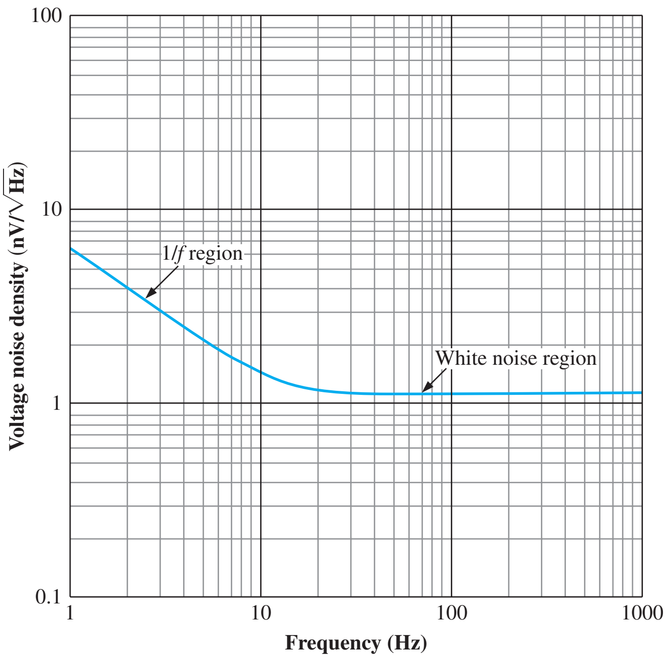


FIGURE 12–13

Noise as a function of frequency for a typical op-amp.

Comparison of Op-Amp Parameters

Table 12–1 provides a comparison of values showing selected parameters for some representative op-amps. As you can see from the table, there is a wide difference in certain specifications. All designs involve certain compromises, so in order for designers to optimize one parameter, they must often sacrifice another parameter. Choosing an op-amp for a particular application depends on which parameters are important to optimize. Parameters depend on the conditions for which they are measured. For details on any of these specifications, consult the datasheet.

Most available op-amps have three important features: short-circuit protection, no latch-up, and input offset nulling. Short-circuit protection keeps the circuit from being damaged if the output becomes shorted, and the no latch-up feature prevents the op-amp from hanging up in one output state (high or low voltage level) under certain input conditions. Input offset nulling is achieved by an external potentiometer that sets the output voltage at precisely zero with zero input.

▼ TABLE 12–1

OP-AMP	CMRR (dB) (TYP)	OPEN-LOOP GAIN (dB) (TYP)	GAIN-BANDWIDTH PRODUCT (MHz) (TYP)	INPUT OFFSET VOLTAGE (mV) (MAX)	INPUT BIAS CURRENT (nA) (MAX)	SLEW RATE (V/μs) (TYP)	COMMENT
AD8009	50	N/A	320[1]	5	150	5500	Extremely fast, low distortion, uses current feedback
AD8055	82	71		5	1200	1400	Low noise, fast, wide bandwidth, gain flatness 0.1 dB, video driver
ADA4891	68	90[2]		2500	0.002	170	CMOS-extremely low bias current, very fast, useful as video amplifier
ADA4092	85	118	1.3	0.2	50	0.4	Single supply (2.7 V to 36 V) or two supply operation, low power
FAN4931	73	102	4	6	0.005	3	Low cost CMOS, low power, output swings to within 10 mV of rail, extremely high input resistance
FHP3130	95	100	60	1	1800	110	High current output (to 100 mA)
FHP3350	90	55	190	1	50	800	High speed; useful as video amp
LM741C	70	106	1	6	500	0.5	General-purpose, overload protection, industry standard
LM7171	110	90	100	1.5	1000	3600	Very fast, high CMRR, useful as an instrumentation amplifier
LMH6629	87	79	800[3]	0.15	23000	530	Fast, ultra low noise, low voltage
OP177	130	142		0.01	1.5	0.3	Ultra-precision; very high CMRR and stability
OPA369	114	134	0.012	0.25	0.010	0.005	Extremely low power, low voltage, rail-to-rail.
OPA378	100	110	0.9	0.02	0.15	0.4	Precision, very low drift, low noise
OPA847	110	98	3900	0.1	42,000	950	Ultra low-noise, wide bandwidth amplifier, voltage feedback

[1] Depends on gain; gain = 10 is shown

[2] Depends on gain; gain = 2 is shown

[3] Small signal

SECTION 12–2 CHECKUP

1. Distinguish between single-ended and double-ended differential mode.
2. Define *common-mode rejection.*
3. For a given value of open-loop differential gain, does a higher common-mode gain result in a higher or lower CMRR?
4. List at least ten op-amp parameters.
5. How is slew rate measured?

12–3 NEGATIVE FEEDBACK

Negative feedback is one of the most useful concepts in electronics, particularly in op-amp applications. **Negative feedback** is the process whereby a portion of the output voltage of an amplifier is returned to the input with a phase angle that opposes (or subtracts from) the input signal.

After completing this section, you should be able to

- ☐ **Explain negative feedback in op-amps**
- ☐ Discuss why negative feedback is used
  - ◆ Describe the effects of negative feedback on certain op-amp parameters

Negative feedback is illustrated in Figure 12–14. The inverting (−) input effectively makes the feedback signal 180° out of phase with the input signal.

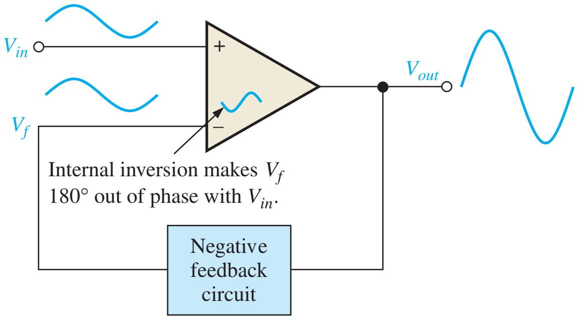

V_{in}
V_f
+
−
V_{out}
Internal inversion makes V_f 180° out of phase with V_{in}.
Negative feedback circuit

FIGURE 12–14

Illustration of negative feedback.

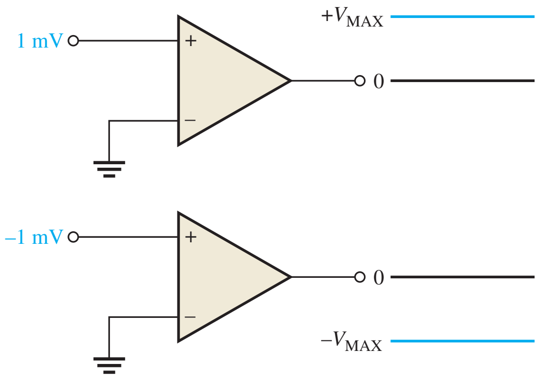
Why Use Negative Feedback?

As you can see in Table 12–1, the inherent open-loop voltage gain of a typical op-amp is very high (usually greater than 100,000). Therefore, an extremely small input voltage drives the op-amp into its saturated output states. In fact, even the input offset voltage of the op-amp can drive it into saturation. For example, assume $V_{IN} = 1$ mV and $A_{ol} = 100{,}000$. Then,

$$V_{IN}A_{ol} = (1\text{ mV})(100{,}000) = 100\text{ V}$$

Since the output level of an op-amp can never reach 100 V, it is driven deep into saturation and the output is limited to its maximum output levels, as illustrated in Figure 12–15 for both a positive and a negative input voltage of 1 mV.

The usefulness of an op-amp operated without negative feedback is generally limited to comparator applications (to be studied in Chapter 13). With negative feedback, the closed-loop voltage gain (A_{cl}) can be reduced and controlled so that the op-amp can function as a



▶ FIGURE 12–15

Without negative feedback, a small input voltage drives the op-amp to its output limits and it becomes nonlinear.

linear amplifier. In addition to providing a controlled, stable voltage gain, negative feedback also provides for control of the input and output impedances and amplifier bandwidth. Table 12–2 summarizes the general effects of negative feedback on op-amp performance.

▼ TABLE 2–2

	VOLTAGE GAIN	INPUT *Z*	OUTPUT *Z*	BANDWIDTH
Without negative feedback	A_{ol} is too high for linear amplifier applications	Relatively high (see Table 12–1)	Relatively low	Relatively narrow (because the gain is so high)
With negative feedback	A_{cl} is set to desired value by the feedback circuit	Can be increased or reduced to a desired value depending on type of circuit	Can be reduced to a desired value	Significantly wider

SECTION 12–3 CHECKUP

1. What are the benefits of negative feedback in an op-amp circuit?
2. Why is it generally necessary to reduce the gain of an op-amp from its open-loop value?

12–4 OP-AMPS WITH NEGATIVE FEEDBACK

An op-amp can be connected using negative feedback to stabilize the gain and increase frequency response. Negative feedback takes a portion of the output and applies it back out of phase with the input, creating an effective reduction in gain. This closed-loop gain is usually much less than the open-loop gain and independent of it.

After completing this section, you should be able to

- ❑ **Analyze op-amps with negative feedback**
- ❑ Discuss closed-loop voltage gain
- ❑ Identify and analyze the noninverting op-amp configuration
- ❑ Identify and analyze the voltage-follower configuration
- ❑ Identify and analyze the inverting amplifier configuration

Closed-Loop Voltage Gain, A_{cl}

The **closed-loop voltage gain** is the voltage gain of an op-amp with external feedback. The amplifier configuration consists of the op-amp and an external negative feedback circuit that connects the output to the inverting input. The closed-loop voltage gain is determined by the external component values and can be precisely controlled by them.

Noninverting Amplifier

An op-amp connected in a **closed-loop** configuration as a **noninverting amplifier** with a controlled amount of voltage gain is shown in Figure 12–16. The input signal is applied to the noninverting (+) input. The output is applied back to the inverting (−) input through the feedback circuit (closed loop) formed by the input resistor R_i and the feedback resistor R_f. This creates negative feedback as follows. Resistors R_i and R_f form a voltage-divider circuit, which reduces V_{out} and connects the reduced voltage V_f to the inverting input. The feedback voltage is expressed as

$$V_f = \left(\frac{R_i}{R_i + R_f}\right)V_{out}$$

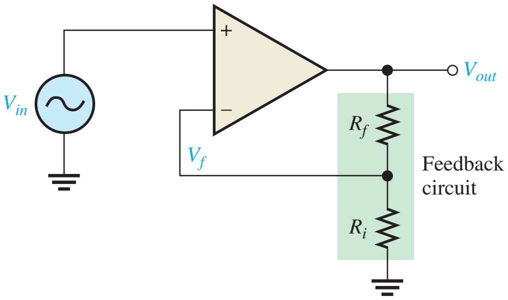


FIGURE 12–16

Noninverting amplifier.

The difference of the input voltage, V_{in}, and the feedback voltage, V_f, is the differential input to the op-amp, as shown in Figure 12–17. This differential voltage is amplified by the open-loop voltage gain of the op-amp (A_{ol}) and produces an output voltage expressed as

$$V_{out} = A_{ol}(V_{in} - V_f)$$

The attenuation, B, of the feedback circuit is

$$B = \frac{R_i}{R_i + R_f}$$

Substituting BV_{out} for V_f in the V_{out} equation,

$$V_{out} = A_{ol}(V_{in} - BV_{out})$$

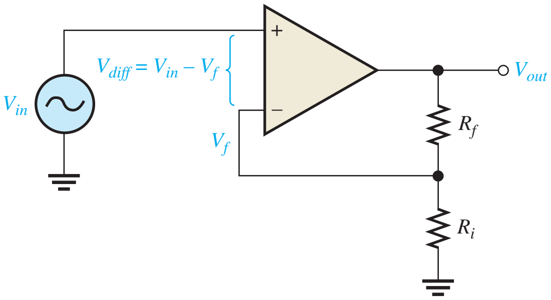


FIGURE 12–17

Differential input, $V_{in} - V_f$.

Then applying basic algebra,

$$V_{out} = A_{ol}V_{in} - A_{ol}BV_{out}$$
$$V_{out} + A_{ol}BV_{out} = A_{ol}V_{in}$$
$$V_{out}(1 + A_{ol}B) = A_{ol}V_{in}$$

Since the overall voltage gain of the amplifier in Figure 12–16 is V_{out}/V_{in}, it can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol}B}$$

The product $A_{ol}B$ is typically much greater than 1, so the equation simplifies to

$$\frac{V_{out}}{V_{in}} \cong \frac{A_{ol}}{A_{ol}B} = \frac{1}{B}$$

The closed-loop gain of the noninverting (NI) amplifier is the reciprocal of the attenuation (B) of the feedback circuit (voltage-divider).

$$A_{cl(\mathrm{NI})} = \frac{V_{out}}{V_{in}} \cong \frac{1}{B} = \frac{R_i + R_f}{R_i}$$

Therefore,

Equation 12–8

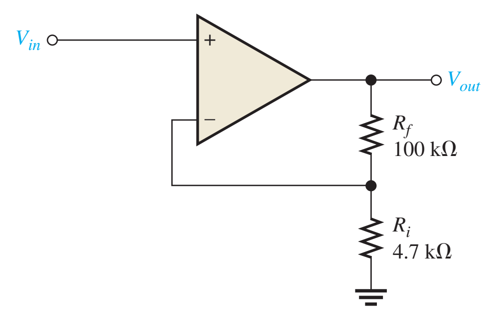
$$\boldsymbol{A_{cl(\mathrm{NI})} = 1 + \frac{R_f}{R_i}}$$

Notice that the closed-loop voltage gain is not at all dependent on the op-amp's open-loop voltage gain under the condition $A_{ol}B \gg 1$. The closed-loop gain can be set by selecting values of R_i and R_f.

EXAMPLE 12–3

Determine the closed-loop voltage gain of the amplifier in Figure 12–18.

▶ FIGURE 12–18



Solution This is a noninverting op-amp configuration. Therefore, the closed-loop voltage gain is

$$A_{cl(\mathrm{NI})} = 1 + \frac{R_f}{R_i} = 1 + \frac{100\ \mathrm{k}\Omega}{4.7\ \mathrm{k}\Omega} = \mathbf{22.3}$$

Related Problem If R_f in Figure 12–18 is increased to 150 kΩ, determine the closed-loop gain.

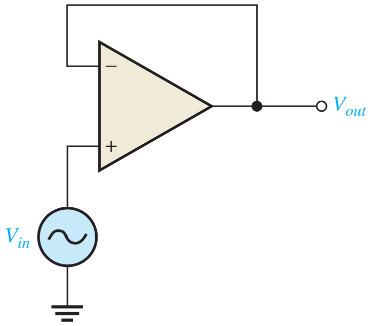
Open the Multisim file E12-03 in the Examples folder on the companion website. Measure the closed-loop voltage gain of the amplifier and compare with the calculated value.

Voltage-Follower

The **voltage-follower** configuration is a special case of the noninverting amplifier where all of the output voltage is fed back to the inverting (−) input by a straight connection, as shown in Figure 12–19. As you can see, the straight feedback connection has a voltage gain of 1 (which means there is no gain). The closed-loop voltage gain of a noninverting amplifier is $1/B$ as previously derived. Since $B = 1$ for a voltage-follower, the closed-loop voltage gain of the voltage-follower is

$$A_{cl(\mathrm{VF})} = 1$$

Equation 12–9



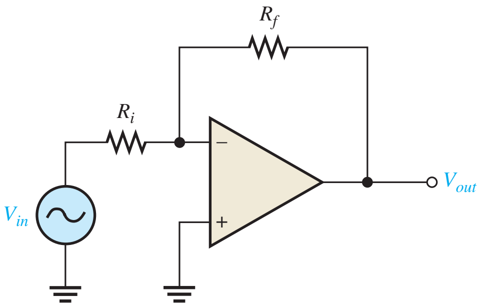
◀ FIGURE 12–19

Op-amp voltage-follower.

The most important features of the voltage-follower configuration are its very high input impedance and its very low output impedance. These features make it a nearly ideal buffer amplifier for interfacing high-impedance sources and low-impedance loads. This is discussed further in Section 12–5.

Inverting Amplifier

An op-amp connected as an **inverting amplifier** with a controlled amount of voltage gain is shown in Figure 12–20. The input signal is applied through a series input resistor R_i to the inverting (−) input. Also, the output is fed back through R_f to the same input. The noninverting (+) input is grounded.



◀ FIGURE 12–20

Inverting amplifier.

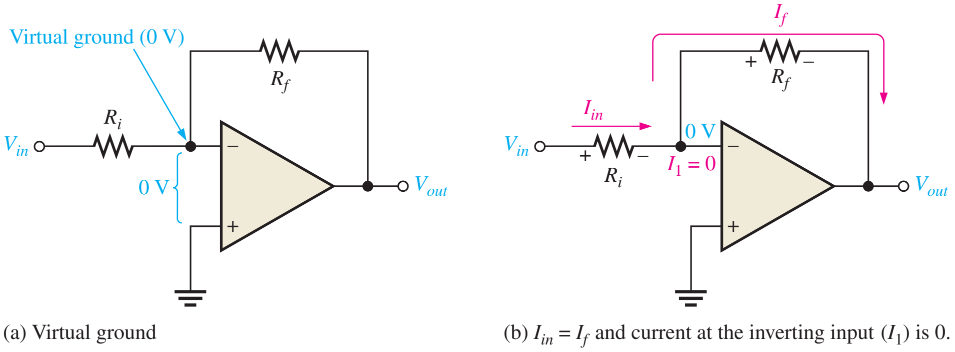
At this point, the ideal op-amp parameters mentioned earlier are useful in simplifying the analysis of this circuit. In particular, the concept of infinite input impedance is of great value. An infinite input impedance implies zero current at the inverting input. If there is zero current through the input impedance, then there must be *no* voltage drop between the inverting and noninverting inputs. This means that the voltage at the inverting (−) input is zero because the noninverting (+) input is grounded. This zero voltage at the inverting input terminal is referred to as *virtual ground.* This condition is illustrated in Figure 12–21(a).

Since there is no current at the inverting input, the current through R_i and the current through R_f are equal, as shown in Figure 12–21(b).

$$I_{in} = I_f$$

FIGURE 12–21

Virtual ground concept and closed-loop voltage gain development for the inverting amplifier.



(a) Virtual ground

(b) $I_{in} = I_f$ and current at the inverting input (I_1) is 0.

The voltage across R_i equals V_{in} because the resistor is connected to virtual ground at the inverting input of the op-amp. Therefore,

$$I_{in} = \frac{V_{in}}{R_i}$$

Also, the voltage across R_f equals $-V_{out}$ because of virtual ground, and therefore,

$$I_f = \frac{-V_{out}}{R_f}$$

Since $I_f = I_{in}$,

$$\frac{-V_{out}}{R_f} = \frac{V_{in}}{R_i}$$

Rearranging the terms,

$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

Of course, V_{out}/V_{in} is the overall gain of the inverting (I) amplifier.

Equation 12–10

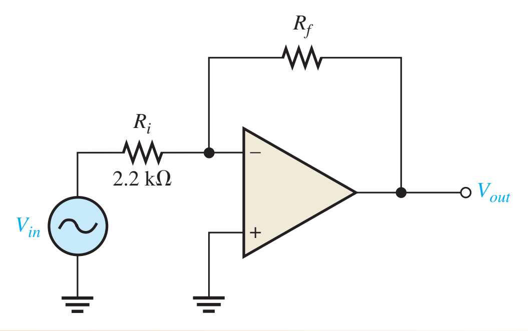
$$\boldsymbol{A_{cl(\mathrm{I})} = -\frac{R_f}{R_i}}$$

Equation 12–10 shows that the closed-loop voltage gain of the inverting amplifier ($A_{cl(\mathrm{I})}$) is the ratio of the feedback resistance (R_f) to the input resistance (R_i). *The closed-loop gain is independent of the op-amp's internal open-loop gain.* Thus, the negative feedback stabilizes the voltage gain. The negative sign indicates inversion.

EXAMPLE 12–4

Given the op-amp configuration in Figure 12–22, determine the value of R_f required to produce a closed-loop voltage gain of −100.

FIGURE 12–22



Solution Knowing that $R_i = 2.2\ \text{k}\Omega$ and the absolute value of the closed-loop gain is $|A_{cl(\text{I})}| = 100$, calculate R_f as follows:

$$|A_{cl(\text{I})}| = \frac{R_f}{R_i}$$

$$R_f = |A_{cl(\text{I})}|R_i = (100)(2.2\ \text{k}\Omega) = \mathbf{220\ k\Omega}$$

Related Problem If R_i is changed to 2.7 kΩ in Figure 12–22, what value of R_f is required to produce a closed-loop gain with an absolute value of 25?

Open the Multisim file E12-04 in the Examples folder on the companion website. The circuit has a value of R_f which was calculated to be 220 kΩ. Measure the closed-loop voltage gain and see if it agrees with the specified value.

SECTION 12–4 CHECKUP

1. What is the main purpose of negative feedback?
2. The closed-loop voltage gain of each of the op-amp configurations discussed is dependent on the internal open-loop voltage gain of the op-amp. (True or False)
3. The attenuation of the negative feedback circuit of a noninverting op-amp configuration is 0.02. What is the closed-loop gain of the amplifier?

12–5 Effects of Negative Feedback on Op-Amp Impedances

Negative feedback affects the input and output impedances of an op-amp. The effects on both inverting and noninverting amplifiers are examined in this section.

After completing this section, you should be able to

- **Discuss how negative feedback affects op-amp impedances**
- Analyze the noninverting amplifier impedances
  - Determine the input impedance
  - Determine the output impedance
- Analyze the voltage-follower impedances
  - Determine the input impedance and output impedance
- Analyze the inverting amplifier impedances
  - Determine the input impedance
  - Determine the output impedance

Impedances of the Noninverting Amplifier

Input Impedance The input impedance of a noninverting amplifier can be developed with the aid of Figure 12–23. For this analysis, assume a small differential voltage, V_d, exists between the two inputs, as indicated. This means that you cannot assume the op-amp's input impedance to be infinite or the input current to be zero. Express the input voltage as

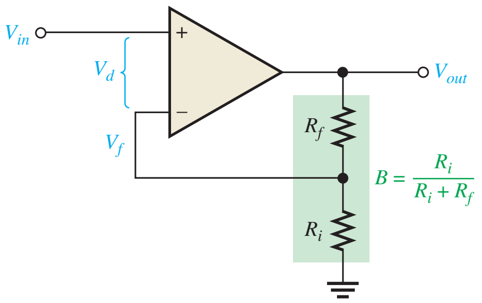
$$V_{in} = V_d + V_f$$

Substituting BV_{out} for the feedback voltage, V_f, yields

$$V_{in} = V_d + BV_{out}$$

Remember, B is the attenuation of the negative feedback circuit and is equal to $R_i/(R_i + R_f)$.

FIGURE 12–23



Since $V_{out} \cong A_{ol}V_d$ (A_{ol} is the open-loop gain of the op-amp),

$$V_{in} = V_d + A_{ol}BV_d = (1 + A_{ol}B)V_d$$

Now substituting $I_{in}Z_{in}$ for V_d,

$$V_{in} = (1 + A_{ol}B)I_{in}Z_{in}$$

where Z_{in} is the open-loop input impedance of the op-amp (without feedback connections).

$$\frac{V_{in}}{I_{in}} = (1 + A_{ol}B)Z_{in}$$

V_{in}/I_{in} is the overall input impedance of a closed-loop noninverting amplifier configuration.

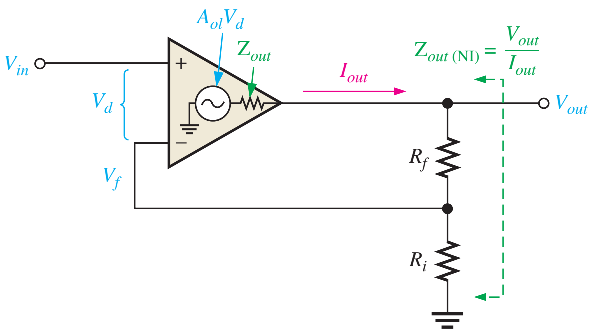
Equation 12–11

$$\mathbf{Z_{in(NI)} = (1 + A_{ol}B)Z_{in}}$$

This equation shows that the input impedance of the noninverting amplifier configuration with negative feedback is much greater than the internal input impedance of the op-amp itself (without feedback).

Output Impedance An expression for output impedance of a noninverting amplifier can be developed with the aid of Figure 12–24.

FIGURE 12–24



By applying Kirchhoff's voltage law to the output circuit,

$$V_{out} = A_{ol}V_d - Z_{out}I_{out}$$

The differential input voltage is $V_d = V_{in} - V_f$; therefore, by assuming that $A_{ol}V_d \gg Z_{out}I_{out}$, you can express the output voltage as

$$V_{out} \cong A_{ol}(V_{in} - V_f)$$

Substituting BV_{out} for V_f,

$$V_{out} \cong A_{ol}(V_{in} - BV_{out})$$

Expanding and factoring yields

$$V_{out} \cong A_{ol}V_{in} - A_{ol}BV_{out}$$

$$A_{ol}V_{in} \cong V_{out} + A_{ol}BV_{out} \cong (1 + A_{ol}B)V_{out}$$

Since the output impedance of the noninverting amplifier configuration is $Z_{out(\mathrm{NI})} = V_{out}/I_{out}$, you can substitute $I_{out}Z_{out(\mathrm{NI})}$ for V_{out}; therefore,

$$A_{ol}V_{in} = (1 + A_{ol}B)I_{out}Z_{out(\mathrm{NI})}$$

Dividing both sides of the previous expression by I_{out},

$$\frac{A_{ol}V_{in}}{I_{out}} = (1 + A_{ol}B)Z_{out(\mathrm{NI})}$$

The term on the left is the internal output impedance of the op-amp (Z_{out}) because, without feedback, $A_{ol}V_{in} = V_{out}$. Therefore,

$$Z_{out} = (1 + A_{ol}B)Z_{out(\mathrm{NI})}$$

Thus,

$$\boldsymbol{Z_{out(\mathrm{NI})} = \frac{Z_{out}}{1 + A_{ol}B}}$$

Equation 12–12

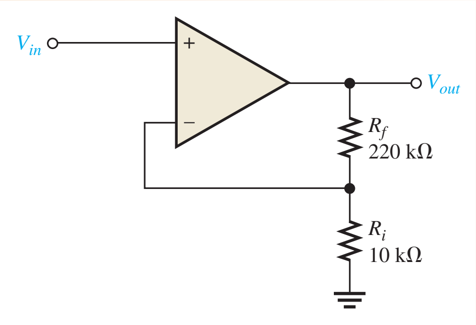
This equation shows that the output impedance of the noninverting amplifier configuration with negative feedback is much less than the internal output impedance, Z_{out}, of the op-amp itself (without feedback) because Z_{out} is divided by the factor $1 + A_{ol}B$.

EXAMPLE 12–5

(a) Determine the input and output impedances of the amplifier in Figure 12–25. The op-amp datasheet gives $Z_{in} = 2\ \mathrm{M\Omega}$, $Z_{out} = 75\ \Omega$, and $A_{ol} = 200{,}000$.

(b) Find the closed-loop voltage gain.

► FIGURE 12–25



Solution **(a)** The attenuation, B, of the feedback circuit is

$$B = \frac{R_i}{R_i + R_f} = \frac{10\ \mathrm{k\Omega}}{230\ \mathrm{k\Omega}} = 0.0435$$

$$Z_{in(\mathrm{NI})} = (1 + A_{ol}B)Z_{in} = [1 + (200{,}000)(0.0435)](2\ \mathrm{M\Omega})$$
$$= (1 + 8700)(2\ \mathrm{M\Omega}) = \mathbf{17.4\ G\Omega}$$

This is such a large number that, for all practical purposes, it can be assumed to be infinite as in the ideal case.

$$Z_{out(\mathrm{NI})} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{75\ \Omega}{1 + 8700} = \mathbf{8.6\ m\Omega}$$

This is such a small number that, for all practical purposes, it can be assumed to be zero as in the ideal case.

(b) $A_{cl(\mathrm{NI})} = 1 + \dfrac{R_f}{R_i} = 1 + \dfrac{220\ \mathrm{k\Omega}}{10\ \mathrm{k\Omega}} = \mathbf{23.0}$

Related Problem **(a)** Determine the input and output impedances in Figure 12–25 for op-amp datasheet values of $Z_{in} = 3.5\ \text{M}\Omega$, $Z_{out} = 82\ \Omega$, and $A_{ol} = 135{,}000$.

(b) Find A_{cl}.

Open the Multisim file E12-05 in the Examples folder on the companion website. Measure the closed-loop voltage gain and compare with the calculated value.

Voltage-Follower Impedances

Since a voltage-follower is a special case of the noninverting amplifier configuration, the same impedance formulas are used but with $B = 1$.

Equation 12–13

$$\mathbf{Z_{in(VF)} = (1 + A_{ol})Z_{in}}$$

Equation 12–14

$$\mathbf{Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}}}$$

As you can see, the voltage-follower input impedance is greater for a given A_{ol} and Z_{in} than for the noninverting amplifier configuration with the voltage-divider feedback circuit. Also, its output impedance is much smaller.

EXAMPLE 12–6 The op-amp in Example 12–5 is used in a voltage-follower configuration. Determine the input and output impedances.

Solution Since $B = 1$,

$$Z_{in(\text{VF})} = (1 + A_{ol})Z_{in} = (1 + 200{,}000)(2\ \text{M}\Omega) \cong \mathbf{400\ G\Omega}$$

$$Z_{out(\text{VF})} = \frac{Z_{out}}{1 + A_{ol}} = \frac{75\ \Omega}{1 + 200{,}000} = \mathbf{375\ \mu\Omega}$$

Notice that $Z_{in(\text{VF})}$ is much greater than $Z_{in(\text{NI})}$, and $Z_{out(\text{VF})}$ is much less than $Z_{out(\text{NI})}$ from Example 12–5. Again for all practical purposes, the ideal values can be assumed.

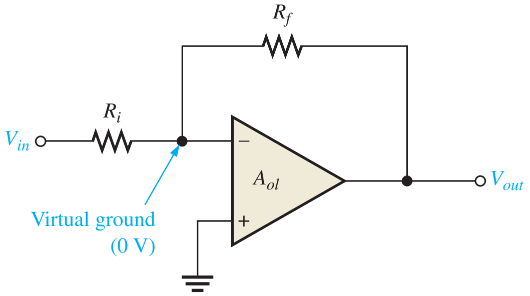
Related Problem If the op-amp in this example is replaced with one having a higher open-loop gain, how are the input and output impedances affected?

Impedances of the Inverting Amplifier

The input and output impedances of an inverting op-amp configuration are developed with the aid of Figure 12–26. Both the input signal and the negative feedback are applied, through resistors, to the inverting (−) terminal as shown.

▶ FIGURE 12–26

Inverting amplifier.

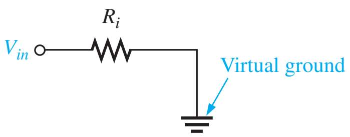


Input Impedance The input impedance for an inverting amplifier is

$$\boldsymbol{Z_{in(\mathrm{I})} \cong R_i}$$

Equation 12–15

This is because the inverting input of the op-amp is at virtual ground (0 V), and the input source simply sees R_i to ground, as shown in Figure 12–27.



▲ FIGURE 12–27

Output Impedance As with a noninverting amplifier, the output impedance of an inverting amplifier is decreased by the negative feedback. In fact, the expression is the same as for the noninverting case.

$$\boldsymbol{Z_{out(\mathrm{I})} = \frac{Z_{out}}{1 + A_{ol}B}}$$

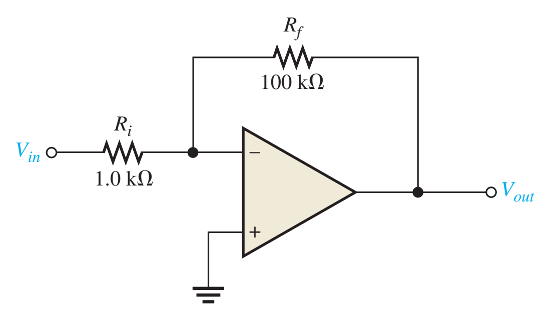
Equation 12–16

The output impedance of both the noninverting and the inverting amplifier configurations is very low; in fact, it is almost zero in practical cases. Because of this near zero output impedance, any load impedance within limits can be connected to the op-amp output and not change the output voltage. The limits for the load impedance are determined by the maximum peak-to-peak swing of the output ($V_{O(\text{p-p})}$) and the current limit of the op-amp.

EXAMPLE 12–7

Find the values of the input and output impedances in Figure 12–28. Also, determine the closed-loop voltage gain. The op-amp has the following parameters: $A_{ol} = 50{,}000$; $Z_{in} = 4\ \mathrm{M}\Omega$; and $Z_{out} = 50\ \Omega$.

► FIGURE 12–28



Solution

$$Z_{in(\mathrm{I})} \cong R_i = \mathbf{1.0\ k\Omega}$$

The feedback attenuation, B, is

$$B = \frac{R_i}{R_i + R_f} = \frac{1.0\ \mathrm{k}\Omega}{101\ \mathrm{k}\Omega} = 0.001$$

Then

$$Z_{out(\mathrm{I})} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{50\ \Omega}{1 + (50{,}000)(0.001)}$$

$$= \mathbf{980\ m\Omega}\ \text{(zero for all practical purposes)}$$

The closed-loop voltage gain is

$$A_{cl(\mathrm{I})} = -\frac{R_f}{R_i} = -\frac{100\ \mathrm{k}\Omega}{1.0\ \mathrm{k}\Omega} = \mathbf{-100}$$

Related Problem Determine the input and output impedances and the closed-loop voltage gain in Figure 12–28. The op-amp parameters and circuit values are as follows: $A_{ol} = 100{,}000$; $Z_{in} = 5\ \text{M}\Omega$; $Z_{out} = 75\ \Omega$; $R_i = 560\ \Omega$; and $R_f = 82\ \text{k}\Omega$.

Open the Multisim file E12-07 in the Examples folder on the companion website and measure the closed-loop voltage gain. Compare to the calculated result.

SECTION 12–5 CHECKUP

1. How does the input impedance of a noninverting amplifier configuration compare to the input impedance of the op-amp itself?
2. When an op-amp is connected in a voltage-follower configuration, does the input impedance increase or decrease?
3. Given that $R_f = 100\ \text{k}\Omega$; $R_i = 2\ \text{k}\Omega$; $A_{ol} = 120{,}000$; $Z_{in} = 2\ \text{M}\Omega$; and $Z_{out} = 60\ \Omega$, what are $Z_{in(\text{I})}$ and $Z_{out(\text{I})}$ for an inverting amplifier configuration?

12–6 BIAS CURRENT AND OFFSET VOLTAGE

Certain deviations from the ideal op-amp must be recognized because of their effects on its operation. Transistors within the op-amp must be biased so that they have the correct values of base and collector currents and collector-to-emitter voltages. The ideal op-amp has no input current at its terminals; but in fact, the practical op-amp has small input bias currents typically in the nA range. Also, small internal imbalances in the transistors effectively produce a small offset voltage between the inputs. These nonideal parameters were described in Section 12–2.

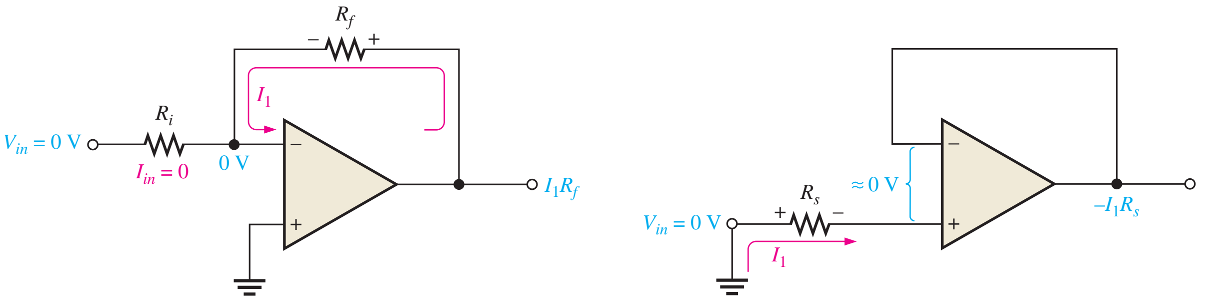
After completing this section, you should be able to

- **Discuss bias current and offset voltage**
- Describe the effect of input bias current
- Discuss bias current compensation
  - Explain bias current compensation in the voltage-follower
  - Explain bias current compensation in the noninverting and inverting amplifiers
  - Discuss the use of a BIFET
- Describe the effect of input offset voltage
- Discuss input offset voltage compensation

Effect of Input Bias Current

Figure 12–29(a) is an inverting amplifier with zero input voltage. Ideally, the current through R_i is zero because the input voltage is zero and the voltage at the inverting (−) terminal is zero. The small input bias current, I_1, is through R_f from the output terminal. I_1 creates a voltage drop across R_f, as indicated. The positive side of R_f is the output terminal, and therefore, the output error voltage is I_1R_f when it should be zero.

Figure 12–29(b) is a voltage-follower with zero input voltage and a source resistance, R_s. In this case, an input bias current, I_1, produces a drop across R_s and creates an output voltage error as shown. The voltage at the inverting input terminal decreases to $-I_1R_s$ because the negative feedback tends to maintain a differential voltage of zero, as indicated. Since the



(a) Input bias current creates output error voltage (I_1R_f) in an inverting amplifier.

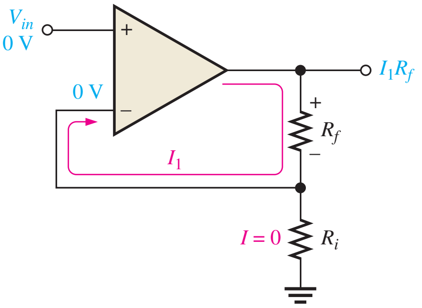
(b) Input bias current creates output error voltage in a voltage-follower.

▲ **FIGURE 12–29**

Effects of bias currents.

inverting terminal is connected directly to the output terminal, the output error voltage is $-I_1R_s$.

Figure 12–30 is a noninverting amplifier with zero input voltage. Ideally, the voltage at the inverting terminal is also zero, as indicated. The input bias current, I_1, produces a voltage drop across R_f and thus creates an output error voltage of I_1R_f, just as with the inverting amplifier.



◀ **FIGURE 12–30**

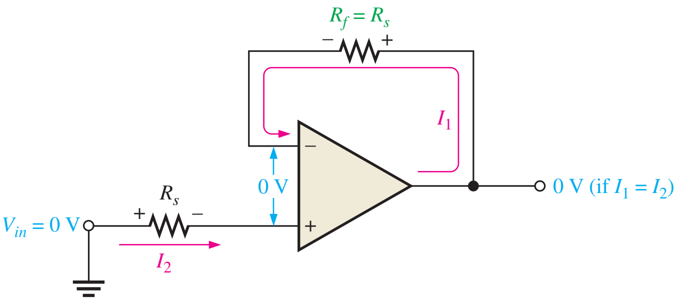
Input bias current creates output error voltage in a noninverting amplifier.

Bias Current Compensation

Voltage-Follower The output error voltage due to bias currents in a voltage-follower can be sufficiently reduced by adding a resistor, R_f, equal to the source resistance, R_s, in the feedback path, as shown in Figure 12–31. The voltage drop created by I_1 across the added resistor subtracts from the $-I_2R_s$ output error voltage. If $I_1 = I_2$, then the output voltage is zero. Usually I_1 does not quite equal I_2; but even in this case, the output error voltage is reduced as follows because I_{OS} is less than I_2.

$$V_{OUT(error)} = |I_1 - I_2|R_s = I_{OS}R_s$$

where I_{OS} is the input offset current.



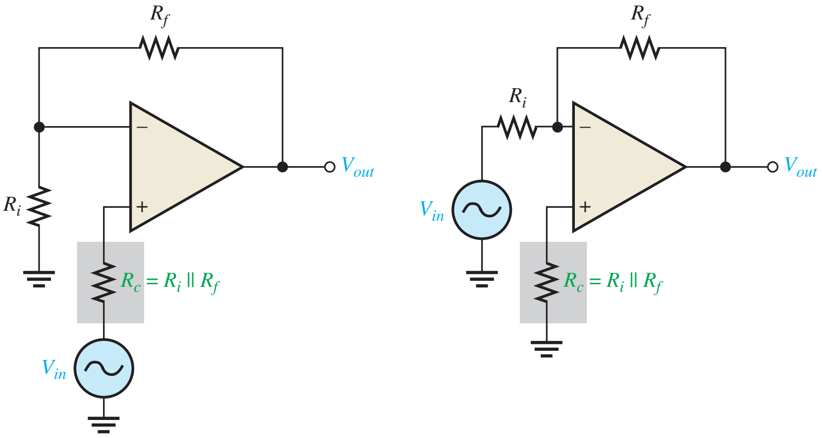
◀ **FIGURE 12–31**

Bias current compensation in a voltage-follower.

Noninverting and Inverting Amplifiers To compensate for the effect of bias current in the noninverting amplifier, a resistor R_c is added, as shown in Figure 12–32(a). The compensating resistor value equals the parallel combination of R_i and R_f. The input current creates a voltage drop across R_c that offsets the voltage across the combination of R_i and R_f, thus sufficiently reducing the output error voltage. The inverting amplifier is similarly compensated, as shown in Figure 12–32(b).

▶ **FIGURE 12–32**

Bias current compensation in the noninverting and inverting amplifier configurations.



(a) Noninverting amplifier

(b) Inverting amplifier

Use of a BIFET Op-Amp to Eliminate the Need for Bias Current Compensation The BIFET op-amp uses both BJTs and JFETs in its internal circuitry. The JFETs are used as the input devices to achieve a higher input impedance than is possible with standard BJT amplifiers. Because of their very high input impedance, BIFETs typically have input bias currents that are much smaller than in BJT op-amps, thus reducing or eliminating the need for bias current compensation.

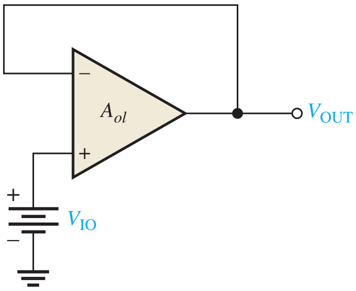
Effect of Input Offset Voltage

The output voltage of an op-amp should be zero when the differential input is zero. However, there is always a small output error voltage present whose value typically ranges from microvolts to millivolts. This is due to unavoidable imbalances within the internal op-amp transistors aside from the bias currents previously discussed. In a negative feedback configuration, the input offset voltage V_{IO} can be visualized as an equivalent small dc voltage source, as illustrated in Figure 12–33 for a voltage-follower. Generally, the output error voltage due to the input offset voltage is

$$V_{OUT(error)} = A_{cl}V_{IO}$$

For the case of the voltage-follower, $A_{cl} = 1$, so

$$V_{OUT(error)} = V_{IO}$$

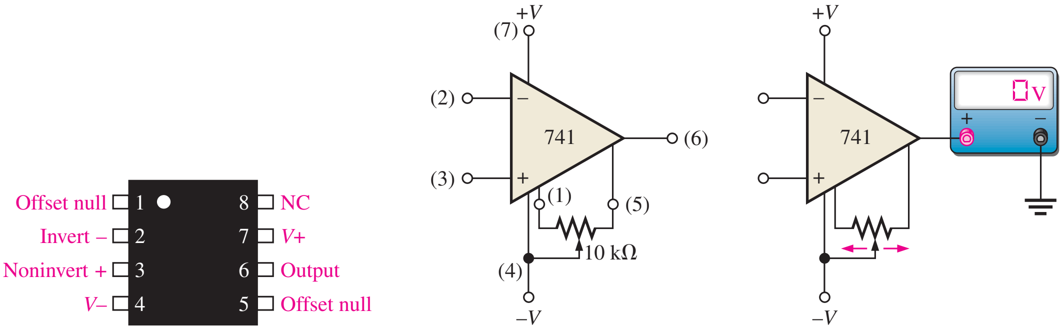


▲ **FIGURE 12–33**

Input offset voltage equivalent.

Input Offset Voltage Compensation

Most integrated circuit op-amps provide a means of compensating for offset voltage. This is usually done by connecting an external potentiometer to designated pins on the IC package, as illustrated in Figure 12–34(a) and (b) for a 741 op-amp. The two terminals are labelled *offset null*. With no input, the potentiometer is simply adjusted until the output voltage reads 0, as shown in Figure 12–34(c).



(a) 8-pin DIP or SMT package (b) External potentiometer (c) Adjust for zero output

▲ FIGURE 12–34

Input offset voltage compensation for a 741 op-amp.

SECTION 12–6 CHECKUP

1. What are two sources of dc output error voltages?
2. How do you compensate for bias current in a voltage-follower?

12–7 OPEN-LOOP FREQUENCY AND PHASE RESPONSES

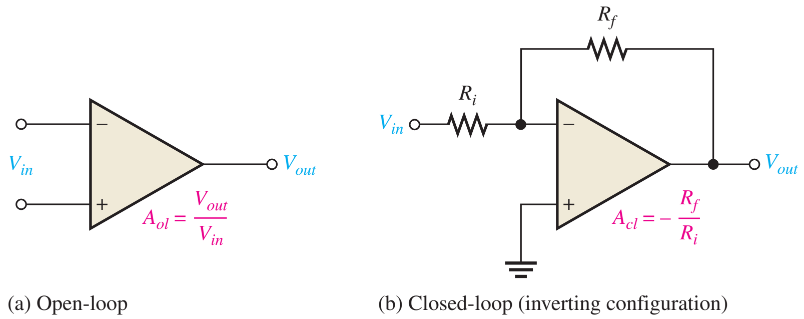
In this section, the open-loop frequency response and the open-loop phase response of an op-amp are covered. Open-loop responses relate to an op-amp with no external feedback. The frequency response indicates how the voltage gain changes with frequency, and the phase response indicates how the phase shift between the input and output signal changes with frequency. The open-loop gain, like the β of a transistor, varies greatly from one device to the next of the same type and cannot be depended upon to have a constant value.

After completing this section, you should be able to

- **Analyze the open-loop frequency response of an op-amp**
- Review and discuss op-amp voltage gains
- Discuss bandwidth limitations
  - Define the 3-dB open-loop bandwidth
  - Define the unity-gain bandwidth
- Analyze the gain vs. frequency
- Analyze the phase shift
- Discuss the overall frequency response
- Discuss the overall phase response

Review of Op-Amp Voltage Gains

Figure 12–35 illustrates the open-loop and closed-loop amplifier configurations. As shown in part (a), the open-loop voltage gain, A_{ol}, of an op-amp is the internal voltage gain of the device and represents the ratio of output voltage to input voltage. Notice that there are no external components, so the open-loop voltage gain is set entirely by the internal design. In the closed-loop op-amp configuration shown in part (b), the closed-loop voltage gain, A_{cl}, is the voltage gain of an op-amp with external feedback. The closed-loop voltage gain is


V_{in}
V_{out}
$A_{ol} = \frac{V_{out}}{V_{in}}$
R_f
R_i
$A_{cl} = -\frac{R_f}{R_i}$
–
+

(a) Open-loop (b) Closed-loop (inverting configuration)

▲ FIGURE 12–35

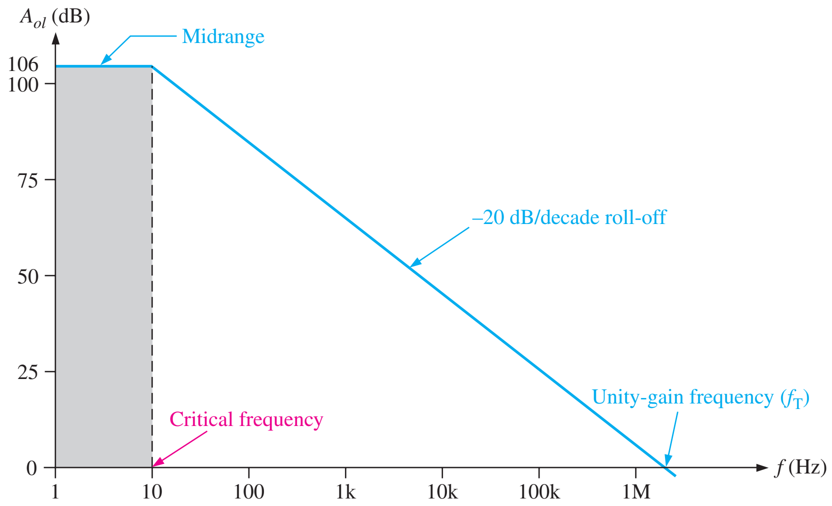
Open-loop and closed-loop op-amp configurations.

determined by the external component values for an inverting amplifier configuration and is always less than the open-loop gain. The closed-loop voltage gain can be precisely controlled by external component values. The closed-loop response of op-amps is covered in Section 12–8.

Bandwidth Limitations

In the previous sections, all of the voltage gain expressions were based on the midrange gain and were considered independent of the frequency. The midrange open-loop gain of an op-amp extends from zero frequency (dc) up to a critical frequency at which the gain is 3 dB less than the midrange value. This concept should be familiar from your study of Chapter 10. Op-amps are dc amplifiers (no capacitive coupling between stages), and therefore, there is no lower critical frequency. This means that the midrange gain extends down to zero frequency (dc), and dc voltages are amplified the same as midrange signal frequencies.

An open-loop response curve (Bode plot) for a certain op-amp is shown in Figure 12–36. Most op-amp datasheets show this type of curve or specify the midrange open-loop gain. Notice that the curve rolls off (decreases) at −20 dB per decade (−6 dB per octave). The midrange gain is 200,000, which is 106 dB, and the critical (cutoff) frequency is approximately 10 Hz.



▲ FIGURE 12–36

Ideal plot of open-loop voltage gain versus frequency for a typical op-amp. The frequency scale is logarithmic.

3 dB Open-Loop Bandwidth Recall from Chapter 10 that the bandwidth of an ac amplifier is the frequency range between the points where the gain is 3 dB less than the midrange gain. In general, the bandwidth equals the upper critical frequency (f_{cu}) minus the lower critical frequency (f_{cl}).

$$BW = f_{cu} - f_{cl}$$

Since f_{cl} for an op-amp is zero, the bandwidth is simply equal to the upper critical frequency.

$$\mathbf{BW = f_{cu}}$$

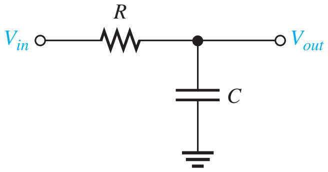
Equation 12–17

From now on, we will refer to f_{cu} as simply f_c; and we will use open-loop (ol) or closed-loop (cl) subscript designators, for example, $f_{c(ol)}$.

Unity-Gain Bandwidth Notice in Figure 12–36 that the gain steadily decreases to a point where it is equal to unity (1 or 0 dB). The value of the frequency at which this unity gain occurs is the *unity-gain frequency* designated f_T. f_T is also called the *unity-gain bandwidth*.

Gain-Versus-Frequency Analysis

The *RC* lag (low-pass) circuits within an op-amp are responsible for the roll-off in gain as the frequency increases, just as was discussed for the discrete amplifiers in Chapter 10. From basic ac circuit theory, the attenuation of an *RC* lag circuit, such as in Figure 12–37, is expressed as



▲ FIGURE 12–37

RC lag circuit.

$$\frac{V_{out}}{V_{in}} = \frac{X_C}{\sqrt{R^2 + X_C^2}}$$

Dividing both the numerator and denominator to the right of the equals sign by X_C,

$$\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + R^2/X_C^2}}$$

The critical frequency of an *RC* circuit is

$$f_c = \frac{1}{2\pi RC}$$

Dividing both sides by f gives

$$\frac{f_c}{f} = \frac{1}{2\pi RCf} = \frac{1}{(2\pi fC)R}$$

Since $X_C = 1/(2\pi fC)$, the previous expression can be written as

$$\frac{f_c}{f} = \frac{X_C}{R}$$

Substituting this result in the previous equation for V_{out}/V_{in} produces the following expression for the attenuation of an *RC* lag circuit in terms of frequency:

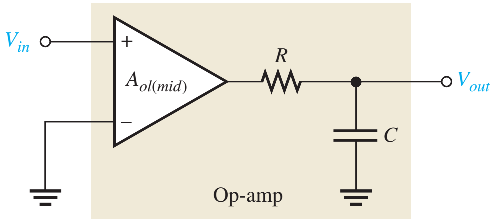
$$\mathbf{\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + f^2/f_c^2}}}$$

Equation 12–18

If an op-amp is represented by a voltage gain element with a gain of $A_{ol(mid)}$ plus a single *RC* lag circuit, as shown in Figure 12–38, it is known as a compensated op-amp. The total open-loop gain of the op-amp is the product of the midrange open-loop gain, $A_{ol(mid)}$, and the attenuation of the *RC* circuit.

▶ FIGURE 12–38

Op-amp represented by a gain element and an internal *RC* circuit.



Equation 12–19

$$\boldsymbol{A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}}$$

As you can see from Equation 12–19, the open-loop gain equals the midrange gain when the signal frequency f is much less than the critical frequency f_c and drops off as the frequency increases. Since f_c is part of the open-loop response of an op-amp, we will refer to it as $f_{c(ol)}$.

The following example demonstrates how the open-loop gain decreases as the frequency increases above $f_{c(ol)}$.

EXAMPLE 12–8

Determine A_{ol} for the following values of f. Assume $f_{c(ol)} = 100$ Hz and $A_{ol(mid)} = 100{,}000$.

(a) $f = 0$ Hz **(b)** $f = 10$ Hz **(c)** $f = 100$ Hz **(d)** $f = 1000$ Hz

Solution

(a) $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_{c(ol)}^2}} = \frac{100{,}000}{\sqrt{1 + 0}} = \mathbf{100{,}000}$

(b) $A_{ol} = \frac{100{,}000}{\sqrt{1 + (0.1)^2}} = \mathbf{99{,}503}$

(c) $A_{ol} = \frac{100{,}000}{\sqrt{1 + (1)^2}} = \frac{100{,}000}{\sqrt{2}} = \mathbf{70{,}710}$

(d) $A_{ol} = \frac{100{,}000}{\sqrt{1 + (10)^2}} = \mathbf{9950}$

Related Problem

Find A_{ol} for the following frequencies. Assume $f_{c(ol)} = 200$ Hz and $A_{ol(mid)} = 80{,}000$.

(a) $f = 2$ Hz **(b)** $f = 10$ Hz **(c)** $f = 2500$ Hz

Phase Shift

As you know from Chapter 10, an *RC* circuit causes a propagation delay from input to output, thus creating a **phase shift** between the input signal and the output signal. An *RC* lag circuit such as found in an op-amp stage causes the output signal voltage to lag the input, as shown in Figure 12–39. From basic ac circuit theory, the phase shift, θ, is

$$\theta = -\tan^{-1}\left(\frac{R}{X_C}\right)$$

Since $R/X_C = f/f_c$,

Equation 12–20

$$\boldsymbol{\theta = -\tan^{-1}\left(\frac{f}{f_c}\right)}$$

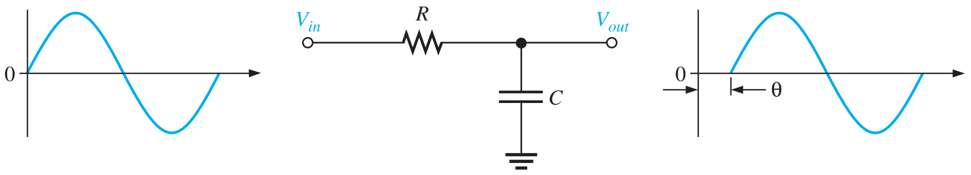


FIGURE 12–39

Output voltage lags input voltage.

The negative sign indicates that the output lags the input. This equation shows that the phase shift increases with frequency and approaches $-90°$ as f becomes much greater than f_c.

EXAMPLE 12–9

Calculate the phase shift for an *RC* lag circuit for each of the following frequencies, and then plot the curve of phase shift versus frequency. Assume $f_c = 100$ Hz.

(a) $f = 1$ Hz **(b)** $f = 10$ Hz **(c)** $f = 100$ Hz
(d) $f = 1000$ Hz **(e)** $f = 10{,}000$ Hz

Solution

(a) $\theta = -\tan^{-1}\left(\frac{f}{f_c}\right) = -\tan^{-1}\left(\frac{1\text{ Hz}}{100\text{ Hz}}\right) = \mathbf{-0.573°}$

(b) $\theta = -\tan^{-1}\left(\frac{10\text{ Hz}}{100\text{ Hz}}\right) = \mathbf{-5.71°}$

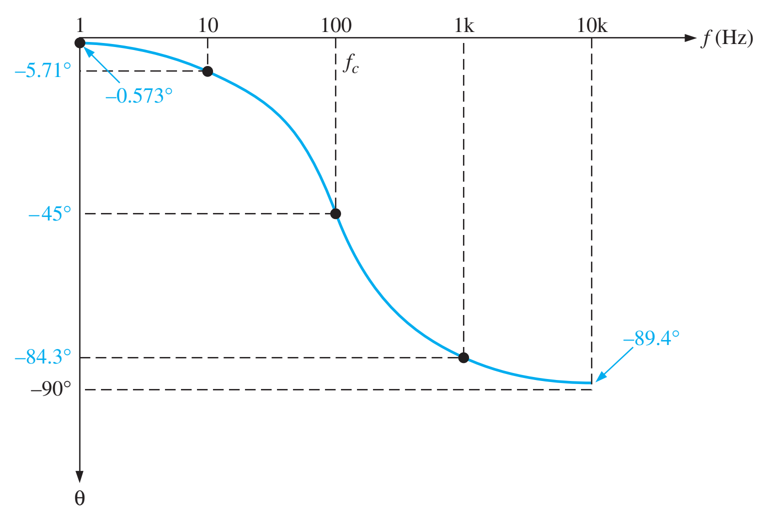
(c) $\theta = -\tan^{-1}\left(\frac{100\text{ Hz}}{100\text{ Hz}}\right) = \mathbf{-45°}$

(d) $\theta = -\tan^{-1}\left(\frac{1000\text{ Hz}}{100\text{ Hz}}\right) = \mathbf{-84.3°}$

(e) $\theta = -\tan^{-1}\left(\frac{10{,}000\text{ Hz}}{100\text{ Hz}}\right) = \mathbf{-89.4°}$

The phase shift-versus-frequency curve is plotted in Figure 12–40. Note that the frequency axis is logarithmic.

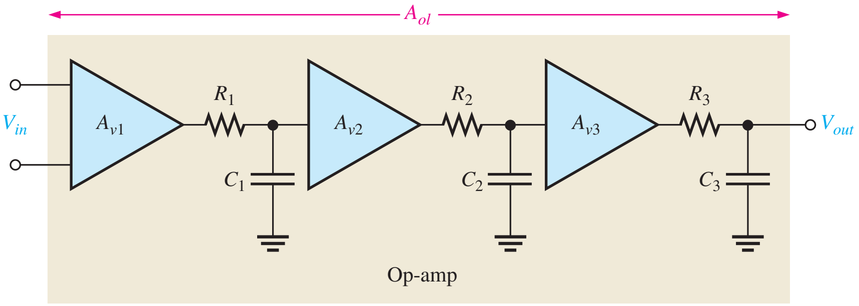
FIGURE 12–40



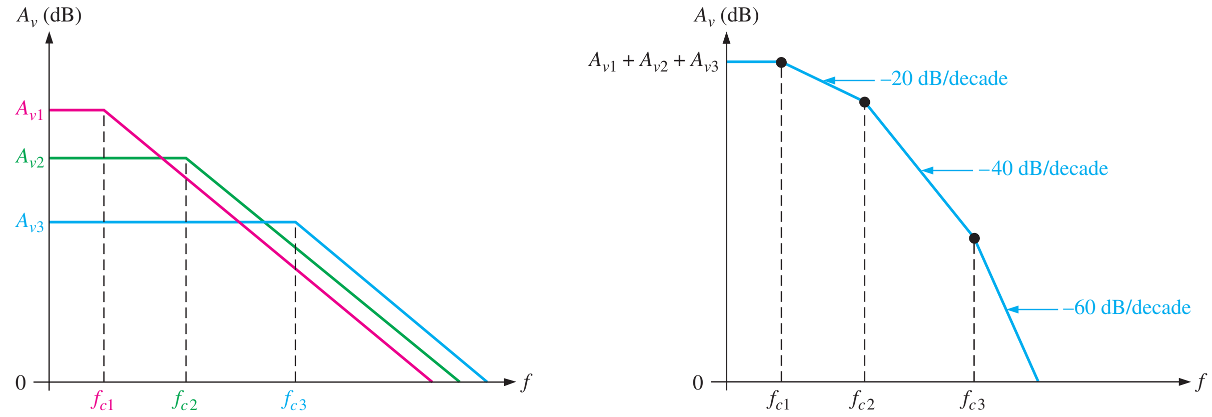
Related Problem At what frequency, in this example, is the phase shift 60°?

Overall Frequency Response

Previously, an op-amp was defined to have a constant roll-off of −20 dB/decade above its critical frequency. For most op-amps this is the case; for some, however, the situation is more complex. The more complex IC operational amplifier may consist of two or more cascaded amplifier stages. The gain of each stage is frequency dependent and rolls off at −20 dB/decade above its critical frequency. Therefore, the total response of an op-amp is a composite of the individual responses of the internal stages. As an example, a three-stage op-amp is represented in Figure 12–41(a), and the frequency response of each stage is shown in Figure 12–41(b). As you know, dB gains are added so that the total op-amp frequency response is as shown in Figure 12–41(c). Since the roll-off rates are additive, the total roll-off rate increases by −20 dB/decade (−6 dB/decade) as each critical frequency is reached.



(a) Representation of an op-amp with three internal stages



(b) Individual responses

(c) Composite response

▲ **FIGURE 12–41**

Op-amp open-loop frequency response.

Overall Phase Response

In a multistage amplifier, each stage contributes to the total phase lag. As you have seen, each *RC* lag circuit can produce up to a −90° phase shift. Since each stage in an op-amp includes an *RC* lag circuit, a three-stage op-amp, for example, can have a maximum phase lag of −270°. Also, the phase lag of each stage is less than −45° when the frequency is below the critical frequency, equal to −45° at the critical frequency, and greater than −45° when the frequency is above the critical frequency. The phase lags of the stages of an op-amp are added to produce a total phase lag, according to the following formula for three stages:

$$\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$$

EXAMPLE 12–10

A certain op-amp has three internal amplifier stages with the following gains and critical frequencies:

Stage 1: $A_{v1} = 40\text{ dB}, f_{c1} = 2\text{ kHz}$

Stage 2: $A_{v2} = 32\text{ dB}, f_{c2} = 40\text{ kHz}$

Stage 3: $A_{v3} = 20\text{ dB}, f_{c3} = 150\text{ kHz}$

Determine the open-loop midrange gain in decibels and the total phase lag when $f = f_{c1}$.

Solution

$$A_{ol(mid)} = A_{v1} + A_{v2} + A_{v3} = 40\text{ dB} + 32\text{ dB} + 20\text{ dB} = 92\text{ dB}$$

$$\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$$

$$= -\tan^{-1}(1) - \tan^{-1}\left(\frac{2}{40}\right) - \tan^{-1}\left(\frac{2}{150}\right) = -45^\circ - 2.86^\circ - 0.76^\circ = \mathbf{-48.6^\circ}$$

Related Problem

The internal stages of a two-stage amplifier have the following characteristics: $A_{v1} = 50\text{ dB}, A_{v2} = 25\text{ dB}, f_{c1} = 1500\text{ Hz}$, and $f_{c2} = 3000\text{ Hz}$. Determine the open-loop midrange gain in decibels and the total phase lag when $f = f_{c1}$.

SECTION 12–7 CHECKUP

1. How do the open-loop voltage gain and the closed-loop voltage gain of an op-amp differ?
2. The upper critical frequency of a particular op-amp is 100 Hz. What is its open-loop 3 dB bandwidth?
3. Does the open-loop gain increase or decrease with frequency above the critical frequency?
4. If the individual stage gains of an op-amp are 20 dB and 30 dB, what is the total gain in decibels?
5. If the individual phase lags are −49° and −5.2°, what is the total phase lag?

12–8 CLOSED-LOOP FREQUENCY RESPONSE

Op-amps are normally used in a closed-loop configuration with negative feedback in order to achieve precise control of the gain and bandwidth. In this section, you will see how feedback affects the gain and frequency response of an op-amp.

After completing this section, you should be able to

- **Analyze the closed-loop frequency response of an op-amp**
  - Review the closed-loop voltage gain for each op-amp configuration
- Analyze the effect of negative feedback on bandwidth
- Define and discuss the gain-bandwidth product

Recall that midrange gain of an op-amp is reduced by negative feedback, as indicated by the following closed-loop gain expressions for the three amplifier configurations previously covered, where B is the feedback attenuation. For a noninverting amplifier,

$$A_{cl(\mathrm{NI})} = \frac{A_{ol}}{1 + A_{ol}B} \cong \frac{1}{B} = 1 + \frac{R_f}{R_i}$$

For an inverting amplifier,

$$A_{cl(\mathrm{I})} \cong -\frac{R_f}{R_i}$$

For a voltage-follower,

$$A_{cl(\mathrm{VF})} = 1$$

Effect of Negative Feedback on Bandwidth

You know how negative feedback affects the gain; now you will learn how it affects the amplifier's bandwidth. The closed-loop critical frequency of an op-amp is

Equation 12–21

$$\boldsymbol{f_{c(cl)} = f_{c(ol)}(1 + BA_{ol(mid)})}$$

This expression shows that the closed-loop critical frequency, $f_{c(cl)}$, is higher than the open-loop critical frequency $f_{c(ol)}$ by the factor $1 + BA_{ol(mid)}$. You will find a derivation of Equation 12–21 in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd.

Since $f_{c(cl)}$ equals the bandwidth for the closed-loop amplifier, the closed-loop bandwidth (BW_{cl}) is also increased by the same factor.

Equation 12–22

$$\boldsymbol{BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})}$$

EXAMPLE 12–11

A certain amplifier has an open-loop midrange gain of 150,000 and an open-loop 3 dB bandwidth of 200 Hz. The attenuation (B) of the feedback loop is 0.002. What is the closed-loop bandwidth?

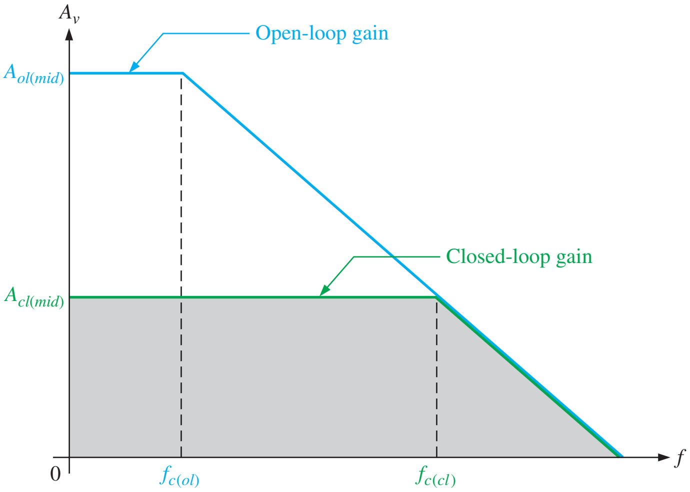
Solution $BW_{cl} = BW_{ol}(1 + BA_{ol(mid)}) = 200\text{ Hz}[1 + (0.002)(150{,}000)] = \mathbf{60.2\text{ kHz}}$

Related Problem If $A_{ol(mid)} = 200{,}000$ and $B = 0.05$, what is the closed-loop bandwidth?

Figure 12–42 graphically illustrates the concept of closed-loop response. When the open-loop gain of an op-amp is reduced by negative feedback, the bandwidth is increased.

▶ **FIGURE 12–42**

Closed-loop gain compared to open-loop gain.



The closed-loop gain is independent of the open-loop gain up to the point of intersection of the two gain curves. This point of intersection is the critical frequency, $f_{c(cl)}$, for the closed-loop response. Notice that the closed-loop gain has the same roll-off rate as the open-loop gain, beyond the closed-loop critical frequency.

Gain-Bandwidth Product

An increase in closed-loop gain causes a decrease in the bandwidth and vice versa, such that the product of gain and bandwidth is a constant. This is true as long as the roll-off rate is fixed, as in the case of a compensated op-amp. If you let A_{cl} represent the gain of any of the closed-loop configurations and $f_{c(cl)}$ represent the closed-loop critical frequency (same as the bandwidth), then

$$A_{cl}f_{c(cl)} = A_{ol}f_{c(ol)}$$

The **gain-bandwidth product** is always equal to the frequency at which the op-amp's open-loop gain is unity or 0 dB (unity-gain bandwidth, f_T).

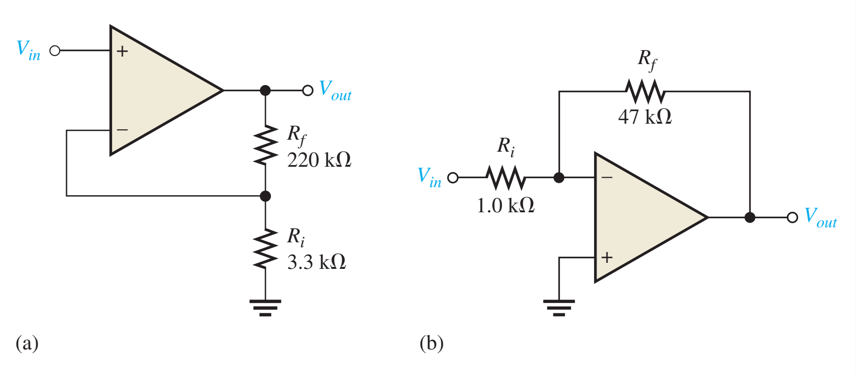
$$\boldsymbol{f_T = A_{cl}f_{c(cl)}}$$

Equation 12–23

EXAMPLE 12–12

Determine the bandwidth of each of the amplifiers in Figure 12–43. Both op-amps have an open-loop gain of 100 dB and a unity-gain bandwidth (f_T) of 3 MHz.

▶ FIGURE 12–43



Solution

(a) For the noninverting amplifier in Figure 12–43(a), the closed-loop gain is

$$A_{cl} = 1 + \frac{R_f}{R_i} = 1 + \frac{220\text{ k}\Omega}{3.3\text{ k}\Omega} = 67.7$$

Use Equation 12–23 and solve for $f_{c(cl)}$ (where $f_{c(cl)} = BW_{cl}$).

$$f_{c(cl)} = BW_{cl} = \frac{f_T}{A_{cl}}$$

$$BW_{cl} = \frac{3\text{ MHz}}{67.7} = \mathbf{44.3\text{ kHz}}$$

(b) For the inverting amplifier in Figure 12–43(b), the closed-loop gain is

$$A_{cl} = -\frac{R_f}{R_i} = -\frac{47\text{ k}\Omega}{1.0\text{ k}\Omega} = -47$$

Using the absolute value of A_{cl}, the closed-loop bandwidth is

$$BW_{cl} = \frac{3\text{ MHz}}{47} = \mathbf{63.8\text{ kHz}}$$

Related Problem Determine the bandwidth of each of the amplifiers in Figure 12–43. Both op-amps have an A_{ol} of 90 dB and a unity-gain bandwidth of 2 MHz.

Open the Multisim file E12-12 in the Examples folder on the companion website. Measure the bandwidth of each amplifier using the Bode plotter and compare with the calculated values.

SECTION 12–8 CHECKUP

1. Is the closed-loop gain always less than the open-loop gain?
2. A certain op-amp is used in a feedback configuration having a gain of 30 and a bandwidth of 100 kHz. If the external resistor values are changed to increase the gain to 60, what is the new bandwidth?
3. What is the unity-gain bandwidth of the op-amp in Question 2?

12–9 TROUBLESHOOTING

As a technician, you may encounter situations in which an op-amp or its associated circuitry has malfunctioned. The op-amp is a complex integrated circuit with many types of internal failures possible. However, since you cannot troubleshoot the op-amp internally, treat it as a single device with only a few connections to it. If it fails, replace it just as you would a resistor, capacitor, or transistor.

After completing this section, you should be able to

- ❑ **Troubleshoot op-amp circuits**
- ❑ Determine faults in the noninverting amplifier
- ❑ Determine faults in the voltage-follower
- ❑ Determine faults in the inverting amplifier

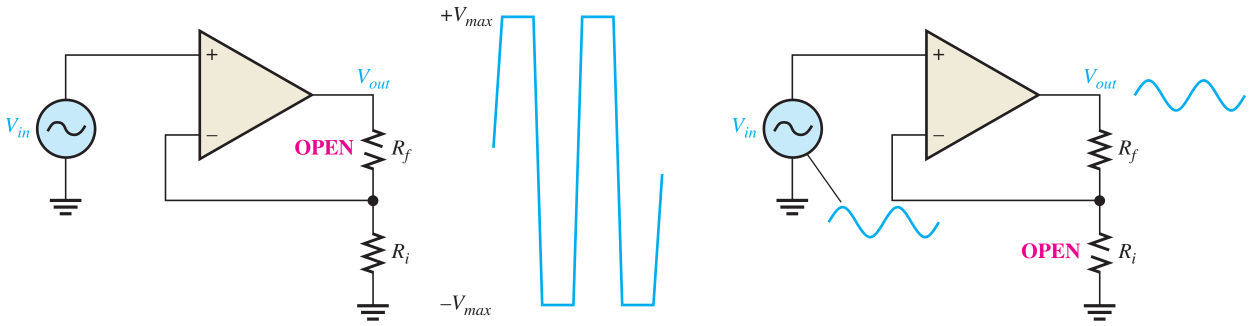
Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire chapter 18 may be covered later or not at all.

In the basic op-amp configurations, there are only a few external components that can fail. These are the feedback resistor, the input resistor, and the potentiometer used for offset voltage compensation. Also, of course, the op-amp itself can fail or there can be faulty contacts in the circuit. Let's examine the three basic configurations for possible faults and the associated symptoms.

The first thing to do when you suspect a faulty circuit is to check for the proper supply voltage and ground at the pins of the op-amp. Having done that, several other possible faults are as follows. A visual inspection should also be done.

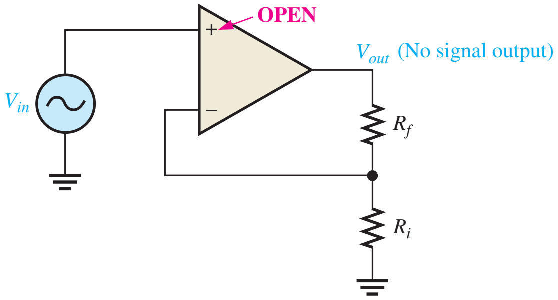
Faults in the Noninverting Amplifier

Open Feedback Resistor If the feedback resistor, R_f, in Figure 12–44 opens, the op-amp is operating with its very high open-loop gain, which causes the input signal to drive the device into nonlinear operation and results in a severely clipped output signal as shown in part (a).



(a) R_f open

(b) R_i open



(c) Input to op-amp open internally

▲ FIGURE 12–44

Faults in the noninverting amplifier.

Open Input Resistor In this case, you still have a closed-loop configuration. Since R_i is open and effectively equal to infinity (∞), the closed-loop gain from Equation 12–8 is

$$A_{cl(\text{NI})} = 1 + \frac{R_f}{R_i} = 1 + \frac{R_f}{\infty} = 1 + 0 = 1$$

This shows that the amplifier acts like a voltage-follower. You would observe an output signal that is the same as the input, as indicated in Figure 12–44(b).

Internally Open Noninverting Op-Amp Input In this situation, because the input voltage is not applied to the op-amp, the output is zero. This is indicated in Figure 12–44(c).

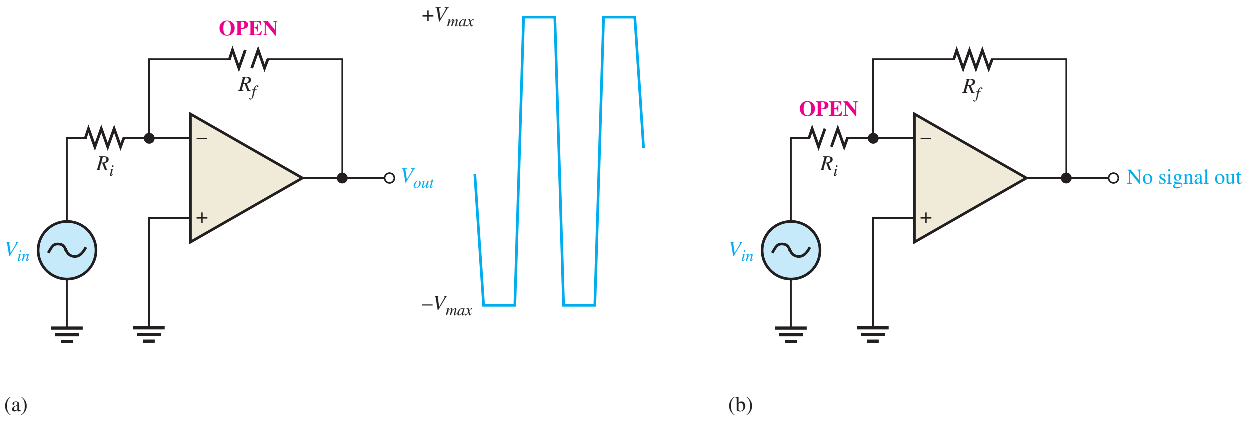
Other Op-Amp Faults In general, an internal failure will result in a loss or distortion of the output signal. The best approach is to first make sure that there are no external failures or faulty conditions. If everything else is good, then the op-amp must be bad.

Faults in the Voltage-Follower

The voltage-follower is a special case of the noninverting amplifier. Except for a faulty op-amp, an open or shorted external connection, or a problem with the offset null potentiometer, about the only thing that can happen in a voltage-follower circuit is an open feedback loop. This would have the same effect as an open feedback resistor as previously discussed.

Faults in the Inverting Amplifier

Open Feedback Resistor If R_f opens, as indicated in Figure 12–45(a), the input signal still feeds through the input resistor and is amplified by the high open-loop gain of the op-amp. This forces the device to be driven into nonlinear operation, and you will see an output something like that shown. This is a similar result as in the noninverting amplifier configuration.



▲ FIGURE 12–45

Faults in the inverting amplifier.

Open Input Resistor This prevents the input signal from getting to the op-amp input, so there will be no output signal, as indicated in Figure 12–45(b).

Failures in the op-amp itself or the offset null potentiometer have the same effects as previously discussed for the noninverting amplifier configuration.

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE12-01
2. Multisim file TSE12-02
3. Multisim file TSE12-03
4. Multisim file TSE12-04
5. Multisim file TSE12-05

SECTION 12–9 CHECKUP

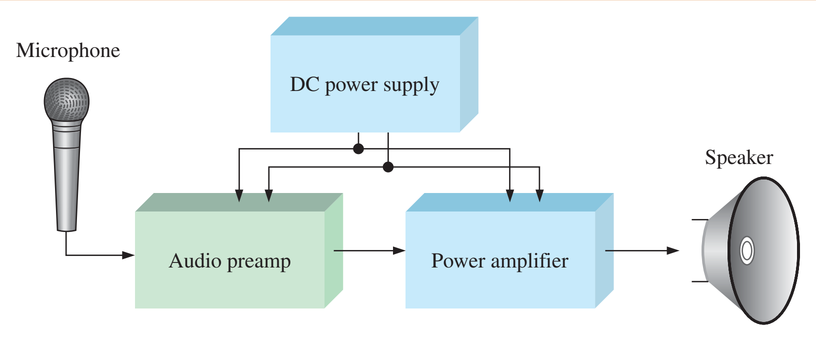
1. If you notice that the op-amp output signal is beginning to clip on one peak as you increase the input signal, what should you check?
2. For a noninverting amplifier, if there is no op-amp output signal when there is a verified input signal at the input pin, what would you suspect as being faulty?

Application Activity: *Op-Amp Audio Amplifier*

The company that manufactures the PA system developed in Chapters 6 and 7 wants to replace the audio amplifier with a new design using an op-amp instead of the discrete transistor preamp circuit to reduce parts and cost. The power amplifier will still retain its basic design with only a few changes. The block diagram of the PA system is shown in Figure 12–46.

▶ FIGURE 12–46

Block diagram of public address system.

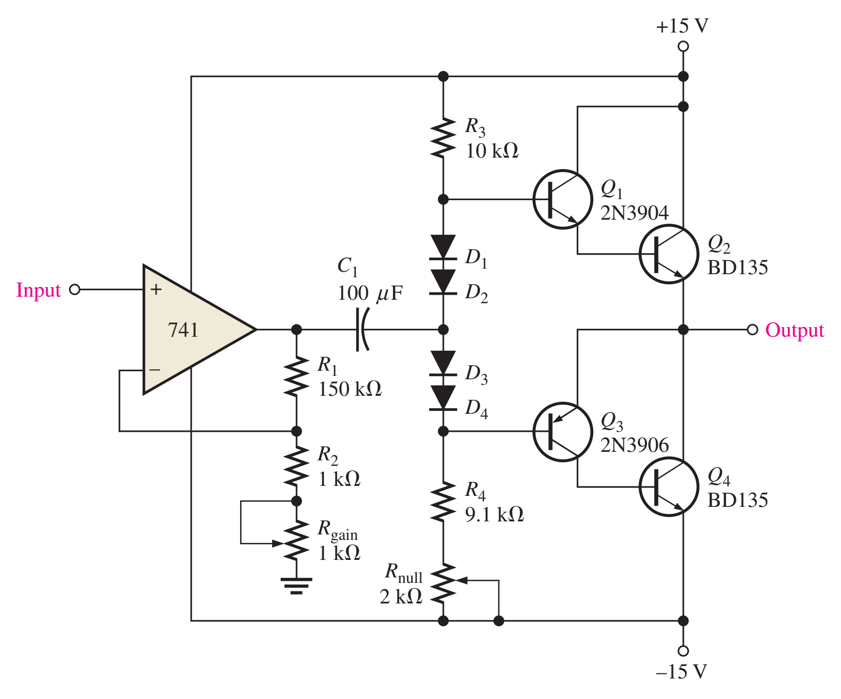

Microphone
DC power supply
Speaker
Audio preamp
Power amplifier

The Circuit

The schematic of the new op-amp design is shown in Figure 12–47. A 741 operational amplifier is used for the preamp stage. The power amplifier retains the original push-pull complementary Darlington configuration with the exception of the driver stage. This has been eliminated because the op-amp, with its very low output resistance, is capable of driving the push-pull power amplifier stage without a buffer interface. The rheostat, R_{gain}, is for adjusting the voltage gain, and the potentiometer, R_{null}, is for output nulling (making the dc output 0 V).

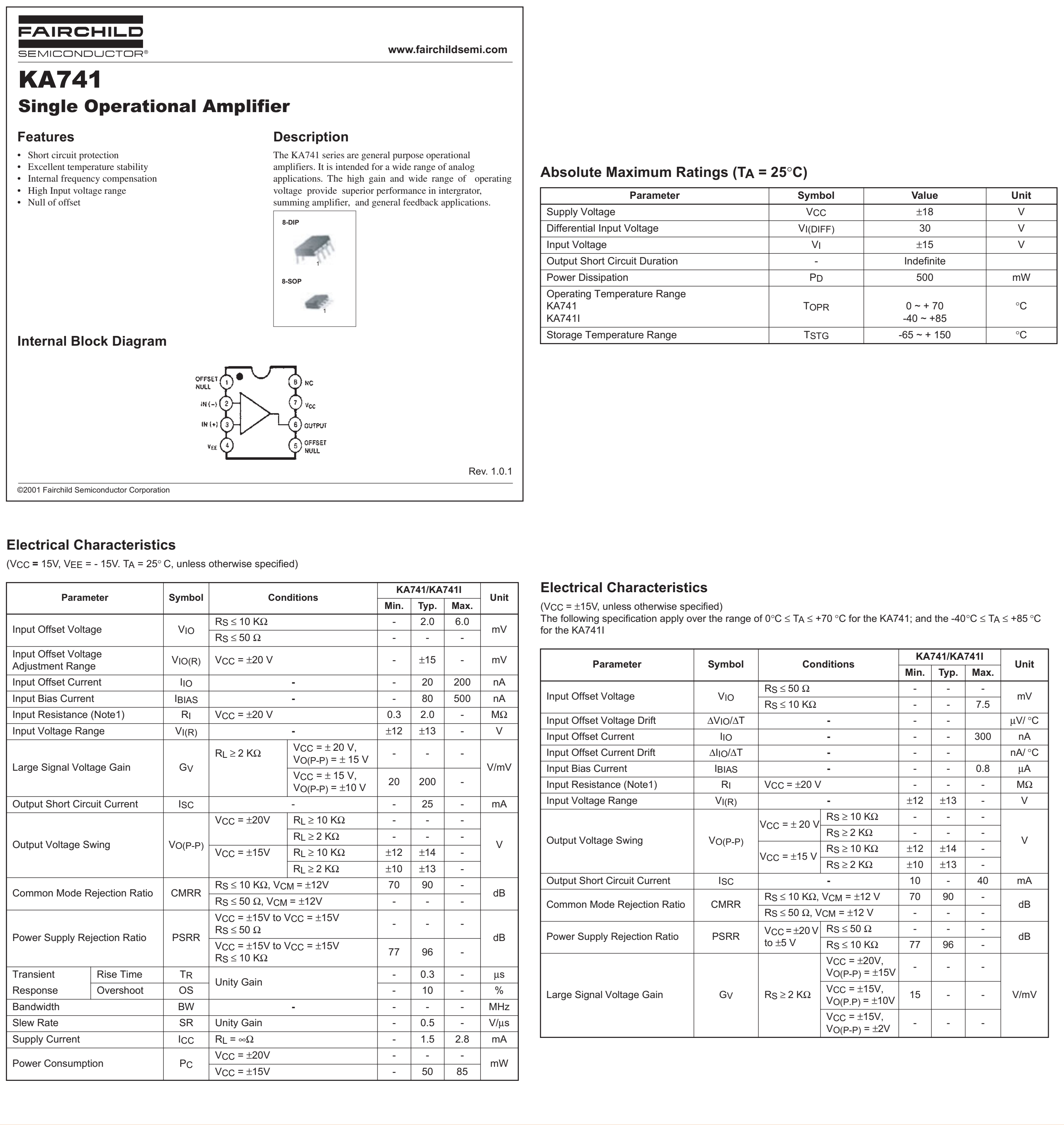
▶ FIGURE 12–47

Audio amplifier.


+15 V
R_3 10 kΩ
Q_1 2N3904
Q_2 BD135
D_1
D_2
C_1 100 μF
Input
+
741
–
Output
R_1 150 kΩ
D_3
D_4
Q_3 2N3906
Q_4 BD135
R_2 1 kΩ
R_4 9.1 kΩ
R_{gain} 1 kΩ
R_{null} 2 kΩ
–15 V

1. Identify the op-amp configuration.
2. Calculate the maximum and minimum voltage gains of the op-amp.
3. What is the maximum rms output of the op-amp stage if the input is 50 mV rms?
4. Determine the ideal maximum power delivered by the audio amplifier to an 8 Ω speaker.

A partial datasheet for a 741 op-amp is shown in Figure 12–48.



FAIRCHILD
SEMICONDUCTOR®

www.fairchildsemi.com

KA741

Single Operational Amplifier

Features

- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset

Description

The KA741 series are general purpose operational amplifiers. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.

Internal Block Diagram

Rev. 1.0.1

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Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration	-	Indefinite	
Power Dissipation	P_D	500	mW
Operating Temperature Range KA741 KA741I	T_{OPR}	 0 ~ + 70 -40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	°C

Electrical Characteristics

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25° C, unless otherwise specified)

Parameter		Symbol	Conditions		KA741/KA741I			Unit
					Min.	Typ.	Max.	
Input Offset Voltage		V_{IO}	$R_S \le 10\ K\Omega$		-	2.0	6.0	mV
			$R_S \le 50\ \Omega$		-	-	-	
Input Offset Voltage Adjustment Range		$V_{IO(R)}$	$V_{CC} = \pm 20\ V$		-	±15	-	mV
Input Offset Current		I_{IO}	-		-	20	200	nA
Input Bias Current		I_{BIAS}	-		-	80	500	nA
Input Resistance (Note1)		R_I	$V_{CC} = \pm 20\ V$		0.3	2.0	-	MΩ
Input Voltage Range		$V_{I(R)}$	-		±12	±13	-	V
Large Signal Voltage Gain		G_V	$R_L \ge 2\ K\Omega$	$V_{CC} = \pm 20\ V$, $V_{O(P-P)} = \pm 15\ V$	-	-	-	V/mV
				$V_{CC} = \pm 15\ V$, $V_{O(P-P)} = \pm 10\ V$	20	200	-	
Output Short Circuit Current		I_{SC}	-		-	25	-	mA
Output Voltage Swing		$V_{O(P-P)}$	$V_{CC} = \pm 20V$	$R_L \ge 10\ K\Omega$	-	-	-	V
				$R_L \ge 2\ K\Omega$	-	-	-	
			$V_{CC} = \pm 15V$	$R_L \ge 10\ K\Omega$	±12	±14	-	
				$R_L \ge 2\ K\Omega$	±10	±13	-	
Common Mode Rejection Ratio		CMRR	$R_S \le 10\ K\Omega$, $V_{CM} = \pm 12V$		70	90	-	dB
			$R_S \le 50\ \Omega$, $V_{CM} = \pm 12V$		-	-	-	
Power Supply Rejection Ratio		PSRR	$V_{CC} = \pm 15V$ to $V_{CC} = \pm 15V$ $R_S \le 50\ \Omega$		-	-	-	dB
			$V_{CC} = \pm 15V$ to $V_{CC} = \pm 15V$ $R_S \le 10\ K\Omega$		77	96	-	
Transient Response	Rise Time	T_R	Unity Gain		-	0.3	-	µs
	Overshoot	OS			-	10	-	%
Bandwidth		BW	-		-	-	-	MHz
Slew Rate		SR	Unity Gain		-	0.5	-	V/µs
Supply Current		I_{CC}	$R_L = \infty\Omega$		-	1.5	2.8	mA
Power Consumption		P_C	$V_{CC} = \pm 20V$		-	-	-	mW
			$V_{CC} = \pm 15V$		-	50	85	

Electrical Characteristics

($V_{CC} = \pm 15V$, unless otherwise specified)
The following specification apply over the range of 0°C ≤ T_A ≤ +70 °C for the KA741; and the -40°C ≤ T_A ≤ +85 °C for the KA741I

Parameter	Symbol	Conditions		KA741/KA741I			Unit
				Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	$R_S \le 50\ \Omega$		-	-	-	mV
		$R_S \le 10\ K\Omega$		-	-	7.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	-		-	-		µV/ °C
Input Offset Current	I_{IO}	-		-	-	300	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	-		-	-		nA/ °C
Input Bias Current	I_{BIAS}	-		-	-	0.8	µA
Input Resistance (Note1)	R_I	$V_{CC} = \pm 20\ V$		-	-	-	MΩ
Input Voltage Range	$V_{I(R)}$	-		±12	±13	-	V
Output Voltage Swing	$V_{O(P-P)}$	$V_{CC} = \pm 20\ V$	$R_S \ge 10\ K\Omega$	-	-	-	V
			$R_S \ge 2\ K\Omega$	-	-	-	
		$V_{CC} = \pm 15\ V$	$R_S \ge 10\ K\Omega$	±12	±14	-	
			$R_S \ge 2\ K\Omega$	±10	±13	-	
Output Short Circuit Current	I_{SC}	-		10	-	40	mA
Common Mode Rejection Ratio	CMRR	$R_S \le 10\ K\Omega$, $V_{CM} = \pm 12\ V$		70	90	-	dB
		$R_S \le 50\ \Omega$, $V_{CM} = \pm 12\ V$		-	-	-	
Power Supply Rejection Ratio	PSRR	$V_{CC} = \pm 20\ V$ to $\pm 5\ V$	$R_S \le 50\ \Omega$	-	-	-	dB
			$R_S \le 10\ K\Omega$	77	96	-	
Large Signal Voltage Gain	G_V	$R_S \ge 2\ K\Omega$	$V_{CC} = \pm 20V$, $V_{O(P-P)} = \pm 15V$	-	-	-	V/mV
			$V_{CC} = \pm 15V$, $V_{O(P.P)} = \pm 10V$	15	-	-	
			$V_{CC} = \pm 15V$, $V_{O(P-P)} = \pm 2V$	-	-	-	

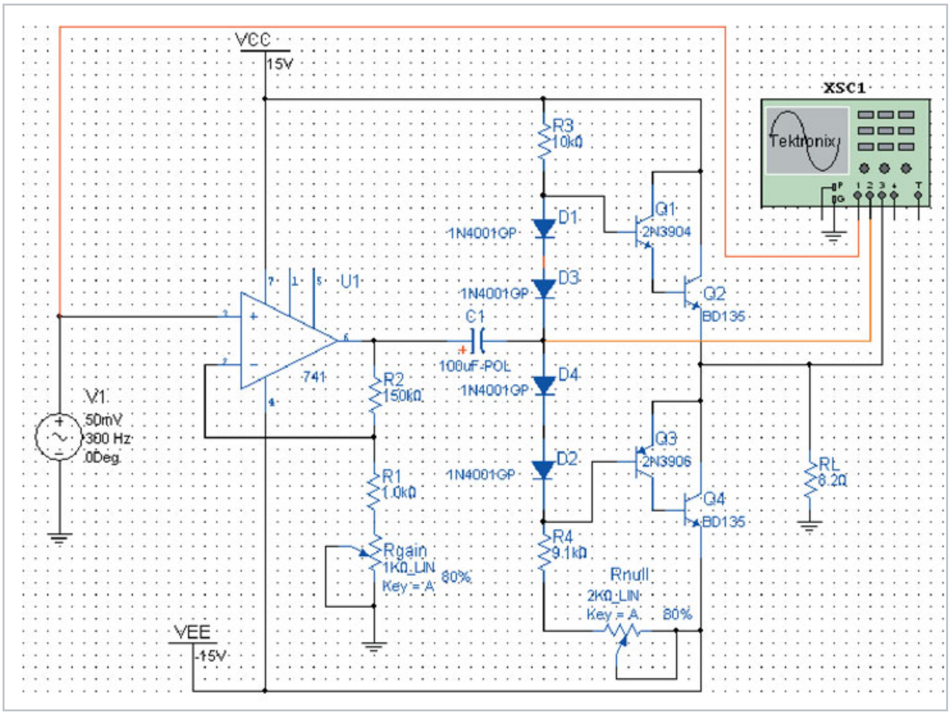
▲ FIGURE 12–48

Partial datasheet for the KA741 op amp. Copyright Fairchild Semiconductor Corporation. Used by permission.

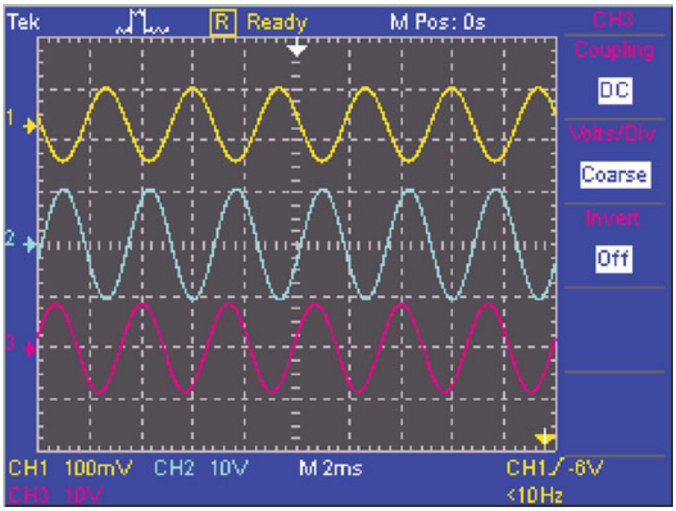
5. Using the datasheet, assign pin numbers to the op-amp in Figure 12–47.
6. Determine the maximum power consumption of the op-amp with the ±15 V supply voltages.
7. To what typical voltage can the output swing with ±15 V supply voltages?

Simulation

The audio amplifier is simulated with an input signal of 50 mV using Multisim. The results are shown in Figure 12–49 where an 8.2 Ω resistor is used to simulate the speaker.


VCC
15V
XSC1
Tektronix
R3
10kΩ
D1
1N4001GP
Q1
2N3904
D3
1N4001GP
Q2
BD135
U1
C1
100uF-POL
741
R2
150kΩ
D4
1N4001GP
V1
50mV
300 Hz
0Deg
Q3
2N3906
D2
1N4001GP
R1
1.0kΩ
Q4
BD135
RL
8.2Ω
R4
9.1kΩ
Rgain
1KΩ_LIN
Key = A
80%
Rnull
2KΩ_LIN
Key = A
80%
VEE
-15V

(a) Circuit screen



Tek R Ready M Pos: 0s

CH3 Coupling DC

Volts/Div Coarse

Invert Off

CH1 100mV CH2 10V M 2ms CH1 ∕ -6V

CH3 10V <10Hz

(b) Input signal, op-amp output signal, and final output signal

▲ **FIGURE 12–49**

Simulation of the audio amplifier.

8. From the scope display in Figure 12–49, determine the rms value of each voltage.
9. Determine the voltage gain of the op-amp stage from the measured signals.
10. Determine the overall voltage gain from the measured signals.

Simulate the op-amp audio amplifier using your Multisim software. Observe the signal voltages with the oscilloscope.

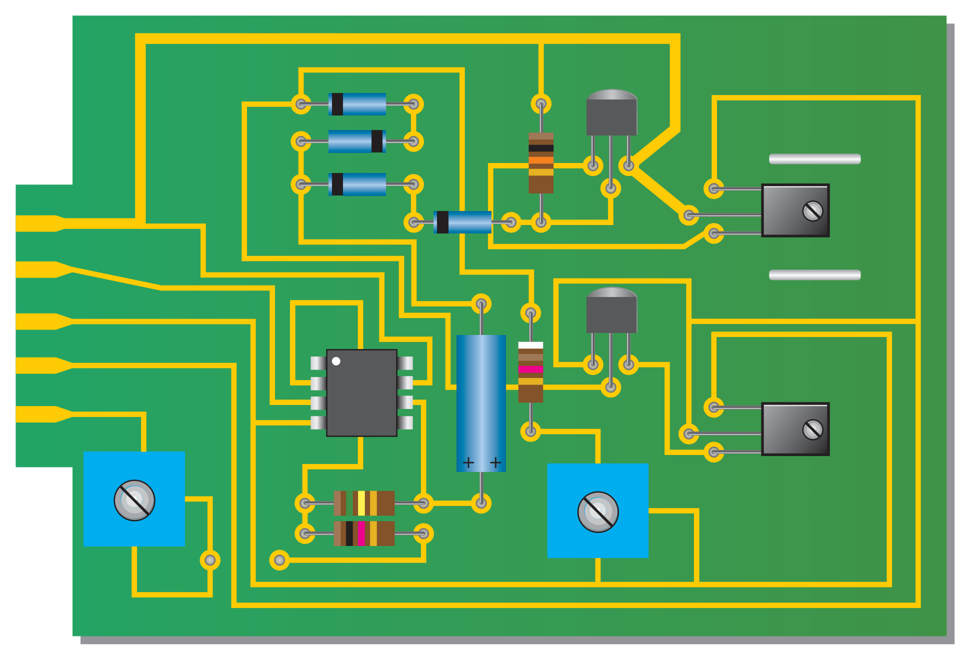
Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a similar circuit, go to Experiment 12–A in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

The original system had two boards, the preamp board and the power amp board. By using the new op-amp design, the audio amplifier is simplified to one board, as shown in Figure 12–50.



▲ **FIGURE 12–50**

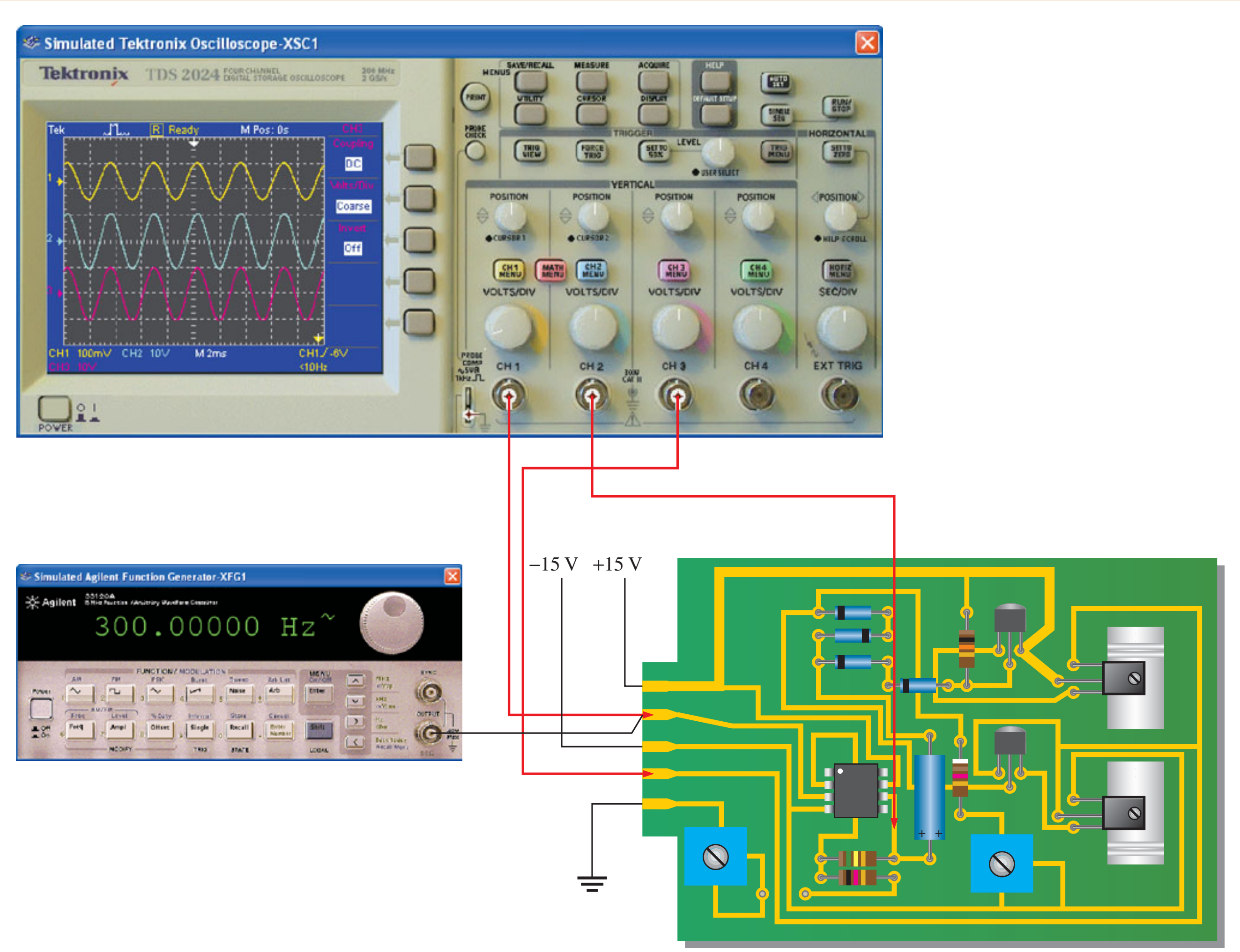
Audio amplifier board.

11. Check the printed circuit board for correctness by comparing it with the schematic in Figure 12–47.
12. Label each input and output pin according to function.

Troubleshooting

Four circuit boards are tested, and the results are shown in Figure 12–51. (Parts (b), (c), and (d) are shown on the next page.)

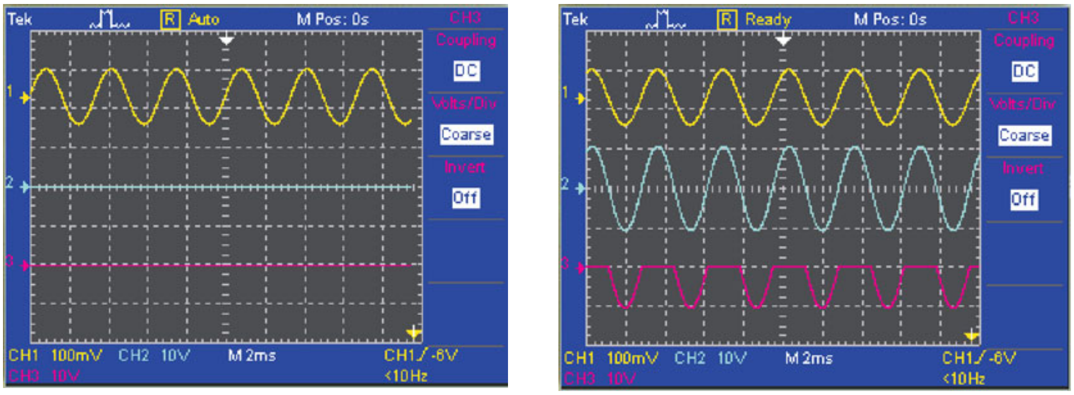
13. Determine the problem, if any, in each of the board tests in Figure 12–51.
14. List possible causes of any problem from item 13.


Simulated Tektronix Oscilloscope-XSC1
Tektronix TDS 2024
Tek
Ready
M Pos: 0s
CH1 100mV CH2 10V M 2ms
CH1 ∕ -6V
<10Hz
DC
Coarse
Off
POWER
CH 1
CH 2
CH 3
CH 4
EXT TRIG
Simulated Agilent Function Generator-XFG1
Agilent
300.00000 Hz
−15 V
+15 V

(a) Test results for board 1

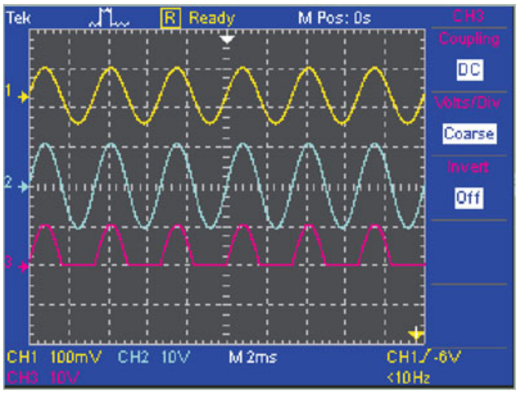
▲ FIGURE 12–51

Results of audio amplifier board tests.


Tek
R Auto
M Pos: 0s
CH3
Coupling
DC
Volts/Div
Coarse
Invert
Off
1
2
3
CH1 100mV CH2 10V M 2ms CH1 -6V
CH3 10V <10Hz
Tek
R Ready
M Pos: 0s
CH3
Coupling
DC
Volts/Div
Coarse
Invert
Off
1
2
3
CH1 100mV CH2 10V M 2ms CH1 -6V
CH3 10V <10Hz

(b) Test results for board 2

(c) Test results for board 3


Tek
R Ready
M Pos: 0s
CH3
Coupling
DC
Volts/Div
Coarse
Invert
Off
1
2
3
CH1 100mV CH2 10V M 2ms CH1 -6V
CH3 10V <10Hz

(d) Test results for board 4

▲ **FIGURE 12–51**

Continued

Programmable Analog Technology

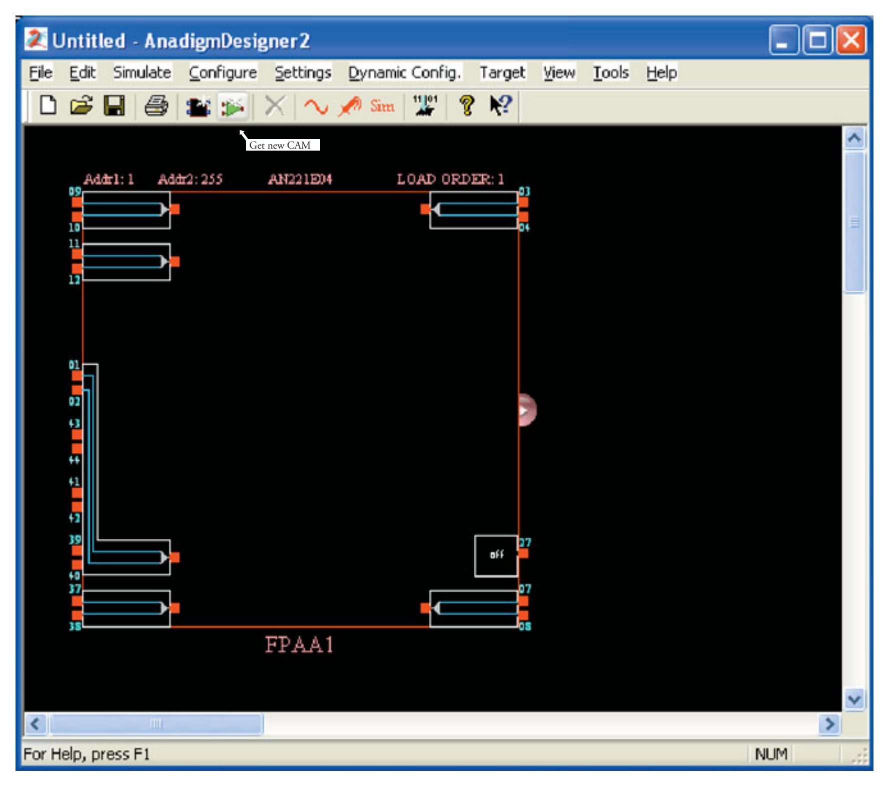
FPAAs (field-programmable analog arrays) and dpASPs (dynamically programmable analog signal processors) are based on switched-capacitor technology that was covered in Chapter 9. These are integrated circuit devices that can be programmed with software for various types of analog functions and designs. Both the FPAA and the dpASP can be reprogrammed, but the FPAA is statically reconfigurable and must first be reset whereas the dpASP can be **dynamically reconfigured** "on-the-fly" while operating in a system. The software allows you to experiment and design with various analog devices that are covered in this textbook by specifying parameters, observing operation, interconnecting devices for more complex circuits, and preparing the software for **downloading** to an actual device. Refer to the tutorial available with the AnadigmDesigner®2 software or the tutorial in the *Laboratory Exercises for Electronic Devices* lab manual.

The Designer2 software differs in its primary purpose from the Multisim software you have been using. Electronic Workbench Multisim is basically a simulation software that allows you to test circuits on the computer using simulated discrete and integrated components. The Multisim software is useful for verifying that a circuit actually works as intended, but it has limited hardware interface capability. AnadigmDesigner2 is both a simulation and a hardware interface tool that allows you to custom program an analog design and implement it in an integrated circuit chip. It is based on an extensive library of analog functions called configurable analog modules (**CAMs**) that can be connected using a simple "drag-and drop" format and tested with virtual instruments on the computer. The design can then be converted to hardware by downloading it to an actual FPAA or dpASP IC chip.

A free trial version of the AnadigmDesigner2 software is available for downloading at www.anadigm.com. The basic steps in implementing a design are as follows using a specific CAM for illustration. These steps apply to any CAM or multiple CAMs.

CAM Selection

The first step in implementing a programmable analog design is to open the AnadigmDesigner2 software. The representation of a blank FPAA or dpASP chip will appear as shown in Figure 12–52. Select the *Configure* icon to open a list of available CAMs, as shown in Figure 12–53.

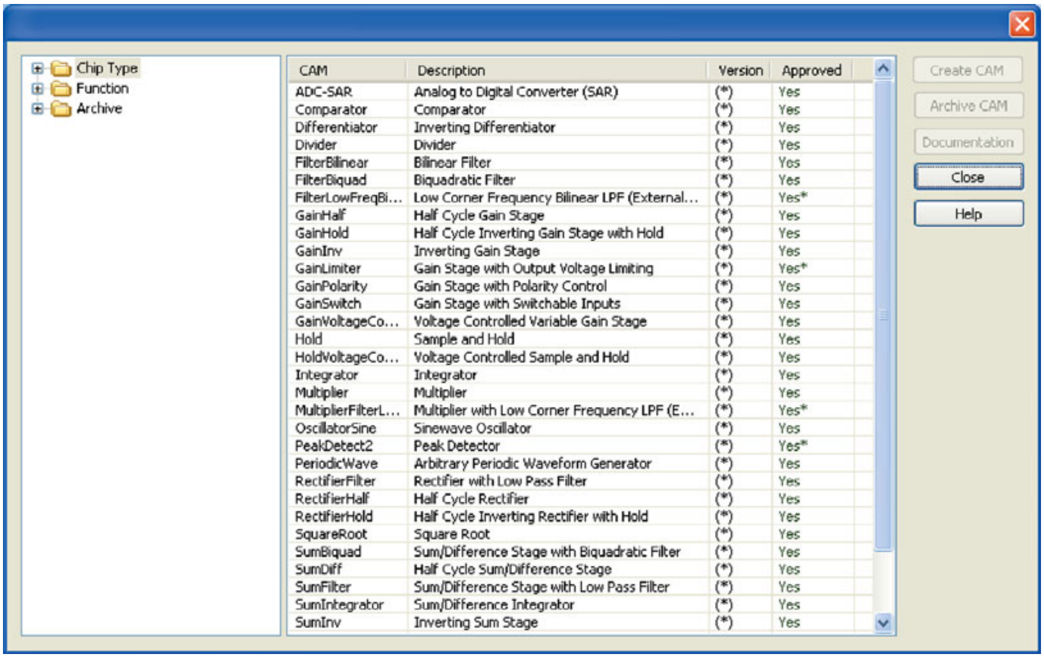

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Sim
Get new CAM
Addr1: 1
Addr2: 255
AN221E04
LOAD ORDER: 1
off
FPAA1
For Help, press F1
NUM

▲ FIGURE 12–52

Click on *Configure* icon.

Configure and Place CAM

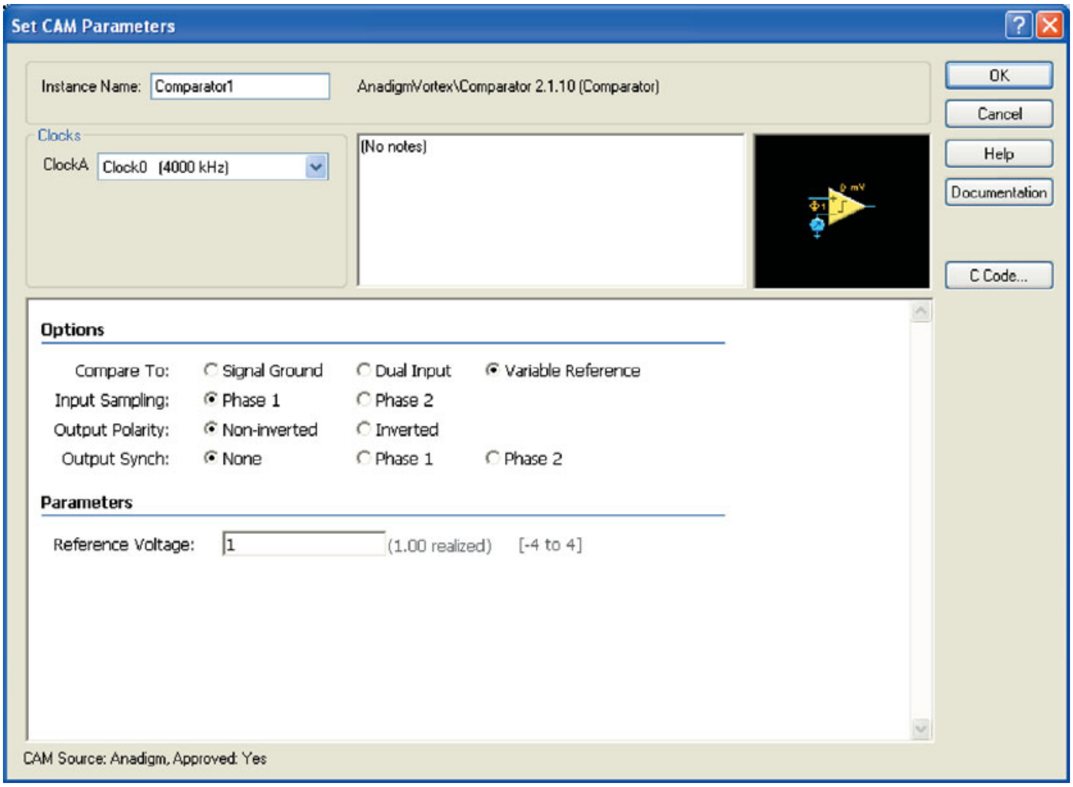
Select the desired CAM and set up the parameters in the *Set CAM Parameters* screen shown in Figure 12–54. Next place the CAM in the chip outline and connect to an input and output, as shown in Figure 12–55. Several CAMs can be placed in one chip and interconnected.



CAM	Description	Version	Approved
ADC-SAR	Analog to Digital Converter (SAR)	(*)	Yes
Comparator	Comparator	(*)	Yes
Differentiator	Inverting Differentiator	(*)	Yes
Divider	Divider	(*)	Yes
FilterBilinear	Bilinear Filter	(*)	Yes
FilterBiquad	Biquadratic Filter	(*)	Yes
FilterLowFreqBi…	Low Corner Frequency Bilinear LPF (External…	(*)	Yes*
GainHalf	Half Cycle Gain Stage	(*)	Yes
GainHold	Half Cycle Inverting Gain Stage with Hold	(*)	Yes
GainInv	Inverting Gain Stage	(*)	Yes
GainLimiter	Gain Stage with Output Voltage Limiting	(*)	Yes*
GainPolarity	Gain Stage with Polarity Control	(*)	Yes
GainSwitch	Gain Stage with Switchable Inputs	(*)	Yes
GainVoltageCo…	Voltage Controlled Variable Gain Stage	(*)	Yes
Hold	Sample and Hold	(*)	Yes
HoldVoltageCo…	Voltage Controlled Sample and Hold	(*)	Yes
Integrator	Integrator	(*)	Yes
Multiplier	Multiplier	(*)	Yes
MultiplierFilterL…	Multiplier with Low Corner Frequency LPF (E…	(*)	Yes*
OscillatorSine	Sinewave Oscillator	(*)	Yes
PeakDetect2	Peak Detector	(*)	Yes*
PeriodicWave	Arbitrary Periodic Waveform Generator	(*)	Yes
RectifierFilter	Rectifier with Low Pass Filter	(*)	Yes
RectifierHalf	Half Cycle Rectifier	(*)	Yes
RectifierHold	Half Cycle Inverting Rectifier with Hold	(*)	Yes
SquareRoot	Square Root	(*)	Yes
SumBiquad	Sum/Difference Stage with Biquadratic Filter	(*)	Yes
SumDiff	Half Cycle Sum/Difference Stage	(*)	Yes
SumFilter	Sum/Difference Stage with Low Pass Filter	(*)	Yes
SumIntegrator	Sum/Difference Integrator	(*)	Yes
SumInv	Inverting Sum Stage	(*)	Yes

▲ FIGURE 12–53

List of available CAMs.



Instance Name: Comparator1

AnadigmVortex\Comparator 2.1.10 (Comparator)

Clocks

ClockA: Clock0 (4000 kHz)

(No notes)

Options

Compare To: ○ Signal Ground ○ Dual Input ● Variable Reference

Input Sampling: ● Phase 1 ○ Phase 2

Output Polarity: ● Non-inverted ○ Inverted

Output Synch: ● None ○ Phase 1 ○ Phase 2

Parameters

Reference Voltage: 1 (1.00 realized) [-4 to 4]

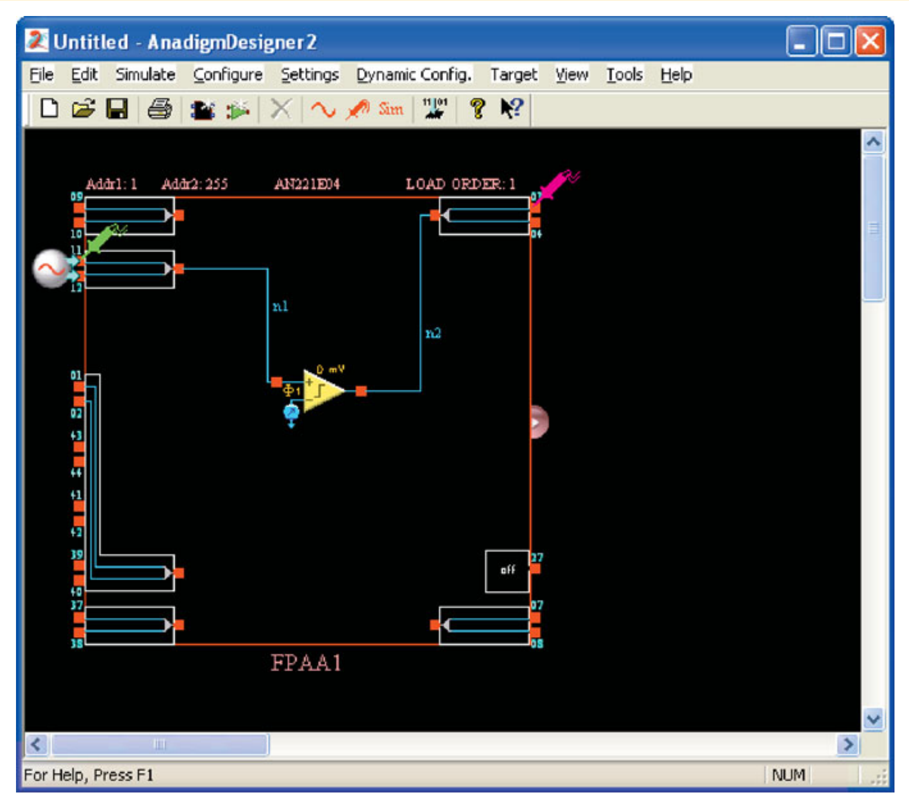
CAM Source: Anadigm, Approved: Yes

▲ FIGURE 12–54

Set CAM parameters.

▶ FIGURE 12–55

CAM placed and connected. Signal source and scope probes placed.

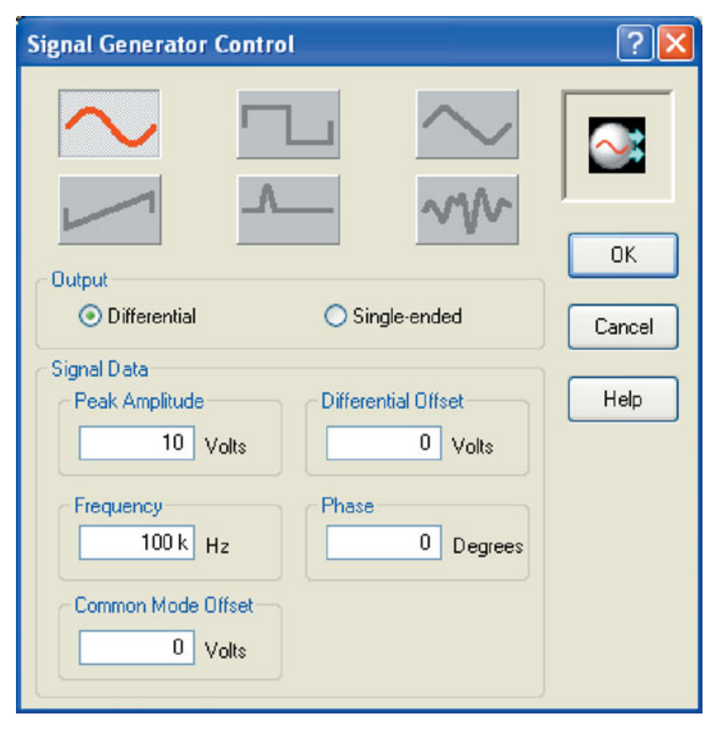

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Sim
Addr1: 1
Addr2: 255
AN221E04
LOAD ORDER: 1
n1
n2
0 mV
Φ1
off
FPAA1
For Help, Press F1
NUM

Test the Design

Place a signal source on the input by clicking on the sine wave icon and set its function and parameters using the *Signal Generator Control* window, as shown in Figure 12–56. Place probes at

▶ FIGURE 12–56

Set signal generator parameters.


Signal Generator Control
OK
Cancel
Help

Output

● Differential ○ Single-ended

Signal Data

Peak Amplitude: 10 Volts

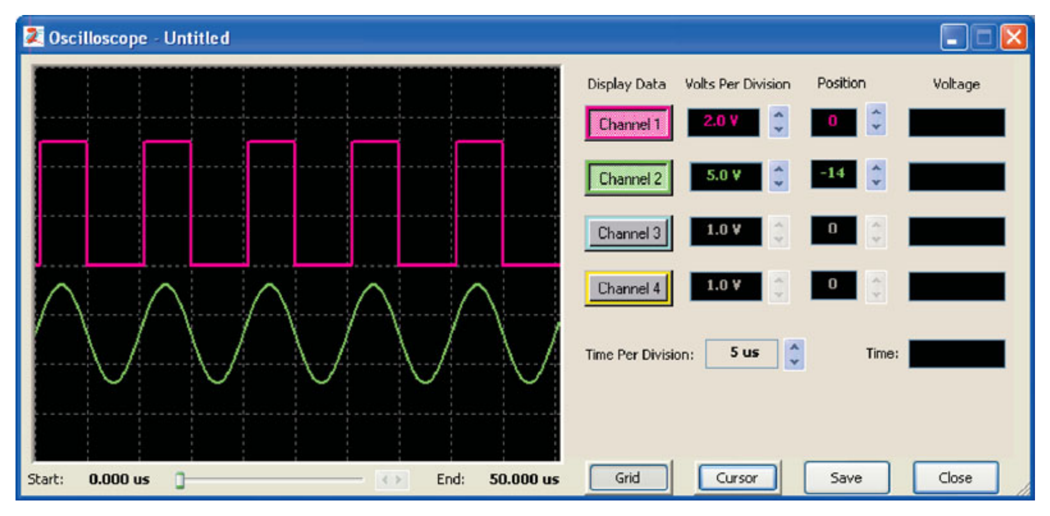
Differential Offset: 0 Volts

Frequency: 100 k Hz

Phase: 0 Degrees

Common Mode Offset: 0 Volts

appropriate points by clicking on the probe icon and then measure the waveforms on the virtual oscilloscope, as shown in Figure 12–57, by clicking on *Sim.*



Display Data	Volts Per Division	Position	Voltage
Channel 1	2.0 V	0	
Channel 2	5.0 V	-14	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

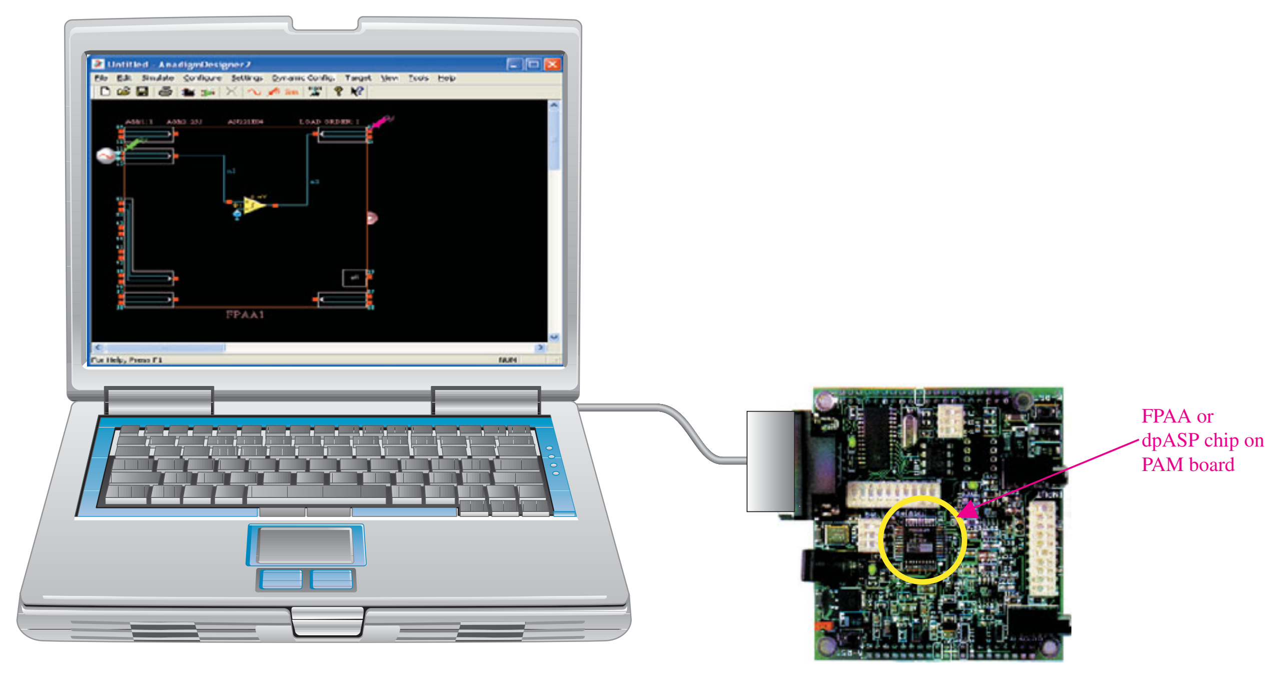
Time Per Division: 5 us
Time:
Start: 0.000 us
End: 50.000 us

▲ **FIGURE 12–57**

Measure waveforms at probe locations.

Download the Design

Once the design is finalized and tested on your computer, it can be downloaded to an actual FPAA or dpASP chip, known as a target device, by selecting *Target* on the screen. The chip is normally mounted on a special PC board with peripheral devices, test points, and connectors so that the downloaded design can be fully tested in hardware. One type of board for this purpose is the programmable analog module (PAM) board available from Servenger LLC (www.servenger.com). Figure 12–58 illustrates the setup.



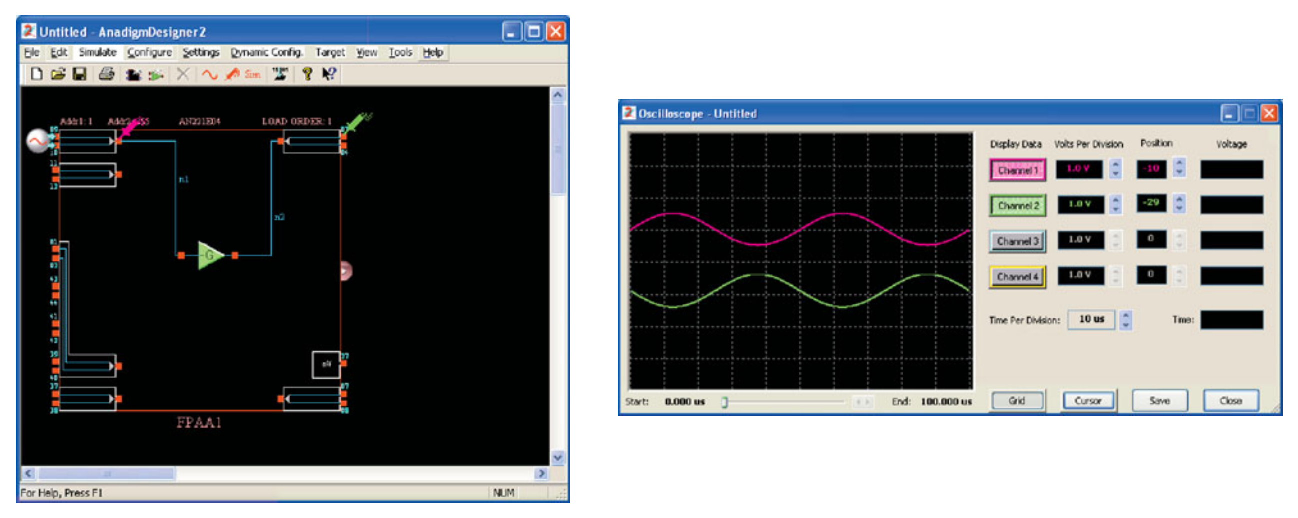
▲ **FIGURE 12–58**

EXAMPLE

Simulate an inverting amplifier with a gain of -1. Apply a sinusoidal input and check both its input and output with the oscilloscope.

Step 1: Open the software and the outline of the blank FPAA chip appears with input and output pins.
Step 2: Select the *Inverting Gain Stage* and drop into the chip outline.
Step 3: Set the gain.
Step 4: Connect a signal generator to an input and set its parameters.
Step 5: Connect a scope probe to an output.
Step 6: Select "begin simulation."
Step 7: Observe input and output waveforms on oscilloscope.

The results of these steps are shown in Figure 12–59.


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1
AN221E04
LOAD ORDER: 1
n1
n2
G
FPAA1
For Help, Press F1
NUM
Oscilloscope - Untitled
Grid
Cursor
Save
Close

Display Data	Volts Per Division	Position	Voltage
Channel 1	1.0 V	-10	
Channel 2	1.0 V	-29	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

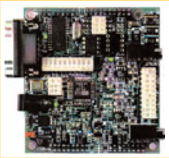
Time Per Division: 10 us
Time:
Start: 0.000 us
End: 100.000 us

▲ FIGURE 12–59

Programming Exercises

1. Simulate and test an inverting amplifier with a gain of -10.
2. Simulate and test a 2-stage noninverting amplifier with a gain of 50.
3. If you have an evaluation board, download each of the simulated circuits.

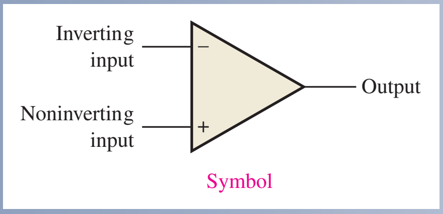
PAM Experiment



To program, download, and test circuits using AnadigmDesigner2 software and the programmable analog module (PAM) board, go to Experiment 12–B in *Laboratory Exercises for Electronic Devices* by David Buchla and Steve Wetterling.

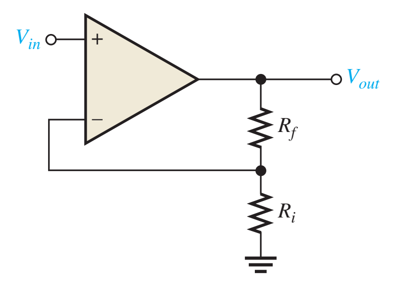
SUMMARY OF OP-AMP CONFIGURATIONS

BASIC OP-AMP


Inverting input
Noninverting input
−
+
Output
Symbol

- Very high open-loop voltage gain
- Very high input impedance
- Very low output impedance

NONINVERTING AMPLIFIER


V_{in}
+
−
V_{out}
R_f
R_i

- Voltage gain:

$$A_{cl(\mathrm{NI})} = 1 + \frac{R_f}{R_i}$$

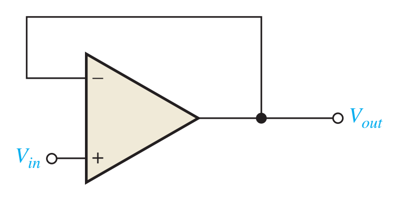
- Input impedance:

$$Z_{in(\mathrm{NI})} = (1 + A_{ol}B)Z_{in}$$

- Output impedance:

$$Z_{out(\mathrm{NI})} = \frac{Z_{out}}{1 + A_{ol}B}$$

VOLTAGE-FOLLOWER



- Voltage gain:

$$A_{cl(\mathrm{VF})} = 1$$

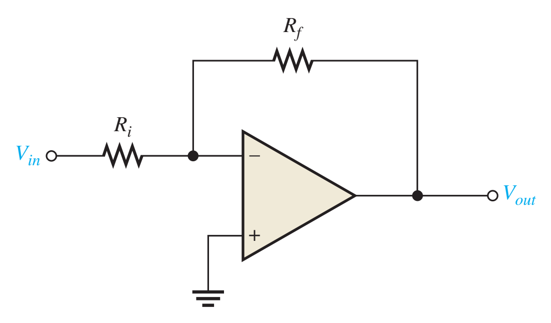
- Input impedance:

$$Z_{in(\mathrm{VF})} = (1 + A_{ol})Z_{in}$$

- Output impedance:

$$Z_{out(\mathrm{VF})} = \frac{Z_{out}}{1 + A_{ol}}$$

INVERTING AMPLIFIER


R_f
R_i
V_{in}
−
+
V_{out}

- Voltage gain:

$$A_{cl(\mathrm{I})} = -\frac{R_f}{R_i}$$

- Input impedance:

$$Z_{in(\mathrm{I})} \cong R_i$$

- Output impedance:

$$Z_{out(\mathrm{I})} = \frac{Z_{out}}{1 + A_{ol}B}$$

SUMMARY

Section 12–1

- The basic op-amp has three terminals not including power and ground: inverting (−) input, noninverting (+) input, and output.
- A differential amplifier forms the input stage of an op-amp.
- Most op-amps require both a positive and a negative dc supply voltage.
- The ideal op-amp has infinite input impedance, zero output impedance, infinite open-loop voltage gain, and infinite bandwidth.
- A practical op-amp has very high input impedance, very low output impedance, and very high open-loop voltage gain.

Section 12–2

- Two types of op-amp input operation are the differential mode and the common mode.
- Common mode occurs when equal in-phase voltages are applied to both input terminals.
- The common-mode rejection ratio (CMRR) is a measure of an op-amp's ability to reject common-mode inputs.
- Open-loop voltage gain is the gain of an op-amp with no external feedback connections.
- Input offset voltage produces an output error voltage (with no input voltage).
- Input bias current also produces an output error voltage (with no input voltage).
- Input offset current is the difference between the two bias currents.
- Slew rate is the rate in volts per microsecond at which the output voltage of an op-amp can change in response to a step input.
- Noise degrades the performance of an amplifier by the introduction of an unwanted signal.

Section 12–3

- Negative feedback occurs when a portion of the output voltage is connected back to the inverting input such that it subtracts from the input voltage, thus reducing the voltage gain but increasing the stability and bandwidth.

Section 12–4

- There are three basic op-amp configurations: inverting, noninverting, and voltage-follower.
- The three basic op-amp configurations employ negative feedback.
- Closed-loop voltage gain is the gain of an op-amp with external feedback.

Section 12–5

- A noninverting amplifier configuration has a higher input impedance and a lower output impedance than the op-amp itself (without feedback).
- An inverting amplifier configuration has an input impedance approximately equal to the input resistor R_i and an output impedance approximately equal to the output impedance of the op-amp itself.
- The voltage-follower has the highest input impedance and the lowest output impedance of the three amplifier configurations.

Section 12–6

- All practical op-amps have small input bias currents and input offset voltages that produce small output error voltages.
- The input bias current effect can be compensated for with external resistors.
- The input offset voltage can be compensated for with an external potentiometer between the two offset null pins provided on the IC op-amp package and as recommended by the manufacturer.

Section 12–7

- The closed-loop voltage gain is always less than the open-loop voltage gain.
- The midrange gain of an op-amp extends down to dc.
- The gain of an op-amp decreases as frequency increases above the critical frequency.
- The bandwidth of an op-amp equals the upper critical frequency.
- The open-loop response curve of a compensated op-amp rolls off at -20 dB/decade above f_c.

Section 12–8

- The internal *RC* lag circuits that are inherently part of the amplifier stages cause the gain to roll off as frequency goes up.
- The internal *RC* lag circuits also cause a phase shift between input and output signals.
- Negative feedback lowers the gain and increases the bandwidth.
- The product of gain and bandwidth is constant for a given op-amp.
- The gain-bandwidth product equals the frequency at which unity voltage gain occurs.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Closed-loop voltage gain (A_{cl}) The voltage gain of an op-amp with external feedback.

CMRR Common-mode rejection ratio; the ratio of open-loop gain to common-mode gain; a measure of an op-amp's ability to reject common-mode signals.

Common mode A condition characterized by the presence of the same signal on both op-amp inputs.

Differential amplifier A type of amplifier with two inputs and two outputs that is used as the input stage of an op-amp.

Differential mode A mode of op-amp operation in which two opposite-polarity signal voltages are applied to the two inputs (double-ended) or in which a signal is applied to one input and ground to the other input (single-ended).

Gain-bandwidth product A constant parameter which is always equal to the frequency at which the op-amp's open-loop gain is unity (1).

Inverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the inverting input.

Negative feedback The process of returning a portion of the output signal to the input of an amplifier such that it is out of phase with the input signal.

Noninverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the noninverting input.

Open-loop voltage gain (A_{ol}) The voltage gain of an op-amp without external feedback.

Operational amplifier (op-amp) A type of amplifier that has very high voltage gain, very high input impedance, very low output impedance, and good rejection of common-mode signals.

Phase shift The relative angular displacement of a time-varying function relative to a reference.

Slew rate The rate of change of the output voltage of an op-amp in response to a step input.

Voltage-follower A closed-loop, noninverting op-amp with a voltage gain of 1.

KEY FORMULAS

Op-Amp Input Modes and Parameters

12–1	$\text{CMRR} = \dfrac{A_{ol}}{A_{cm}}$	Common-mode rejection ratio
12–2	$\text{CMRR} = 20 \log\left(\dfrac{A_{ol}}{A_{cm}}\right)$	Common-mode rejection ratio (dB)
12–3	$I_{\text{BIAS}} = \dfrac{I_1 + I_2}{2}$	Input bias current
12–4	$I_{\text{OS}} = \lvert I_1 - I_2 \rvert$	Input offset current
12–5	$V_{\text{OS}} = I_{\text{OS}} R_{in}$	Offset voltage
12–6	$V_{\text{OUT(error)}} = A_v I_{\text{OS}} R_{in}$	Output error voltage
12–7	$\text{Slew rate} = \dfrac{\Delta V_{out}}{\Delta t}$	Slew rate

Op-Amp Configurations

12–8	$A_{cl(\text{NI})} = 1 + \dfrac{R_f}{R_i}$	Voltage gain (noninverting)
12–9	$A_{cl(\text{VF})} = 1$	Voltage gain (voltage-follower)
12–10	$A_{cl(\text{I})} = -\dfrac{R_f}{R_i}$	Voltage gain (inverting)

Op-Amp Impedances

12–11	$Z_{in(\mathrm{NI})} = (1 + A_{ol}B)Z_{in}$	Input impedance (noninverting)
12–12	$Z_{out(\mathrm{NI})} = \dfrac{Z_{out}}{1 + A_{ol}B}$	Output impedance (noninverting)
12–13	$Z_{in(\mathrm{VF})} = (1 + A_{ol})Z_{in}$	Input impedance (voltage-follower)
12–14	$Z_{out(\mathrm{VF})} = \dfrac{Z_{out}}{1 + A_{ol}}$	Output impedance (voltage-follower)
12–15	$Z_{in(\mathrm{I})} \cong R_i$	Input impedance (inverting)
12–16	$Z_{out(\mathrm{I})} = \dfrac{Z_{out}}{1 + A_{ol}B}$	Output impedance (inverting)

Op-Amp Frequency Responses

12–17	$BW = f_{cu}$	Op-amp bandwidth
12–18	$\dfrac{V_{out}}{V_{in}} = \dfrac{1}{\sqrt{1 + f^2/f_c^2}}$	*RC* attenuation
12–19	$A_{ol} = \dfrac{A_{ol(\mathrm{mid})}}{\sqrt{1 + f^2/f_c^2}}$	Open-loop voltage gain
12–20	$\theta = -\tan^{-1}\left(\dfrac{f}{f_c}\right)$	*RC* phase shift
12–21	$f_{c(cl)} = f_{c(ol)}(1 + BA_{ol(mid)})$	Closed-loop critical frequency
12–22	$BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})$	Closed-loop bandwidth
12–23	$f_T = A_{cl}f_{c(cl)}$	Unity-gain bandwidth

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. An ideal op-amp has an infinite input impedance.
2. An ideal op-amp has a very high output impedance.
3. The op-amp can operate in both the differential mode or the common mode.
4. Common-mode rejection means that a signal appearing on both inputs is effectively cancelled.
5. CMRR stands for common-mode rejection reference.
6. Slew rate determines how fast the output can change in response to a step input.
7. Negative feedback reduces the gain of an op-amp from its open-loop value.
8. Negative feedback reduces the bandwidth of an op-amp from its open-loop value.
9. A noninverting amplifier uses negative feedback.
10. The gain of a voltage-follower is very high.
11. Negative feedback affects the input and output impedances of an op-amp.
12. A compensated op-amp has a gain roll-off of −20 dB/decade above the critical frequency.
13. The gain-bandwidth product equals the unity-gain frequency.
14. If the feedback resistor in an inverting amplifier opens, the gain becomes zero.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If R_f is decreased in the circuit of Figure 12–18, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
2. If $V_{in} = 1$ mV and R_f opens in the circuit of Figure 12–18, the output voltage will
   (a) increase **(b)** decrease **(c)** not change

3. If R_i is increased in the circuit of Figure 12–18, the voltage gain will
(a) increase **(b)** decrease **(c)** not change

4. If 10 mV are applied to the input to the op-amp circuit of Figure 12–22 and R_f is increased, the output voltage will
(a) increase **(b)** decrease **(c)** not change

5. In Figure 12–28, if R_f is changed from 100 kΩ to 68 kΩ, the feedback attenuation will
(a) increase **(b)** decrease **(c)** not change

6. If the closed-loop gain in Figure 12–43(a) is increased by increasing the value of R_f, the closed-loop bandwidth will
(a) increase **(b)** decrease **(c)** not change

7. If R_f is changed to 470 kΩ and R_i is changed to 10 kΩ in Figure 12–43(b), the closed-loop bandwidth will
(a) increase **(b)** decrease **(c)** not change

8. If R_i in Figure 12–43(b) opens, the output voltage will
(a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 12–1

1. An integrated circuit (IC) op-amp has
(a) two inputs and two outputs **(b)** one input and one output
(c) two inputs and one output

2. Which of the following characteristics does not necessarily apply to an op-amp?
(a) High gain **(b)** Low power
(c) High input impedance **(d)** Low output impedance

3. A differential amplifier
(a) is part of an op-amp **(b)** has one input and one output
(c) has two outputs **(d)** answers (a) and (c)

Section 12–2

4. When an op-amp is operated in the single-ended differential mode,
(a) the output is grounded
(b) one input is grounded and a signal is applied to the other
(c) both inputs are connected together
(d) the output is not inverted

5. In the double-ended differential mode,
(a) a signal is applied between the two inputs **(b)** the gain is 1
(c) the outputs are different amplitudes **(d)** only one supply voltage is used

6. In the common mode,
(a) both inputs are grounded **(b)** the outputs are connected together
(c) an identical signal appears on both inputs **(d)** the output signals are in-phase

7. Common-mode gain is
(a) very high **(b)** very low
(c) always unity **(d)** unpredictable

8. If $A_{ol} = 3500$ and $A_{cm} = 0.35$, the CMRR is
(a) 1225 **(b)** 10,000
(c) 80 dB **(d)** answers (b) and (c)

9. With zero volts on both inputs, an op-amp ideally should have an output equal to
(a) the positive supply voltage **(b)** the negative supply voltage
(c) zero **(d)** the CMRR

10. Of the values listed, the most realistic value for open-loop gain of an op-amp is
(a) 1 **(b)** 2000 **(c)** 80 dB **(d)** 100,000

11. A certain op-amp has bias currents of 50 μA and 49.3 μA. The input offset current is
(a) 700 nA **(b)** 99.3 μA **(c)** 49.7 μA **(d)** none of these

12. The output of a particular op-amp increases 8 V in 12 μs. The slew rate is
(a) 96 V/μs **(b)** 0.67 V/μs **(c)** 1.5 V/μs **(d)** none of these

Section 12–3

13. The purpose of offset nulling is to
(a) reduce the gain **(b)** equalize the input signals
(c) zero the output error voltage **(d)** answers (b) and (c)

14. The use of negative feedback
(a) reduces the voltage gain of an op-amp **(b)** makes the op-amp oscillate
(c) makes linear operation possible **(d)** answers (a) and (c)

Section 12–4

15. For an op-amp with negative feedback, the output is
(a) equal to the input
(b) increased
(c) fed back to the inverting input
(d) fed back to the noninverting input

16. A certain noninverting amplifier has an R_i of 1.0 kΩ and an R_f of 100 kΩ. The closed-loop gain is
(a) 100,000 **(b)** 1000 **(c)** 101 **(d)** 100

17. If the feedback resistor in Question 16 is open, the voltage gain
(a) increases **(b)** decreases **(c)** is not affected **(d)** depends on R_i

18. A certain inverting amplifier has a closed-loop gain of 25. The op-amp has an open-loop gain of 100,000. If another op-amp with an open-loop gain of 200,000 is substituted in the configuration, the closed-loop gain
(a) doubles **(b)** drops to 12.5 **(c)** remains at 25 **(d)** increases slightly

19. A voltage-follower
(a) has a gain of 1 **(b)** is noninverting
(c) has no feedback resistor **(d)** has all of these

Section 12–5

20. Negative feedback
(a) increases the input and output impedances
(b) increases the input impedance and the bandwidth
(c) decreases the output impedance and the bandwidth
(d) does not affect impedances or bandwidth

Section 12–6

21. Bias current compensation
(a) reduces gain **(b)** reduces output error voltage
(c) increases bandwidth **(d)** has no effect

Section 12–7

22. The midrange open-loop gain of an op-amp
(a) extends from the lower critical frequency to the upper critical frequency
(b) extends from 0 Hz to the upper critical frequency
(c) rolls off at 20 dB/decade beginning at 0 Hz
(d) answers (b) and (c)

23. The frequency at which the open-loop gain is equal to 1 is called
(a) the upper critical frequency **(b)** the cutoff frequency
(c) the notch frequency **(d)** the unity-gain frequency

24. Phase shift through an op-amp is caused by
(a) the internal *RC* circuits **(b)** the external *RC* circuits
(c) the gain roll-off **(d)** negative feedback

25. Each *RC* circuit in an op-amp

(a) causes the gain to roll off at −6 dB/octave

(b) causes the gain to roll off at −20 dB/decade

(c) reduces the midrange gain by 3 dB

(d) answers (a) and (b)

26. If a certain op-amp has a midrange open-loop gain of 200,000 and a unity-gain frequency of 5 MHz, the gain-bandwidth product is

(a) 200,000 Hz **(b)** 5,000,000 Hz

(c) 1×10^{12} Hz **(d)** not determinable from the information

Section 12–8

27. The bandwidth of an ac amplifier having a lower critical frequency of 1 kHz and an upper critical frequency of 10 kHz is

(a) 1 kHz **(b)** 9 kHz **(c)** 10 kHz **(d)** 11 kHz

28. The bandwidth of a dc amplifier having an upper critical frequency of 100 kHz is

(a) 100 kHz **(b)** unknown **(c)** infinity **(d)** 0 kHz

29. When negative feedback is used, the gain-bandwidth product of an op-amp

(a) increases **(b)** decreases **(c)** stays the same **(d)** fluctuates

30. If a certain op-amp has a closed-loop gain of 20 and an upper critical frequency of 10 MHz, the gain-bandwidth product is

(a) 200 MHz **(b)** 10 MHz **(c)** the unity-gain frequency **(d)** answers (a) and (c)

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 12–1

Introduction to Operational Amplifiers

1. Compare a practical op-amp to an ideal op-amp.
2. Two IC op-amps are available to you. Their characteristics are listed below. Choose the one you think is more desirable.

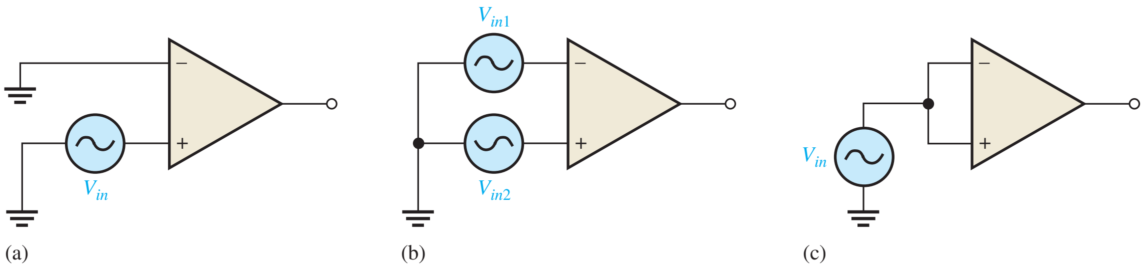
Op-amp 1: $Z_{in} = 5\ \text{M}\Omega, Z_{out} = 100\Omega, A_{ol} = 50{,}000$

Op-amp 2: $Z_{in} = 10\ \text{M}\Omega, Z_{out} = 75\ \Omega, A_{ol} = 150{,}000$

Section 12–2

Op-Amp Input Modes and Parameters

3. Identify the type of input mode for each op-amp in Figure 12–60.
4. A certain op-amp has a CMRR of 250,000. Convert this to decibels.
5. The open-loop gain of a certain op-amp is 175,000. Its common-mode gain is 0.18. Determine the CMRR in decibels.
6. An op-amp datasheet specifies a CMRR of 300,000 and an A_{ol} of 90,000. What is the common-mode gain?
7. Determine the bias current, I_{BIAS}, given that the input currents to an op-amp are 8.3 μA and 7.9 μA.



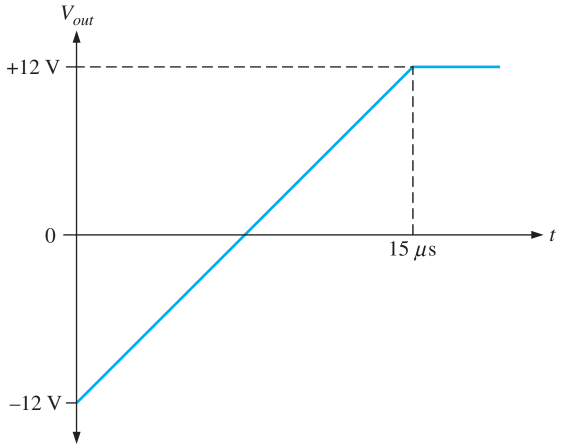
▲ FIGURE 12–60

8. Distinguish between input bias current and input offset current, and then calculate the input offset current in Problem 7.

9. Figure 12–61 shows the output voltage of an op-amp in response to a step input. What is the slew rate?

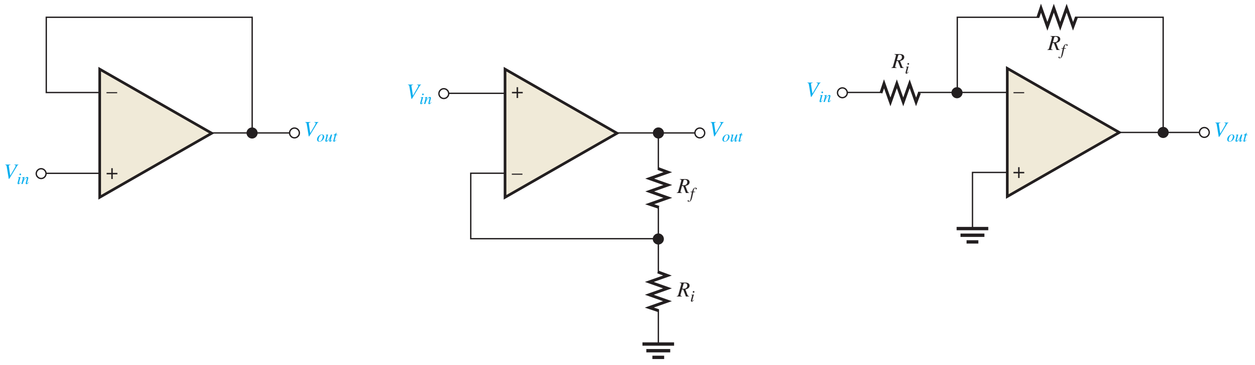
10. How long does it take the output voltage of an op-amp to go from -10 V to $+10$ V if the slew rate is 0.5 V/μS?

▶ FIGURE 12–61



Section 12–4 Op-Amps with Negative Feedback

11. Identify each of the op-amp configurations in Figure 12–62.



(a) (b) (c)

▲ FIGURE 12–62

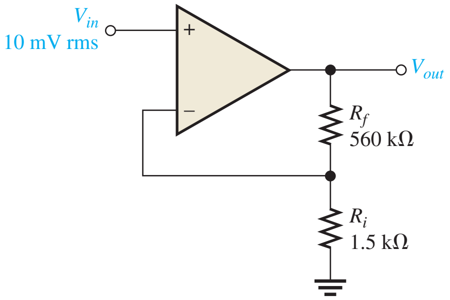
12. A noninverting amplifier has an R_i of 1.0 kΩ and an R_f of 100 kΩ. Determine V_f and B if $V_{out} = 5$ V.

13. For the amplifier in Figure 12–63, determine the following:

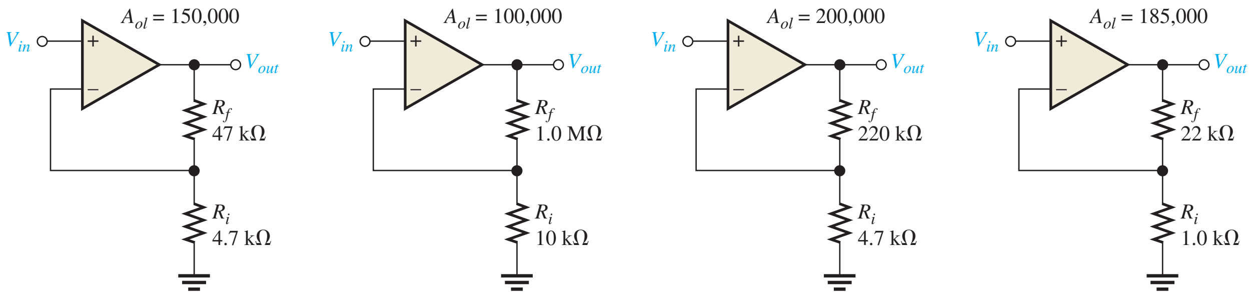
(a) $A_{cl(NI)}$ **(b)** V_{out} **(c)** V_f

▶ FIGURE 12–63

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F12-63).



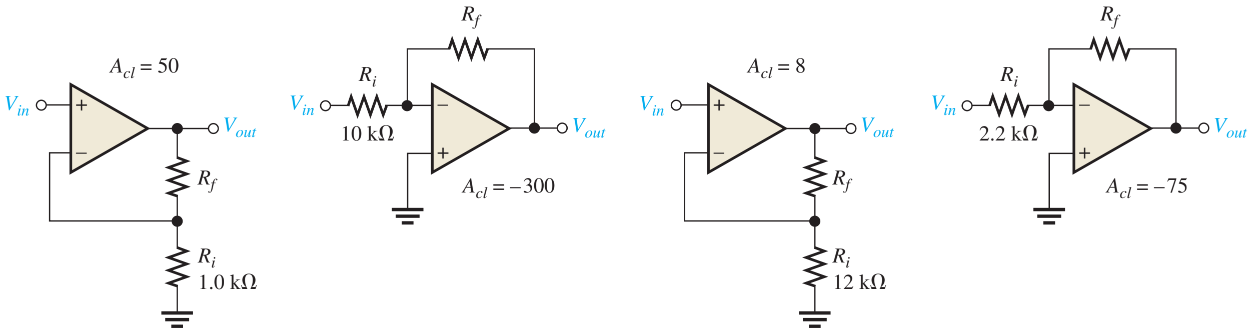
14. Determine the closed-loop gain of each amplifier in Figure 12–64.


A_{ol} = 150,000
V_{in}
V_{out}
R_f 47 kΩ
R_i 4.7 kΩ
A_{ol} = 100,000
V_{in}
V_{out}
R_f 1.0 MΩ
R_i 10 kΩ
A_{ol} = 200,000
V_{in}
V_{out}
R_f 220 kΩ
R_i 4.7 kΩ
A_{ol} = 185,000
V_{in}
V_{out}
R_f 22 kΩ
R_i 1.0 kΩ
+
−

(a) (b) (c) (d)

▲ **FIGURE 12–64**

15. Find the value of R_f that will produce the indicated closed-loop gain in each amplifier in Figure 12–65.

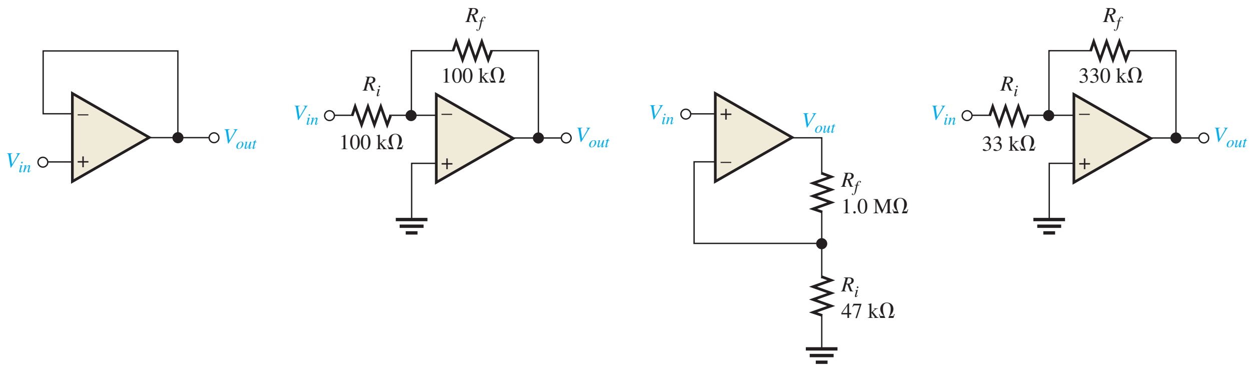

A_{cl} = 50
V_{in}
V_{out}
R_f
R_i 1.0 kΩ
R_f
R_i
V_{in}
10 kΩ
V_{out}
A_{cl} = −300
A_{cl} = 8
V_{in}
V_{out}
R_f
R_i 12 kΩ
R_f
R_i
V_{in}
2.2 kΩ
V_{out}
A_{cl} = −75
+
−

(a) (b) (c) (d)

▲ **FIGURE 12–65**

16. Find the gain of each amplifier in Figure 12–66.

17. If a signal voltage of 10 mV rms is applied to each amplifier in Figure 12–66, what are the output voltages and what is their phase relationship with inputs?


V_{in}
V_{out}
R_f
100 kΩ
R_i
V_{in}
100 kΩ
V_{out}
V_{in}
V_{out}
R_f 1.0 MΩ
R_i 47 kΩ
R_f
330 kΩ
R_i
V_{in}
33 kΩ
V_{out}
+
−

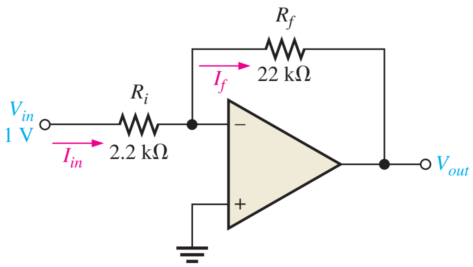
(a) (b) (c) (d)

▲ **FIGURE 12–66**

18. Determine the approximate values for each of the following quantities in Figure 12–67.

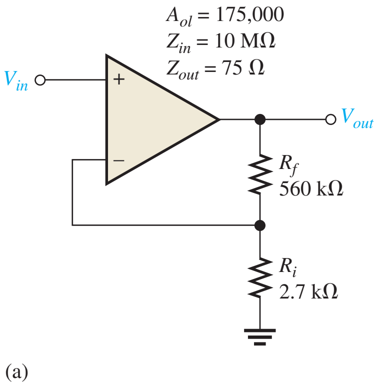
(a) I_{in} **(b)** I_f **(c)** V_{out} **(d)** closed-loop gain

▶ FIGURE 12–67


R_f
22 kΩ
I_f
R_i
V_{in}
1 V
I_{in}
2.2 kΩ
–
+
V_{out}

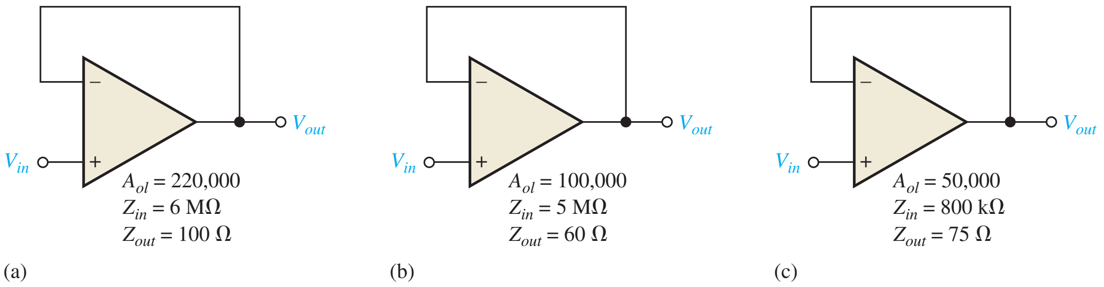
Section 12–5 Effects of Negative Feedback on Op-Amp Impedances

19. Determine the input and output impedances for each amplifier configuration in Figure 12–68.


A_{ol} = 175,000
Z_{in} = 10 MΩ
Z_{out} = 75 Ω
V_{in}
+
–
V_{out}
R_f
560 kΩ
R_i
2.7 kΩ
(a)
A_{ol} = 200,000
Z_{in} = 1 MΩ
Z_{out} = 25 Ω
V_{in}
V_{out}
R_f
47 kΩ
R_i
1.5 kΩ
(b)
A_{ol} = 50,000
Z_{in} = 2 MΩ
Z_{out} = 50 Ω
V_{in}
V_{out}
R_f
1.0 MΩ
R_i
56 kΩ
(c)

▲ FIGURE 12–68

20. Repeat Problem 19 for each circuit in Figure 12–69.


–
+
V_{out}
V_{in}
A_{ol} = 220,000
Z_{in} = 6 MΩ
Z_{out} = 100 Ω
(a)
V_{out}
V_{in}
A_{ol} = 100,000
Z_{in} = 5 MΩ
Z_{out} = 60 Ω
(b)
V_{out}
V_{in}
A_{ol} = 50,000
Z_{in} = 800 kΩ
Z_{out} = 75 Ω
(c)

▲ FIGURE 12–69

21. Repeat Problem 19 for each circuit in Figure 12–70.

Section 12–6 Bias Current and Offset Voltage

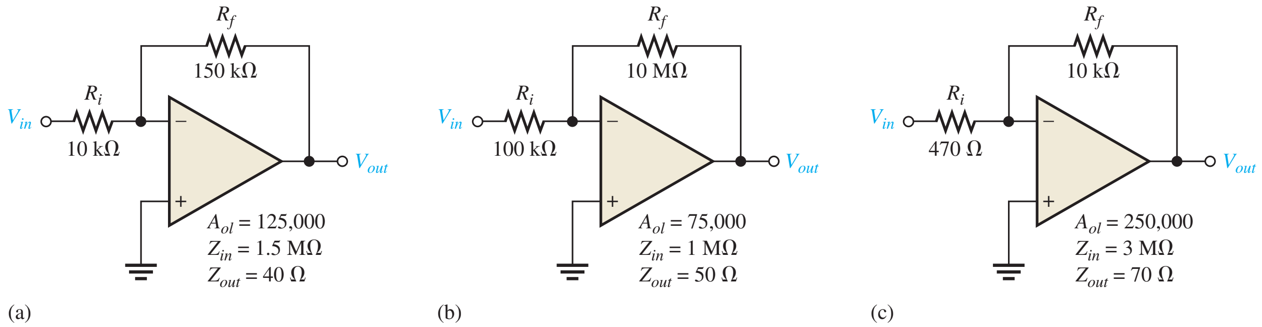
22. A voltage-follower is driven by a voltage source with a source resistance of 75 Ω.

(a) What value of compensating resistor is required for bias current, and where should the resistor be placed?

(b) If the two input currents after compensation are 42 μA and 40 μA, what is the output error voltage?

23. Determine the compensating resistor value for each amplifier configuration in Figure 12–68, and indicate the placement of the resistor.

24. A particular op-amp voltage-follower has an input offset voltage of 2 nV. What is the output error voltage?



▲ FIGURE 12–70

For Problem 21.

25. What is the input offset voltage of an op-amp if a dc output voltage of 35 mV is measured when the input voltage is zero? The op-amp's open-loop gain is specified to be 200,000.

Section 12–7 Open-Loop Frequency and Phase Responses

26. The midrange open-loop gain of a certain op-amp is 120 dB. Negative feedback reduces this gain by 50 dB. What is the closed-loop gain?

27. The upper critical frequency of an op-amp's open-loop response is 200 Hz. If the midrange gain is 175,000, what is the ideal gain at 200 Hz? What is the actual gain? What is the op-amp's open-loop bandwidth?

28. An *RC* lag circuit has a critical frequency of 5 kHz. If the resistance value is 1.0 kΩ, what is X_C when $f = 3$ kHz?

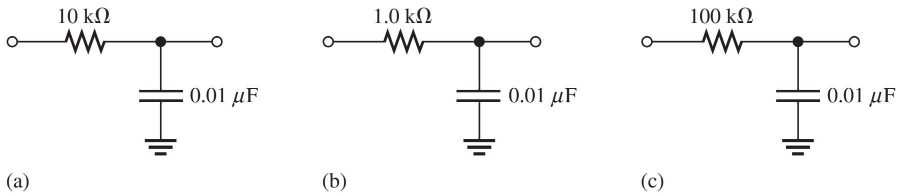
29. Determine the attenuation of an *RC* lag circuit with $f_c = 12$ kHz for each of the following frequencies.

(a) 1 kHz **(b)** 5 kHz **(c)** 12 kHz **(d)** 20 kHz **(e)** 100 kHz

30. The midrange open-loop gain of a certain op-amp is 80,000. If the open-loop critical frequency is 1 kHz, what is the open-loop gain at each of the following frequencies?

(a) 100 Hz **(b)** 1 kHz **(c)** 10 kHz **(d)** 1 MHz

31. Determine the phase shift through each circuit in Figure 12–71 at a frequency of 2 kHz.



▲ FIGURE 12–71

32. An *RC* lag circuit has a critical frequency of 8.5 kHz. Determine the phase shift for each frequency and plot a graph of its phase angle versus frequency.

(a) 100 Hz **(b)** 400 Hz **(c)** 850 Hz **(d)** 8.5 kHz **(e)** 25 kHz **(f)** 85 kHz

33. A certain op-amp has three internal amplifier stages with midrange gains of 30 dB, 40 dB, and 20 dB. Each stage also has a critical frequency associated with it as follows: $f_{c1} = 600$ Hz, $f_{c2} = 50$ kHz, and $f_{c3} = 200$ kHz.

(a) What is the midrange open-loop gain of the op-amp, expressed in dB?

(b) What is the total phase shift through the amplifier, including inversion, when the signal frequency is 10 kHz?

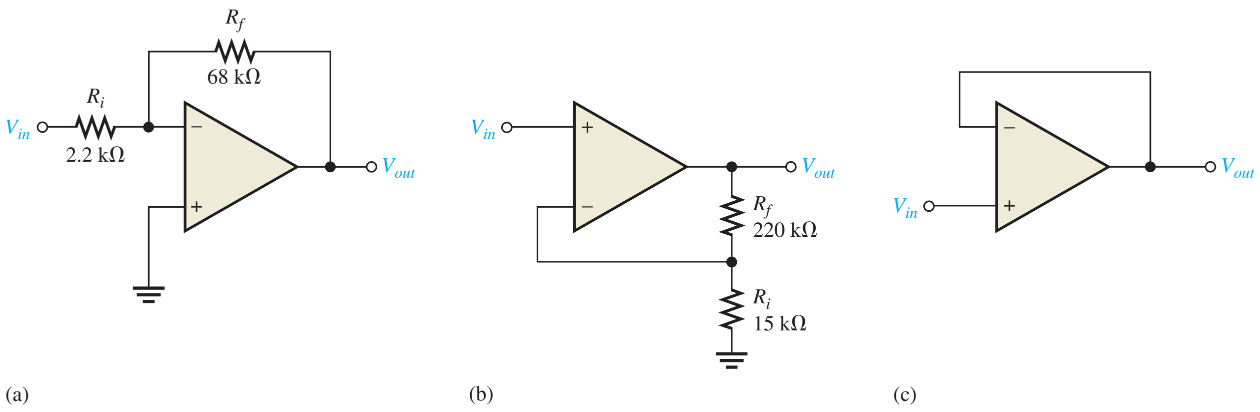
34. What is the gain roll-off rate in Problem 33 between the following frequencies?

(a) 0 Hz and 600 Hz **(b)** 600 Hz and 50 kHz

(c) 50 kHz and 200 kHz **(d)** 200 kHz and 1 MHz

Section 12–8 Closed-Loop Frequency Response

35. Determine the midrange gain in dB of each amplifier in Figure 12–72. Are these open-loop or closed-loop gains?


R_f
68 kΩ
R_i
V_{in}
2.2 kΩ
V_{out}
(a)
V_{in}
V_{out}
R_f
220 kΩ
R_i
15 kΩ
(b)
V_{out}
V_{in}
(c)

▲ FIGURE 12–72

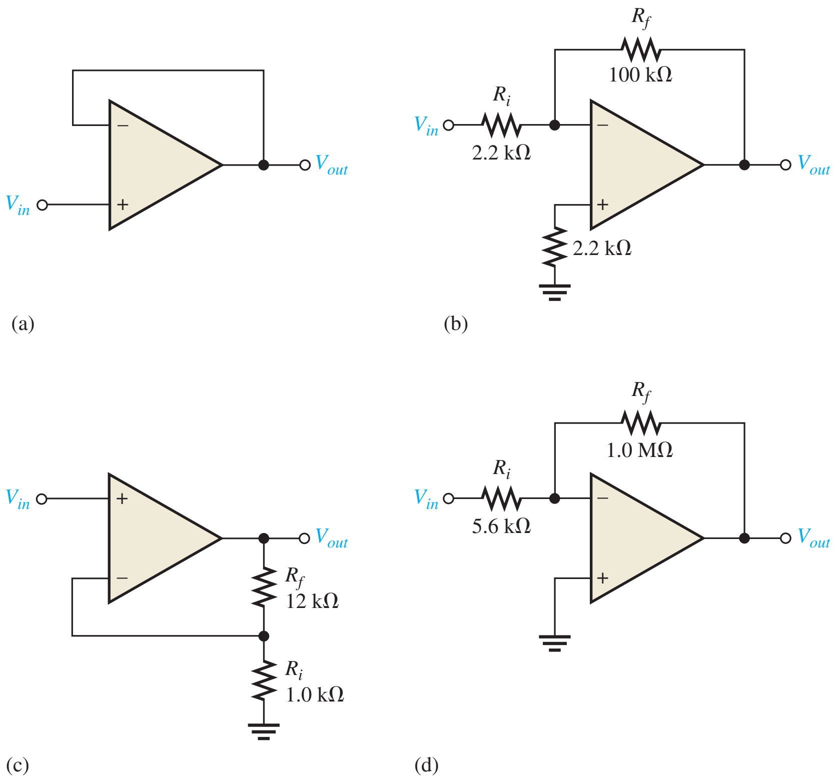
36. A certain amplifier has an open-loop gain in midrange of 180,000 and an open-loop critical frequency of 1500 Hz. If the attenuation of the feedback path is 0.015, what is the closed-loop bandwidth?

37. Given that $f_{c(ol)} = 750$ Hz, $A_{ol} = 89$ dB, and $f_{c(cl)} = 5.5$ kHz, determine the closed-loop gain in decibels.

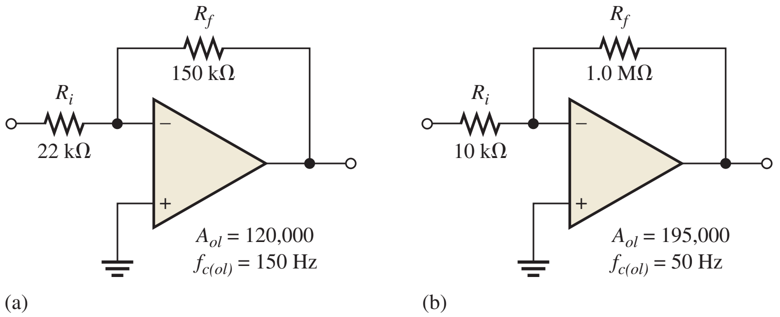
38. What is the unity-gain bandwidth in Problem 37?

39. For each amplifier in Figure 12–73, determine the closed-loop gain and bandwidth. The op-amps in each circuit exhibit an open-loop gain of 125 dB and a unity-gain bandwidth of 2.8 MHz.

► FIGURE 12–73


V_{out}
V_{in}
(a)
R_f
100 kΩ
R_i
V_{in}
2.2 kΩ
V_{out}
2.2 kΩ
(b)
V_{in}
V_{out}
R_f
12 kΩ
R_i
1.0 kΩ
(c)
R_f
1.0 MΩ
R_i
V_{in}
5.6 kΩ
V_{out}
(d)

40. Which of the amplifiers in Figure 12–74 has the smaller bandwidth?



R_f
150 kΩ
R_i
22 kΩ
−
+
A_{ol} = 120,000
$f_{c(ol)}$ = 150 Hz
(a)
R_f
1.0 MΩ
R_i
10 kΩ
−
+
A_{ol} = 195,000
$f_{c(ol)}$ = 50 Hz
(b)

▲ FIGURE 12–74

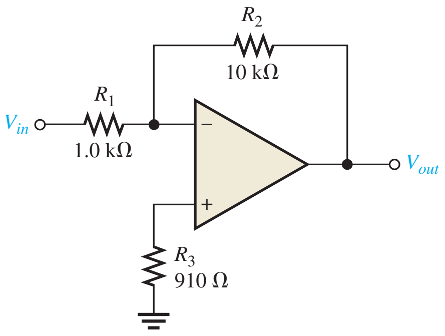
Section 12–9

Troubleshooting

41. Determine the most likely fault(s) for each of the following symptoms in Figure 12–75 with a 100 mV signal applied.

(a) No output signal.

(b) Output severely clipped on both positive and negative swings.



R_2
10 kΩ
R_1
V_{in}
1.0 kΩ
−
+
V_{out}
R_3
910 Ω

▲ FIGURE 12–75

42. Determine the effect on the output if the circuit in Figure 12–75 has the following fault (one fault at a time).

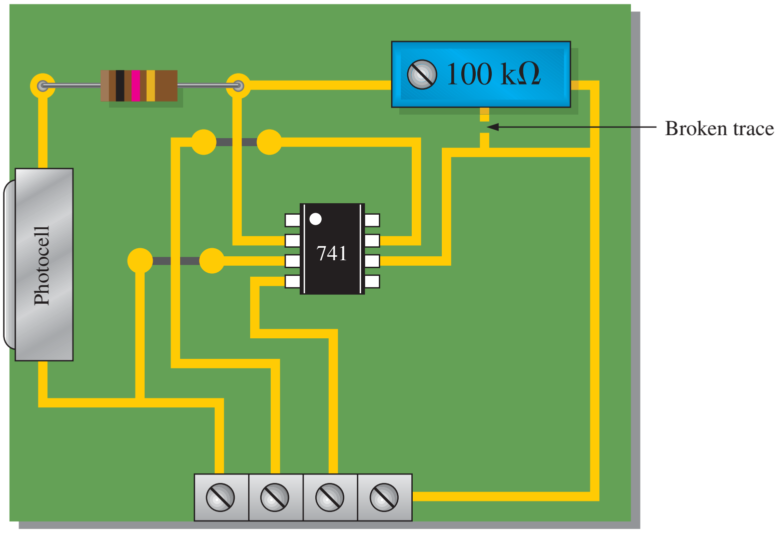
(a) Output pin is shorted to the inverting input.

(b) R_3 is open.

(c) R_3 is 10 kΩ instead of 910 Ω.

(d) R_1 and R_2 are swapped.

43. On the circuit board in Figure 12–76, what happens if the middle lead (wiper) of the 100 kΩ potentiometer is broken?



▲ FIGURE 12–76

APPLICATION ACTIVITY PROBLEMS

44. In the amplifier circuit of Figure 12–47, list the possible faults that will cause the push-pull stage to operate nonlinearly.

45. What indication would you observe if a 100 kΩ resistor is incorrectly installed for R_2 in Figure 12–47?

46. What voltage will you measure on the output of the amplifier in Figure 12–47 if diode D_1 opens?

DATASHEET PROBLEMS

47. Refer to the partial 741 datasheet (LM741) in Figure 12–77. Determine the input resistance (impedance) of a noninverting amplifier which uses a 741 op-amp with $R_f = 47\text{ k}\Omega$ and $R_i = 470\ \Omega$. Use typical values.

48. Refer to the partial datasheet in Figure 12–77. Determine the input impedances of a LM741 op-amp connected as an inverting amplifier with a closed-loop voltage gain of 100 and $R_f = 100\text{ k}\Omega$.

49. Refer to Figure 12–77 and determine the minimum open-loop voltage gain for an LM741 expressed as a ratio of output volts to input volts.

50. Refer to Figure 12–77. How long does it typically take the output voltage of an LM741 to make a transition from -8 V to $+8$ V in response to a step input?

ADVANCED PROBLEMS

51. Design a noninverting amplifier with an appropriate closed-loop voltage gain of 150 and a minimum input impedance of 100 MΩ using a 741 op-amp. Include bias current compensation.

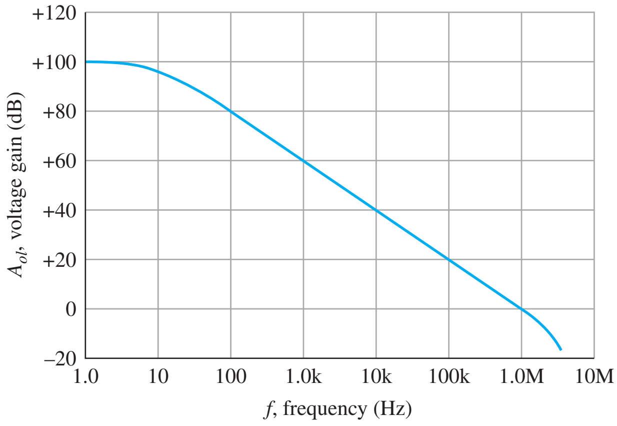
52. Design an inverting amplifier using a 741 op-amp. The voltage gain must be 68 ± 5% and the input impedance must be approximately 10 kΩ. Include bias current compensation.

Electrical Characteristics

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$T_A = 25°C$	—	—	—	—	—	—	—	—	—	
	$R_S \leq 10\ k\Omega$	—	—	—	—	—	5.0	—	2.0	6.0	mV
	$R_S \leq 50\ \Omega$	—	0.8	3.0	—	—	—	—	—	—	mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	—	—	—	—	—	—	—	
	$R_S \leq 50\ \Omega$	—	—	4.0	—	—	—	—	—	—	mV
	$R_S \leq 10\ k\Omega$	—	—	—	—	—	6.0	—	—	7.5	mV
Average input offset voltage drift		—	—	15	—	—	—	—	—	—	μV/°C
		—	—	—	—	—	—	—	—	—	
Input offset voltage adjustment range	$T_A = 25°C, V_S = \pm 20\ V$	±10	—	—	—	±15	—	—	±15	—	mV
		—	—	—	—	—	—	—	—	—	
Input offset current	$T_A = 25°C$	—	3.0	30	—	20	200	—	20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	70	—	85	500	—	—	300	nA
Average input offset current drift		—	—	0.5	—	—	—	—	—	—	nA/°C
		—	—	—	—	—	—	—	—	—	
Input bias current	$T_A = 25°C$	—	30	80	—	80	500	—	80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	0.210	—	—	1.5	—	—	0.8	μA
Input resistance	$T_A = 25°C, V_S = \pm 20\ V$	1.0	6.0	—	0.3	2.0	—	0.3	2.0	—	MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	0.5	—	—	—	—	—	—	—	—	MΩ
	$V_S = \pm 20\ V$	—	—	—	—	—	—	—	—	—	
Input voltage range	$T_A = 25°C$	—	—	—	—	—	—	—	±12	±13	V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	—	±12	±13	—	—	—	—	V
Large-signal voltage gain	$T_A = 25°C, R_L \geq 2\ k\Omega$	—	—	—	—	—	—	—	—	—	
	$V_S = \pm 20\ V, V_O = \pm 15\ V$	50	—	—	—	—	—	—	—	—	V/mV
	$V_S = \pm 15\ V, V_O = \pm 10\ V$	—	—	—	50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	—	—	—	—	—	—	—	
	$R_L \geq 2\ k\Omega$	—	—	—	—	—	—	—	—	—	
	$V_S = \pm 20\ V, V_O = \pm 15\ V$	32	—	—	—	—	—	—	—	—	V/mV
	$V_S = \pm 15\ V, V_O = \pm 10\ V$	—	—	—	25	—	—	15	—	—	V/mV
	$V_S = \pm 5\ V, V_O = \pm 2\ V$	10	—	—	—	—	—	—	—	—	V/mV
Output voltage swing	$V_S = \pm 20\ V$	—	—	—	—	—	—	—	—	—	
	$R_L \geq 10\ k\Omega$	±16	—	—	—	—	—	—	—	—	V
	$R_L \geq 2\ k\Omega$	±15	—	—	—	—	—	—	—	—	V
	$V_S = \pm 15\ V$	—	—	—	—	—	—	—	—	—	
	$R_L \geq 10\ k\Omega$	—	—	—	±12	±14	—	±12	±14	—	V
	$R_L \geq 2\ k\Omega$	—	—	—	±10	±13	—	±10	±13	—	V
Output short circuit	$T_A = 25°C$	10	25	35	—	25	—	—	25	—	mA
Current	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10	—	40	—	—	—	—	—	—	mA
Common-mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$	—	—	—	—	—	—	—	—	—	
rejection ratio	$R_S \leq 10\ k\Omega, V_{CM} = \pm 12\ V$	—	—	—	70	90	—	70	90	—	dB
	$R_S \leq 50\ \Omega, V_{CM} = \pm 12\ V$	80	95	—	—	—	—	—	—	—	dB
Supply voltage rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,	—	—	—	—	—	—	—	—	—	
ratio	$V_S = \pm 20\ V$ to $V_S = \pm 5\ V$	—	—	—	—	—	—	—	—	—	
	$R_S \leq 50\ \Omega$	86	96	—	—	—	—	—	—	—	dB
	$R_S \leq 10\ k\Omega$	—	—	—	77	96	—	77	96	—	dB
Transient response	$T_A = 25°C$, Unity gain	—	—	—	—	—	—	—	—	—	
Rise time		—	0.25	0.8	—	0.3	—	—	0.3	—	μs
Overshoot		—	6.0	20	—	5	—	—	5	—	%
Bandwidth	$T_A = 25°C$	0.437	1.5	—	—	—	—	—	—	—	MHz
Slew rate	$T_A = 25°C$, Unity gain	0.3	0.7	—	—	0.5	—	—	0.5	—	V/μs
Supply current	$T_A = 25°C$			—	—	1.7	2.8	—	1.7	2.8	mA
Power consumption	$T_A = 25°C$	—	—	—	—	—	—	—	—	—	
	$V_S = \pm 20\ V$	—	80	150	—	—	—	—	—	—	mW
	$V_S = \pm 15\ V$	—	—	—	—	50	85	—	50	85	mW
LM741A	$V_S = \pm 20\ V$	—	—	—	—	—	—	—	—	—	
	$T_A = T_{AMIN}$	—	—	165	—	—	—	—	—	—	mW
	$T_A = T_{AMAX}$	—	—	135	—	—	—	—	—	—	mW
LM741	$V_S = \pm 15\ V$	—	—	—	—	—	—	—	—	—	
	$T_A = T_{AMIN}$	—	—	—	—	60	100	—	—	—	mW
	$T_A = T_{AMAX}$	—	—	—	—	45	75	—	—	—	mW

▲ FIGURE 12–77

53. Design a noninverting amplifier with an upper critical frequency, f_{cu}, of 10 kHz using a 741 op-amp. The dc supply voltages are ±15 V. Refer to Figure 12–78. Include bias current compensation.

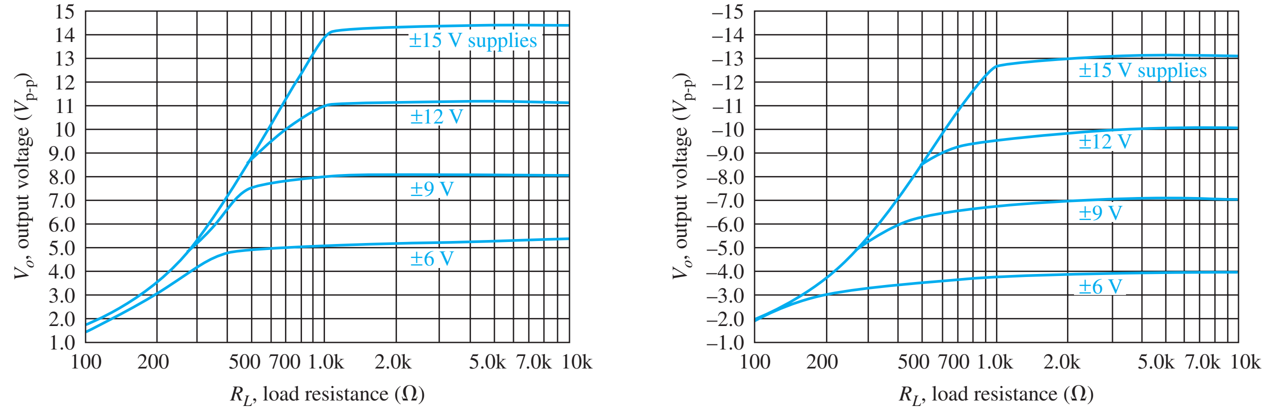


▲ FIGURE 12–78

54. For the circuit you designed in Problem 53, determine the minimum load resistance if the minimum output voltage swing is to be ±10 V. Refer to the datasheet graphs in Figure 12–79.

55. Design an inverting amplifier using a 741 op-amp if a midrange voltage gain of 50 and a bandwidth of 20 kHz is required. Include bias current compensation.

56. What is the maximum closed-loop voltage gain that can be achieved with a 741 op-amp if the bandwidth must be no less than 5 kHz?



(a) Positive output voltage swing versus load resistance

(b) Negative output voltage swing versus load resistance

▲ FIGURE 12–79

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

57. Open file TSP12-57 and determine the fault.

58. Open file TSP12-58 and determine the fault.

59. Open file TSP12-59 and determine the fault.

60. Open file TSP12-60 and determine the fault.

61. Open file TSP12-61 and determine the fault.

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63. Open file TSP12-63 and determine the fault.
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66. Open file TSP12-66 and determine the fault.
67. Open file TSP12-67 and determine the fault.
68. Open file TSP12-68 and determine the fault.
69. Open file TSP12-69 and determine the fault.
70. Open file TSP12-70 and determine the fault.
71. Open file TSP12-71 and determine the fault.
72. Open file TSP12-72 and determine the fault.

BASIC OP-AMP CIRCUITS

13

CHAPTER OUTLINE

13–1 Comparators
13–2 Summing Amplifiers
13–3 Integrators and Differentiators
13–4 Troubleshooting
Application Activity
Programmable Analog Technology

CHAPTER OBJECTIVES

- Describe and analyze the operation of several types of comparator circuits
- Describe and analyze the operation of several types of summing amplifiers
- Describe and analyze the operation of integrators and differentiators
- Troubleshoot op-amp circuits

KEY TERMS

- Comparator
- Hysteresis
- Schmitt trigger
- Bounding
- Summing amplifier
- Integrator
- Differentiator

APPLICATION ACTIVITY PREVIEW

In the Application Activity in this chapter, an audio signal generator manufactured by a certain company is modified to include a pulse generator to provide a signal source for digital circuits. A voltage comparator generates the pulse waveform from the sine wave output of the audio generator. The duty cycle of the pulse waveform can be varied and is compatible with +5 V logic circuits.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

In the last chapter, you learned about the principles, operation, and characteristics of the operational amplifier. Op-amps are used in such a wide variety of circuits and applications that it is impossible to cover all of them in one chapter, or even in one book. Therefore, in this chapter, four fundamentally important circuits are covered to give you a foundation in op-amp circuits.

13–1 COMPARATORS

Operational amplifiers are often used as comparators to compare the amplitude of one voltage with another. In this application, the op-amp is used in the open-loop configuration, with the input voltage on one input and a reference voltage on the other.

After completing this section, you should be able to

- ❑ **Describe and analyze the operation of several types of comparator circuits**
- ❑ Discuss the operation of a zero-level detector
- ❑ Describe the operation of a nonzero-level detector
  - ◆ Calculate the reference voltage ◆ Analyze a nonzero-level detector
- ❑ Discuss how input noise affects comparator operation
  - ◆ Define *hysteresis* ◆ Explain how to reduce noise effects with hysteresis
  - ◆ Calculate the upper and lower trigger points ◆ Explain what a Schmitt trigger is
- ❑ Describe the operation of comparators with output bounding
  - ◆ Define *bounding* ◆ Analyze a comparator with both hysteresis and output bounding
- ❑ Discuss examples of comparator applications
  - ◆ Explain the operation of an over-temperature sensing circuit
  - ◆ Describe analog-to-digital (A/D) conversion

A **comparator** is a specialized op-amp circuit that compares two input voltages and produces an output that is always at either one of two states, indicating the greater or less than relationship between the inputs. Comparators provide very fast switching times, and many have additional capabilities (such as fast propagation delay or internal reference voltages) to optimize the comparison function. For example, some ultra-high-speed comparators can have propagation delays of as little as 500 ps. Because the output is always in one of two states, comparators are often used to interface between an analog and digital circuit.

For less critical applications, an op-amp running without negative feedback (open-loop) is often used as a comparator. Although op-amps are much slower and lack other special features, they have very high open-loop gain, which enables them to detect very tiny differences in the inputs. In general, comparators cannot be used as op-amps, but op-amps can be used as comparators in noncritical applications. Because an op-amp without negative feedback is essentially a comparator, we will look at the comparison function using a typical op-amp.

Zero-Level Detection

One application of an op-amp used as a comparator is to determine when an input voltage exceeds a certain level. Figure 13–1(a) shows a zero-level detector. Notice that the inverting (−) input is grounded to produce a zero level and that the input signal voltage is applied to the noninverting (+) input. Because of the high open-loop voltage gain, a very small difference voltage between the two inputs drives the amplifier into saturation, causing the output voltage to go to its limit. For example, consider an op-amp having $A_{ol} =$ 100,000. A voltage difference of only 0.25 mV between the inputs could produce an output voltage of $(0.25\text{ mV})(100{,}000) = 25\text{ V}$ *if* the op-amp were capable. However, since most op-amps have maximum output voltage limitations near the value of their dc supply voltages, the device would be driven into saturation.

Figure 13–1(b) shows the result of a sinusoidal input voltage applied to the noninverting (+) input of the zero-level detector. When the sine wave is positive, the output is at its maximum positive level. When the sine wave crosses 0, the amplifier is driven to its opposite state and the output goes to its maximum negative level, as shown. As you can see, the zero-level detector can be used as a squaring circuit to produce a square wave from a sine wave.

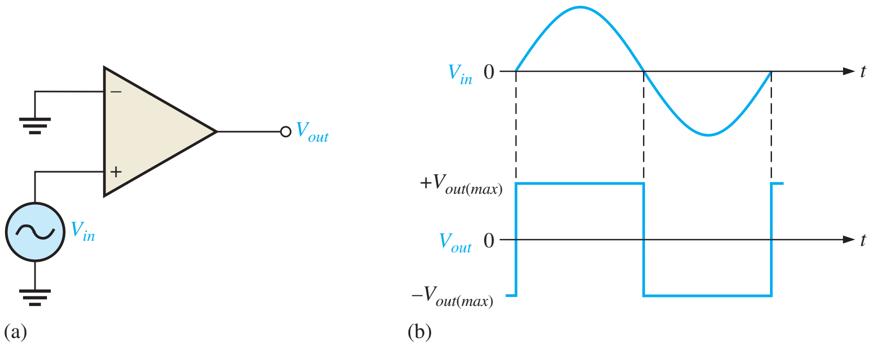

Vout
Vin
(a)
Vin 0
t
+Vout(max)
Vout 0
t
−Vout(max)
(b)

FIGURE 13–1

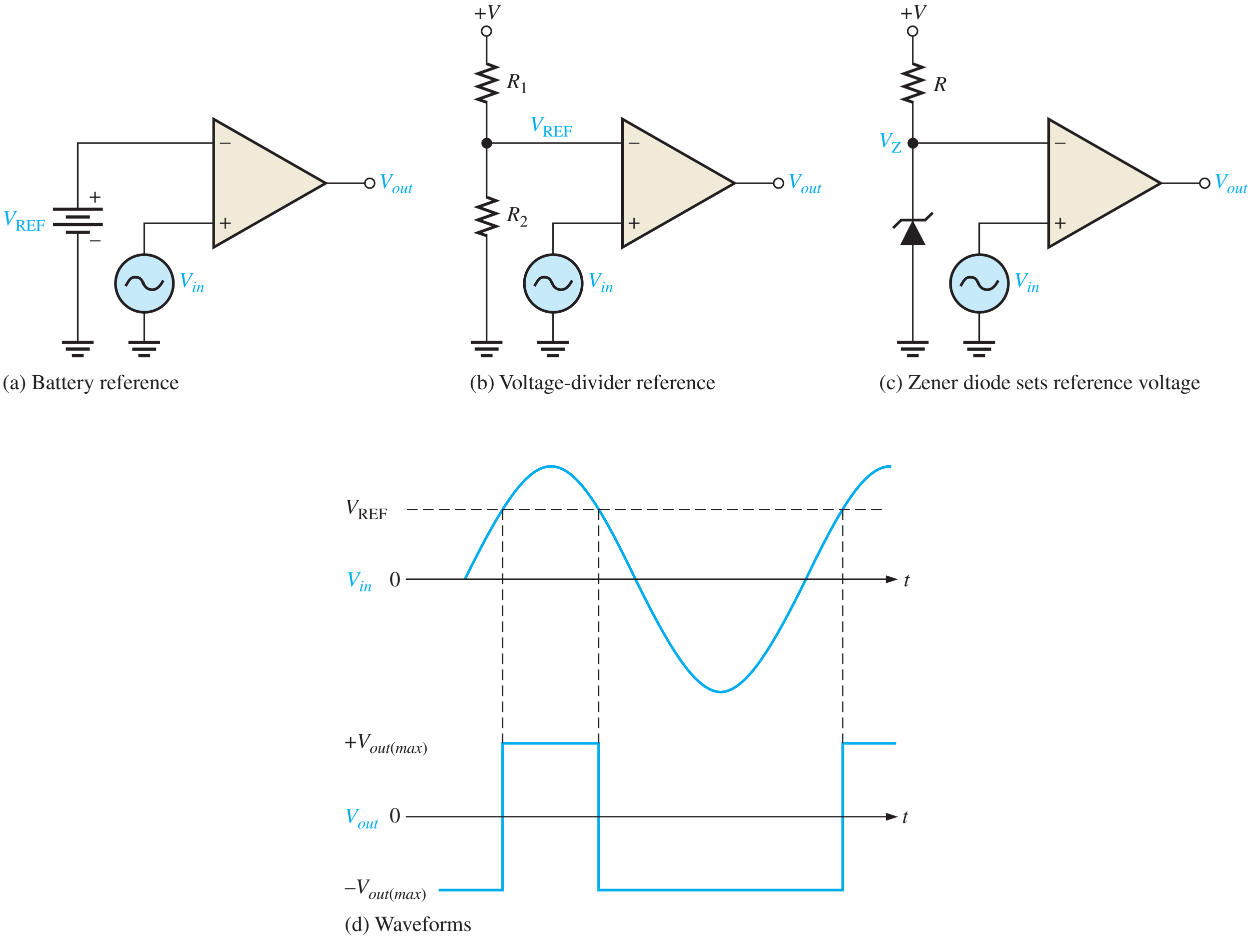
The op-amp as a zero-level detector.

Nonzero-Level Detection

The zero-level detector in Figure 13–1 can be modified to detect positive and negative voltages by connecting a fixed reference voltage source to the inverting (−) input, as shown in Figure 13–2(a). A more practical arrangement is shown in Figure 13–2(b) using a voltage divider to set the reference voltage, V_{REF}, as follows:

$$V_{\text{REF}} = \frac{R_2}{R_1 + R_2}(+V)$$

where $+V$ is the positive op-amp dc supply voltage. The circuit in Figure 13–2(c) uses a zener diode to set the reference voltage ($V_{\text{REF}} = V_Z$). As long as V_{in} is less than V_{REF}, the


VREF
+
−
Vout
Vin
+V
R1
VREF
R2
Vout
Vin
+V
R
VZ
Vout
Vin
VREF
Vin 0
t
+Vout(max)
Vout 0
t
−Vout(max)

(a) Battery reference

(b) Voltage-divider reference

(c) Zener diode sets reference voltage

(d) Waveforms

FIGURE 13–2

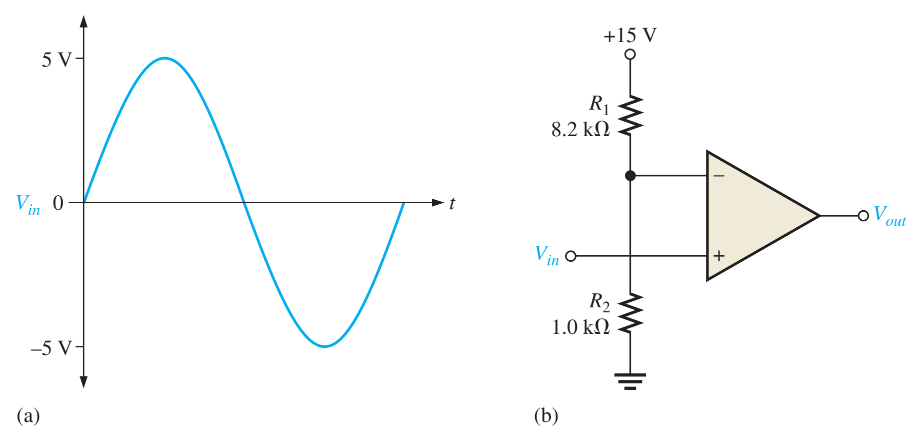
Nonzero-level detectors.

output remains at the maximum negative level. When the input voltage exceeds the reference voltage, the output goes to its maximum positive voltage, as shown in Figure 13–2(d) with a sinusoidal input voltage.

EXAMPLE 13–1

The input signal in Figure 13–3(a) is applied to the comparator in Figure 13–3(b). Draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ±14 V.

▶ **FIGURE 13–3**

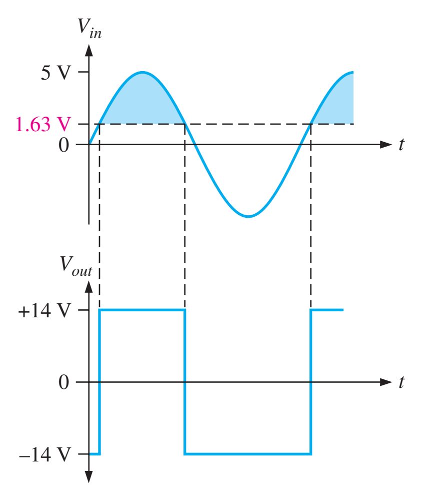


Solution The reference voltage is set by R_1 and R_2 as follows:

$$V_{\text{REF}} = \frac{R_2}{R_1 + R_2}(+V) = \frac{1.0\,\text{k}\Omega}{8.2\,\text{k}\Omega + 1.0\,\text{k}\Omega}(+15\text{ V}) = 1.63\text{ V}$$

As shown in Figure 13–4, each time the input exceeds +1.63 V, the output voltage switches to its +14 V level, and each time the input goes below +1.63 V, the output switches back to its −14 V level.

▶ **FIGURE 13–4**



Related Problem[*] Determine the reference voltage in Figure 13–3 if $R_1 = 22\text{ k}\Omega$ and $R_2 = 3.3\text{ k}\Omega$.

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[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Open the Multisim file E13-01 in the Examples folder on the companion website. Compare the output waveform to the specified input at any arbitrary frequency and verify that the reference voltage agrees with the calculated value.

Effects of Input Noise on Comparator Operation

In many practical situations, noise (unwanted voltage fluctuations) appears on the input line. This noise voltage becomes superimposed on the input voltage, as shown in Figure 13–5 for the case of a sine wave, and can cause a comparator to erratically switch output states.

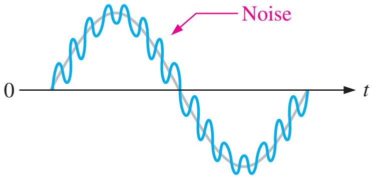


FIGURE 13–5

Sine wave with superimposed noise.

In order to understand the potential effects of noise voltage, consider a low-frequency sinusoidal voltage applied to the noninverting (+) input of an op-amp comparator used as a zero-level detector, as shown in Figure 13–6(a). Part (b) of the figure shows the input sine wave plus noise and the resulting output. When the sine wave approaches 0, the fluctuations due to noise may cause the total input to vary above and below 0 several times, thus producing an erratic output voltage.

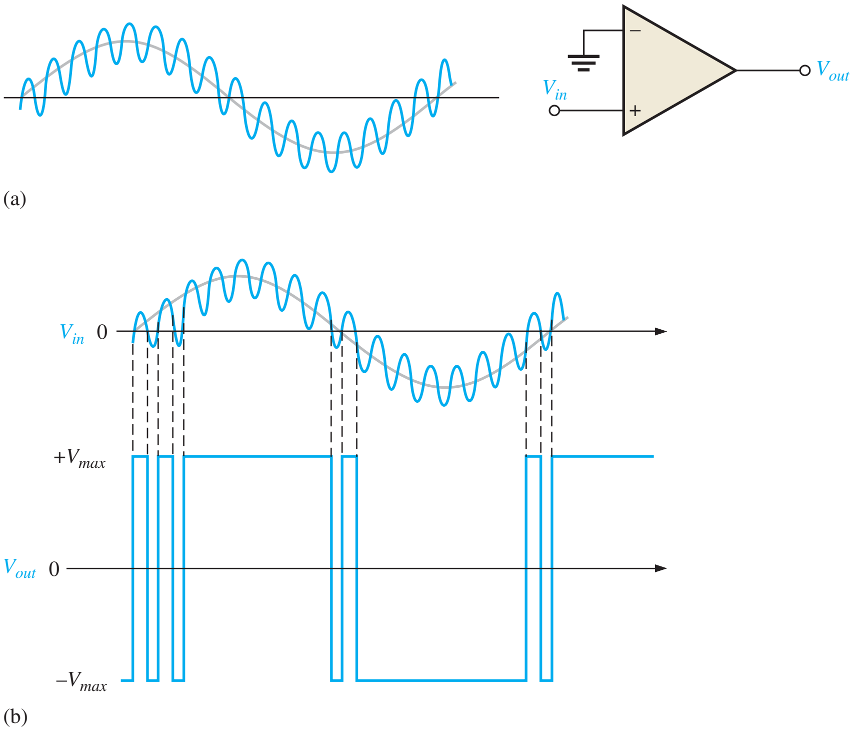


FIGURE 13–6

Effects of noise on comparator circuit.

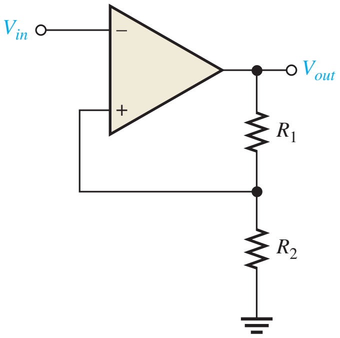
Reducing Noise Effects with Hysteresis An erratic output voltage caused by noise on the input occurs because the op-amp comparator switches from its negative output state to its positive output state at the same input voltage level that causes it to switch in the opposite direction, from positive to negative. This unstable condition occurs when the input voltage hovers around the reference voltage, and any small noise fluctuations cause the comparator to switch first one way and then the other.

In order to make the comparator less sensitive to noise, a technique incorporating positive feedback, called **hysteresis**, can be used. Basically, hysteresis means that there is a higher reference level when the input voltage goes from a lower to higher value than when it goes from a higher to a lower value. A good example of hysteresis is a common household thermostat that turns the furnace on at one temperature and off at another.

The two reference levels are referred to as the upper trigger point (UTP) and the lower trigger point (LTP). This two-level hysteresis is established with a positive feedback arrangement, as shown in Figure 13–7. Notice that the noninverting (+) input is connected to a resistive voltage divider such that a portion of the output voltage is fed back to the input. The input signal is applied to the inverting (−) input in this case.

▶ FIGURE 13–7

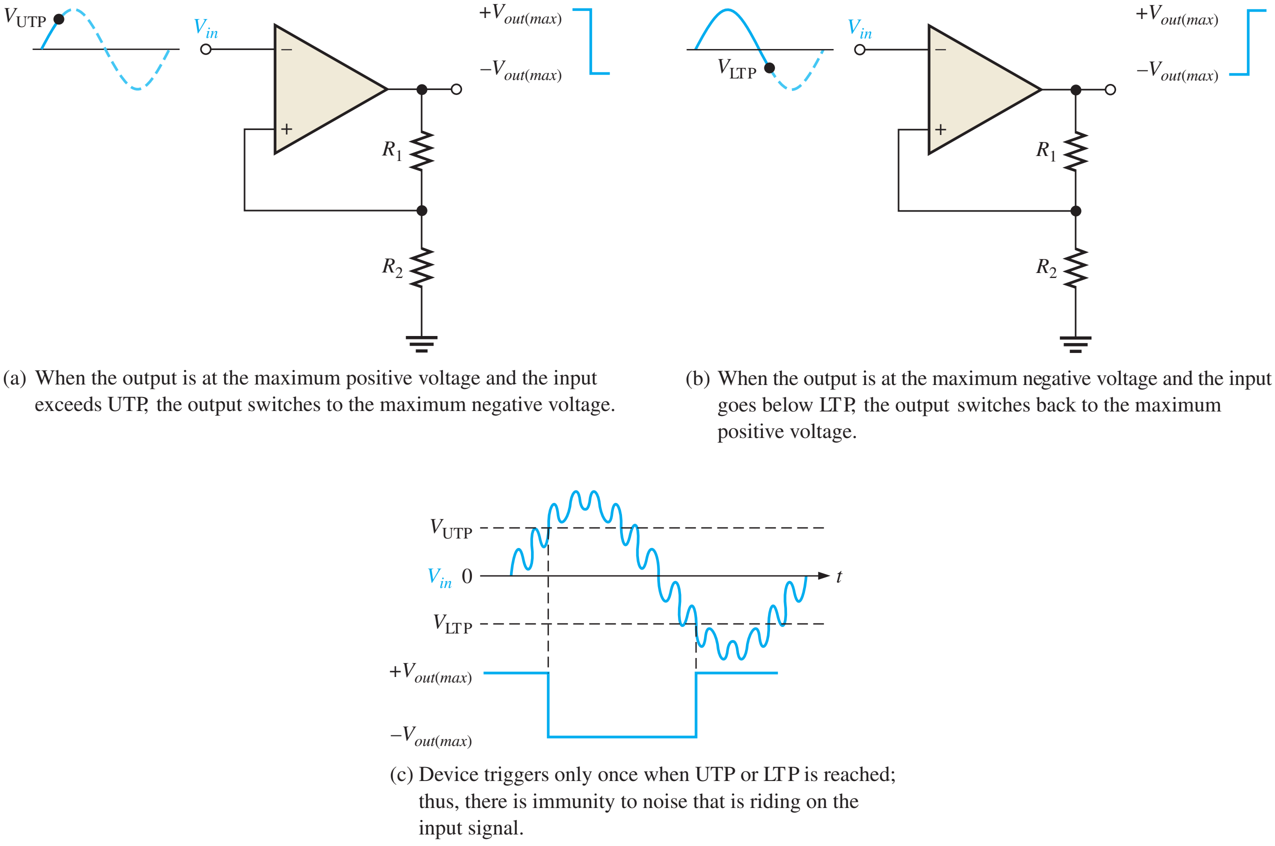
Comparator with positive feedback for hysteresis.



The basic operation of the comparator with hysteresis is illustrated in Figure 13–8. Assume that the output voltage is at its positive maximum, $+V_{out(max)}$. The voltage fed back to the noninverting input is V_{UTP} and is expressed as

Equation 13–1

$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$$



(a) When the output is at the maximum positive voltage and the input exceeds UTP, the output switches to the maximum negative voltage.

(b) When the output is at the maximum negative voltage and the input goes below LTP, the output switches back to the maximum positive voltage.

(c) Device triggers only once when UTP or LTP is reached; thus, there is immunity to noise that is riding on the input signal.

▲ FIGURE 13–8

Operation of a comparator with hysteresis.

When V_{in} exceeds V_{UTP}, the output voltage drops to its negative maximum, $-V_{out(max)}$, as shown in part (a). Now the voltage fed back to the noninverting input is V_{LTP} and is expressed as

$$V_{\text{LTP}} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$$

Equation 13–2

The input voltage must now fall below V_{LTP}, as shown in part (b), before the device will switch from the maximum negative voltage back to the maximum positive voltage. This means that a small amount of noise voltage has no effect on the output, as illustrated by Figure 13–8(c).

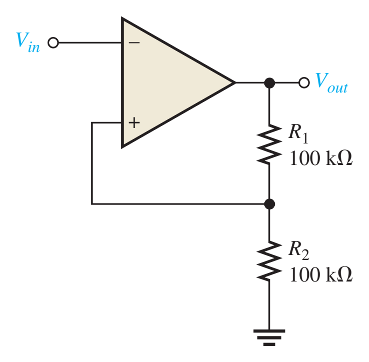
A comparator with built-in hysteresis is sometimes known as a **Schmitt trigger**. The amount of hysteresis is defined by the difference of the two trigger levels.

$$V_{\text{HYS}} = V_{\text{UTP}} - V_{\text{LTP}}$$

Equation 13–3

EXAMPLE 13–2 Determine the upper and lower trigger points for the comparator circuit in Figure 13–9. Assume that $+V_{out(max)} = +5\text{ V}$ and $-V_{out(max)} = -5\text{ V}$.

▶ FIGURE 13–9



Solution

$$V_{\text{UTP}} = \frac{R_2}{R_1 + R_2}(+V_{out(max)}) = 0.5(5\text{ V}) = \mathbf{+2.5\text{ V}}$$

$$V_{\text{LTP}} = \frac{R_2}{R_1 + R_2}(-V_{out(max)}) = 0.5(-5\text{ V}) = \mathbf{-2.5\text{ V}}$$

Related Problem Determine the upper and lower trigger points in Figure 13–9 for $R_1 = 68\text{ k}\Omega$ and $R_2 = 82\text{ k}\Omega$. Also assume the maximum output voltage levels are now ±7 V.

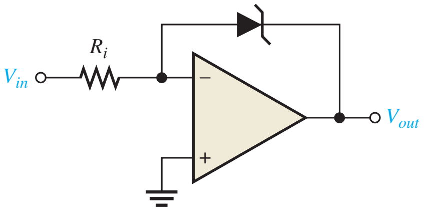
Open the Multisim file E13-02 in the Examples folder on the companion website. Determine the upper and lower trigger points and compare with the calculated values using a 5 V rms, 60 Hz sine wave for the input.

Output Bounding

In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than that provided by the saturated op-amp. A single zener diode can be used, as shown in Figure 13–10, to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other. This process of limiting the output range is called **bounding**.

▶ FIGURE 13–10

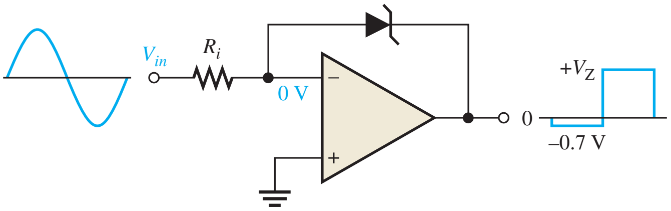
Comparator with output bounding.



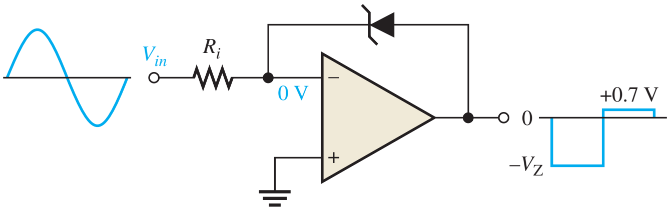
The operation is as follows. Since the anode of the zener is connected to the inverting (−) input, it is at virtual ground (≅ 0 V). Therefore, when the output voltage reaches a positive value equal to the zener voltage, it limits at that value, as illustrated in Figure 13–11(a). When the output switches negative, the zener acts as a regular diode and becomes forward-biased at 0.7 V, limiting the negative output voltage to this value, as shown in part (b). Turning the zener around limits the output voltage in the opposite direction.

▶ FIGURE 13–11

Operation of a bounded comparator.



(a) Bounded at a positive value

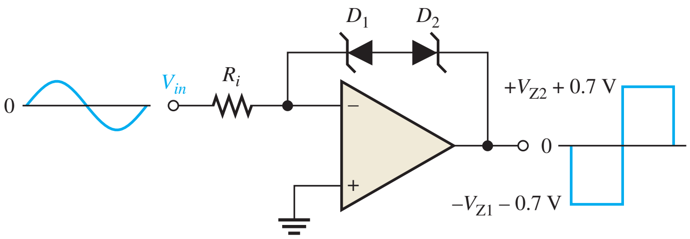


(b) Bounded at a negative value

Two zener diodes arranged as in Figure 13–12 limit the output voltage to the zener voltage plus the forward voltage drop (0.7 V) of the forward-biased zener, both positively and negatively, as shown.

▶ FIGURE 13–12

Double-bounded comparator.

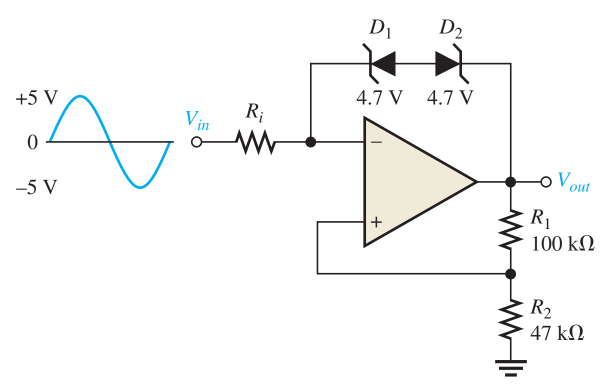


EXAMPLE 13–3

Determine the output voltage waveform for Figure 13–13.

Solution This comparator has both hysteresis and zener bounding. The voltage across D_1 and D_2 in either direction is 4.7 V + 0.7 V = 5.4 V. This is because one zener is always forward-biased with a drop of 0.7 V when the other one is in breakdown.

FIGURE 13–13



The voltage at the inverting (−) op-amp input is $V_{out} \pm 5.4$ V. Since the differential voltage is negligible, the voltage at the noninverting (+) op-amp input is also approximately $V_{out} \pm 5.4$ V. Thus,

$$V_{R1} = V_{out} - (V_{out} \pm 5.4\ \text{V}) = \pm 5.4\ \text{V}$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{\pm 5.4\ \text{V}}{100\ \text{k}\Omega} = \pm 54\ \mu\text{A}$$

Since the noninverting input current is negligible,

$$I_{R2} = I_{R1} = \pm 54\ \mu\text{A}$$

$$V_{R2} = R_2 I_{R2} = (47\ \text{k}\Omega)(\pm 54\ \mu\text{A}) = \pm 2.54\ \text{V}$$

$$V_{out} = V_{R1} + V_{R2} = \pm 5.4\ \text{V} \pm 2.54\ \text{V} = \pm 7.94\ \text{V}$$

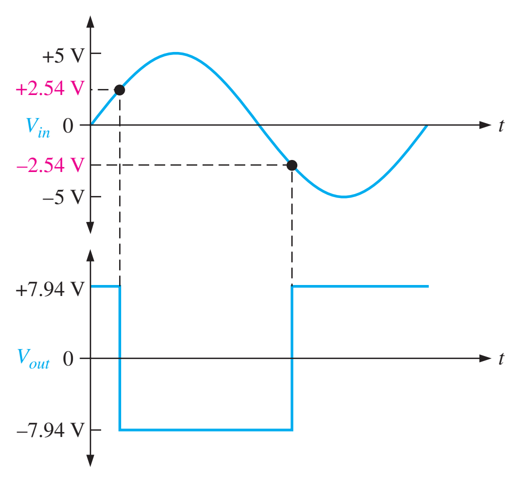
The upper trigger point (UTP) and the lower trigger point (LTP) are as follows:

$$V_{\text{UTP}} = \left(\frac{R_2}{R_1 + R_2}\right)(+V_{out}) = \left(\frac{47\ \text{k}\Omega}{147\ \text{k}\Omega}\right)(+7.94\ \text{V}) = +2.54\ \text{V}$$

$$V_{\text{LTP}} = \left(\frac{R_2}{R_1 + R_2}\right)(-V_{out}) = \left(\frac{47\ \text{k}\Omega}{147\ \text{k}\Omega}\right)(-7.94\ \text{V}) = -2.54\ \text{V}$$

The output waveform for the given input voltage is shown in Figure 13–14.

FIGURE 13–14



Related Problem Determine the upper and lower trigger points for Figure 13–13 if $R_1 = 150\ \text{k}\Omega$, $R_2 = 68\ \text{k}\Omega$, and the zener diodes are 3.3 V devices.

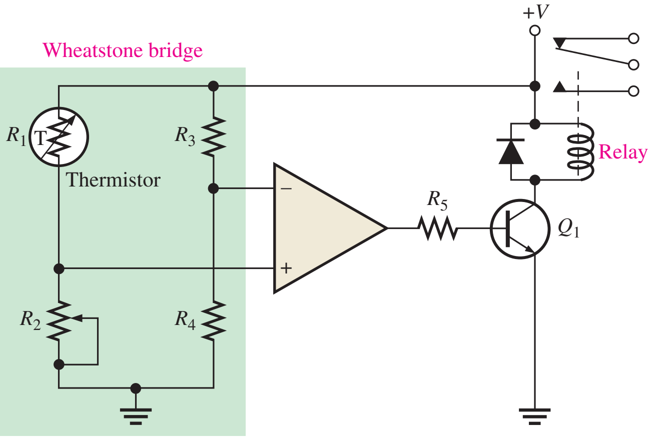
Open the Multisim file E13-03 in the Examples folder on the companion website. Compare the output waveform to the specified input at any arbitrary frequency and see if the upper and lower trigger points agree with the calculated values.

Comparator Applications

Over-Temperature Sensing Circuit Figure 13–15 shows an op-amp comparator used in a precision over-temperature sensing circuit to determine when the temperature reaches a certain critical value. The circuit consists of a Wheatstone bridge with the op-amp used to detect when the bridge is balanced. One leg of the bridge contains a thermistor (R_1), which is a temperature-sensing resistor with a negative temperature coefficient (its resistance decreases as temperature increases). The potentiometer (R_2) is set at a value equal to the resistance of the thermistor at the critical temperature. At normal temperatures (below critical), R_1 is greater than R_2, thus creating an unbalanced condition that drives the op-amp to its low saturated output level and keeps transistor Q_1 off.

▶ **FIGURE 13–15**

An over-temperature sensing circuit.



As the temperature increases, the resistance of the thermistor decreases. When the temperature reaches the critical value, R_1 becomes equal to R_2, and the bridge becomes balanced (since $R_3 = R_4$). At this point the op-amp switches to its high saturated output level, turning Q_1 on. This energizes the relay, which can be used to activate an alarm or initiate an appropriate response to the over-temperature condition.

Analog-to-Digital (A/D) Conversion **A/D conversion** is a common interfacing process often used when a linear **analog** system must provide inputs to a **digital** system. Many methods for A/D conversion are available. However, in this discussion, only one type is used to demonstrate the concept.

The *simultaneous,* or *flash,* method of A/D conversion uses parallel comparators to compare the linear input signal with various reference voltages developed by a voltage divider. When the input voltage exceeds the reference voltage for a given comparator, a high level is produced on that comparator's output. Figure 13–16 shows an analog-to-digital converter (ADC) that produces three-digit binary numbers on its output, which represent the values of the analog input voltage as it changes. This converter requires seven comparators. In general, $2^n - 1$ comparators are required for conversion to an n-digit binary number. The large number of comparators necessary for a reasonably sized binary number is one of the drawbacks of the simultaneous ADC, but IC technology has reduced the problem somewhat by combining multiple comparators and associated circuits on a single IC chip. For example, 6- or 8-bit flash converters are readily available. These ADCs are useful in applications that require the fastest possible conversion times, such as video processing.

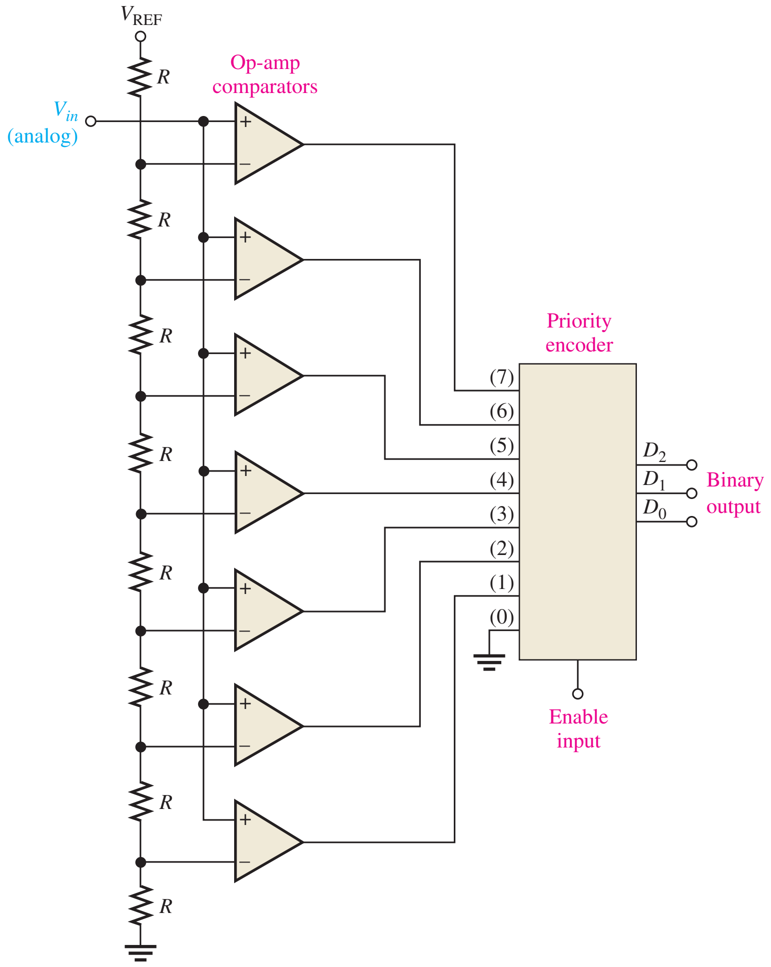


FIGURE 13–16

A simplified simultaneous (flash) analog-to-digital converter (ADC) using op-amps as comparators.

In Figure 13–16, the reference voltage for each comparator is set by the resistive voltage-divider circuit and V_{REF}. The output of each comparator is connected to an input of the priority encoder. The *priority encoder* is a digital device that produces a binary number on its output representing the highest value input.

The encoder samples its input when a pulse occurs on the enable line (sampling pulse), and a three-digit binary number proportional to the value of the analog input signal appears on the encoder's outputs.

The sampling rate determines the accuracy with which the sequence of binary numbers represents the changing input signal. The more samples taken in a given unit of time, the more accurately the analog signal is represented in digital form.

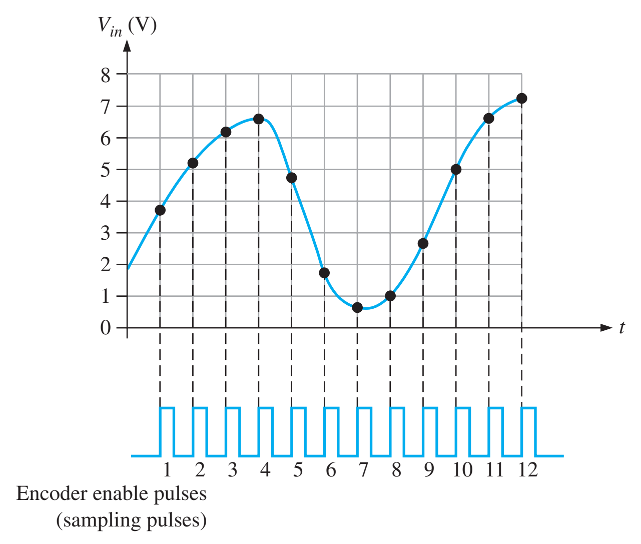
The following example illustrates the basic operation of the simultaneous ADC in Figure 13–16.

EXAMPLE 13–4

Determine the binary number sequence of the three-digit simultaneous ADC in Figure 13–16 for the input signal in Figure 13–17 and the sampling pulses (encoder enable) shown. Draw the resulting digital output waveforms.

▶ **FIGURE 13–17**

Sampling of values on analog waveform for conversion to digital.

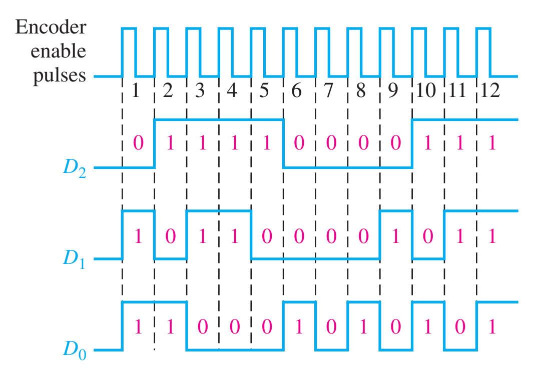


Solution The resulting binary output sequence is listed as follows and is shown in the waveform diagram of Figure 13–18 in relation to the sampling pulses.

011, 101, 110, 110, 100, 001, 000, 001, 010, 101, 110, 111

▶ **FIGURE 13–18**

Resulting digital outputs for sampled values in Figure 13–17. D_0 is the least significant digit.



Related Problem If the frequency of the enable pulses in Figure 13–17 is doubled, does the resulting binary output sequence represent the analog waveform more or less accurately?

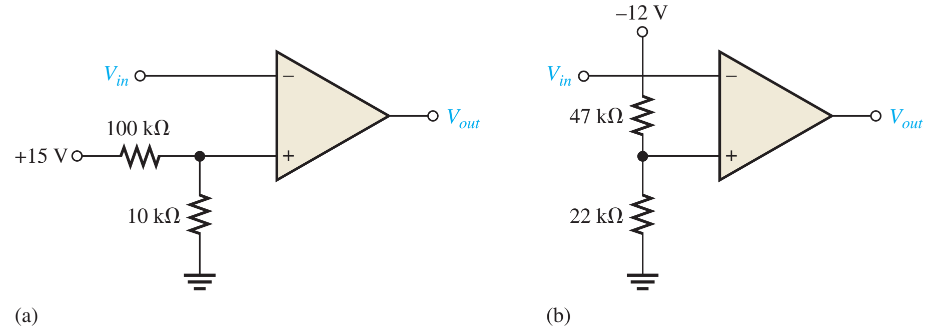
Specific Comparators

The LM111 and LM311 are examples of specific comparators that exhibit high switching speeds and other features not normally found on the general type of op-amp. These comparators can operate with supply voltages from ±15 V to a single +5 V. The open collector output provides the capability of driving loads that require voltages up to 50 V referenced to ground or to the supply voltages. An offset balancing input and a strobe input allow the output to be turned on or off regardless of the differential input.

SECTION 13–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What is the reference voltage for each comparator in Figure 13–19?
2. What is the purpose of hysteresis in a comparator?
3. Define the term *bounding* in relation to a comparator's output.



▲ FIGURE 13–19

13–2 SUMMING AMPLIFIERS

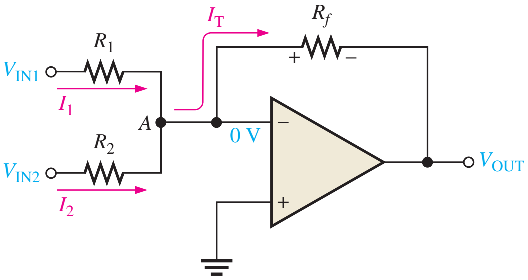
The summing amplifier is an application of the inverting op-amp configuration covered in Chapter 12. The averaging amplifier and the scaling amplifier are variations of the basic summing amplifier.

After completing this section, you should be able to

- **Describe and analyze the operation of several types of summing amplifiers**
- Discuss the operation of a unity-gain summing amplifier
  - Determine the output voltage
- Describe how to achieve gains greater than unity (1)
  - Calculate the gain of a given summing amplifier and determine the output voltage
- Discuss the operation of an averaging amplifier
  - Calculate the output voltage for given input voltages
- Describe the operation of a scaling adder
  - Discuss how different weights can be assigned to the inputs
- Discuss and analyze a digital-to-analog converter (DAC) using a scaling adder
  - Explain the binary-weighted resistor DAC ◆ Describe the *R*/2*R* ladder method

Summing Amplifier with Unity Gain

A **summing amplifier** has two or more inputs, and its output voltage is proportional to the negative of the algebraic sum of its input voltages. A two-input summing amplifier is shown in Figure 13–20, but any number of inputs can be used. The operation of the circuit and derivation of the output expression are as follows. Two voltages, V_{IN1} and V_{IN2}, are applied to the inputs and produce currents I_1 and I_2, as shown. Using the concepts of infinite



◀ FIGURE 13–20

Two-input inverting summing amplifier.

input impedance and virtual ground, you can determine that the inverting (−) input of the op-amp is approximately 0 V and has no current through it. This means that both input currents I_1 and I_2 combine at a summing point, A, and form the total current (I_T), which goes through R_f, as indicated in Figure 13–20.

$$I_T = I_1 + I_2$$

Since $V_{OUT} = -I_T R_f$, the following steps apply:

$$V_{OUT} = -(I_1 + I_2)R_f = -\left(\frac{V_{IN1}}{R_1} + \frac{V_{IN2}}{R_2}\right)R_f$$

If all three of the resistors are equal ($R_1 = R_2 = R_f = R$), then

$$V_{OUT} = -\left(\frac{V_{IN1}}{R} + \frac{V_{IN2}}{R}\right)R = -(V_{IN1} + V_{IN2})$$

The previous equation shows that the output voltage has the same magnitude as the sum of the two input voltages but with a negative sign, indicating inversion.

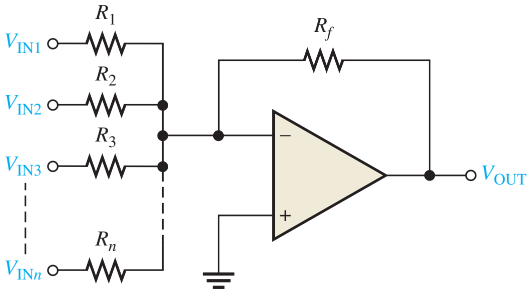
A general expression is given in Equation 13–4 for a unity-gain summing amplifier with n inputs, as shown in Figure 13–21 where all resistors are equal in value.

Equation 13–4

$$\mathbf{V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})}$$

▶ FIGURE 13–21

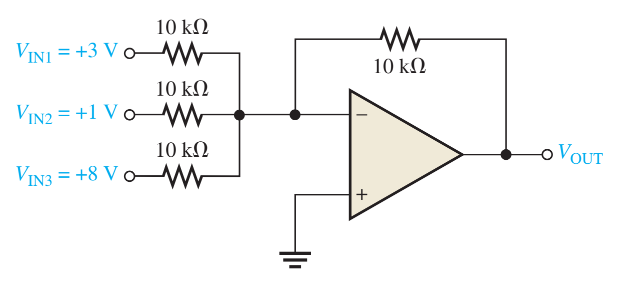
Summing amplifier with *n* inputs.



EXAMPLE 13–5

Determine the output voltage in Figure 13–22.

▶ FIGURE 13–22



Solution

$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3}) = -(3\text{ V} + 1\text{ V} + 8\text{ V}) = \mathbf{-12\text{ V}}$$

Related Problem If a fourth input of −0.5 V is added to Figure 13–22 with a 10 kΩ resistor, what is the output voltage?

Open the Multisim file E13-05 in the Examples folder on the companion website. Apply the indicated dc voltages to the inputs of the summing amplifier and verify that the output is the inverted sum of the inputs.

Summing Amplifier with Gain Greater Than Unity

When R_f is larger than the input resistors, the amplifier has a gain of R_f/R, where R is the value of each equal-value input resistor. The general expression for the output is

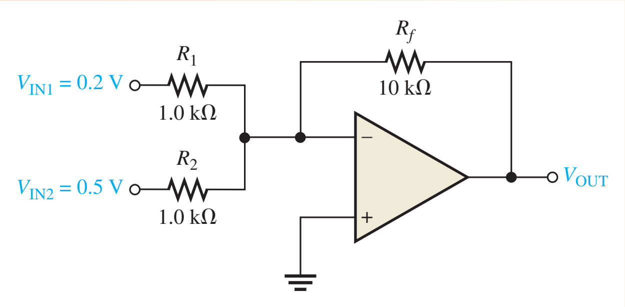
$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + \cdots + V_{INn})$$

Equation 13–5

As you can see, the output voltage has the same magnitude as the sum of all the input voltages multiplied by a constant determined by the ratio $-(R_f/R)$.

EXAMPLE 13–6 Determine the output voltage for the summing amplifier in Figure 13–23.

▶ FIGURE 13–23



Solution $R_f = 10\text{ k}\Omega$ and $R = R_1 = R_2 = 1.0\text{ k}\Omega$. Therefore,

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2}) = -\frac{10\text{ k}\Omega}{1.0\text{ k}\Omega}(0.2\text{ V} + 0.5\text{ V}) = -10(0.7\text{ V}) = \mathbf{-7\text{ V}}$$

Related Problem Determine the output voltage in Figure 13–23 if the two input resistors are 2.2 kΩ and the feedback resistor is 18 kΩ.

Open the Multisim file E13-06 in the Examples folder on the companion website. Apply the indicated dc voltages to the inputs of the summing amplifier and verify that the output is the inverted sum of the inputs times a gain of 10.

Averaging Amplifier

A summing amplifier can be made to produce the mathematical average of the input voltages. This is done by setting the ratio R_f/R equal to the reciprocal of the number of inputs (n).

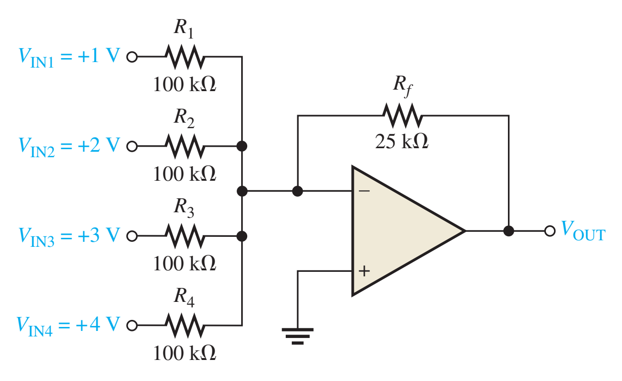
$$\frac{R_f}{R} = \frac{1}{n}$$

You obtain the average of several numbers by first adding the numbers and then dividing by the quantity of numbers you have. Examination of Equation 13–5 and a little thought will convince you that a summing amplifier can be designed to do this. The next example will illustrate.

EXAMPLE 13–7

Show that the amplifier in Figure 13–24 produces an output whose magnitude is the mathematical average of the input voltages.

▶ FIGURE 13–24



Solution Since the input resistors are equal, $R = 100\text{ k}\Omega$. The output voltage is

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + V_{IN3} + V_{IN4})$$
$$= -\frac{25\text{ k}\Omega}{100\text{ k}\Omega}(1\text{ V} + 2\text{ V} + 3\text{ V} + 4\text{ V}) = -\frac{1}{4}(10\text{ V}) = \mathbf{-2.5\text{ V}}$$

A simple calculation shows that the average of the input values is the same magnitude as V_{OUT} but of opposite sign.

$$V_{IN(avg)} = \frac{1\text{ V} + 2\text{ V} + 3\text{ V} + 4\text{ V}}{4} = \frac{10\text{ V}}{4} = 2.5\text{ V}$$

Related Problem Specify the changes required in the averaging amplifier in Figure 13–24 in order to handle five inputs.

Open the Multisim file E13-07 in the Examples folder on the companion website. Apply the indicated dc voltages to the inputs of the summing amplifier and verify that the output is the inverted average of the inputs.

Scaling Adder

A different weight can be assigned to each input of a summing amplifier by simply adjusting the values of the input resistors. As you have seen, the output voltage can be expressed as

Equation 13–6

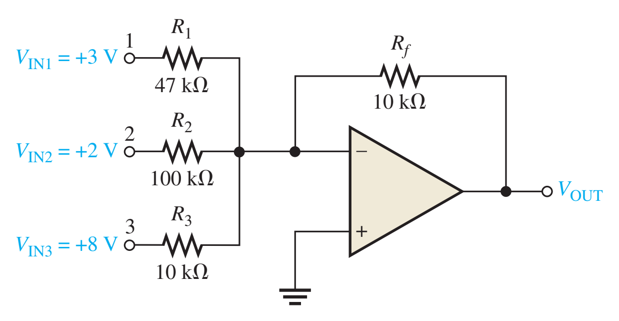
$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \cdots + \frac{R_f}{R_n}V_{INn}\right)$$

The weight of a particular input is set by the ratio of R_f to the resistance, R_x, for that input ($R_x = R_1, R_2, \cdots R_n$). For example, if an input voltage is to have a weight of 1, then $R_x = R_f$. Or, if a weight of 0.5 is required, $R_x = 2R_f$. The smaller the value of input resistance R_x, the greater the weight, and vice versa.

EXAMPLE 13–8

Determine the weight of each input voltage for the scaling adder in Figure 13–25 and find the output voltage.

▶ FIGURE 13–25



Solution Weight of input 1: $\frac{R_f}{R_1} = \frac{10\text{ k}\Omega}{47\text{ k}\Omega} = \mathbf{0.213}$

Weight of input 2: $\frac{R_f}{R_2} = \frac{10\text{ k}\Omega}{100\text{ k}\Omega} = \mathbf{0.100}$

Weight of input 3: $\frac{R_f}{R_3} = \frac{10\text{ k}\Omega}{10\text{ k}\Omega} = \mathbf{1.00}$

The output voltage is

$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \frac{R_f}{R_3}V_{IN3}\right)$$
$$= -[0.213(3\text{ V}) + 0.100(2\text{ V}) + 1.00(8\text{ V})]$$
$$= -(0.639\text{ V} + 0.2\text{ V} + 8\text{ V}) = \mathbf{-8.84\text{ V}}$$

Related Problem Determine the weight of each input voltage in Figure 13–25 if $R_1 = 22$ kΩ, $R_2 = 82$ kΩ, $R_3 = 56$ kΩ, and $R_f = 10$ kΩ. Also find V_{OUT}.

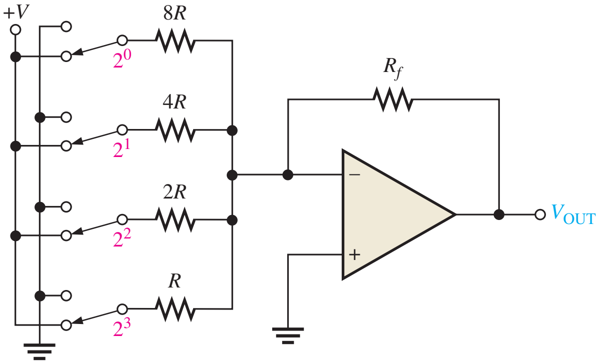
Open the Multisim file E13-08 in the Examples folder on the companion website. Apply the indicated dc voltages to the inputs of the summing amplifier and verify that the output agrees with the calculated value.

Applications

D/A conversion is an important interface process for converting digital signals to analog (linear) signals. An example is a voice signal that is digitized for storage, processing, or transmission and must be changed back into an approximation of the original audio signal in order to drive a speaker.

One method of D/A conversion uses a scaling adder with input resistor values that represent the binary weights of the digital input code. Although this is not the most widely used method, it serves to illustrate how a scaling adder can be applied. A more common method for D/A conversion is known as the *R*/2*R* ladder method. The *R*/2*R* ladder is introduced here for comparison although it does not use a scaling adder.

Figure 13–26 shows a four-digit digital-to-analog converter (DAC) of this type (called a *binary-weighted resistor DAC*). The switch symbols represent transistor switches for applying each of the four binary digits to the inputs. The inverting (−) input is at virtual ground, and so the output voltage is proportional to the current through the feedback resistor R_f (sum of input currents). The lowest-value resistor *R* corresponds to the highest weighted binary input (2^3). All of the other resistors are multiples of *R* and correspond to the binary weights 2^2, 2^1, and 2^0.

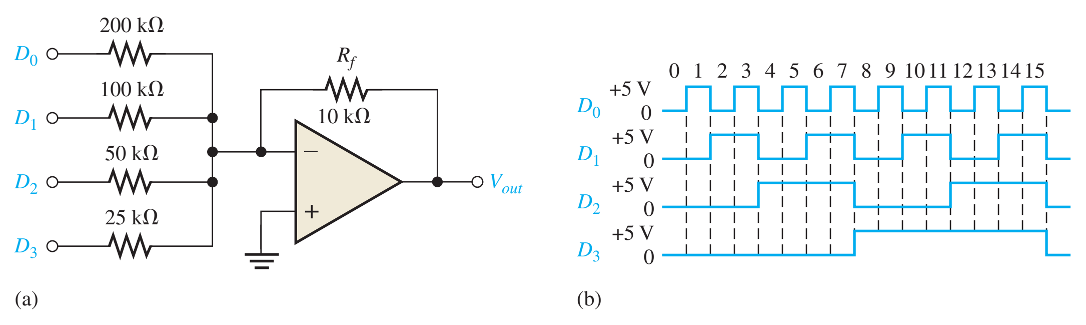


▶ FIGURE 13–26

A scaling adder as a four-digit digital-to-analog converter (DAC).

EXAMPLE 13–9

Determine the output voltage of the DAC in Figure 13–27(a). The sequence of four-digit binary codes represented by the waveforms in Figure 13–27(b) are applied to the inputs. A high level is a binary 1, and a low level is a binary 0. The least significant binary digit is D_0.



▲ FIGURE 13–27

Solution First, determine the current for each of the weighted inputs. Since the inverting input of the op-amp is at 0 V (virtual ground) and a binary 1 corresponds to a high level (+5 V), the current through any of the input resistors equals 5 V divided by the resistance value.

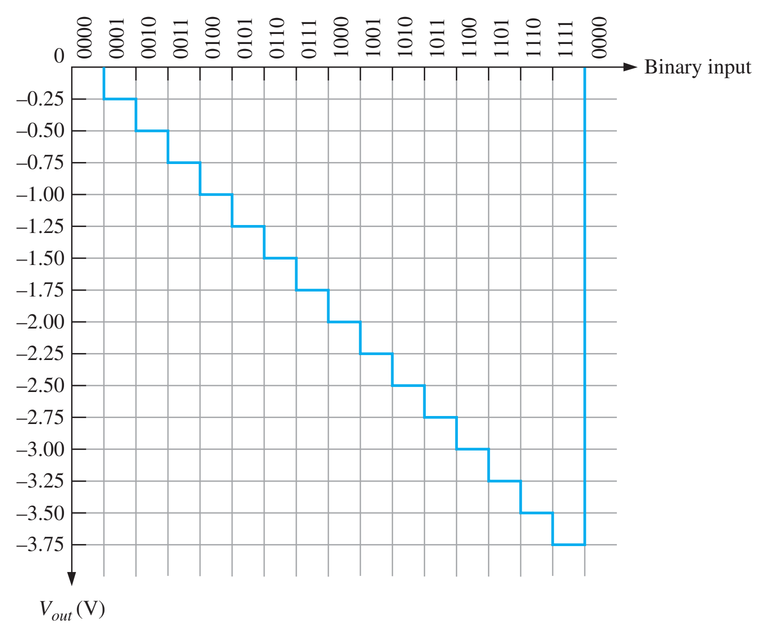
$$I_0 = \frac{5\text{ V}}{200\text{ k}\Omega} = 0.025\text{ mA}$$
$$I_1 = \frac{5\text{ V}}{100\text{ k}\Omega} = 0.05\text{ mA}$$
$$I_2 = \frac{5\text{ V}}{50\text{ k}\Omega} = 0.1\text{ mA}$$
$$I_3 = \frac{5\text{ V}}{25\text{ k}\Omega} = 0.2\text{ mA}$$

There is almost no current at the inverting op-amp input because of its extremely high impedance. Therefore, assume that all of the input current is through R_f. Since one end of R_f is at 0 V (virtual ground), the drop across R_f equals the output voltage, which is negative with respect to virtual ground.

$$V_{OUT(D0)} = -R_f I_0 = -(10\text{ k}\Omega)(0.025\text{ mA}) = \mathbf{-0.25\text{ V}}$$
$$V_{OUT(D1)} = -R_f I_1 = -(10\text{ k}\Omega)(0.05\text{ mA}) = \mathbf{-0.5\text{ V}}$$
$$V_{OUT(D2)} = -R_f I_2 = -(10\text{ k}\Omega)(0.1\text{ mA}) = \mathbf{-1\text{ V}}$$
$$V_{OUT(D3)} = -R_f I_3 = -(10\text{ k}\Omega)(0.2\text{ mA}) = \mathbf{-2\text{ V}}$$

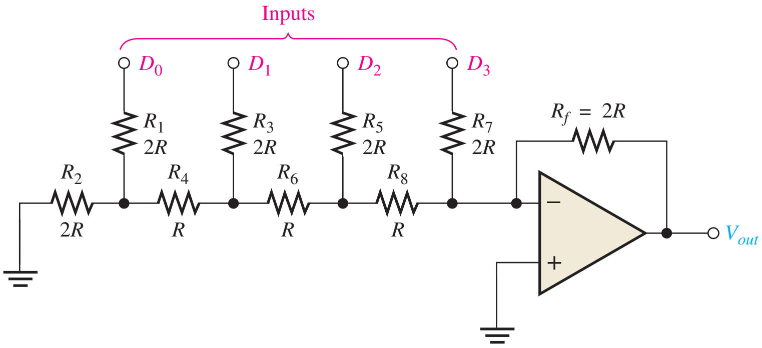
From Figure 13–27(b), the first binary input code is 0000, which produces an output voltage of 0 V. The next input code is 0001 (it stands for decimal 1). For this, the output voltage is −0.25 V. The next code is 0010, which produces an output voltage of −0.5 V. The next code is 0011, which produces an output voltage of −0.25 V + (−0.5 V) = −0.75 V. Each successive binary code increases the output voltage by −0.25 V. So, for this particular straight binary sequence on the inputs, the output is a stairstep waveform going from 0 V to −3.75 V in −0.25 V steps, as shown in Figure 13–28. If the steps are very small, the output approximates a straight line (linear).

▶ FIGURE 13–28



Related Problem If the 200 kΩ resistor in Figure 13–27(a) is changed to 400 kΩ, would the other resistor values have to be changed? If so, specify the values.

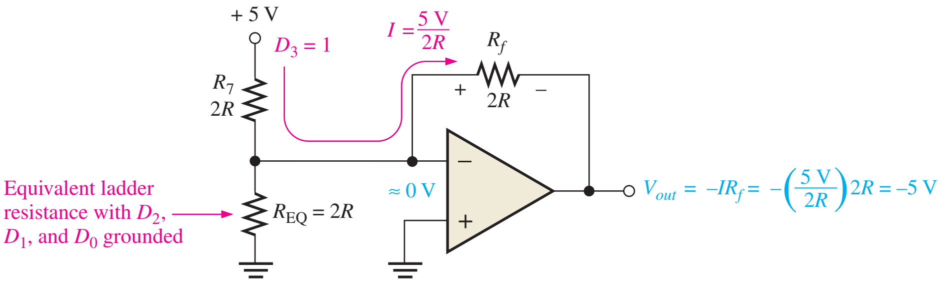
As mentioned before, the *R*/2*R* ladder is more commonly used for D/A conversion than the scaling adder and is shown in Figure 13–29 for four bits. It overcomes one of the disadvantages of the binary-weighted-input DAC because it requires only two resistor values.



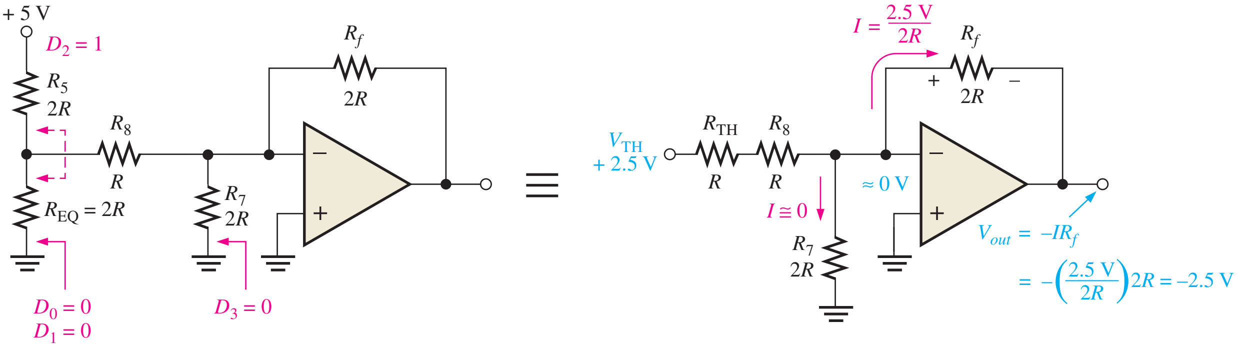
◀ FIGURE 13–29

An *R*/2*R* ladder DAC.

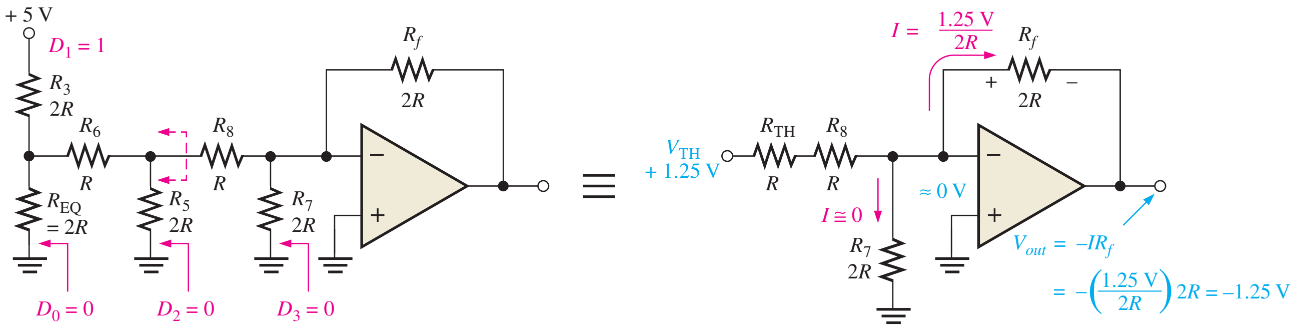
Assume that the D_3 input is HIGH (+5 V) and the others are LOW (ground, 0 V). This condition represents the binary number 1000. A circuit analysis will show that this reduces to the equivalent form shown in Figure 13–30(a). Essentially no current goes through the


+ 5 V
D3 = 1
I = 5 V / 2R
Rf
R7
2R
+
2R
–
Equivalent ladder resistance with D2, D1, and D0 grounded
REQ = 2R
≈ 0 V
–
+
Vout = –IRf = –(5 V / 2R)2R = –5 V

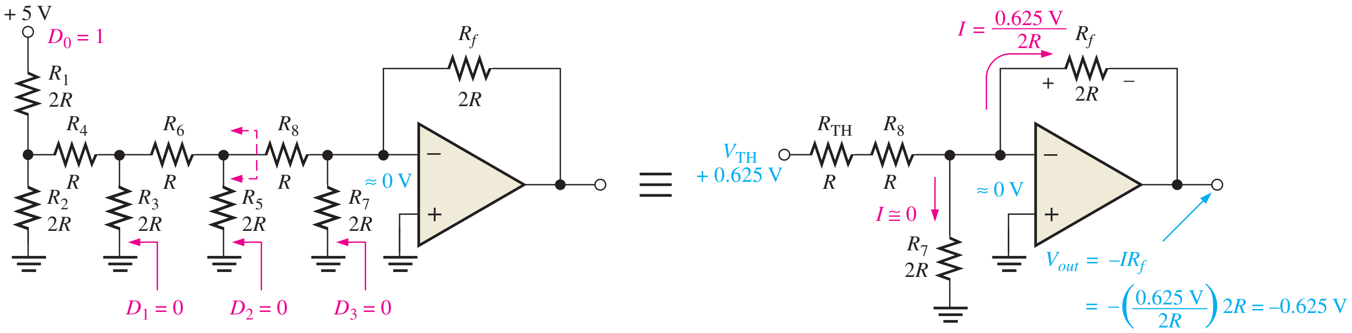
(a) Equivalent circuit for $D_3 = 1$, $D_2 = 0$, $D_1 = 0$, $D_0 = 0$


+ 5 V
D2 = 1
R5
2R
R8
R
REQ = 2R
R7
2R
Rf
2R
D0 = 0
D1 = 0
D3 = 0
≡
VTH
+ 2.5 V
RTH
R
R8
R
I ≅ 0
R7
2R
≈ 0 V
I = 2.5 V / 2R
Rf
+
2R
–
Vout = –IRf
= –(2.5 V / 2R)2R = –2.5 V

(b) Equivalent circuit for $D_3 = 0$, $D_2 = 1$, $D_1 = 0$, $D_0 = 0$


+ 5 V
D1 = 1
R3
2R
R6
R
REQ
= 2R
R5
2R
R8
R
R7
2R
Rf
2R
D0 = 0
D2 = 0
D3 = 0
≡
VTH
+ 1.25 V
RTH
R
R8
R
I ≅ 0
R7
2R
≈ 0 V
I = 1.25 V / 2R
Rf
+
2R
–
Vout = –IRf
= –(1.25 V / 2R)2R = –1.25 V

(c) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 1$, $D_0 = 0$


+ 5 V
D0 = 1
R1
2R
R4
R
R2
2R
R6
R
R3
2R
R8
R
R5
2R
R7
2R
≈ 0 V
Rf
2R
D1 = 0
D2 = 0
D3 = 0
≡
VTH
+ 0.625 V
RTH
R
R8
R
I ≅ 0
R7
2R
≈ 0 V
I = 0.625 V / 2R
Rf
+
2R
–
Vout = –IRf
= –(0.625 V / 2R)2R = –0.625 V

(d) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 0$, $D_0 = 1$

▲ **FIGURE 13–30**

Analysis of the $R/2R$ ladder DAC.

$2R$ equivalent resistance because the inverting input is at virtual ground. Thus, all of the current ($I = 5\text{ V}/2R$) through R_7 is also through R_f, and the output voltage is -5 V. The operational amplifier keeps the inverting ($-$) input near zero volts (≈ 0 V) because of negative feedback. Therefore, all current is through R_f rather than into the inverting input.

Figure 13–30(b) shows the equivalent circuit when the D_2 input is at $+5$ V and the others are at ground. This condition represents 0100. If we thevenize looking from R_8, we get 2.5 V in series with R, as shown. This results in a current through R_f of $I = 2.5\text{ V}/2R$, which gives an output voltage of -2.5 V. Keep in mind that there is no current into the op-amp inverting input and that there is no current through R_7 because it has 0 V across it, due to the virtual ground.

Figure 13–30(c) shows the equivalent circuit when the D_1 input is at $+5$ V and the others are at ground. This condition represents 0010. Again thevenizing looking from R_8, you get 1.25 V in series with R as shown. This results in a current through R_f of $I = 1.25\text{ V}/2R$, which gives an output voltage of -1.25 V.

In part (d) of Figure 13–30, the equivalent circuit representing the case where D_0 is at $+5$ V and the other inputs are at ground is shown. This condition represents 0001. Thevenizing from R_8 gives an equivalent of 0.625 V in series with R as shown. The resulting current through R_f is $I = 0.625\text{ V}/2R$, which gives an output voltage of -0.625 V.

Notice that each successively lower-weighted input produces an output voltage that is halved, so that the output voltage is proportional to the binary weight of the input bits.

SECTION 13–2 CHECKUP

1. Define *summing point.*
2. What is the value of R_f/R for a five-input averaging amplifier?
3. A certain scaling adder has two inputs, one having twice the weight of the other. If the resistor value for the lower-weighted input is 10 kΩ, what is the value of the other input resistor?

13–3 INTEGRATORS AND DIFFERENTIATORS

An op-amp **integrator** simulates mathematical integration, which is basically a summing process that determines the total area under the curve of a function. An op-amp **differentiator** simulates mathematical differentiation, which is a process of determining the instantaneous rate of change of a function. It is not necessary for you to understand mathematical integration or differentiation, at this point, in order to learn how an integrator and differentiator work. Ideal integrators and differentiators are used to show basic principles. Practical integrators often have an additional resistor in parallel with the feedback capacitor to prevent saturation. Practical differentiators may include a resistor in series with the comparator to reduce high frequency noise.

After completing this section, you should be able to

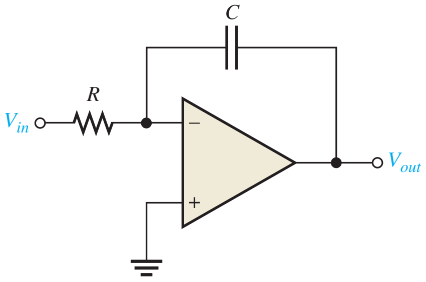
- ❑ **Describe and analyze the operation of integrators and differentiators**
- ❑ Describe and identify the op-amp integrator
  - ◆ Discuss the ideal integrator ◆ Explain how a capacitor charges
  - ◆ Discuss the capacitor voltage, the output voltage, and the rate of change of the output voltage ◆ Describe the practical integrator
- ❑ Describe and identify the op-amp differentiator
  - ◆ Discuss the ideal differentiator ◆ Discuss the practical differentiator

The Op-Amp Integrator

The Ideal Integrator An ideal integrator is shown in Figure 13–31. Notice that the feedback element is a capacitor that forms an RC circuit with the input resistor.

▶ FIGURE 13–31

An op-amp integrator.



How a Capacitor Charges To understand how an integrator works, it is important to review how a capacitor charges. Recall that the charge Q on a capacitor is proportional to the charging current (I_C) and the time (t).

$$Q = I_C t$$

Also, in terms of the voltage, the charge on a capacitor is

$$Q = CV_C$$

From these two relationships, the capacitor voltage can be expressed as

$$V_C = \left(\frac{I_C}{C}\right)t$$

This expression has the form of an equation for a straight line that begins at zero with a constant slope of I_C/C. Remember from algebra that the general formula for a straight line is $y = mx + b$. In this case, $y = V_C$, $m = I_C/C$, $x = t$, and $b = 0$.

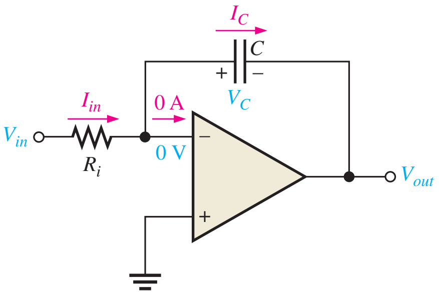
Recall that the capacitor voltage in a simple RC circuit is not linear but is exponential. This is because the charging current continuously decreases as the capacitor charges and causes the rate of change of the voltage to continuously decrease. The key thing about using an op-amp with an RC circuit to form an integrator is that the capacitor's charging current is made constant, thus producing a straight-line (linear) voltage rather than an exponential voltage. Now let's see why this is true.

In Figure 13–32, the inverting input of the op-amp is at virtual ground (0 V), so the voltage across R_i equals V_{in}. Therefore, the input current is

$$I_{in} = \frac{V_{in}}{R_i}$$

▶ FIGURE 13–32

Currents in an integrator.



If V_{in} is a constant voltage, then I_{in} is also a constant because the inverting input always remains at 0 V, keeping a constant voltage across R_i. Because of the very high input impedance of the op-amp, there is negligible current at the inverting input. This makes all of the input current go through the capacitor, as indicated in Figure 13–32, so

$$I_C = I_{in}$$

The Capacitor Voltage Since I_{in} is constant, so is I_C. The constant I_C charges the capacitor linearly and produces a linear voltage across C. The positive side of the capacitor is held at 0 V by the virtual ground of the op-amp. The voltage on the negative side of the capacitor, which is the op-amp output voltage, decreases linearly from zero as the capacitor charges, as shown in Figure 13–33. This voltage, V_C, is called a *negative ramp* and is the consequence of a constant positive input.

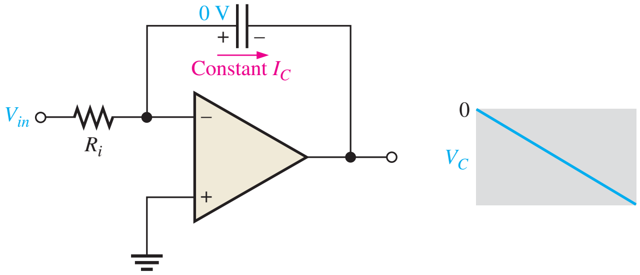


FIGURE 13–33

A linear ramp voltage is produced across the capacitor by the constant charging current.

The Output Voltage V_{out} is the same as the voltage on the negative side of the capacitor. When a constant positive input voltage in the form of a step or pulse (a pulse has a constant amplitude when high) is applied, the output ramp decreases negatively until the op-amp saturates at its maximum negative level. This is indicated in Figure 13–34.

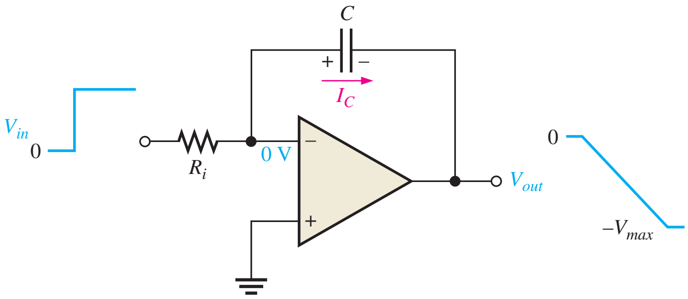


FIGURE 13–34

A constant input voltage produces a ramp on the output of the integrator.

Rate of Change of the Output Voltage The rate at which the capacitor charges, and therefore the slope of the output ramp, is set by the ratio I_C/C, as you have seen. Since $I_C = V_{in}/R_i$, the rate of change or slope of the integrator's output voltage is $\Delta V_{out}/\Delta t$.

$$\boldsymbol{\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}}$$

Equation 13–7

Integrators are especially useful in triangular-wave oscillators as you will see in Chapter 16.

EXAMPLE 13–10

(a) Determine the rate of change of the output voltage in response to the input square wave, as shown for the ideal integrator in Figure 13–35(a). The output voltage is initially zero. The pulse width is 100 μs.

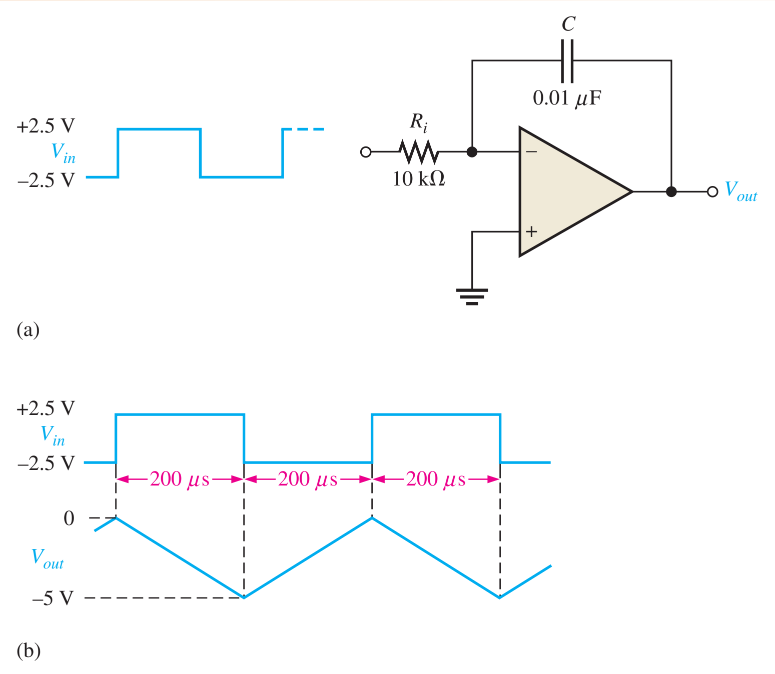
(b) Describe the output and draw the waveform.

Solution

(a) The rate of change of the output voltage during the time that the input is at +2.5 V (capacitor charging) is

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C} = -\frac{2.5\text{ V}}{(10\text{ k}\Omega)(0.01\ \mu\text{F})} = -25\text{ kV/s} = \mathbf{-25\ mV/\boldsymbol{\mu}s}$$

FIGURE 13–35



The rate of change of the output during the time that the input is negative (capacitor discharging) is the same as during charging except it is positive.

$$\frac{\Delta V_{out}}{\Delta t} = +\frac{V_{in}}{R_i C} = \mathbf{+25\ mV/\mu s}$$

(b) When the input is at +2.5 V, the output is a negative-going ramp. When the input is at −2.5 V, the output is a positive-going ramp.

$$\Delta V_{out} = (25\text{ mV}/\mu\text{s})(200\ \mu\text{s}) = 5\text{ V}$$

During the time the input is at +2.5 V, the output will go from 0 to −5 V. During the time the input is at −2.5 V, the output will go from −5 V to 0 V. Therefore, the output is a triangular wave with peaks at 0 V and − 5 V, as shown in Figure 13–35(b).

Related Problem Modify the integrator in Figure 13–35 to make the output change from 0 to −5 V in 100 μs with the same input.

Open the Multisim file E13-10 in the Examples folder on the companion website. Using the function generator, apply the indicated pulse waveform to the input and verify that the output voltage is a 5 V peak-to-peak triangular waveform.

The Practical Integrator The ideal integrator uses a capacitor in the feedback path, which is open to dc. This implies that the gain at dc is the open-loop gain of the op-amp. In a practical integrator, any dc error voltage due to offset error will cause the output to produce a ramp that moves toward either positive or negative saturation (depending on the offset), even when no signal is present.

Practical integrators must have some means of overcoming the effects of offset and bias current. Various solutions are available, such as chopper stabilized amplifiers; however, the simplest solution is to use a resistor in parallel with the capacitor in the feedback path, as shown in Figure 13–36. The feedback resistor, R_f, should be large compared to the input resistor R_{in}, in order to have a negligible effect on the output waveform. In addition, a compensating resistor, R_c, may be added to the noninverting input to balance the effects of bias current.

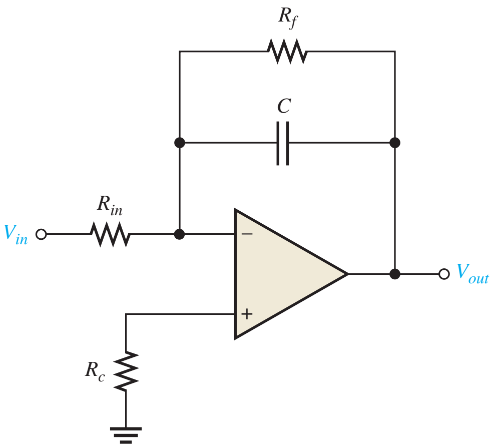


FIGURE 13–36

The Op-Amp Differentiator

The Ideal Differentiator An ideal differentiator is shown in Figure 13–37. Notice how the placement of the capacitor and resistor differ from the integrator. The capacitor is now the input element, and the resistor is the feedback element. A differentiator produces an output that is proportional to the rate of change of the input voltage.

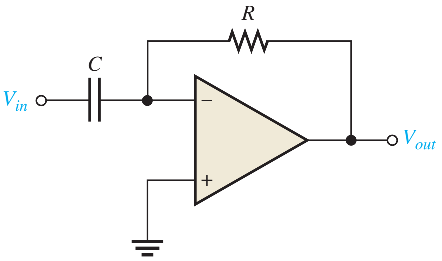


FIGURE 13–37

An op-amp differentiator.

To see how the differentiator works, apply a positive-going ramp voltage to the input as indicated in Figure 13–38. In this case, $I_C = I_{in}$ and the voltage across the capacitor is equal to V_{in} at all times ($V_C = V_{in}$) because of virtual ground on the inverting input.

From the basic formula, $V_C = (I_C/C)t$, the capacitor current is

$$I_C = \left(\frac{V_C}{t}\right)C$$

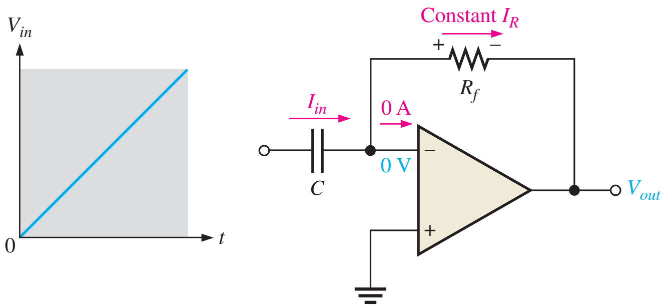


FIGURE 13–38

A differentiator with a ramp input.

Since the current at the inverting input is negligible, $I_R = I_C$. Both currents are constant because the slope of the capacitor voltage (V_C/t) is constant. The output voltage is also constant and equal to the voltage across R_f because one side of the feedback resistor is always 0 V (virtual ground).

$$V_{out} = I_R R_f = I_C R_f$$

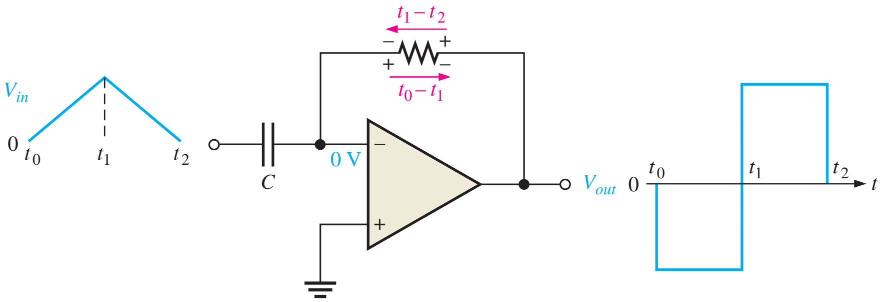
Equation 13–8

$$\mathbf{V_{out} = -\left(\frac{V_C}{t}\right)R_f C}$$

The output is negative when the input is a positive-going ramp and positive when the input is a negative-going ramp, as illustrated in Figure 13–39. During the positive slope of the input, the capacitor is charging from the input source and the constant current through the feedback resistor is in the direction shown. During the negative slope of the input, the current is in the opposite direction because the capacitor is discharging.

▶ FIGURE 13–39

Output of a differentiator with a series of positive and negative ramps (triangle wave) on the input.

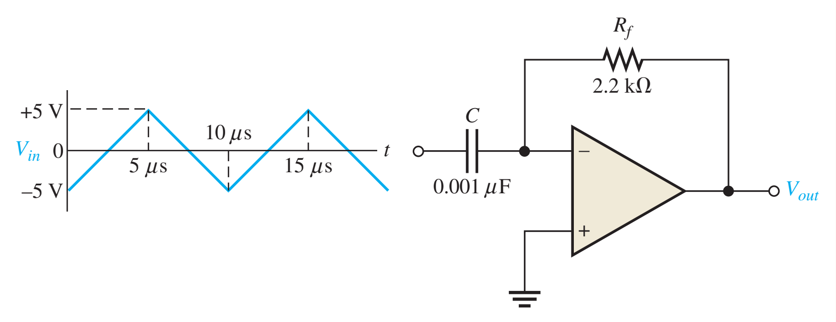


Notice in Equation 13–8 that the term V_C/t is the slope of the input. If the slope increases, V_{out} increases. If the slope decreases, V_{out} decreases. The output voltage is proportional to the slope (rate of change) of the input. The constant of proportionality is the time constant, $R_f C$.

EXAMPLE 13–11

Determine the output voltage of the ideal op-amp differentiator in Figure 13–40 for the triangular-wave input shown.

▶ FIGURE 13–40



Solution Starting at $t = 0$, the input voltage is a positive-going ramp ranging from -5 V to $+5$ V (a $+10$ V change) in 5 μs. Then it changes to a negative-going ramp ranging from $+5$ V to -5 V (a -10 V change) in 5 μs.

The time constant is

$$R_f C = (2.2\ \text{k}\Omega)(0.001\ \mu\text{F}) = 2.2\ \mu\text{s}$$

Determine the slope or rate of change (V_C/t) of the positive-going ramp and calculate the output voltage as follows:

$$\frac{V_C}{t} = \frac{10\text{ V}}{5\ \mu\text{s}} = 2\text{ V}/\mu\text{s}$$

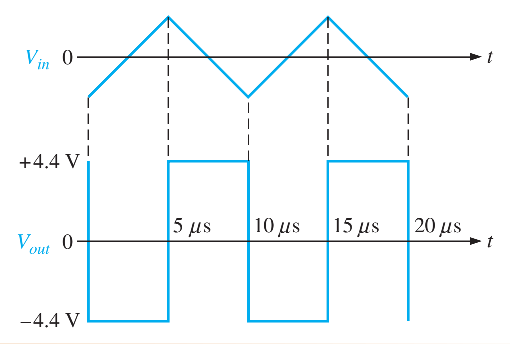
$$V_{out} = -\left(\frac{V_C}{t}\right)R_f C = -(2\text{ V}/\mu\text{s})2.2\ \mu\text{s} = \mathbf{-4.4\ V}$$

Likewise, the slope of the negative-going ramp is -2 V/μs, and the output voltage is

$$V_{out} = -(-2\text{ V}/\mu\text{s})2.2\ \mu\text{s} = \mathbf{+4.4\ V}$$

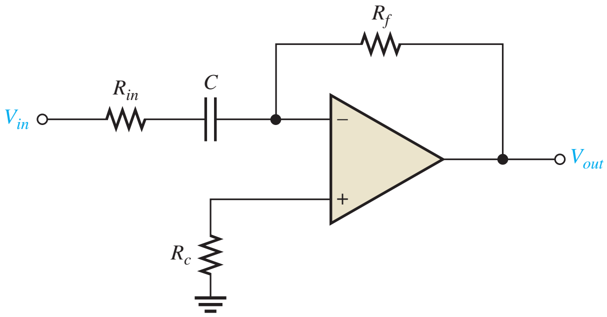
Figure 13–41 shows a graph of the output voltage waveform relative to the input.

▶ FIGURE 13–41



Related Problem What would the output voltage be if the feedback resistor in Figure 13–40 is changed to 3.3 kΩ?

The Practical Differentiator The ideal differentiator uses a capacitor in series with the inverting input. Because a capacitor has very low impedance at high frequencies, the combination of R_f and C form a very high gain amplifier at high frequencies. This means that a differentiator circuit tends to be noisy because electrical noise mainly consists of high frequencies. The solution to this problem is simply to add a resistor, R_{in}, in series with the capacitor to act as a low-pass filter and reduce the gain at high frequencies. The resistor should be small compared to the feedback resistor in order to have a negligible effect on the desired signal. Figure 13–42 shows a practical differentiator. A bias compensating resistor may also be used on the noninverting input.



◀ FIGURE 13–42

SECTION 13–3 CHECKUP

1. What is the feedback element in an ideal op-amp integrator?
2. For a constant input voltage to an integrator, why is the voltage across the capacitor linear?
3. What is the feedback element in an op-amp differentiator?
4. How is the output of a differentiator related to the input?

13–4 TROUBLESHOOTING

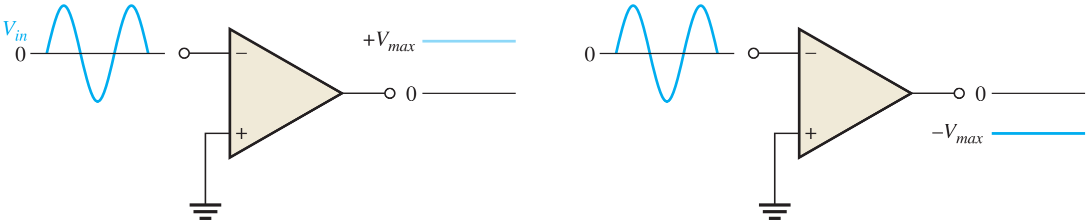
Although integrated circuit op-amps are extremely reliable and trouble-free, failures do occur from time to time. One type of internal failure mode is a condition where the op-amp output is in a saturated state, resulting in a constant high or constant low level, regardless of the input. Also, external component failures will produce various types of failure modes in op-amp circuits. Some examples are presented in this section.

After completing this section, you should be able to

- ❑ **Troubleshoot op-amp circuits**
- ❑ Describe and explain symptoms of several component failures in a bounded comparator
- ❑ Describe symptons of component failures in a summing amplifier

Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting coverage or, optionally, the entire chapter 18 may be covered later or not at all.

Figure 13–43 illustrates an internal failure of a comparator circuit that results in a “stuck” output.



(a) Output failed in the HIGH state

(b) Output failed in the LOW state

▲ FIGURE 13–43

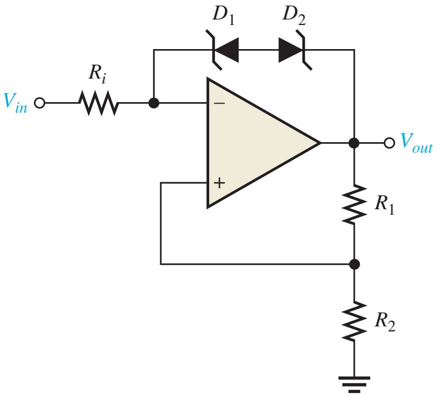
Internal comparator failures typically result in the output being “stuck” in the HIGH or LOW state.

Symptoms of External Component Failures in Comparator Circuits

A comparator with zener-bounding and hysteresis is shown in Figure 13–44. In addition to a failure of the op-amp itself, a zener diode or one of the resistors could be faulty. For example,

► FIGURE 13–44

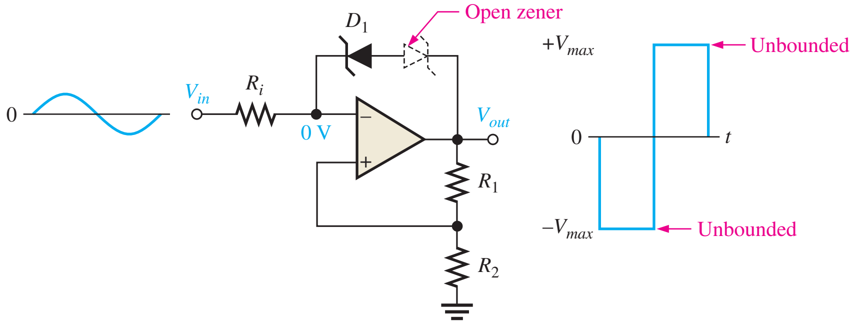
A bounded comparator with hysteresis.



suppose one of the zener diodes opens. This effectively eliminates both zeners, and the circuit operates as an unbounded comparator, as indicated in Figure 13–45(a). With a shorted diode, the output is limited to the zener voltage (bounded) only in one direction, depending on which diode remains operational, as illustrated in Figure 13–45(b). In the other direction, the output is held at the forward diode voltage.

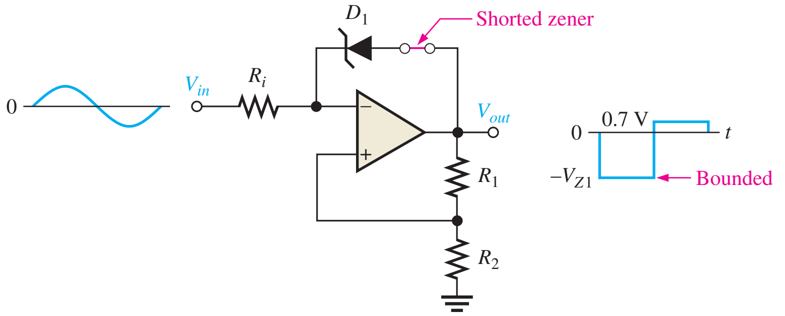
FIGURE 13–45

Examples of comparator circuit failures and their effects.



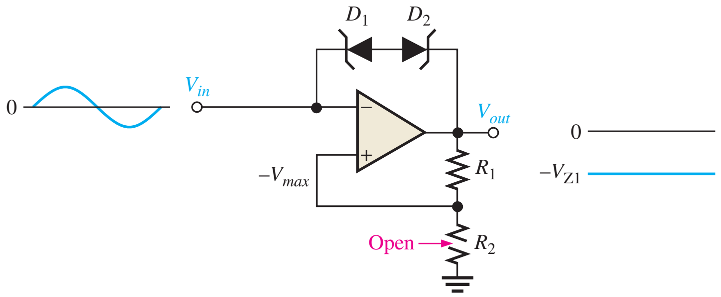
0
V_{in}
R_i
0 V
D_1
Open zener
−
+
V_{out}
R_1
R_2
$+V_{max}$
0
t
$-V_{max}$
Unbounded
Unbounded

(a) The effect of an open zener



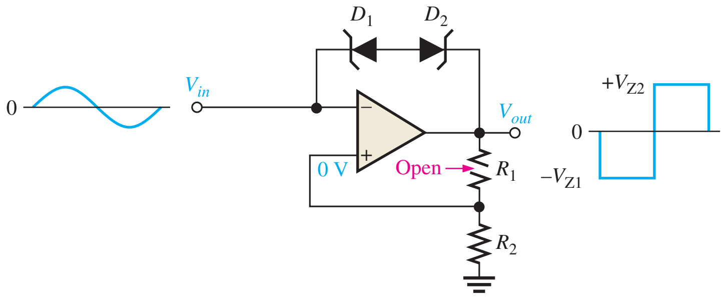
0
V_{in}
R_i
D_1
Shorted zener
−
+
V_{out}
R_1
R_2
0.7 V
0
t
$-V_{Z1}$
Bounded

(b) The effect of a shorted zener



0
V_{in}
D_1
D_2
−
+
V_{out}
$-V_{max}$
R_1
Open
R_2
0
$-V_{Z1}$

(c) Open R_2 causes output to "stick" in one state



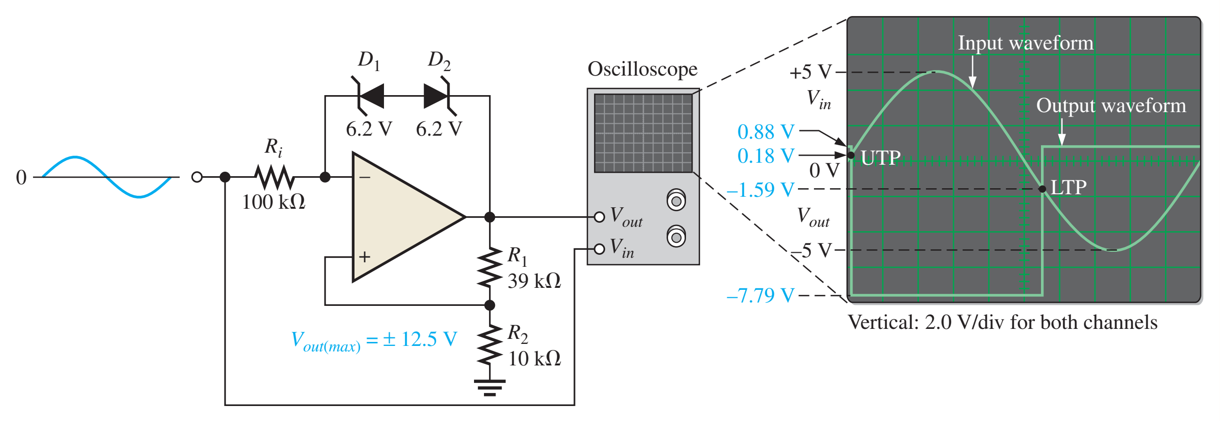
0
V_{in}
D_1
D_2
−
+
0 V
Open
V_{out}
R_1
R_2
$+V_{Z2}$
0
$-V_{Z1}$

(d) Open R_1 forces the circuit to operate as a zero-level detector

Recall that R_1 and R_2 set the UTP and LTP for the hysteresis comparator. Now, suppose that R_2 opens. Essentially all of the output voltage is fed back to the noninverting (+) input, and, since the input voltage will never exceed the output, the device will remain in one of its bounded states. This symptom can also indicate a faulty op-amp, as mentioned before. Now, assume that R_1 opens. This leaves the noninverting input near ground potential and causes the circuit to operate as a zero-level detector. These conditions are shown in parts (c) and (d) of Figure 13–45.

EXAMPLE 13–12

One channel of a dual-trace oscilloscope is connected to the comparator output and the other channel is connected to the input, as shown in Figure 13–46. From the observed waveforms, determine if the circuit is operating properly, and if not, what the most likely failure is.



▲ FIGURE 13–46

Solution The output should be limited to ±8.67 V. However, the positive maximum is +0.88 V and the negative maximum is −7.79 V. This indicates that D_2 is shorted. Refer to Example 13–3 for analysis of the bounded comparator.

Related Problem What would the output voltage look like if D_1 shorted rather than D_2?

Symptoms of Component Failures in Summing Amplifiers

If one of the input resistors in a unity-gain summing amplifier opens, the output will be less than the normal value by the amount of the voltage applied to the open input. Stated another way, the output will be the sum of the remaining input voltages.

If the summing amplifier has a nonunity gain, an open input resistor causes the output to be less than normal by an amount equal to the gain times the voltage at the open input.

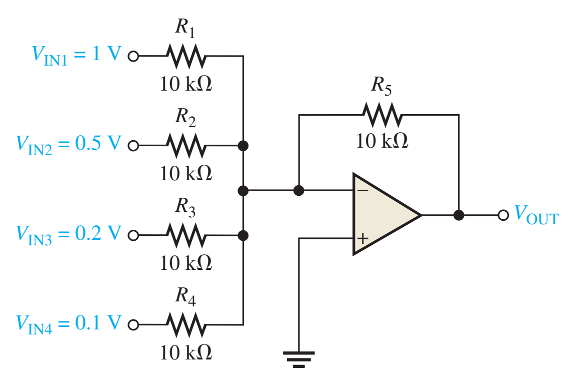
EXAMPLE 13–13

(a) What is the normal output voltage in Figure 13–47?

(b) What is the output voltage if R_2 opens?

(c) What happens if R_5 opens?

FIGURE 13–47



R_1
V_{IN1} = 1 V
10 kΩ
R_2
V_{IN2} = 0.5 V
10 kΩ
R_3
V_{IN3} = 0.2 V
10 kΩ
R_4
V_{IN4} = 0.1 V
10 kΩ
R_5
10 kΩ
−
+
V_{OUT}

Solution

(a) $V_{OUT} = -(V_{IN1} + V_{IN2} + \cdots + V_{INn})$

$$= -(1\text{ V} + 0.5\text{ V} + 0.2\text{ V} + 0.1\text{ V}) = \mathbf{-1.8\ V}$$

(b) $V_{OUT} = -(1\text{ V} + 0.2\text{ V} + 0.1\text{ V}) = \mathbf{-1.3\ V}$

(c) If the feedback resistor opens, the circuit becomes a comparator and the output goes to $-V_{max}$.

Related Problem

In Figure 13–47, $R_5 = 47\text{ k}\Omega$. What is the output voltage if R_1 opens?

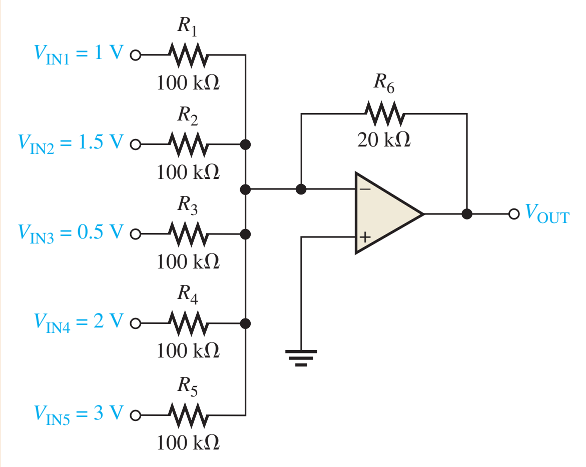
As another example, let's look at an averaging amplifier. An open input resistor will result in an output voltage that is the average of all the inputs with the open input averaged in as a zero.

EXAMPLE 13–14

(a) What is the normal output voltage for the averaging amplifier in Figure 13–48?

(b) If R_4 opens, what is the output voltage? What does the output voltage represent?

FIGURE 13–48



R_1
V_{IN1} = 1 V
100 kΩ
R_2
V_{IN2} = 1.5 V
100 kΩ
R_3
V_{IN3} = 0.5 V
100 kΩ
R_4
V_{IN4} = 2 V
100 kΩ
R_5
V_{IN5} = 3 V
100 kΩ
R_6
20 kΩ
−
+
V_{OUT}

Solution Since the input resistors are equal, $R = 100\text{ k}\Omega$. $R_f = R_6$.

$$\textbf{(a)}\quad V_{\text{OUT}} = -\frac{R_f}{R}(V_{\text{IN1}} + V_{\text{IN2}} + \cdots + V_{\text{IN}n})$$

$$= -\frac{20\text{ k}\Omega}{100\text{ k}\Omega}(1\text{ V} + 1.5\text{ V} + 0.5\text{ V} + 2\text{ V} + 3\text{ V}) = -\frac{1}{5}(8\text{ V}) = \mathbf{-1.6\text{ V}}$$

$$\textbf{(b)}\quad V_{\text{OUT}} = -\frac{20\text{ k}\Omega}{100\text{ k}\Omega}(1\text{ V} + 1.5\text{ V} + 0.5\text{ V} + 3\text{ V}) = -\frac{1}{5}(6\text{ V}) = \mathbf{-1.2\text{ V}}$$

1.2 V is the average of five voltages with the 2 V input replaced by 0 V. Notice that the output is not the average of the four remaining input voltages.

Related Problem If R_4 is open, as was the case in this example, what would you have to do to make the output equal to the average of the remaining four input voltages?

Multisim Troubleshooting Exercises

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

1. Multisim file TSE13-01
2. Multisim file TSE13-02
3. Multisim file TSE13-03
4. Multisim file TSE13-04
5. Multisim file TSE13-05
6. Multisim file TSE13-06
7. Multisim file TSE13-07
8. Multisim file TSE13-08
9. Multisim file TSE13-09
10. Multisim file TSE13-10

SECTION 13–4 CHECKUP

1. Describe one type of internal op-amp failure.
2. If a certain malfunction is attributable to more than one possible component failure, what would you do to isolate the problem?

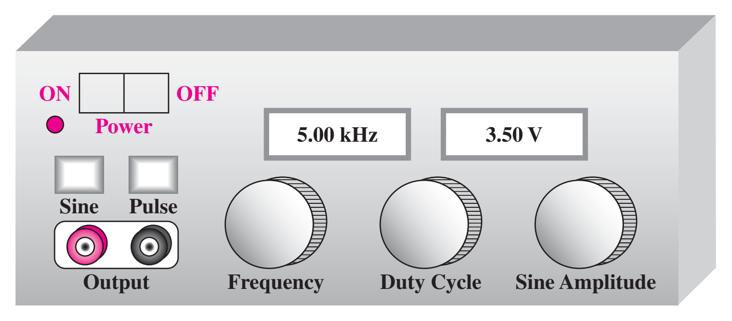
Application Activity: *Sine/Pulse Waveform Generator*

Your company manufactures a battery-operated audio signal generator that produces a sinusoidal output with a variable frequency and amplitude and operates from ±12 V dc voltages. The frequency can be varied from 20 Hz to 20 kHz, and the peak amplitude can be varied from 50 mV to 10 V with front panel controls.

A new version of the signal generator is being designed that adds a pulse waveform generator to the audio signal generator in a single unit. The pulse generator will produce an output with a variable duty cycle that can be used to drive 5 V digital logic circuits. The sine wave generator will remain the same, but the frequency control and the output terminals will be common to both the sine wave generator and the pulse generator. The output function will be switch-selectable, and the pulse waveform will require an additional front panel control for adjusting the duty cycle. The minimum specifications are given in Table 13–1. The front panel for the sine/pulse generator is shown in Figure 13–49.

▶ TABLE 13–1

	OUTPUT VOLTAGE RANGE	FREQUENCY RANGE	DUTY CYCLE RANGE
Sine	0.1 V–20 V p-p	20 Hz–20 kHz	——
Pulse	5 V amplitude	20 Hz–20 kHz	15%–85%



▲ FIGURE 13–49

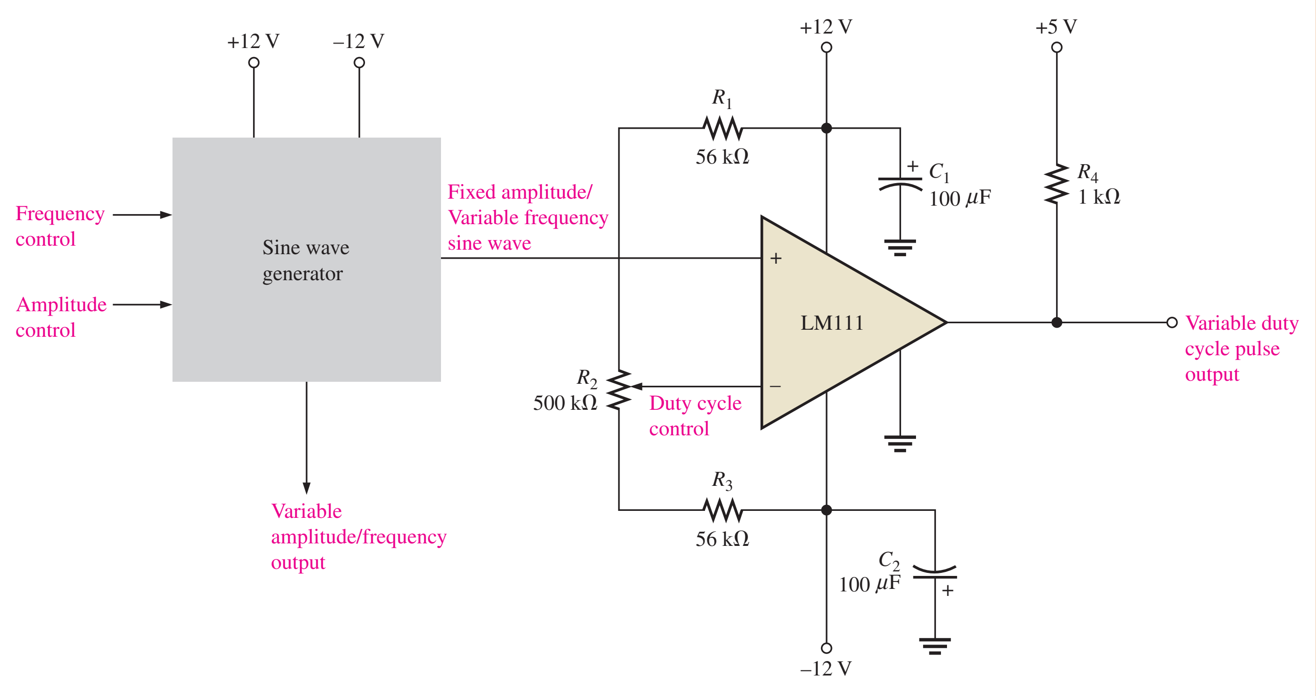
Front panel of the sine/pulse generator.

The Circuit

The schematic of the new design is shown in Figure 13–50. The pulse waveform is derived from the 10 V peak sine wave that is available internally in the existing signal generator. An LM111 comparator is used for producing the pulse waveform using the sine wave as the driving source. The variable reference voltage at the inverting input of the comparator provides the duty cycle control. The duty cycle adjustment range is from 10% to 90%.

The LM111 comparator has an open collector output that is pulled up to +5 V with a 1 kΩ resistor, and the emitter of the output transistor is connected to ground, as shown. As a result, the output pulses vary between 0 V and +5 V.

1. Which components determine the comparator's variable reference voltage?
2. Calculate the minimum reference voltage.
3. Calculate the maximum reference voltage.
4. What sets the amplitude of the output pulses?
5. Explain how the duty cycle control works.



+12 V
−12 V
Frequency control
Amplitude control
Sine wave generator
Variable amplitude/frequency output
Fixed amplitude/ Variable frequency sine wave
R_1
56 kΩ
+12 V
+ C_1
100 μF
+5 V
R_4
1 kΩ
+
LM111
−
Variable duty cycle pulse output
R_2
500 kΩ
Duty cycle control
R_3
56 kΩ
C_2
100 μF
+
−12 V

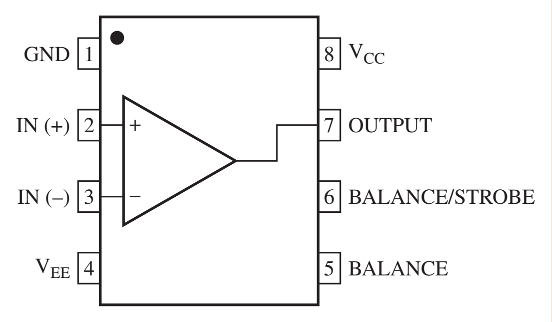
▲ **FIGURE 13–50**

Sine/Pulse generator.

The pin diagram from the LM111 datasheet is shown in Figure 13–51. Pins 5 and 6 are unused in this application.

▶ **FIGURE 13–51**

Pin diagram for the LM111 comparator.



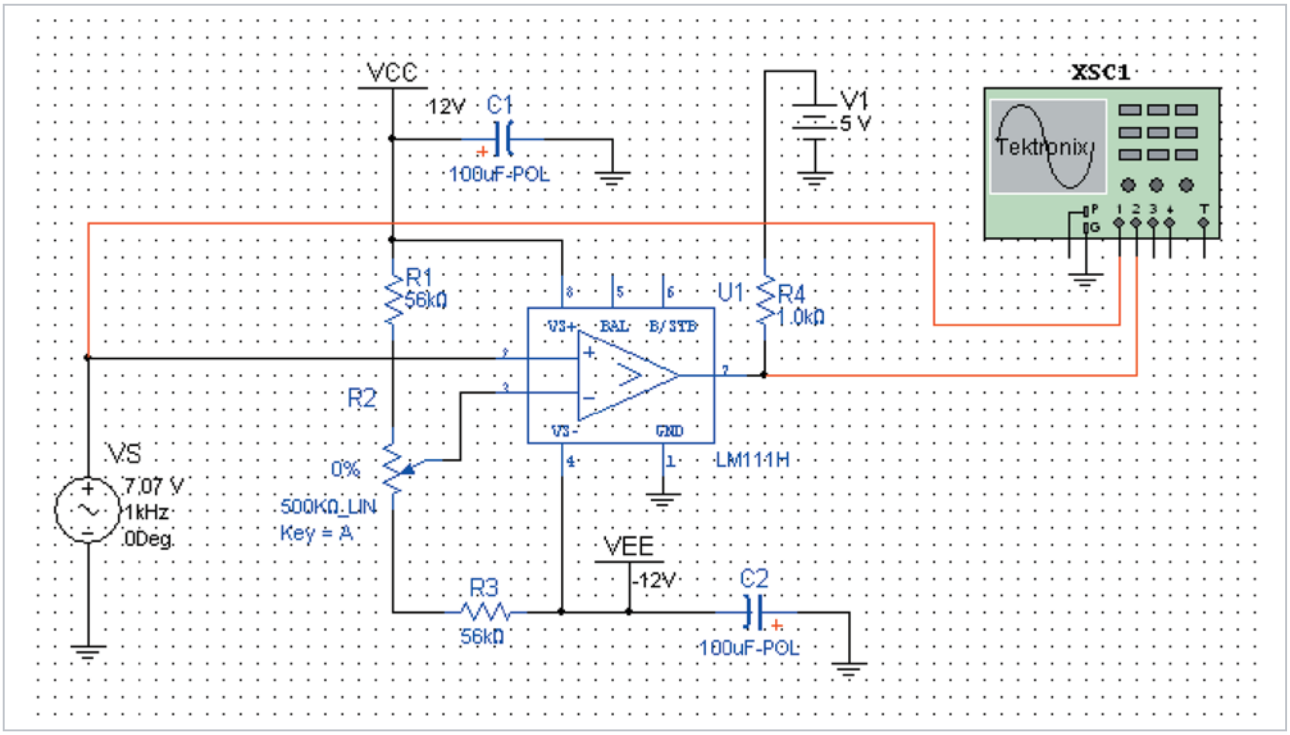
GND 1
IN (+) 2
IN (−) 3
V_{EE} 4
8 V_{CC}
7 OUTPUT
6 BALANCE/STROBE
5 BALANCE
+
−

6. Referencing the pin diagram, assign pin numbers to the comparator in Figure 13–50.

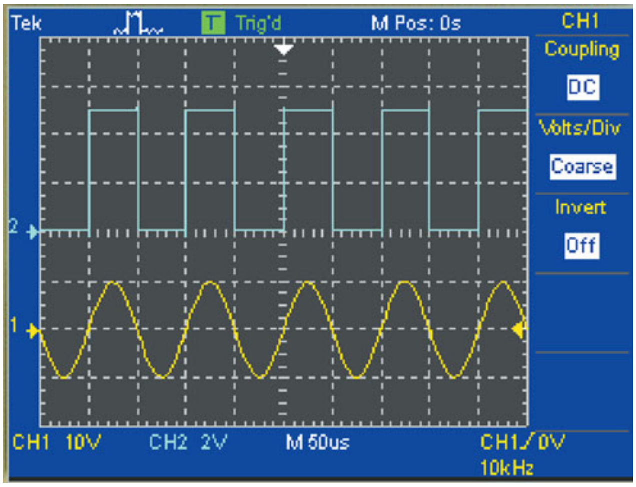
Simulation

The sine/pulse generator is simulated using Multisim with an input signal of 7.07 V rms to represent the existing sine wave generator output. The results are shown in Figure 13–52 where the duty cycle of the pulse waveform is set to 50%.

7. From the scope display in Figure 13–52, verify the rms value of the sine wave.
8. Measure the amplitude of the pulse waveform on the display.
9. Verify the frequency of the waveforms on the display.


VCC
12V
C1
100uF-POL
V1
5 V
XSC1
Tektronix
R1
56kΩ
U1
R4
1.0kΩ
VS+
BAL
B/STB
VS-
GND
R2
VS
7.07 V
1kHz
0Deg
0%
500KΩ_LIN
Key = A
LM111H
VEE
-12V
C2
R3
56kΩ
100uF-POL

(a) Circuit screen


Tek
Trig'd
M Pos: 0s
CH1
Coupling
DC
Volts/Div
Coarse
Invert
Off
2
1

CH1 10V CH2 2V M 50us CH1 ⁄ 0V
10kHz

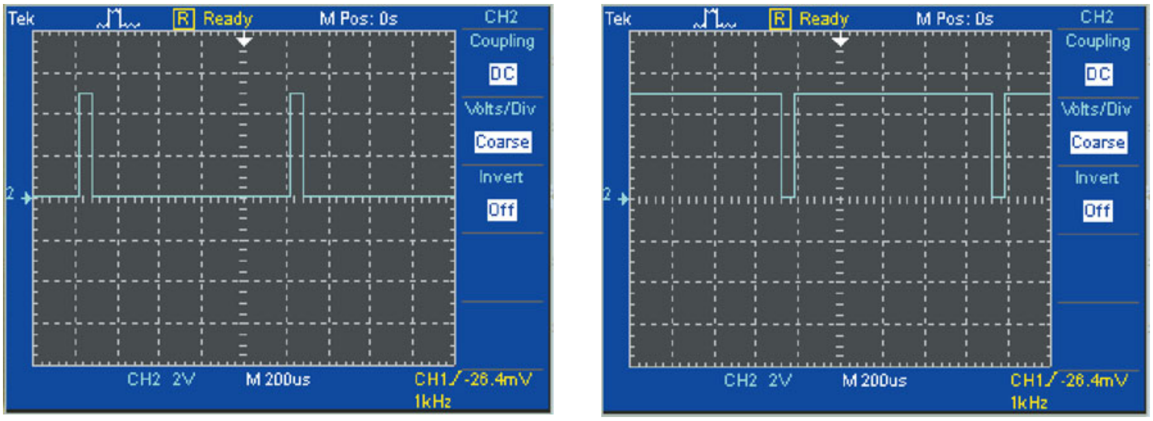
(b) Internal sine wave and the pulse output set at 50% duty cycle

▲ FIGURE 13–52

Simulation of the sine/pulse generator at a frequency of 10 kHz.

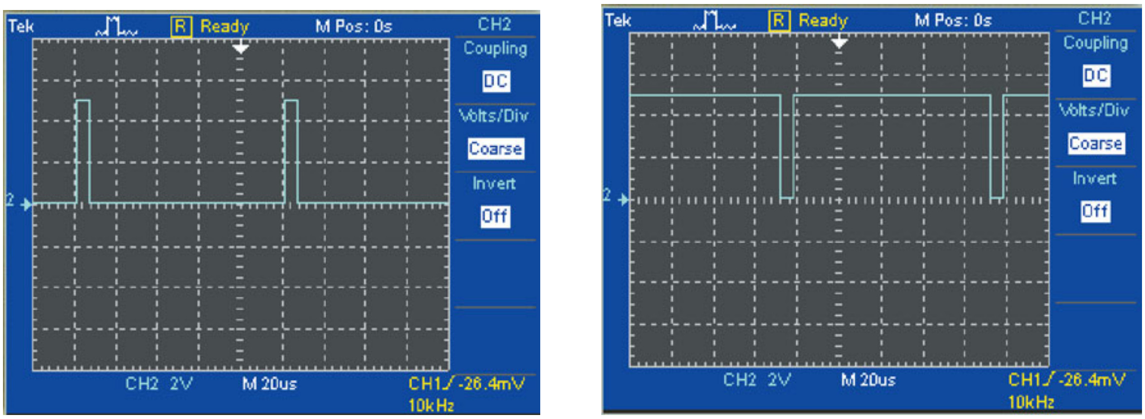
Figure 13–53 shows the simulation results for the pulse duty cycle measurement at test frequencies of 1 kHz and 10 kHz.

10. In Figure 13–53, determine if the minimum and maximum duty cycles meet or exceed specifications for the frequencies shown.


Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
2
CH2 2V
M 200us
CH1 ╱ -26.4mV
1kHz
Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
2
CH2 2V
M 200us
CH1 ╱ -26.4mV
1kHz

(a) Minimum duty cycle at 1 kHz

(b) Maximum duty cycle at 1 kHz


Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
2
CH2 2V
M 20us
CH1 ╱ -26.4mV
10kHz
Tek
R Ready
M Pos: 0s
CH2
Coupling
DC
Volts/Div
Coarse
Invert
Off
2
CH2 2V
M 20us
CH1 ╱ -26.4mV
10kHz

(c) Minimum duty cycle at 10 kHz

(d) Maximum duty cycle at 10 kHz

▲ **FIGURE 13–53**

Simulation results.

Simulate the sine/pulse generator using your Multisim software. Observe the output voltages with the oscilloscope as the duty cycle control is varied.

Hint: Before running a simulation that includes a comparator, it may be necessary to reset the default value of the relative error tolerance to avoid interpolation error, which results in slow transitions particularly at higher frequencies. To do this, select *Simulate* and click on *Interactive Simulation Settings.* Navigate to the *Analysis Options* tab and choose *Customize.* Change the *Relative Tolerance Error* to be le-005.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

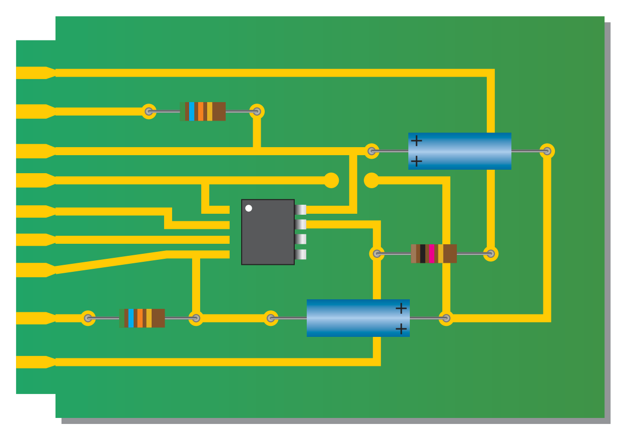
To build and test a similar circuit, go to Experiment 13–A in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The pulse generator board is shown in Figure 13–54. This board will be added to the existing audio generator and connected to the front panel controls to complete the sine/pulse generator.

FIGURE 13–54

Pulse generator board.



11. Check the printed circuit board for correctness by comparing with the schematic in Figure 13–50.
12. Label each input and output pin according to function.

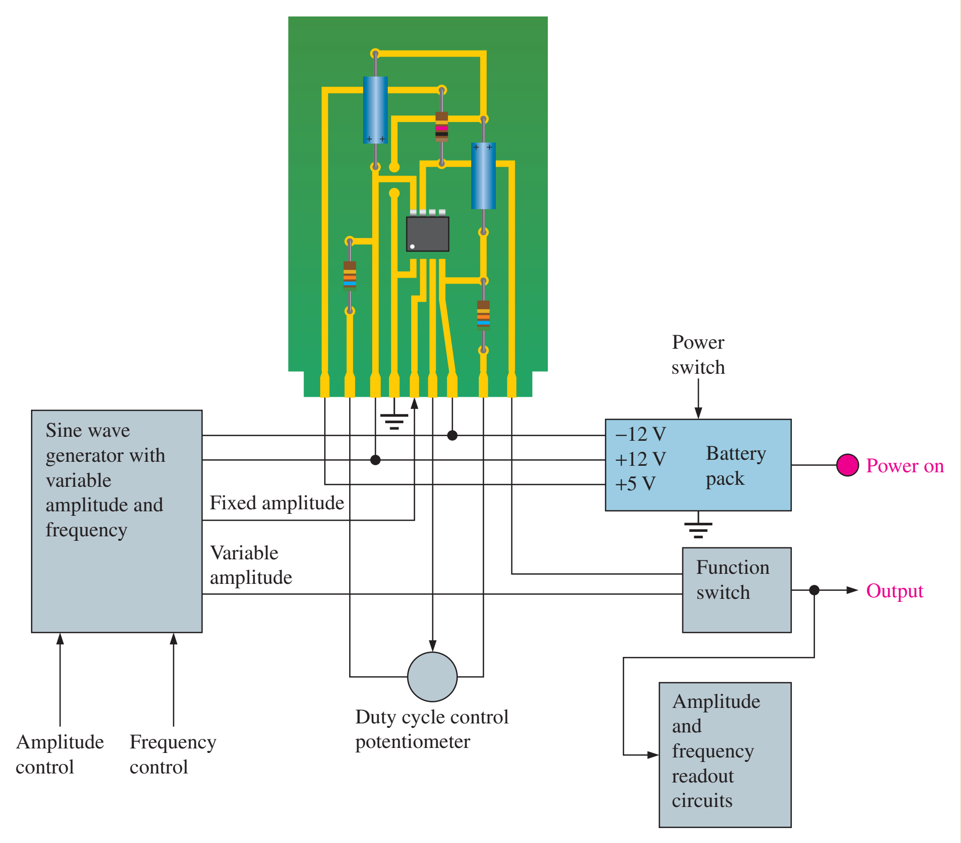
The Sine/Pulse Generator System Diagram

The complete generator unit consists of the sine wave generator, the pulse generator, the front panel controls, and the battery power supply, as shown in Figure 13–55.

13. Verify the connection from the pulse generator board to the various system components.

FIGURE 13–55

System diagram.


Power switch
Sine wave generator with variable amplitude and frequency
Fixed amplitude
Variable amplitude
−12 V
+12 V
+5 V
Battery pack
Power on
Function switch
Output
Amplitude control
Frequency control
Duty cycle control potentiometer
Amplitude and frequency readout circuits

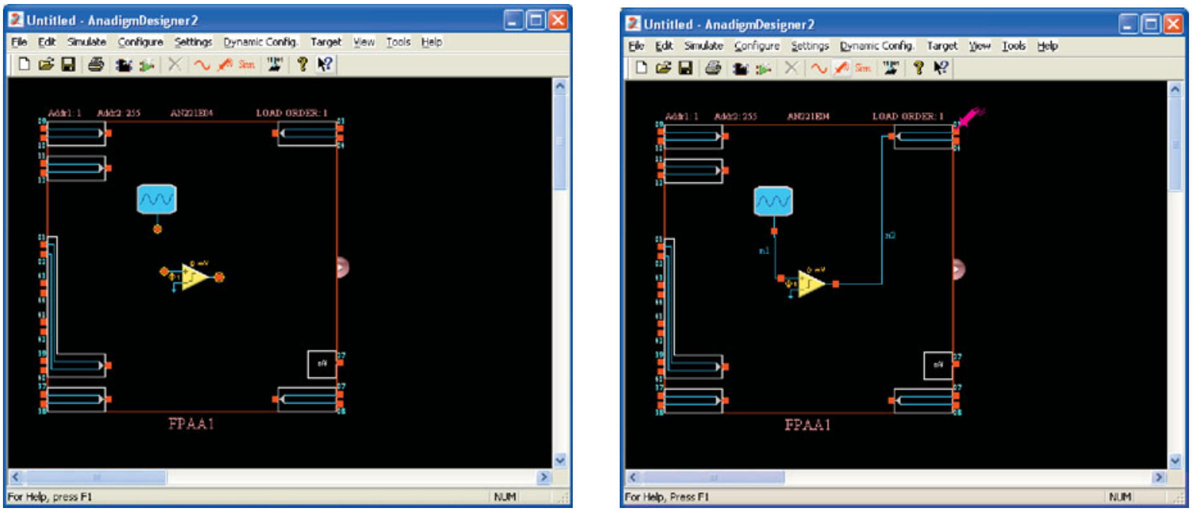
Programmable Analog Technology

Assignment

Create a square-wave generator using a sine wave oscillator and a comparator.

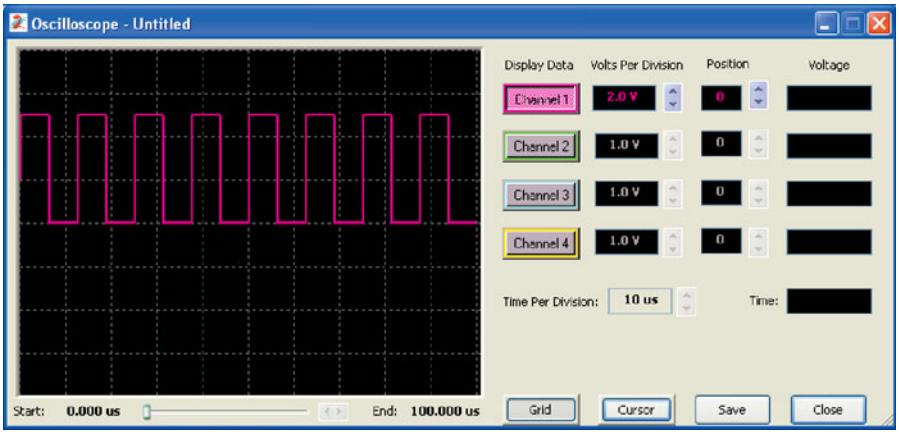
Procedure: Open your Designer2 software and configure and test the FPAA using the default settings as shown in Figure 13–56.

Analysis: Determine the amplitude and frequency of the output in Figure 13–56.


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
FPAA1
For Help, press F1
NUM
n1
n2

(a) Select and place the sine wave oscillator and comparator CAMs.

(b) Connect the CAMs and place probe.


Oscilloscope - Untitled
Display Data
Volts Per Division
Position
Voltage
Channel 1
2.0 V
0
Channel 2
1.0 V
0
Channel 3
1.0 V
0
Channel 4
1.0 V
0
Time Per Division:
10 us
Time:
Start:
0.000 us
End:
100.000 us
Grid
Cursor
Save
Close

(c) Click on *Sim* to run the simulation.

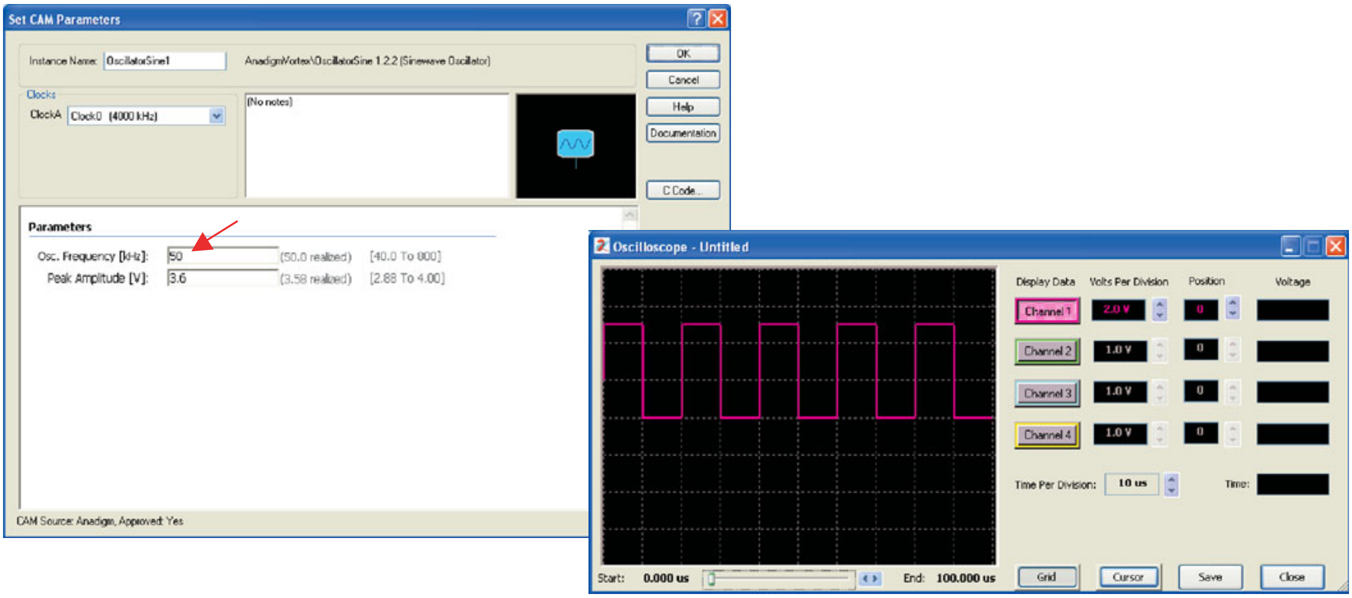
▲ FIGURE 13–56

Design Modifications

Design changes can be made prior to downloading the design or after the design has been downloaded to the chip.

1. Change the frequency and amplitude of the square wave to 50 kHz.

   Procedure: Click on the sine wave oscillator icon to open the *Set CAM Parameters* window. Enter new frequency and run the simulation, as shown in Figure 13–57.



Set CAM Parameters

Instance Name: OscillatorSine1 AnadigmVortex\OscillatorSine 1.2.2 (Sinewave Oscillator)

Clocks

ClockA Clock0 (4000 kHz)

(No notes)

Parameters

Osc. Frequency [kHz]: 50 (50.0 realized) [40.0 To 800]

Peak Amplitude [V]: 3.6 (3.58 realized) [2.88 To 4.00]

CAM Source: Anadigm, Approved: Yes

Oscilloscope - Untitled

Display Data	Volts Per Division	Position	Voltage
Channel 1	2.0 V	0	
Channel 2	1.0 V	0	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

Time Per Division: 10 us Time:

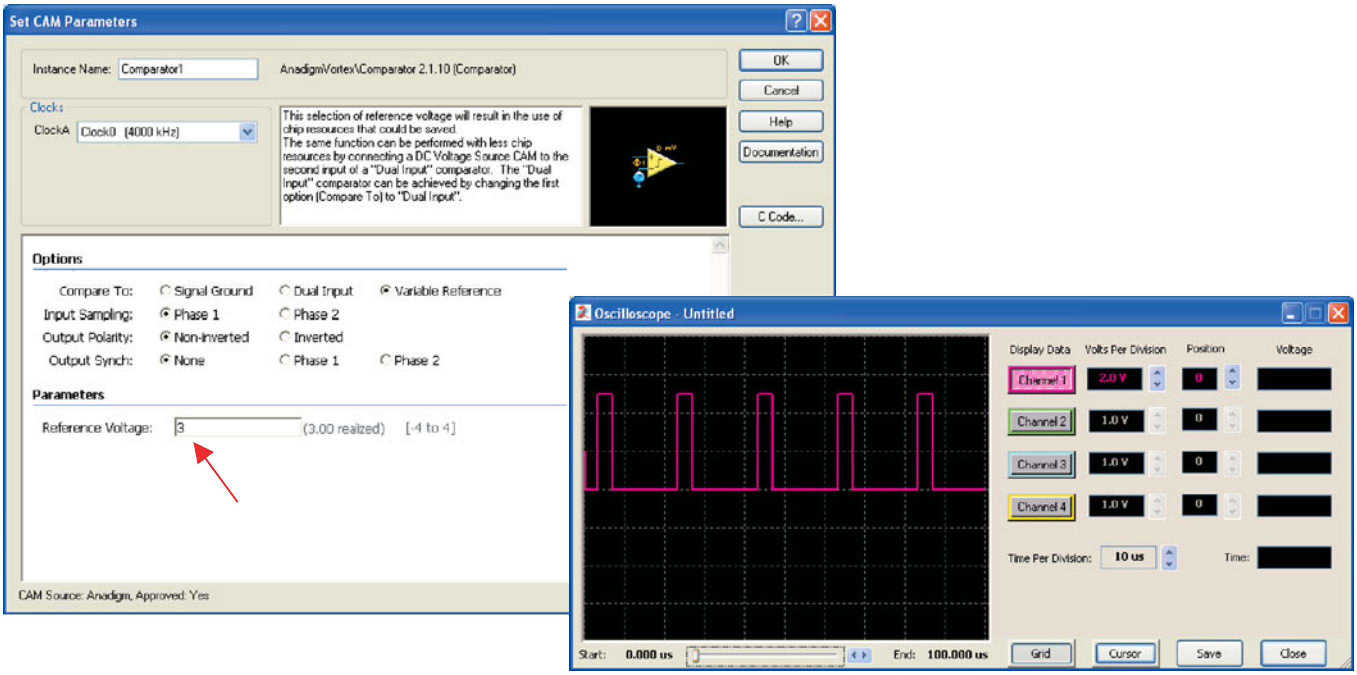
Start: 0.000 us End: 100.000 us

▲ FIGURE 13–57

Analysis: Verify the frequency of the square wave on the scope display in Figure 13–57.

2. Decrease the duty cycle of the square wave.

   Procedure: Click on the comparator icon to open the *Set CAM Parameters* window. Choose variable reference, and set it to +3 V, as shown in Figure 13–58. Run the simulation. (The reference can be set to any voltage within the specified range to achieve a desired duty cycle.)



Set CAM Parameters

Instance Name: Comparator1 AnadigmVortex\Comparator 2.1.10 (Comparator)

Clocks

ClockA Clock0 (4000 kHz)

This selection of reference voltage will result in the use of chip resources that could be saved.
The same function can be performed with less chip resources by connecting a DC Voltage Source CAM to the second input of a "Dual Input" comparator. The "Dual Input" comparator can be achieved by changing the first option (Compare To) to "Dual Input".

Options

Compare To: ○ Signal Ground ○ Dual Input ● Variable Reference

Input Sampling: ● Phase 1 ○ Phase 2

Output Polarity: ● Non-inverted ○ Inverted

Output Synch: ● None ○ Phase 1 ○ Phase 2

Parameters

Reference Voltage: 3 (3.00 realized) [-4 to 4]

CAM Source: Anadigm, Approved: Yes

Oscilloscope - Untitled

Display Data	Volts Per Division	Position	Voltage
Channel 1	2.0 V	0	
Channel 2	1.0 V	0	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

Time Per Division: 10 us Time:

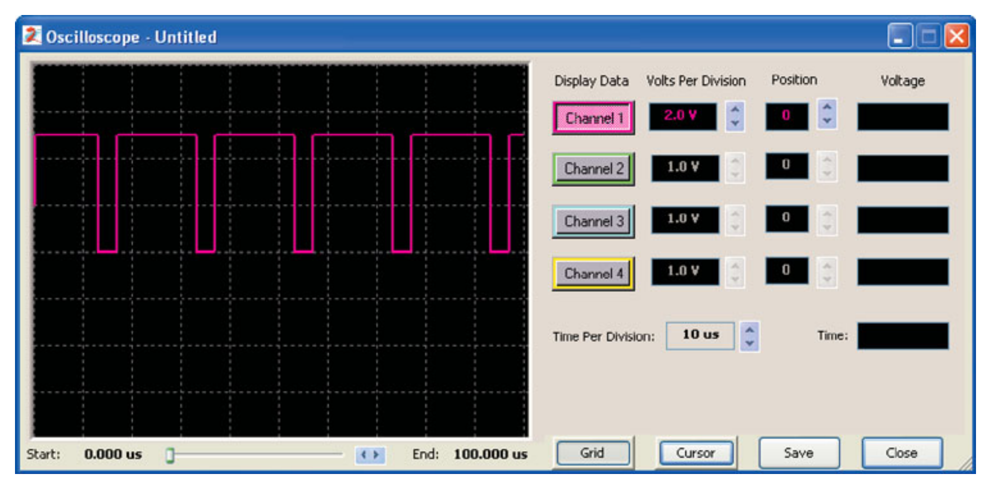
Start: 0.000 us End: 100.000 us

▲ FIGURE 13–58

Analysis: Measure the duty cycle of the pulse waveform on the scope display in Figure 13–58.

3. Increase the duty cycle of the square wave.

   Procedure: Click on the comparator icon to open the *Set CAM Parameters* window. Choose variable reference, and set it to −3 V. Run the simulation. The result is shown in Figure 13–59.



Oscilloscope - Untitled

Display Data	Volts Per Division	Position	Voltage
Channel 1	2.0 V	0	
Channel 2	1.0 V	0	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

Time Per Division: 10 us

Time:

Start: 0.000 us

End: 100.000 us

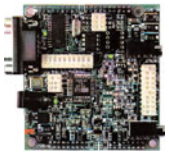
FIGURE 13–59

Analysis: Measure the duty cycle of the pulse waveform in Figure 13–59.

Programming Exercises

1. Open your Designer2 software.
2. Implement the pulse waveform generator described.
3. Change the frequency to 100 kHz.
4. Decrease the duty cycle to less than that shown in Figure 13–58.
5. Increase the duty cycle to greater than that shown in Figure 13–59.

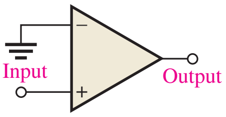
PAM Experiment



To program, download, and test a circuit using AnadigmDesigner2 software and the programmable analog module (PAM) board, go to Experiment 13–B in *Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling.

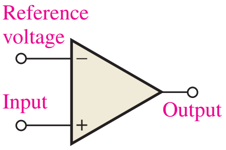
SUMMARY OF COMPARATORS AND OP-AMP CIRCUITS

COMPARATORS



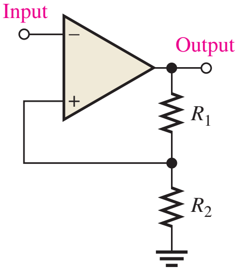
Input
Output
–
+

Zero-level detector



Reference voltage
Input
Output
–
+

Nonzero-level detector

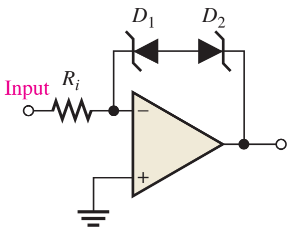


Input
Output
–
+
R_1
R_2

$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$$

$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$$

Comparator with hysteresis



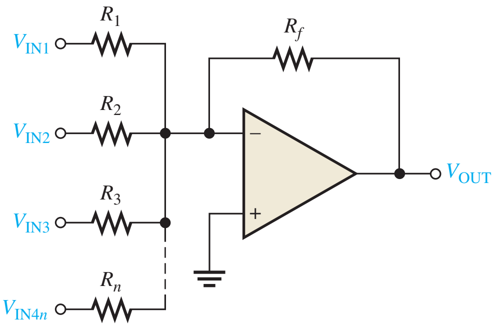
D_1
D_2
Input
R_i
–
+

$$+V_{out(max)} = V_{Z1} + 0.7\text{ V}$$

$$-V_{out(max)} = -(V_{Z2} + 0.7\text{ V})$$

Bounded comparator

SUMMING AMPLIFIER



V_{IN1}
R_1
R_f
V_{IN2}
R_2
–
V_{OUT}
V_{IN3}
R_3
+
R_n
V_{IN4n}

Summing amplifier

- Unity-gain amplifier.

$$R_f = R_1 = R_2 = R_3 = \cdots = R_n$$

$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})$$

- Greater than unity-gain amplifier:

$$R_f > R$$

$$R = R_1 = R_2 = R_3 = \cdots = R_n$$

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})$$

- Averaging amplifier:

$$\frac{R_f}{R} = \frac{1}{n}$$

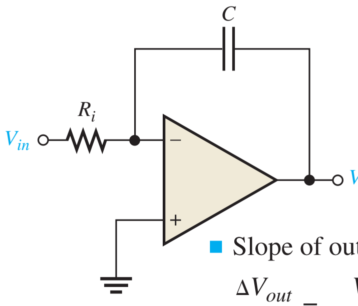
$$R = R_1 = R_2 = R_3 = \cdots = R_n$$

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})$$

- Scaling adder:

$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \frac{R_f}{R_3}V_{IN3} + \cdots + \frac{R_f}{R_n}V_{INn}\right)$$

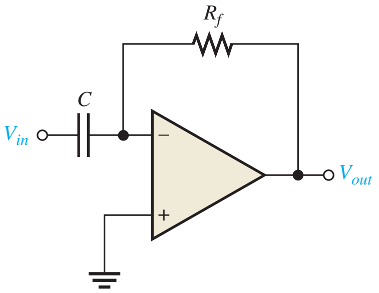
INTEGRATOR AND DIFFERENTIATOR



- Slope of output voltage:

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_iC}$$

Integrator



- Output voltage:

$$V_{out} = -\left(\frac{V_C}{t}\right)R_fC$$

$$V_C = V_{in}$$

Differentiator

SUMMARY

Section 13-1

- In an op-amp comparator, when the input voltage exceeds a specified reference voltage, the output changes state.
- Hysteresis gives an op-amp noise immunity.
- A comparator switches to one state when the input reaches the upper trigger point (UTP) and back to the other state when the input drops below the lower trigger point (LTP).
- The difference between the UTP and the LTP is the hysteresis voltage.
- Bounding limits the output amplitude of a comparator.

Section 13–2

- The output voltage of a summing amplifier is proportional to the sum of the input voltages.
- An averaging amplifier is a summing amplifier with a closed-loop gain equal to the reciprocal of the number of inputs.
- In a scaling adder, a different weight can be assigned to each input, thus making the input contribute more or contribute less to the output.

Section 13–3

- Integration is a mathematical process for determining the area under a curve.
- Integration of a step input produces a ramp output with a slope proportional to the amplitude.
- Differentiation is a mathematical process for determining the rate of change of a function.
- Differentiation of a ramp input produces a step output with an amplitude proportional to the slope.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Bounding The process of limiting the output range of an amplifier or other circuit.

Comparator A circuit that compares two input voltages and produces an output in either of two states indicating the greater than or less than relationship of the inputs.

Differentiator A circuit that produces an output which approximates the instantaneous rate of change of the input function.

Hysteresis Characteristic of a circuit in which two different trigger levels create an offset or lag in the switching action.

Integrator A circuit that produces an output which approximates the area under the curve of the input function.

Schmitt trigger A comparator with built-in hysteresis.

Summing amplifier An op-amp configuration with two or more inputs that produces an output voltage that is proportional to the negative of the algebraic sum of its input voltages.

KEY FORMULAS

Comparator

13–1	$V_{\text{UTP}} = \dfrac{R_2}{R_1 + R_2}(+V_{out(max)})$	Upper trigger point
13–2	$V_{\text{LTP}} = \dfrac{R_2}{R_1 + R_2}(-V_{out(max)})$	Lower trigger point
13–3	$V_{\text{HYS}} = V_{\text{UTP}} - V_{\text{LTP}}$	Hysteresis voltage

Summing Amplifier

13–4	$V_{\text{OUT}} = -(V_{\text{IN1}} + V_{\text{IN2}} + \cdots + V_{\text{IN}n})$	*n*-input adder
13–5	$V_{\text{OUT}} = -\dfrac{R_f}{R}(V_{\text{IN1}} + V_{\text{IN2}} + \cdots + V_{\text{IN}n})$	Adder with gain
13–6	$V_{\text{OUT}} = -\left(\dfrac{R_f}{R_1}V_{\text{IN1}} + \dfrac{R_f}{R_2}V_{\text{IN2}} + \cdots + \dfrac{R_f}{R_n}V_{\text{IN}n}\right)$	Scaling adder with gain

Integrator and Differentiator

13–7	$\dfrac{\Delta V_{out}}{\Delta t} = -\dfrac{V_{in}}{R_i C}$	Integrator output rate of change
13–8	$V_{out} = -\left(\dfrac{V_C}{t}\right)R_f C$	Differentiator output voltage with ramp input

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. The output of a comparator has two states.
2. The reference voltage on a comparator input establishes the gain.
3. Hysteresis incorporates positive feedback.
4. A comparator with hyteresis has two trigger points.
5. A summing amplifier can have more than two inputs.
6. The gain of a summing amplifier must always be unity (1).
7. DAC stands for digital-to-analog comparator.
8. An *R*/2*R* ladder circuit is one form of DAC.
9. An integrator produces a ramp when a step input is applied.
10. In a practical integrator, a resistor is connected across the capacitor.
11. When a triangular waveform is applied to a differential, a sine wave appears on the output.
12. In a practical differentiator, a resistor is connected in series with the capacitor.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If R_2 opens in the comparator of Figure 13–3, the output voltage amplitude will
   (a) increase **(b)** decrease **(c)** not change
2. In the trigger circuit of Figure 13–9, if R_1 is decreased to 50 kΩ, the upper trigger-point voltage will
   (a) increase **(b)** decrease **(c)** not change

3. If the zener diodes in Figure 13–13 are changed to ones with a rating of 5.6 V, the output voltage amplitude will

   (a) increase **(b)** decrease **(c)** not change

4. If the top resistor in Figure 13–22 opens, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

5. If V_{IN2} is changed to -1 V in Figure 13–22, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

6. If V_{IN1} is increased to 0.4 V and V_{IN2} is reduced to 0.3 V in Figure 13–23, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

7. If V_{IN3} is changed to -7 V in Figure 13–24, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

8. If R_f in Figure 13–25 opens, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

9. If the value of C in Figure 13–35 is reduced, the frequency of the output waveform will

   (a) increase **(b)** decrease **(c)** not change

10. If the frequency of the input waveform in Figure 13–40 is increased, the amplitude of the output voltage will

    (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 13–1

1. In a zero-level detector, the output changes state when the input

   (a) is positive **(b)** is negative **(c)** crosses zero **(d)** has a zero rate of change

2. The zero-level detector is one application of a

   (a) comparator **(b)** differentiator **(c)** summing amplifier **(d)** diode

3. Noise on the input of a comparator can cause the output to

   (a) hang up in one state
   (b) go to zero
   (c) change back and forth erratically between two states
   (d) produce the amplified noise signal

4. The effects of noise can be reduced by

   (a) lowering the supply voltage **(b)** using positive feedback
   (c) using negative feedback **(d)** using hysteresis
   (e) answers (b) and (d)

5. A comparator with hysteresis

   (a) has one trigger point **(b)** has two trigger points
   (c) has a variable trigger point **(d)** is like a magnetic circuit

6. In a comparator with hysteresis,

   (a) a bias voltage is applied between the two inputs
   (b) only one supply voltage is used
   (c) a portion of the output is fed back to the inverting input
   (d) a portion of the output is fed back to the noninverting input

7. Using output bounding in a comparator

   (a) makes it faster **(b)** keeps the output positive
   (c) limits the output levels **(d)** stabilizes the output

Section 13–2

8. A summing amplifier can have

   (a) only one input **(b)** only two inputs **(c)** any number of inputs

9. If the voltage gain for each input of a summing amplifier with a 4.7 kΩ feedback resistor is unity, the input resistors must have a value of

(a) 4.7 kΩ

(b) 4.7 kΩ divided by the number of inputs

(c) 4.7 kΩ times the number of inputs

10. An averaging amplifier has five inputs. The ratio R_f/R_i must be

(a) 5 **(b)** 0.2 **(c)** 1

11. In a scaling adder, the input resistors are

(a) all the same value **(b)** all of different values

(c) each proportional to the weight of its input **(d)** related by a factor of two

Section 13–3

12. In an ideal integrator, the feedback element is a

(a) resistor **(b)** capacitor **(c)** zener diode **(d)** voltage divider

13. For a step input, the output of an integrator is

(a) a pulse **(b)** a triangular waveform **(c)** a spike **(d)** a ramp

14. The rate of change of an integrator's output voltage in response to a step input is set by

(a) the *RC* time constant **(b)** the amplitude of the step input

(c) the current through the capacitor **(d)** all of these

15. In a differentiator, the feedback element is a

(a) resistor **(b)** capacitor **(c)** zener diode **(d)** voltage divider

16. The output of a differentiator is proportional to

(a) the *RC* time constant **(b)** the rate at which the input is changing

(c) the amplitude of the input **(d)** answers (a) and (b)

17. When you apply a triangular waveform to the input of a differentiator, the output is

(a) a dc level **(b)** an inverted triangular waveform

(c) a square waveform **(d)** the first harmonic of the triangular waveform

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

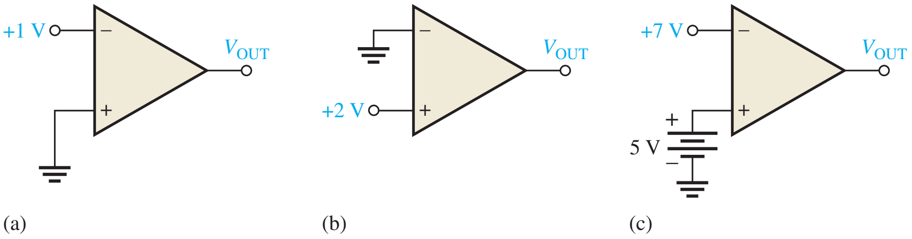
BASIC PROBLEMS

Section 13–1

Comparators

1. A certain op-amp has an open-loop gain of 80,000. The maximum saturated output levels of this particular device are ±12 V when the dc supply voltages are ±15 V. If a differential voltage of 0.15 mV rms is applied between the inputs, what is the peak-to-peak value of the output?

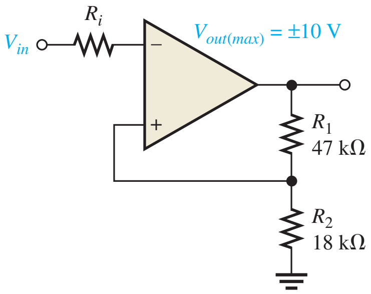
2. Determine the output level (maximum positive or maximum negative) for each comparator in Figure 13–60.



▲ FIGURE 13–60

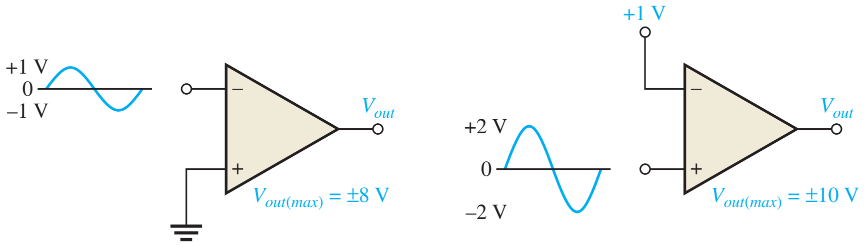
▶ FIGURE 13–61

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F13–61).


R_i
V_{in}
$V_{out(max)} = \pm 10$ V
–
+
R_1
47 kΩ
R_2
18 kΩ

3. Calculate the V_{UTP} and V_{LTP} in Figure 13–61. $V_{out(max)} = \pm 10$ V.
4. What is the hysteresis voltage in Figure 13–61?
5. Draw the output voltage waveform for each circuit in Figure 13–62 with respect to the input. Show voltage levels.

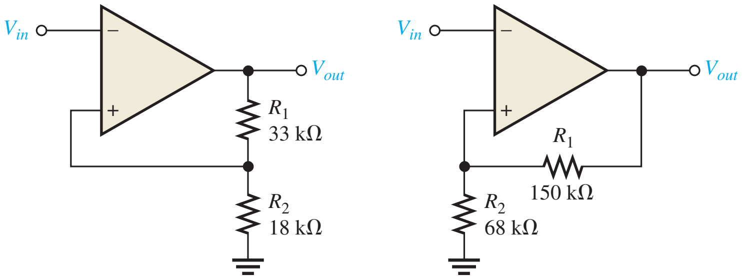
▶ FIGURE 13–62


+1 V
0
–1 V
–
+
V_{out}
$V_{out(max)} = \pm 8$ V
+1 V
+2 V
0
–2 V
–
+
V_{out}
$V_{out(max)} = \pm 10$ V

(a) (b)

6. Determine the hysteresis voltage for each comparator in Figure 13–63. The maximum output levels are ±11 V.

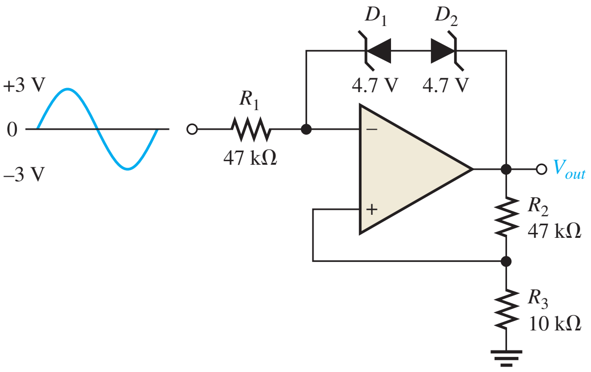
▶ FIGURE 13–63


V_{in}
–
+
V_{out}
R_1
33 kΩ
R_2
18 kΩ
V_{in}
–
+
V_{out}
R_1
150 kΩ
R_2
68 kΩ

(a) (b)

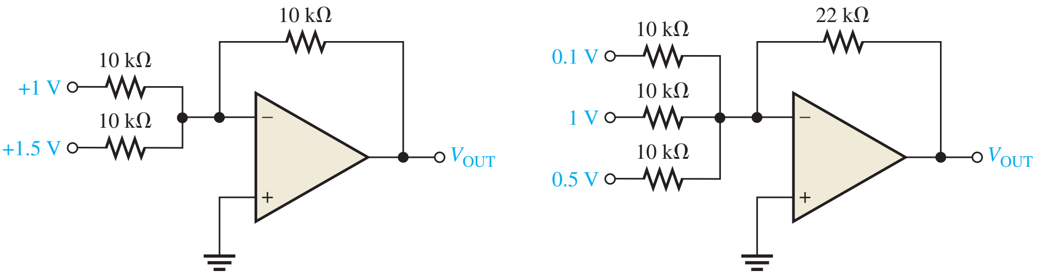
7. A 6.2 V zener diode is connected from the output to the inverting input in Figure 13–61 with the cathode at the output. What are the positive and negative output levels?
8. Determine the output voltage waveform in Figure 13–64.

▶ FIGURE 13–64


D_1
D_2
4.7 V
4.7 V
+3 V
0
–3 V
R_1
47 kΩ
–
+
V_{out}
R_2
47 kΩ
R_3
10 kΩ

Section 13–2 Summing Amplifiers

9. Determine the output voltage for each circuit in Figure 13–65.


10 kΩ
10 kΩ
+1 V
10 kΩ
+1.5 V
−
+
V_{OUT}
10 kΩ
22 kΩ
0.1 V
10 kΩ
1 V
10 kΩ
0.5 V
−
+
V_{OUT}

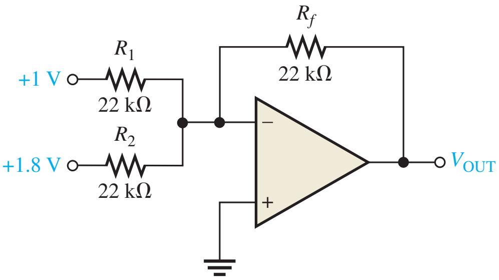
(a) (b)

▲ FIGURE 13–65

10. Refer to Figure 13–66. Determine the following:

(a) V_{R1} and V_{R2} **(b)** Current through R_f **(c)** V_{OUT}

▶ FIGURE 13–66


R_f
22 kΩ
R_1
+1 V
22 kΩ
R_2
+1.8 V
22 kΩ
−
+
V_{OUT}

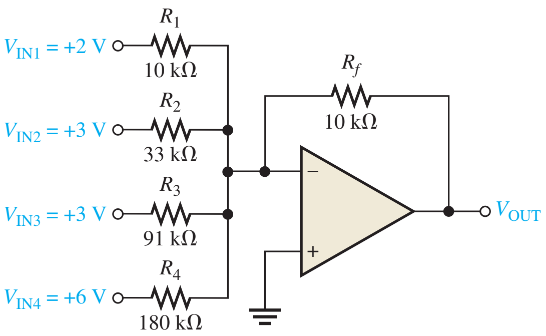
11. Find the value of R_f necessary to produce an output that is five times the sum of the inputs in Figure 13–66.

12. Show a summing amplifier that will average eight input voltages. Use input resistances of 10 kΩ each.

13. Find the output voltage when the input voltages shown in Figure 13–67 are applied to the scaling adder. What is the current through R_f?

14. Determine the values of the input resistors required in a six-input scaling adder so that the lowest weighted input is 1 and each successive input has a weight twice the previous one. Use $R_f = 100\text{ k}\Omega$.

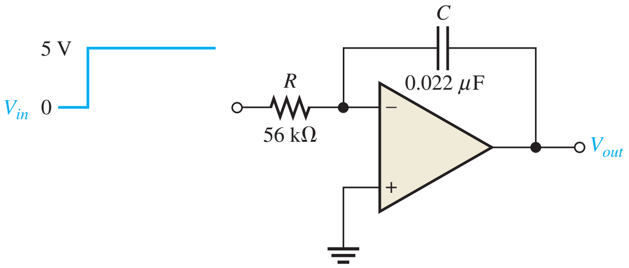
▶ FIGURE 13–67


R_1
$V_{IN1} = +2$ V
10 kΩ
R_2
$V_{IN2} = +3$ V
33 kΩ
R_3
$V_{IN3} = +3$ V
91 kΩ
R_4
$V_{IN4} = +6$ V
180 kΩ
R_f
10 kΩ
−
+
V_{OUT}

Section 13–3 Integrators and Differentiators

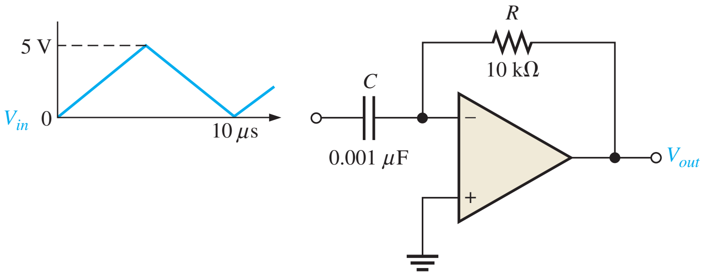
15. Determine the rate of change of the output voltage in response to the step input to the integrator in Figure 13–68.

▶ **FIGURE 13–68**



16. A triangular waveform is applied to the input of the circuit in Figure 13–69 as shown. Determine what the output should be and sketch its waveform in relation to the input.

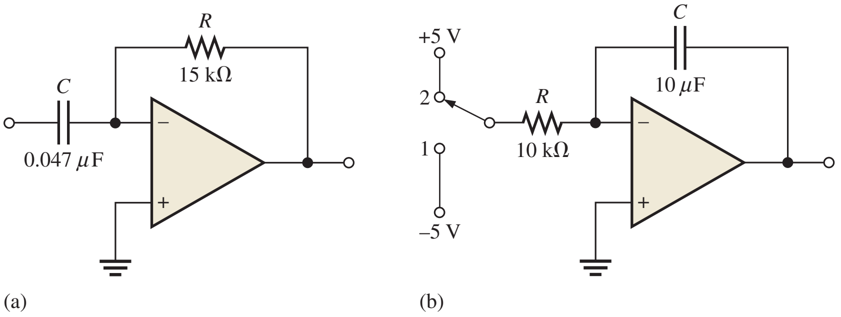
▶ **FIGURE 13–69**



17. What is the magnitude of the capacitor current in Problem 16?

18. A triangular waveform with a peak-to-peak voltage of 2 V and a period of 1 ms is applied to the differentiator in Figure 13–70(a). What is the output voltage?

19. Beginning in position 1 in Figure 13–70(b), the switch is thrown into position 2 and held there for 10 ms, then back to position 1 for 10 ms, and so forth. Sketch the resulting output waveform if its initial value is 0 V. The saturated output levels of the op-amp are ±12 V.



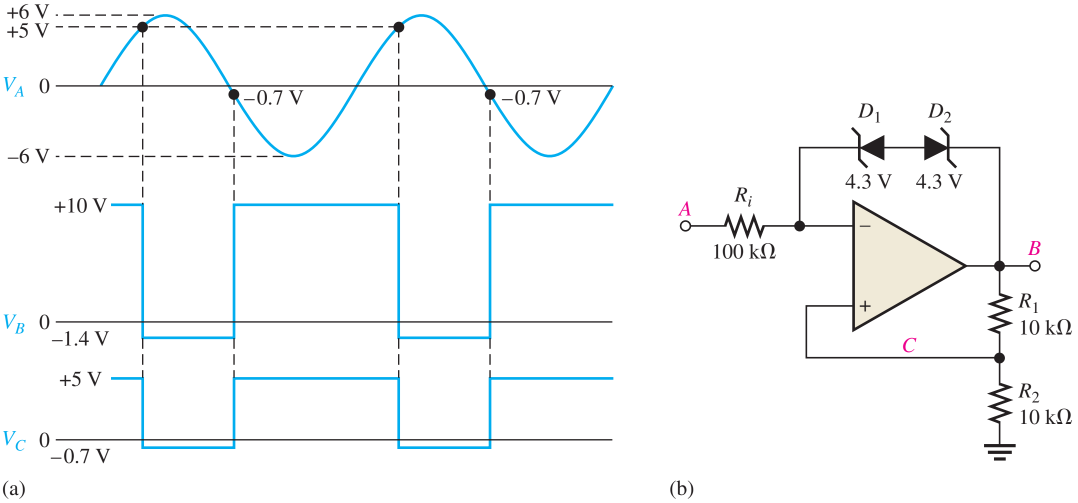
(a)

(b)

▲ **FIGURE 13–70**

Section 13–4 Troubleshooting

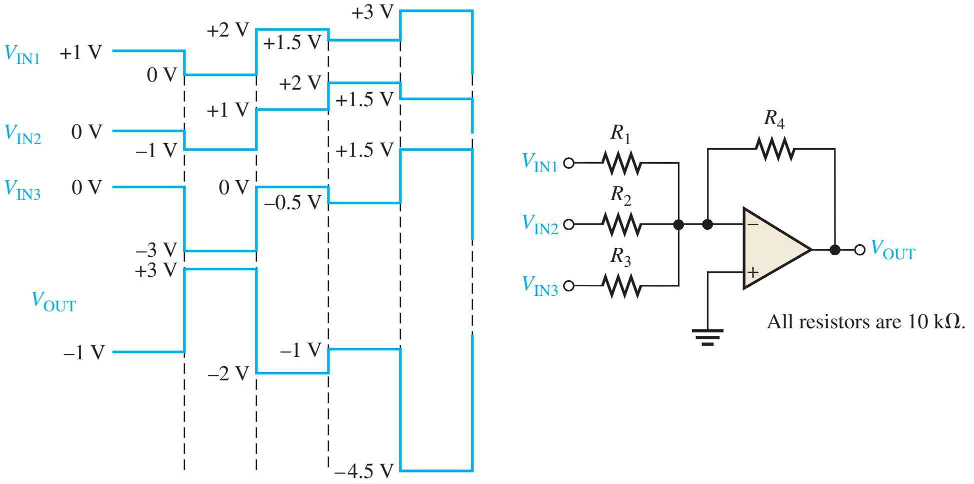
20. The waveforms given in Figure 13–71(a) are observed at the indicated points in Figure 13–71(b). Is the circuit operating properly? If not, what is a likely fault?



+6 V
+5 V
V_A 0
–0.7 V
–0.7 V
–6 V
+10 V
V_B 0
–1.4 V
+5 V
V_C 0
–0.7 V
(a)
D_1
D_2
4.3 V
4.3 V
A
R_i
100 kΩ
B
R_1
10 kΩ
C
R_2
10 kΩ
(b)

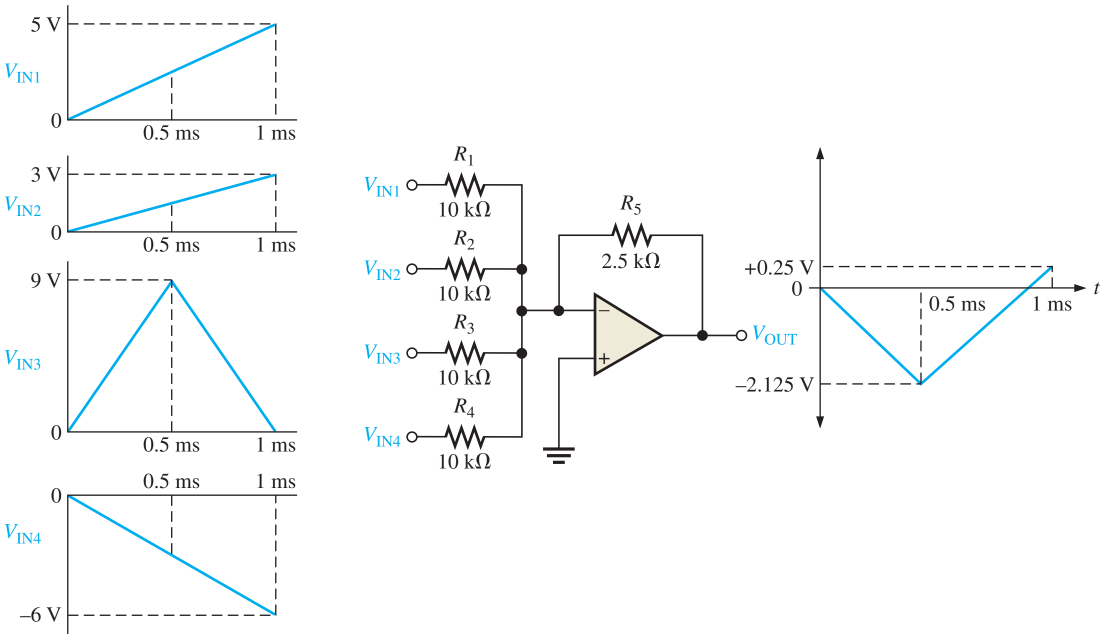
FIGURE 13–71

21. The sequences of voltage levels shown in Figure 13–72 are applied to the summing amplifier and the indicated output is observed. First, determine if this output is correct. If it is not correct, determine the fault.



V_{IN1} +1 V
0 V
+2 V
+1.5 V
+3 V
V_{IN2} 0 V
–1 V
+1 V
+2 V
+1.5 V
+1.5 V
V_{IN3} 0 V
0 V
–0.5 V
–3 V
+3 V
V_{OUT}
–1 V
–2 V
–1 V
–4.5 V
R_1
R_2
R_3
R_4
V_{IN1}
V_{IN2}
V_{IN3}
V_{OUT}
All resistors are 10 kΩ.

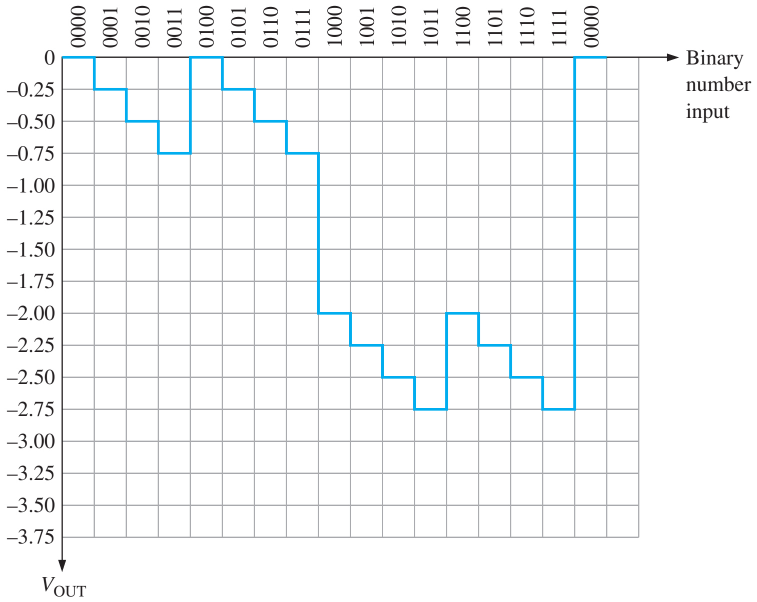
FIGURE 13–72


5 V
V_{IN1}
0
0.5 ms
1 ms
3 V
V_{IN2}
0
0.5 ms
1 ms
9 V
V_{IN3}
0
0.5 ms
1 ms
0.5 ms
1 ms
0
V_{IN4}
−6 V
R_1
10 kΩ
R_2
10 kΩ
R_3
10 kΩ
R_4
10 kΩ
R_5
2.5 kΩ
V_{OUT}
+0.25 V
0
−2.125 V
0.5 ms
1 ms
t

▲ FIGURE 13–73

22. The given ramp voltages are applied to the op-amp circuit in Figure 13–73. Is the given output correct? If it isn't, what is the problem?

23. The DAC with inputs as shown in Figure 13–27 produces the output shown in Figure 13–74. Determine the fault in the circuit.

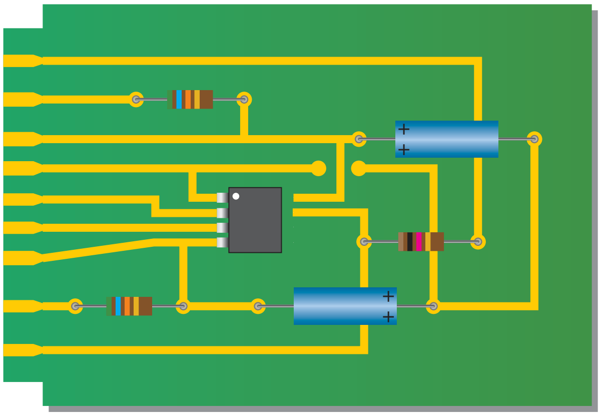


▲ FIGURE 13–74

APPLICATION ACTIVITY PROBLEMS

24. The PC board, shown in Figure 13–75, for the application activity has just come off the assembly line and a pass/fail test indicates that it doesn't work. The board now comes to you for troubleshooting. What is the very first thing you should do? Can you isolate the problem(s) by this first step in this case?

FIGURE 13–75



25. Describe the effect of an open decoupling capacitor on the PC board in Figure 13–75.

26. Assume that a 1.0 kΩ resistor is inadvertently used for R_1 in Figure 13–50. What effect does this have on the circuit operation?

ADVANCED PROBLEMS

27. Calculate the percent duty cycle in Figure 13–50 for minimum and maximum settings of R_2. A 10 V peak sine wave is applied to the noninverting input of the comparator with no hysteresis.

28. Redesign the circuit in Figure 13–50 for a 5 V peak sine wave.

29. Design an integrator that will produce an output voltage with a slope of 100 mV/μs when the input voltage is a constant 5 V. Specify the input frequency of a square wave with an amplitude of 5 V that will result in a 5 V peak-to-peak triangular wave output.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

30. Open file TSP13-30 and determine the fault.

31. Open file TSP13-31 and determine the fault.

32. Open file TSP13-32 and determine the fault.

33. Open file TSP13-33 and determine the fault.

34. Open file TSP13-34 and determine the fault.

35. Open file TSP13-35 and determine the fault.

36. Open file TSP13-36 and determine the fault.

37. Open file TSP13-37 and determine the fault.

38. Open file TSP13-38 and determine the fault.

39. Open file TSP13-39 and determine the fault.

14

SPECIAL-PURPOSE OP-AMP CIRCUITS

CHAPTER OUTLINE

14–1 Instrumentation Amplifiers
14–2 Isolation Amplifiers
14–3 Operational Transconductance Amplifiers (OTAs)
14–4 Log and Antilog Amplifiers
14–5 Converters and Other Op-Amp Circuits
Application Activity
Programmable Analog Technology

CHAPTER OBJECTIVES

- Explain and analyze the operation of an instrumentation amplifier
- Explain and analyze the operation of an isolation amplifier
- Explain and analyze the operation of an operation transconductance amplifier (OTA)
- Explain and analyze the operation of log and antilog amplifiers
- Explain and analyze other types of op-amp circuits

KEY TERMS

- Instrumentation amplifier
- Isolation amplifier
- Operational transconductance amplifier (OTA)
- Transconductance
- Natural Logarithm

APPLICATION ACTIVITY PREVIEW

The Application Activity in this chapter describes a liquid-level control system for an industrial storage tank. A pressure sensor, which is a type of transducer, is used to detect a change in pressure in a tube inserted in the liquid. The voltage from the pressure sensor is sent to the control circuit that consists of an instrumentation amplifier and a comparator. When the liquid in the tank reaches a predetermined minimum level, the circuit causes a pump to turn on and refill the tank to a predetermined maximum level. Also, a method for minimizing the effects of noise in an industrial environment is introduced in this chapter and used in the application.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

A general-purpose op-amp, such as the 741, is a versatile and widely used device. However, some specialized IC amplifiers are available that have certain features or characteristics oriented to special applications. Most of these devices are actually derived from the basic op-amp. These special circuits include the instrumentation amplifier that is used in high-noise environments, the isolation amplifier that is used in high-voltage and medical applications, the operational transconductance amplifier (OTA) that is used as a voltage-to-current amplifier, and the logarithmic amplifiers that are used for linearizing certain types of inputs and for mathematical operations. Log amplifiers are also used in communication systems, including fiber optics.

14–1 INSTRUMENTATION AMPLIFIERS

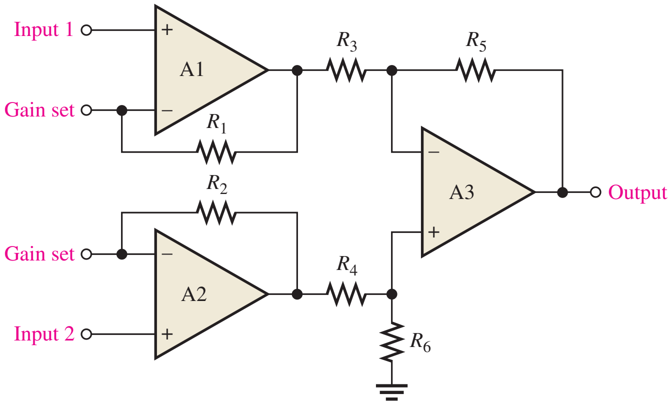
Instrumentation amplifiers are commonly used in environments with high common-mode noise such as in data acquisition systems where remote sensing of input variables is required.

After completing this section, you should be able to

- **Explain and analyze the operation of an instrumentation amplifier**
- Show how op-amps are connected to form an instrumentation amplifier
  - Set the voltage gain
  - Explain how a capacitor charges
  - Discuss an application
- Describe the features of a specific instrumentation amplifier
  - Discuss the AD622
  - Calculate the value for the gain-setting resistor
  - Describe how the gain varies with frequency
- Discuss noise effects in an instrumentation amplifier
  - Define *guarding*
  - Describe the AD522 instrumentation amplifier with a guard output

An **instrumentation amplifier** is a differential voltage-gain device that amplifies the difference between the voltages existing at its two input terminals. The main purpose of an instrumentation amplifier is to amplify small signals that may be riding on large common-mode voltages. The key characteristics are high input impedance, high common-mode rejection, low output offset, and low output impedance. The basic instrumentation amplifier is an integrated circuit that internally has three operational amplifiers and several resistors. The voltage gain is usually set with an external resistor.

A basic instrumentation amplifier is shown in Figure 14–1. Op-amps A1 and A2 are noninverting configurations that provide high input impedance and voltage gain. Op-amp A3 is used as a unity-gain differential amplifier with high-precision resistors that are all equal in value ($R_3 = R_4 = R_5 = R_6$).



◀ FIGURE 14–1

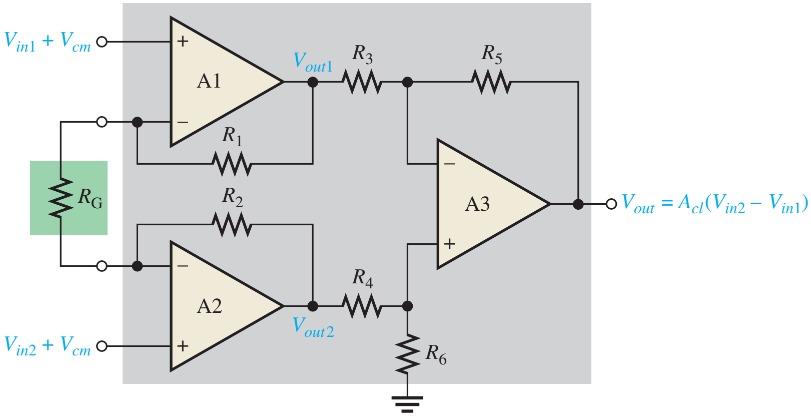
The basic instrumentation amplifier using three op-amps.

The gain-setting resistor, R_G, is connected externally as shown in Figure 14–2. Op-amp A1 receives the differential input signal V_{in1} on its noninverting (+) input and amplifies this signal with a voltage gain of

$$A_v = 1 + \frac{R_1}{R_G}$$

FIGURE 14–2

The basic instrumentation amplifier with an external gain-setting resistor R_G. Differential and common-mode signals are indicated.



Op-amp A1 also has V_{in2} as an input signal to its inverting (−) input through op-amp A2 and the path formed by R_2 and R_G. The input signal V_{in2} is amplified by op-amp A1 with a voltage gain of

$$A_v = \frac{R_1}{R_G}$$

The overall closed-loop gain of the instrumentation amplifier is

Equation 14–1

$$\mathbf{A_{cl} = 1 + \frac{2R}{R_G}}$$

where $R_1 = R_2 = R$. Equation 14–1 shows that the gain of the instrumentation amplifier can be set by the value of the external resistor R_G when R_1 and R_2 have a known fixed value. See "Derivations of Selected Equations" at www.pearsonhighered.com/floyd for the derivation.

The external gain-setting resistor R_G can be calculated for a desired voltage gain by applying Equation 14–1.

Equation 14–2

$$\mathbf{R_G = \frac{2R}{A_{cl} - 1}}$$

Instrumentation amplifiers in which the gain is set to specific values using a binary input instead of a resistor are also available.

EXAMPLE 14–1

Determine the value of the external gain-setting resistor R_G for a certain IC instrumentation amplifier with $R_1 = R_2 = 25\ \text{k}\Omega$. The closed-loop voltage gain is to be 500.

Solution

$$R_G = \frac{2R}{A_{cl} - 1} = \frac{50\ \text{k}\Omega}{500 - 1} \cong \mathbf{100\ \Omega}$$

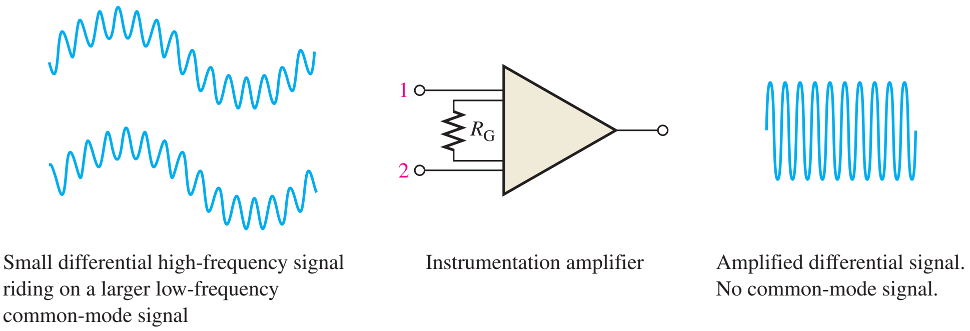
Related Problem[*] What value of external gain-setting resistor is required for an instrumentation amplifier with $R_1 = R_2 = 39\ \text{k}\Omega$ to produce a gain of 325?

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Applications

The instrumentation amplifier is normally used to measure small differential signal voltages that are superimposed on a common-mode voltage often much larger than the signal voltage. Applications include situations where a quantity is sensed by a remote device, such as a temperature- or pressure-sensitive transducer, and the resulting small electrical signal is sent over a long line subject to electrical noise that produces common-mode voltages in the line. The instrumentation amplifier at the end of the line must amplify the small signal from the remote sensor and reject the large common-mode voltage. Figure 14–3 illustrates this.

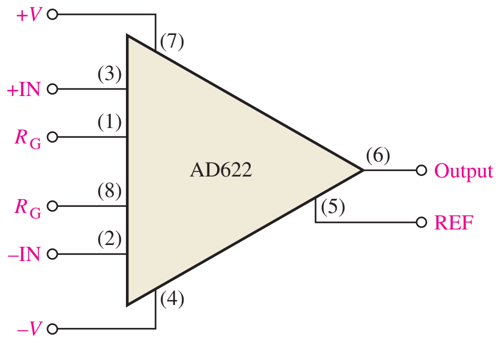

1
2
R_G
Small differential high-frequency signal riding on a larger low-frequency common-mode signal
Instrumentation amplifier
Amplified differential signal. No common-mode signal.

◀ **FIGURE 14–3**

Illustration of the rejection of large common-mode voltages and the amplification of smaller signal voltages by an instrumentation amplifier.

A Specific Instrumentation Amplifier

Now that you have the basic idea of how an instrumentation amplifier works, let's look at a specific device. A representative device, the AD622, is shown in Figure 14–4 where IC pin numbers are given for reference. This instrumentation amplifier is based on the design using three op-amps that was shown in Figure 14–1.


+V
(7)
+IN
(3)
R_G
(1)
AD622
(6)
Output
R_G
(8)
(5)
REF
–IN
(2)
(4)
–V

◀ **FIGURE 14–4**

The AD622 instrumentation amplifier.

Some of the features of the AD622 are as follows. The voltage gain can be adjusted from 2 to 1000 with an external resistor R_G. There is unity gain with no external resistor. The input impedance is 10 GΩ. The common-mode rejection ratio (CMRR) has a minimum value of 66 dB. Recall that a higher CMRR means better rejection of common-mode voltages. The AD622 has a bandwidth of 800 kHz at a gain of 10 and a slew rate of 1.2 V/μs.

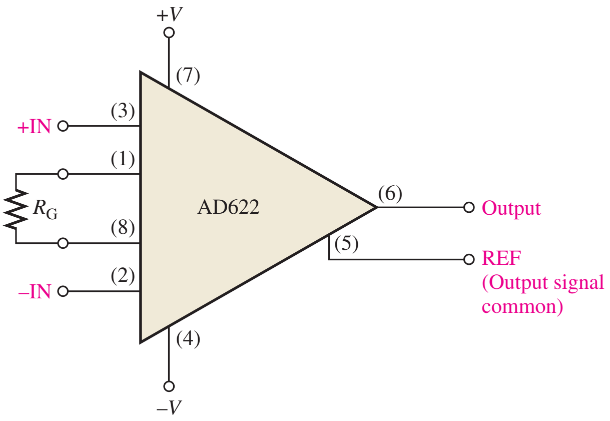
Setting the Voltage Gain For the AD622, an external resistor must be used to achieve a voltage gain greater than unity, as indicated in Figure 14–5. Resistor R_G is connected between the R_G terminals (pins 1 and 8). No resistor is required for unity. R_G is selected for the desired gain based on the following formula:

$$R_G = \frac{50.5\ \text{k}\Omega}{A_v - 1}$$

Notice that this formula is the same as Equation 14–2 for the three-op-amp configuration with an external R_G where the internal resistors R_1 and R_2 are each 25.25 kΩ.

FIGURE 14–5

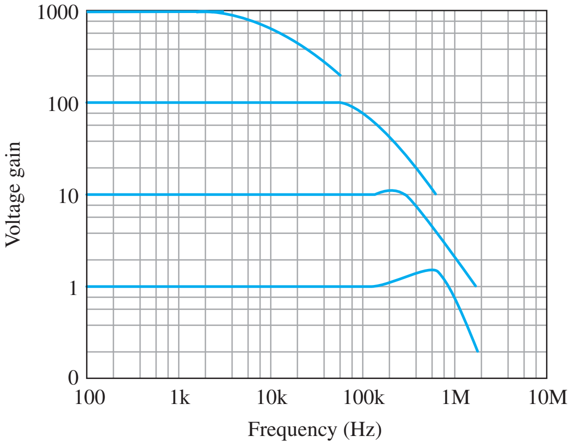
The AD622 with a gain-setting resistor.


+V
(7)
(3)
+IN
(1)
R_G
(8)
(2)
–IN
AD622
(6)
Output
(5)
REF
(Output signal common)
(4)
–V

Gain versus Frequency The graph in Figure 14–6 shows how the gain varies with frequency for gains of 1, 10, 100, and 1000. As the curves show, the bandwidth decreases as the gain increases.

FIGURE 14–6

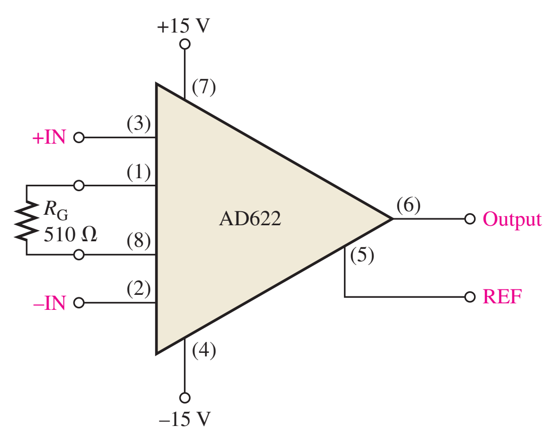
Gain versus frequency for the AD622 instrumentation amplifier.



EXAMPLE 14–2

Calculate the voltage gain and determine the bandwidth using the graph in Figure 14–6 for the instrumentation amplifier in Figure 14–7.

FIGURE 14–7


+15 V
(7)
(3)
+IN
(1)
R_G
510 Ω
(8)
(2)
–IN
AD622
(6)
Output
(5)
REF
(4)
–15 V

Solution Determine the voltage gain as follows:

$$R_G = \frac{50.5\text{ k}\Omega}{A_v - 1}$$

$$A_v - 1 = \frac{50.5\text{ k}\Omega}{R_G}$$

$$A_v = \frac{50.5\text{ k}\Omega}{510\ \Omega} + 1 = \mathbf{100}$$

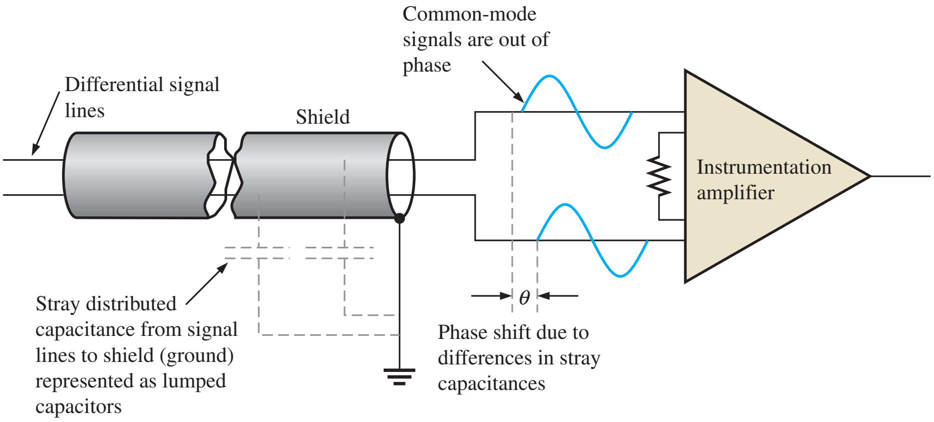
Determine the approximate bandwidth from the graph at the point where the curve begins to drop in Figure 14–6.

$$BW \approx \mathbf{80\text{ kHz}}$$

Related Problem Modify the circuit in Figure 14–7 for a gain of approximately 45.

Noise Effects in Instrumentation Amplifier Applications

Various types of transducers are used to sense temperature, strain, pressure, and other parameters in many types of applications. Instrumentation amplifiers are generally used to process the small voltages produced by a transducer and often are used in noisy industrial environments where long cables connect the transducer output to the amplifier inputs. Noise in the form of common-mode signals picked up from external sources can be minimized, but not totally eliminated, by using coaxial cable in which the differential signal wires are surrounded by a metal mesh sheathing called a *shield.* As you know, in an electrically noisy environment any common-mode signals that are induced on the signal lines are rejected because both inputs to the amplifier have the same common-mode signal. However, when a shielded cable is used, there are stray capacitances distributed along its length between each signal line and the shield. The differences in these stray capacitances, particularly at higher frequencies, result in a phase shift between the two common-mode signals, as illustrated in Figure 14–8. The result is a degradation in the common-mode rejection of the amplifier because the two signals are no longer in phase and do not completely cancel so that a differential voltage is created at the amplifier inputs.


Common-mode signals are out of phase
Differential signal lines
Shield
Instrumentation amplifier
Stray distributed capacitance from signal lines to shield (ground) represented as lumped capacitors
θ
Phase shift due to differences in stray capacitances

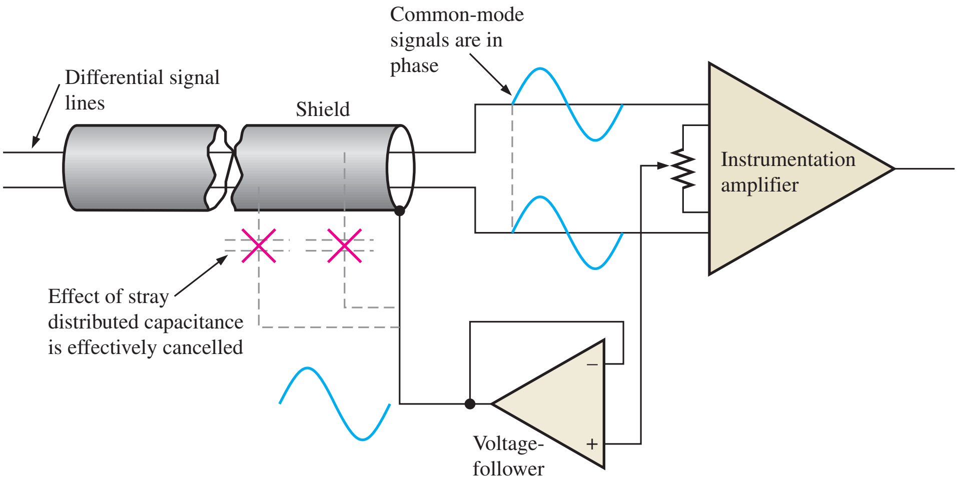
◀ **FIGURE 14–8**

Degradation of common-mode rejection in a shielded cable connection due to unwanted phase shifts.

Shield Guard **Guarding** is a technique to reduce the effects of noise on the common-mode operation of an instrumentation amplifier operating in critical environments by connecting the common-mode voltage to the shield of a coaxial cable. The common-mode signal is fed back to the shield by a voltage-follower stage, as shown in Figure 14–9. The purpose is to eliminate voltage differences between the signal lines and the shield, virtually eliminating leakage currents and cancelling the effects of the distributed capacitances so that the common-mode voltages are the same in both lines.

FIGURE 14–9

Instrumentation amplifier with shield guard to prevent degradation of the common-mode rejection.

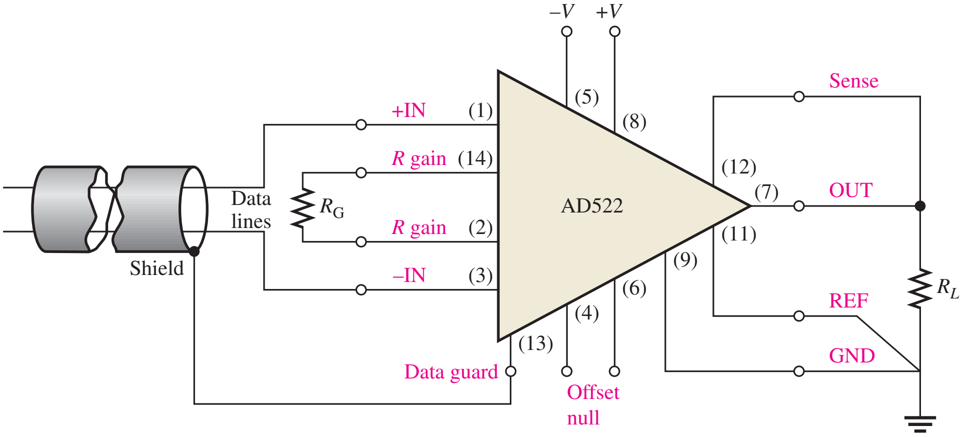

Common-mode signals are in phase
Differential signal lines
Shield
Instrumentation amplifier
Effect of stray distributed capacitance is effectively cancelled
Voltage-follower
−
+

The voltage-follower is a low-impedance source that drives the common-mode signal onto the shield to eliminate the voltage difference between the signal lines and the shield. When the voltage between each signal line and the shield is zero, the leakage currents are also zero and the capacitive reactances become infinitely large. An infinitely large X_C implies a zero capacitance.

A Specific Instrumentation Amplifier with a Guard Output Most instrumentation amplifiers can be configured externally to provide a shield guard driver. Certain IC amplifiers, however, provide an internally generated guard output that is intended for very critical environments. An example is the AD522, shown in Figure 14–10, which is a precision IC instrumentation amplifier designed for applications requiring high accuracy under worst-case operating conditions and with very small signals. The pin labeled DATA GUARD is the shield-guard output.

FIGURE 14–10

The AD522 instrumentation amplifier in a typical configuration.


−V
+V
(5)
(8)
Sense
+IN
(1)
R gain
(14)
(12)
(7)
OUT
Data lines
R_G
AD522
R gain
(2)
(11)
Shield
−IN
(3)
(9)
(6)
R_L
(4)
REF
(13)
GND
Data guard
Offset null

SECTION 14–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What is the main purpose of an instrumentation amplifier and what are three of its key characteristics?
2. What components do you need to construct a basic instrumentation amplifier?
3. How is the gain determined in an instrumentation amplifier?
4. In a certain AD622 configuration, $R_G = 10\ \text{k}\Omega$. What is the voltage gain?
5. Describe the purpose of a shield guard.

14–2 ISOLATION AMPLIFIERS

An isolation amplifier provides dc isolation between input and output. It is used for the protection of human life or sensitive equipment in those applications where hazardous power-line leakage or high-voltage transients are possible. The principal areas of application are in medical instrumentation, power plant instrumentation, industrial processing, and automated testing.

After completing this section, you should be able to

- **Explain and analyze the operation of an isolation amplifier**
- Describe a basic capacitor-coupled isolation amplifier
  - Show the block diagram
  - Define *modulation*
  - Discuss the modulation process
  - Describe the ISO124 as an example of an isolation amplifier
- Describe a transformer-coupled isolation amplifier
  - Discuss the 3656KG
  - Establish the voltage gain
  - Describe a medical application

A Basic Capacitor-Coupled Isolation Amplifier

An **isolation amplifier** is a device that consists of two electrically isolated stages. The input stage and the output stage are separated from each other by an isolation barrier so that a signal must be processed in order to be coupled across the isolation barrier. Some isolation amplifiers use optical coupling or transformer coupling to provide isolation between the stages. However, many modern isolation amplifiers use capacitive coupling for isolation. Each stage has separate supply voltages and grounds so that there are no common electrical paths between them. A simplified block diagram for a typical isolation amplifier is shown in Figure 14–11. Notice two different ground symbols are used to reinforce the concept of stage separation.

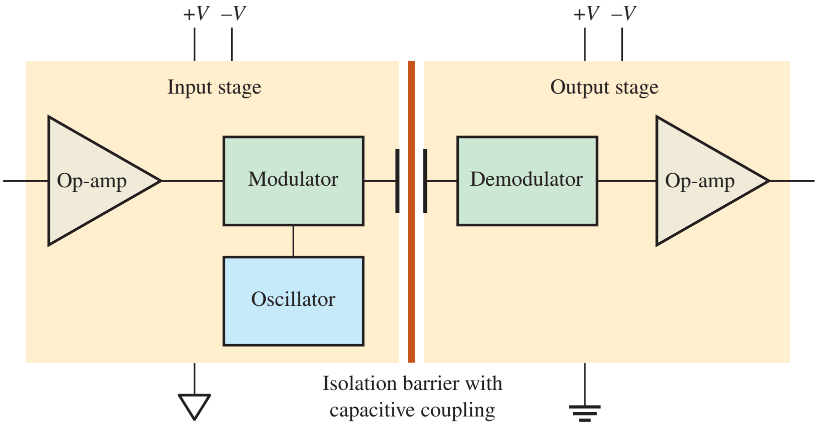


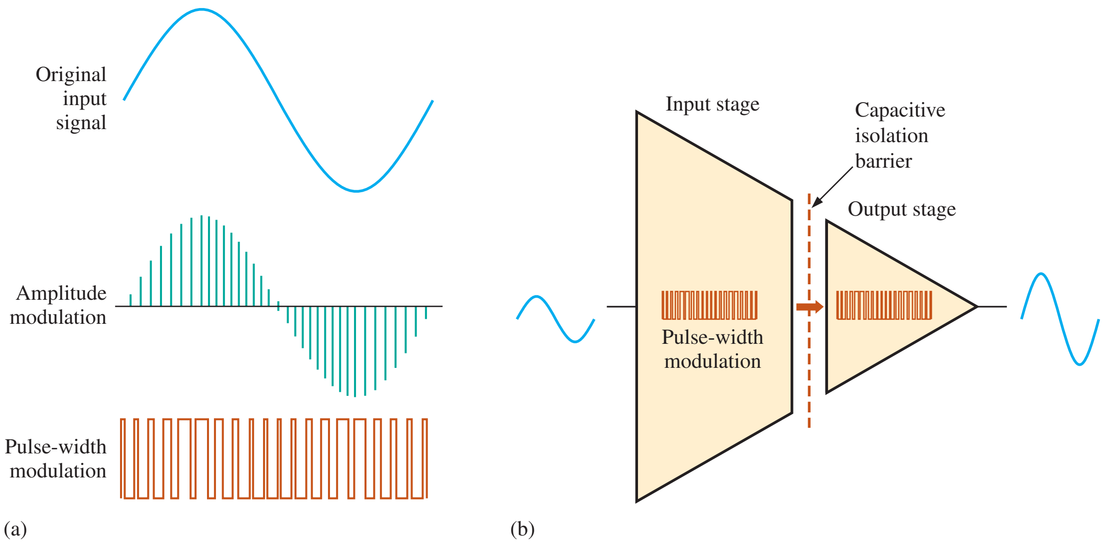
FIGURE 14–11

Simplified block diagram of a typical isolation amplifier.

The input stage consists of an amplifier, an oscillator, and a modulator. **Modulation** is the process of allowing a signal containing information to modify a characteristic of another signal, such as amplitude, frequency, or pulse width, so that the information in the first signal is also contained in the second. In this case, the modulator uses a high-frequency square-wave oscillator to modify the original signal. A small-value capacitor in the isolation barrier is used to couple the lower-frequency modulated signal or dc voltage from the input to the output. Without modulation, prohibitively high-value capacitors would be necessary with a resulting degradation in the isolation between the stages.

The output stage consists of a demodulator that extracts the original input signal from the modulated signal so that the original signal from the input stage is back to its original form.

The high-frequency oscillator output in Figure 14–11 can be either amplitude or pulse-width modulated by the signal from the input amplifier (oscillators are covered in Chapter 16). In amplitude modulation, the amplitude of the oscillator output is varied corresponding to the variations of the input signal, as indicated in Figure 14–12(a), which uses one cycle of a sine wave for illustration. In pulse-width modulation, the duty cycle of the oscillator output is varied by changing the pulse width corresponding to the variations of the input signal. An isolation amplifier using pulse-width modulation is represented in Figure 14–12(b).



▲ FIGURE 14–12

Modulation.

Although it uses a relatively complex process internally, the isolation amplifier is still just an amplifier and is simple to use. When separate dc supply voltages and an input signal are applied, an amplified output signal is the result. The isolation function itself is an unseen process.

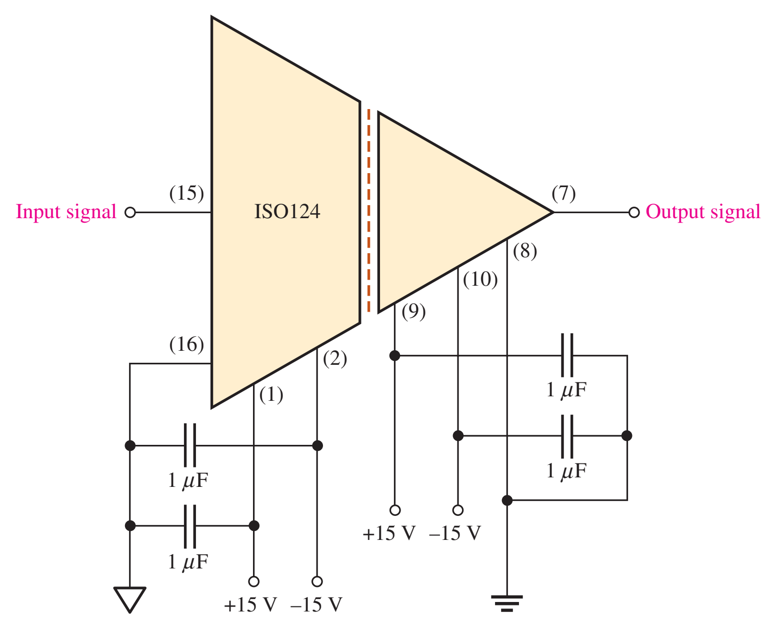
EXAMPLE 14–3

The ISO124 is an integrated circuit isolation amplifier. It has a voltage gain of 1 and operates on positive and negative dc supply voltages for both stages. This device uses pulse-width modulation (sometimes called duty cycle modulation) with a frequency of 500 kHz. It is recommended that the supply voltages be decoupled with external capacitors to reduce noise. Show the appropriate connections.

Solution The manufacturer recommends a 1 μF tantalum capacitor (for low leakage) from each dc power supply pin to ground. This is shown in Figure 14–13 where the supply voltages are ±15 V.

FIGURE 14–13

Basic signal and power connections for an ISO124 isolation amplifier.


Input signal
(15)
ISO124
(7)
Output signal
(8)
(10)
(9)
(16)
(2)
(1)
1 μF
1 μF
1 μF
1 μF
+15 V
−15 V
+15 V
−15 V

Related Problem The output signal may have some ripple introduced by the demodulation process. How could this ripple be removed?

A Transformer-Coupled Isolation Amplifier

The Texas Instruments (Burr-Brown) 3656KG is an example of an isolation amplifier that uses transformer coupling to isolate the two stages. Unlike the ISO124, which has a fixed unity gain, the 3656KG provides for external gain adjustment of both stages. A diagram of the 3656KG with external gain resistors and decoupling capacitors is shown in Figure 14–14.

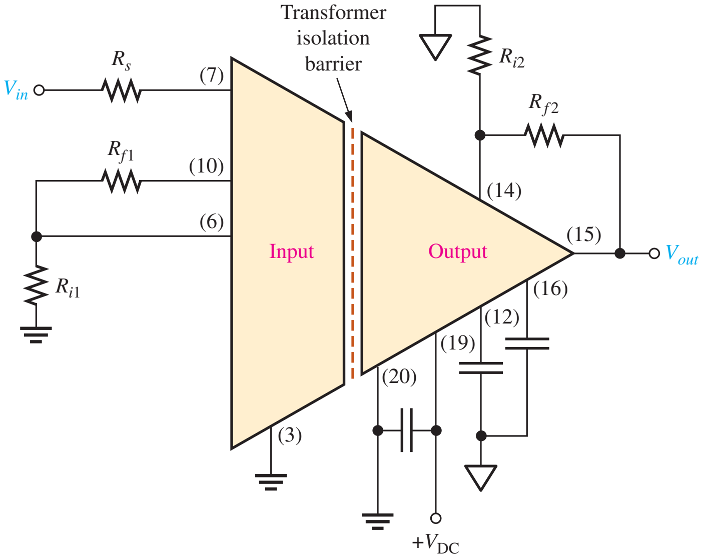

Transformer isolation barrier
V_{in}
R_s
(7)
R_{f1}
(10)
(6)
R_{i1}
Input
Output
(3)
R_{i2}
R_{f2}
(14)
(15)
V_{out}
(16)
(12)
(19)
(20)
$+V_{DC}$

FIGURE 14–14

The 3656KG isolation amplifier.

The voltage gains of both the input stage and the output stage can be set with external resistors connected as shown in the figure. The gain of the input stage is

Equation 14–3

$$\boldsymbol{A_{v1} = \frac{R_{f1}}{R_{i1}} + 1}$$

The gain of the output stage is

Equation 14–4

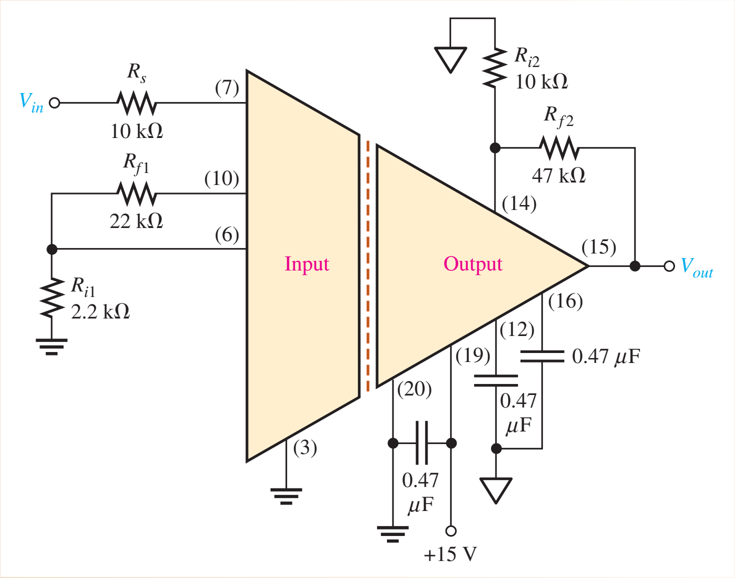
$$\boldsymbol{A_{v2} = \frac{R_{f2}}{R_{i2}} + 1}$$

The total amplifier gain is the product of the gains of the input and output stages.

$$A_{v(tot)} = A_{v1}A_{v2}$$

EXAMPLE 14–4

Determine the total voltage gain of the 3656KG isolation amplifier in Figure 14–15.


V_{in}
R_s
10 kΩ
(7)
R_{f1}
22 kΩ
(10)
(6)
R_{i1}
2.2 kΩ
Input
(3)
R_{i2}
10 kΩ
R_{f2}
47 kΩ
(14)
Output
(15)
V_{out}
(16)
(12)
0.47 μF
(19)
(20)
0.47 μF
0.47 μF
+15 V

▲ FIGURE 14–15

Solution The voltage gain of the input stage is

$$A_{v1} = \frac{R_{f1}}{R_{i1}} + 1 = \frac{22\text{ k}\Omega}{2.2\text{ k}\Omega} + 1 = 10 + 1 = 11$$

The voltage gain of the output stage is

$$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1 = \frac{47\text{ k}\Omega}{10\text{ k}\Omega} + 1 = 4.7 + 1 = 5.7$$

The total voltage gain of the isolation amplifier is

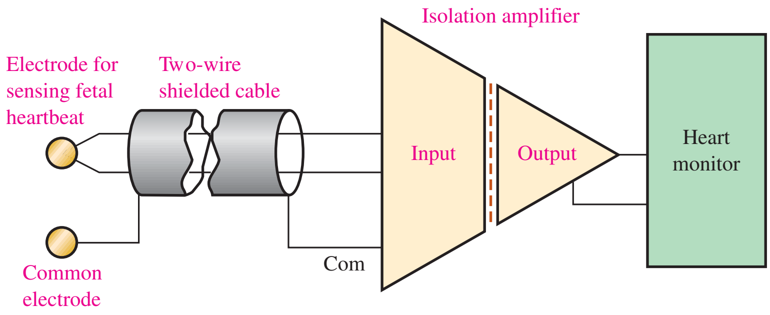
$$A_{v(tot)} = A_{v1}A_{v2} = (11)(5.7) = \mathbf{62.7}$$

Related Problem Select resistor values in Figure 14–15 that will produce a total voltage gain of approximately 100.

Applications

As previously mentioned, the isolation amplifier is used in applications that require no common grounds between a transducer and the processing circuits where interfacing to sensitive equipment is required. In chemical, nuclear, and metal-processing industries, for example, millivolt signals typically exist in the presence of large common-mode voltages that can be in the kilovolt range. In this type of environment, the isolation amplifier can amplify small signals from very noisy equipment and provide a safe output to sensitive equipment such as computers.

Another important application is in various types of medical equipment. In medical applications where body functions such as heart rate and blood pressure are monitored, the very small monitored signals are combined with large common-mode signals, such as 60 Hz power-line pickup from the skin. In these situations, without isolation, dc leakage or equipment failure could be fatal. Figure 14–16 shows a simplified diagram of an isolation amplifier in a cardiac-monitoring application. In this situation, heart signals, which are very small, are combined with much larger common-mode signals caused by muscle noise, electrochemical noise, residual electrode voltage, and 60 Hz power-line pickup from the skin.



▲ FIGURE 14–16

Fetal heartbeat monitoring using an isolation amplifier.

The monitoring of the fetal heartbeat, as illustrated, is the most demanding type of cardiac monitoring because in addition to the fetal heartbeat that typically generates 50 μV, there is also the mother's heartbeat that typically generates 1 mV. The common-mode voltages can run from about 1 mV to about 100 mV. The CMR (common-mode rejection) of the isolation amplifier separates the signal of the fetal heartbeat from that of the mother's heartbeat and from those common-mode signals. Therefore, the signal from the fetal heartbeat is essentially all that the amplifier sends to the monitoring equipment.

SECTION 14–2 CHECKUP

1. In what types of applications are isolation amplifiers used?
2. What are the two stages in a typical isolation amplifier and what is the purpose of having two stages?
3. How are the stages in an isolation amplifier connected?
4. What is the purpose of the oscillator in an isolation amplifier?

14–3 OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS (OTAS)

Conventional op-amps are, as you know, primarily voltage amplifiers in which the output voltage equals the gain times the input voltage. The **operational transconductance amplifier (OTA)** is primarily a voltage-to-current amplifier in which the output current equals the gain times the input voltage.

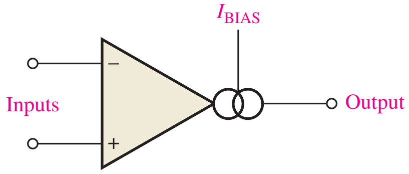
After completing this section, you should be able to

- ❏ **Explain and analyze the operation of an operation transconductance amplifier (OTA)**
  - ◆ Identify the OTA schematic symbol
- ❏ Discuss the gain of an OTA
  - ◆ Define *transconductance* ◆ Explain how the transconductance is a function of bias current
- ❏ Describe some OTA circuits
  - ◆ Discuss the OTA as an inverting amplifier ◆ Discuss the OTA with resistance-controlled gain ◆ Discuss the OTA with voltage-controlled gain
- ❏ Describe the LM13700 as an example of a specific OTA
  - ◆ Describe how the input and output resistances change with bias current
- ❏ Discuss two OTA applications
  - ◆ Describe an amplitude modulator ◆ Describe a Schmitt trigger

Figure 14–17 shows the symbol for an OTA. The double circle symbol at the output represents an output current source that is dependent on a bias current. Like the conventional op-amp, the OTA has two differential input terminals, a high input impedance, and a high CMRR. Unlike the conventional op-amp, the OTA has a bias-current input terminal, a high output impedance, and no fixed open-loop voltage gain.

▶ FIGURE 14–17

Symbol for an operational transconductance amplifier (OTA).



Transconductance

The **transconductance** of an electronic device is the ratio of the output current to the input voltage. For an OTA, voltage is the input variable and current is the output variable; therefore, the ratio of output current to input voltage is also its gain. Consequently, the voltage-to-current gain of an OTA is the transconductance, g_m.

Equation 14–5

$$g_m = \frac{I_{out}}{V_{in}}$$

In an OTA, the transconductance is dependent on a constant (K) times the bias current (I_{BIAS}), as indicated in Equation 14–6. The value of the constant is dependent on the internal circuit design.

Equation 14–6

$$g_m = KI_{BIAS}$$

The output current is controlled by the input voltage and the bias current as shown by the following formula:

$$I_{out} = g_m V_{in} = KI_{BIAS}V_{in}$$

The relationship of the transconductance and the bias current in an OTA is an important characteristic. The graph in Figure 14–18 illustrates a typical relationship. Notice that the transconductance increases linearly with the bias current. The constant of proportionality, K, is the slope of the line. In this case, K is approximately 16 μS/μA.

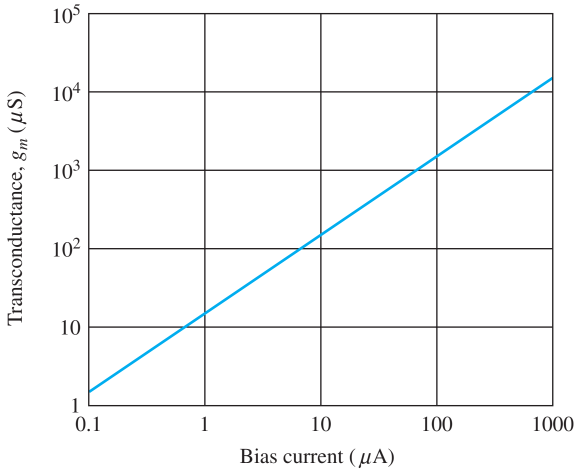


FIGURE 14–18

Example of a transconductance versus bias current graph for a typical OTA.

EXAMPLE 14–5 If an OTA has a $g_m = 1000\ \mu\text{S}$, what is the output current when the input voltage is 25 mV?

Solution

$$I_{out} = g_m V_{in} = (1000\ \mu\text{S})(25\ \text{mV}) = \mathbf{25\ \mu A}$$

Related Problem Based on $K \cong 16\ \mu\text{S}/\mu\text{A}$, calculate the approximate bias current required to produce $g_m = 1000\ \mu\text{S}$.

Basic OTA Circuits

Figure 14–19 shows the OTA used as an inverting amplifier with a fixed voltage gain. The voltage gain is set by the transconductance and the load resistance as follows.

$$V_{out} = I_{out}R_L$$

Dividing both sides by V_{in},

$$\frac{V_{out}}{V_{in}} = \left(\frac{I_{out}}{V_{in}}\right)R_L$$

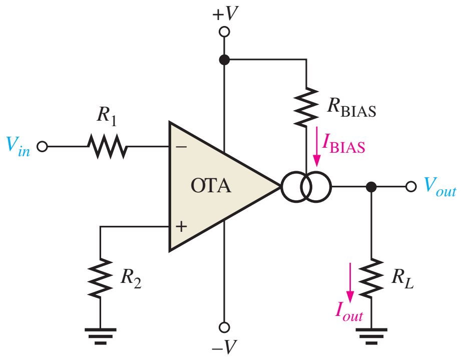


FIGURE 14–19

An OTA as an inverting amplifier with a fixed voltage gain.

Since V_{out}/V_{in} is the voltage gain and $I_{out}/V_{in} = g_m$,

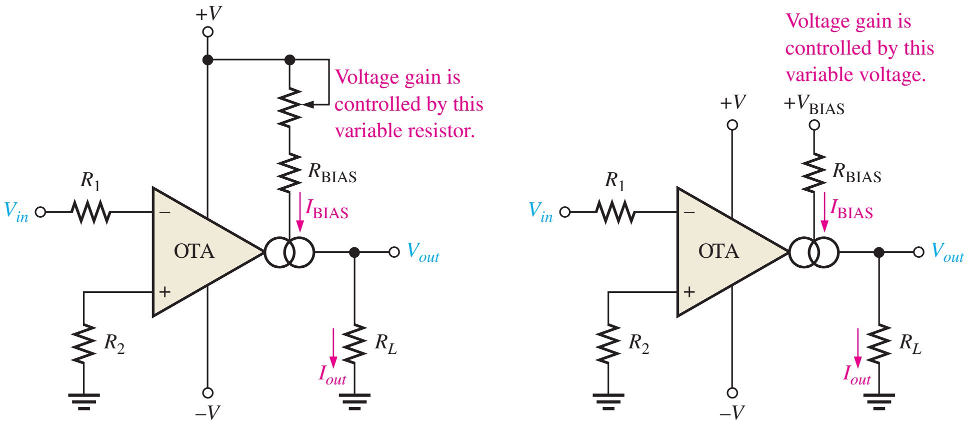
$$A_v = g_m R_L$$

The transconductance of the amplifier in Figure 14–19 is determined by the amount of bias current, which is set by the dc supply voltages and the bias resistor R_{BIAS}.

One of the most useful features of an OTA is that the voltage gain can be controlled by the amount of bias current. This can be done manually, as shown in Figure 14–20(a), by using a variable resistor in series with R_{BIAS} in the circuit of Figure 14–19. By changing the resistance, you can produce a change in I_{BIAS}, which changes the transconductance. A change in the transconductance changes the voltage gain. The voltage gain can also be controlled with an externally applied variable voltage, as shown in Figure 14–20(b). A variation in the applied bias voltage causes a change in the bias current.

▶ **FIGURE 14–20**

An OTA as an inverting amplifier with a variable-voltage gain.



+V
Voltage gain is controlled by this variable resistor.
R_BIAS
I_BIAS
R_1
V_in
OTA
V_out
R_2
R_L
I_out
–V
Voltage gain is controlled by this variable voltage.
+V
+V_BIAS
R_BIAS
I_BIAS
R_1
V_in
OTA
V_out
R_2
R_L
I_out
–V

(a) Amplifier with resistance-controlled gain

(b) Amplifier with voltage-controlled gain

A Specific OTA

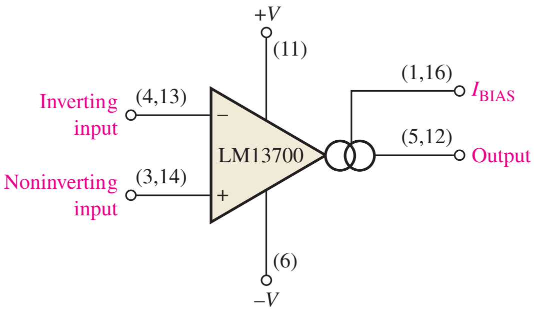
The LM13700 is a typical OTA and serves as a representative device. The LM13700 is a dual-device package containing two OTAs and buffer circuits. Figure 14–21 shows the pin configuration using a single OTA in the package. The maximum dc supply voltages are ±18 V, and its transconductance characteristic happens to be the same as indicated by the graph in Figure 14–18. For an LM13700, the bias current is determined by the following formula:

$$I_{BIAS} = \frac{+V_{BIAS} - (-V) - 1.4\text{ V}}{R_{BIAS}}$$

The 1.4 V is due to the internal circuit where a base-emitter junction and a diode connect the external R_{BIAS} with the negative supply voltage $(-V)$. The positive bias voltage, $+V_{BIAS}$, may be obtained from the positive supply voltage, $+V$.

▶ **FIGURE 14–21**

An LM13700 OTA. There are two in an IC package. The buffer transistors are not shown. Pin numbers for both OTAs are given in parentheses.



+V
(11)
(1,16)
I_BIAS
Inverting input
(4,13)
(5,12)
Output
LM13700
Noninverting input
(3,14)
(6)
–V

Not only does the transconductance of an OTA vary with bias current, but so do the input and output resistances. Both the input and output resistances decrease as the bias current increases, as shown in Figure 14–22.

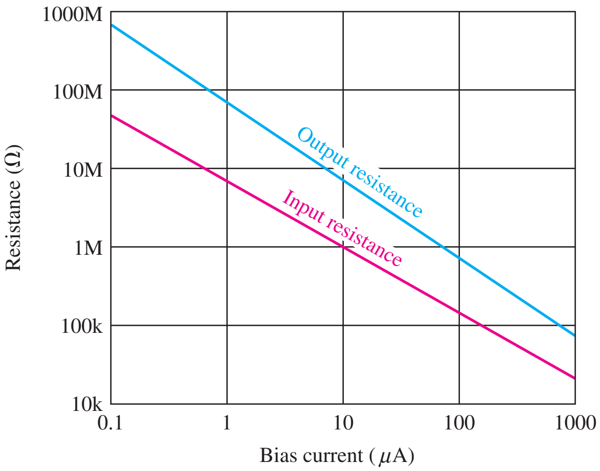


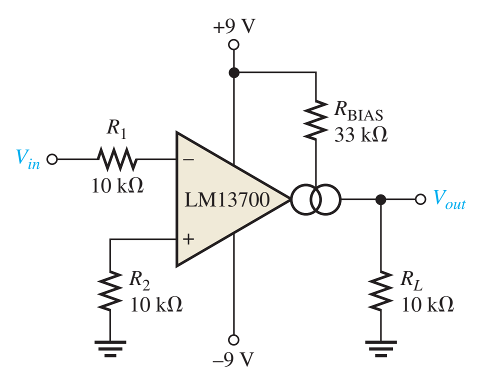
FIGURE 14–22

Example of input and output resistances versus bias current.

EXAMPLE 14–6

The OTA in Figure 14–23 is connected as an inverting fixed-gain amplifier where $+V_{BIAS} = +V$. Determine the approximate voltage gain.

FIGURE 14–23



Solution Calculate the bias current as follows:

$$I_{BIAS} = \frac{+V_{BIAS} - (-V) - 1.4\text{ V}}{R_{BIAS}} = \frac{9\text{ V} - (-9\text{ V}) - 1.4\text{ V}}{33\text{ k}\Omega} = 503\ \mu\text{A}$$

Using $K \cong 16\ \mu\text{S}/\mu\text{A}$ from the graph in Figure 14–18, the value of transconductance corresponding to $I_{BIAS} = 503\ \mu\text{A}$ is approximately

$$g_m = KI_{BIAS} \cong (16\ \mu\text{S}/\mu\text{A})(503\ \mu\text{A}) = 8.05 \times 10^3\ \mu\text{S}$$

Using this value of g_m, calculate the voltage gain.

$$A_v = g_m R_L \cong (8.05 \times 10^3\ \mu\text{S})(10\text{ k}\Omega) = \mathbf{80.5}$$

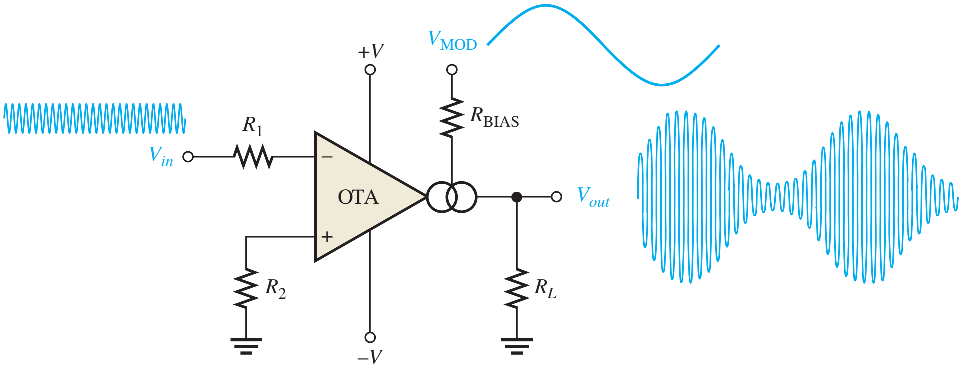
Related Problem If the OTA in Figure 14–23 is operated with dc supply voltages of ±12 V, will this change the voltage gain and, if so, to what value?

Two OTA Applications

Amplitude Modulator Figure 14–24 illustrates an OTA connected as an amplitude modulator. The voltage gain is varied by applying a modulation voltage to the bias input. When a constant-amplitude input signal is applied, the amplitude of the output

FIGURE 14–24

The OTA as an amplitude modulator.



signal will vary according to the modulation voltage on the bias input. The gain is dependent on bias current, and bias current is related to the modulation voltage by the following relationship:

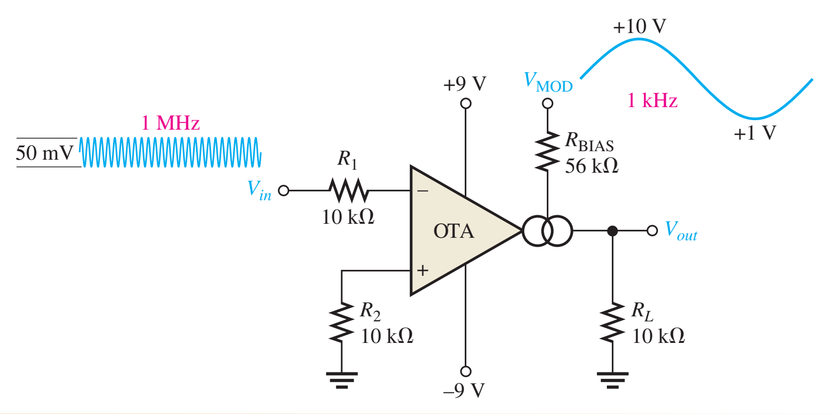
$$I_{BIAS} = \frac{V_{MOD} - (-V) - 1.4\text{ V}}{R_{BIAS}}$$

This modulating action is shown in Figure 14–24 for a higher-frequency sinusoidal input voltage and a lower-frequency sinusoidal modulating voltage.

EXAMPLE 14–7

The input to the OTA amplitude modulator in Figure 14–25 is a 50 mV peak-to-peak, 1 MHz sine wave. Determine the output signal, given the modulation voltage shown is applied to the bias input.

FIGURE 14–25



Solution The maximum voltage gain is when I_{BIAS}, and thus g_m, is maximum. This occurs at the maximum peak of the modulating voltage, V_{MOD}.

$$I_{BIAS(max)} = \frac{V_{MOD(max)} - (-V) - 1.4\text{ V}}{R_{BIAS}} = \frac{10\text{ V} - (-9\text{ V}) - 1.4\text{ V}}{56\text{ k}\Omega} = 314\ \mu\text{A}$$

From the graph in Figure 14–18, the constant K is approximately 16 μS/μA.

$$\begin{aligned} g_m &= KI_{BIAS(max)} \cong (16\ \mu\text{S}/\mu\text{A})(314\ \mu\text{A}) = 5.02\text{ mS} \\ A_{v(max)} &= g_mR_L \cong (5.02\text{ mS})(10\text{ k}\Omega) = 50.2 \\ V_{out(max)} &= A_{v(max)}V_{in} \cong (50.2)(50\text{ mV}) = 2.51\text{ V} \end{aligned}$$

Calculate the minimum output voltage as follows:

$$I_{\text{BIAS(min)}} = \frac{V_{\text{MOD(min)}} - (-V) - 1.4\text{ V}}{R_{\text{BIAS}}} = \frac{1\text{ V} - (-9\text{ V}) - 1.4\text{ V}}{56\text{ k}\Omega} = 154\ \mu\text{A}$$

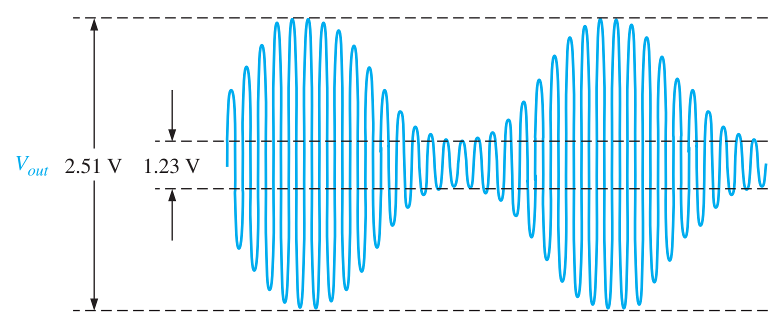
$$g_m = KI_{\text{BIAS(min)}} \cong (16\ \mu\text{S}/\mu\text{A})(154\ \mu\text{A}) = 2.46\text{ mS}$$

$$A_{v(min)} = g_m R_L \cong (2.46\text{ mS})(10\text{ k}\Omega) = 24.6$$

$$V_{out(min)} = A_{v(min)}V_{in} \cong (24.6)(50\text{ mV}) = 1.23\text{ V}$$

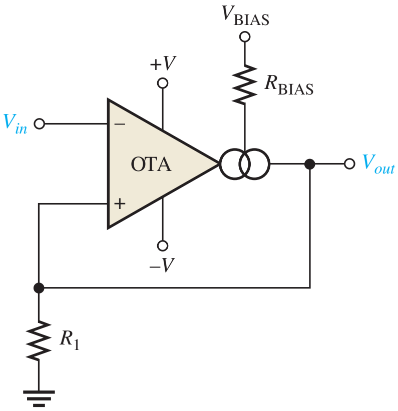
The resulting output voltage is shown in Figure 14–26.

▶ **FIGURE 14–26**



Related Problem Repeat this example with the sinusoidal modulating signal replaced by a square wave with the same maximum and minimum levels and a bias resistor of 39 kΩ.

Schmitt Trigger Figure 14–27 shows an OTA used in a Schmitt-trigger configuration. Basically, a Schmitt trigger is a comparator with hysteresis where the input voltage is large enough to drive the device into its saturated states. When the input voltage exceeds a certain threshold value or trigger point, the device switches to one of its saturated output states. When the input falls below another threshold value, the device switches to its other saturated output state.



◀ **FIGURE 14–27**

The OTA as a Schmitt trigger.

In the case of the OTA Schmitt trigger, the threshold levels are set by the current through resistor R_1. The maximum output current in an OTA equals the bias current. Therefore, in the saturated output states, $I_{out} = I_{\text{BIAS}}$. The maximum positive output voltage is $I_{out}R_1$, and this voltage is the positive threshold value or upper trigger point. When the input voltage exceeds this value, the output switches to its maximum negative voltage, which is $-I_{out}R_1$. Since $I_{out} = I_{BIAS}$, the trigger points can be controlled by the bias current. Figure 14–28 illustrates this operation.

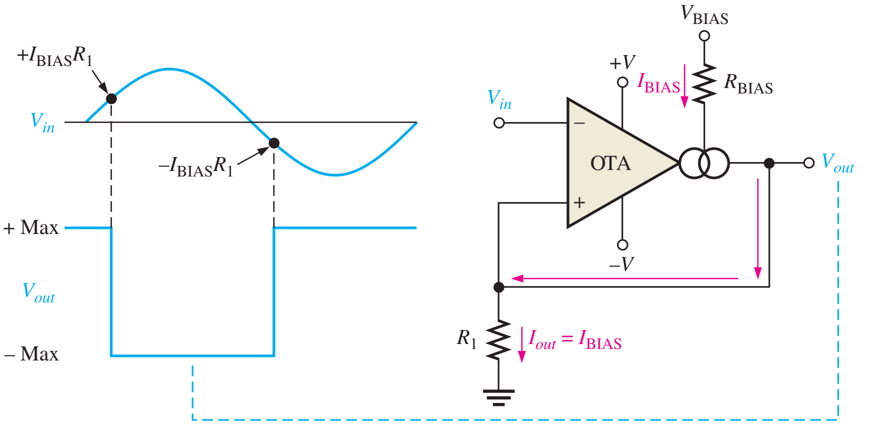


FIGURE 14–28

Basic operation of the OTA Schmitt trigger.

SECTION 14–3 CHECKUP

1. What does OTA stand for?
2. If the bias current in an OTA is increased, does the transconductance increase or decrease?
3. What happens to the voltage gain if the OTA is connected as a fixed-voltage amplifier and the supply voltages are increased?
4. What happens to the voltage gain if the OTA is connected as a variable-gain voltage amplifier and the voltage at the bias terminal is decreased?

14–4 LOG AND ANTILOG AMPLIFIERS

Log and antilog amplifiers are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. They are often used in high-frequency communication systems, including fiber optics, for processing wide dynamic range signals.

After completing this section, you should be able to

- **Explain and analyze the operation of log and antilog amplifiers**
  - Define *logarithm*
- Describe the basic log amplifier
  - Define *natural logarithm* ◆ Explain how a diode provides a logarithmic characteristic ◆ Describe the operation of a log amplifier with a diode in the feedback loop ◆ Describe the operation of a log amplifier with a BJT in the feedback loop
- Describe the basic antilog amplifier
  - Define *antilogarithm* ◆ Explain how a diode or transistor is connected to form an antilog amplifier
- Discuss signal compression with log amplifiers
  - Describe the difference between linear and logarithmic signal compression

The **logarithm** of a number is the power to which the base must be raised to get that number. A logarithmic (log) amplifier produces an output that is proportional to the logarithm of the input, and an antilogarithmic (antilog) amplifier takes the antilog or inverse log of the input.

The Basic Logarithmic Amplifier

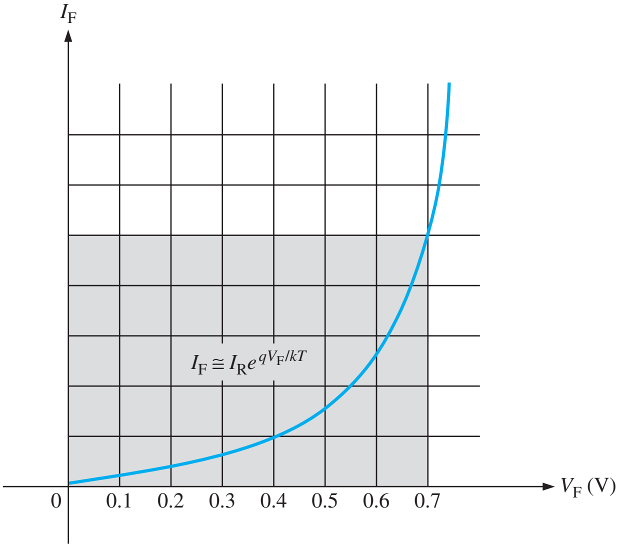
The key element in a log amplifier is a device that exhibits a logarithmic characteristic that, when placed in the feedback loop of an op-amp, produces a logarithmic response. This means that the output voltage is a function of the logarithm of the input voltage, as expressed by the following general equation:

$$V_{out} = -K\ln(V_{in})$$

Equation 14–7

where K is a constant and ln is the natural logarithm to the base e. A **natural logarithm** is the exponent to which the base e must be raised in order to equal a given quantity. Although we will use natural logarithms in the formulas in this section, each expression can be converted to a logarithm to the base 10 ($\log_{10}$) using the relationship $\ln x = 2.3\log_{10}x$.

The semiconductor *pn* junction in the form of either a diode or the base-emitter junction of a BJT provides a logarithmic characteristic. You may recall that a diode has a nonlinear characteristic up to a forward voltage of approximately 0.7 V. Figure 14–29 shows the characteristic curve, where V_F is the forward diode voltage and I_F is the forward diode current.



◀ FIGURE 14–29

A portion of a diode (*pn* junction) characteristic curve (V_F versus I_F).

As you can see on the graph, the diode curve is nonlinear. Not only is the characteristic curve nonlinear, it is logarithmic and is specifically defined by the following formula:

$$I_F \cong I_R e^{qV_F/kT}$$

where I_R is the reverse leakage current, q is the charge on an electron, k is Boltzmann's constant, and T is the absolute temperature in Kelvin. From the previous equation, the diode forward voltage, V_F, can be determined as follows. Take the natural logarithm (*ln* is the logarithm to the base e) of both sides.

$$\ln I_F = \ln I_R e^{qV_F/kT}$$

The ln of a product of two terms equals the sum of the ln of each term.

$$\ln I_F = \ln I_R + \ln e^{qV_F/kT} = \ln I_R + \frac{qV_F}{kT}$$

$$\ln I_F - \ln I_R = \frac{qV_F}{kT}$$

The difference of two ln terms equals the ln of the quotient of the terms.

$$\ln\left(\frac{I_F}{I_R}\right) = \frac{qV_F}{kT}$$

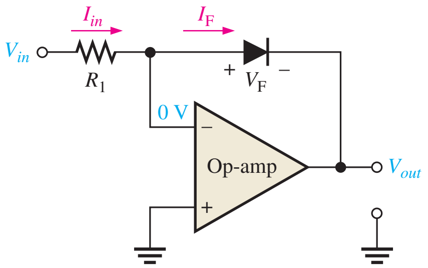
Solving for V_F,

$$V_F = \left(\frac{kT}{q}\right)\ln\left(\frac{I_F}{I_R}\right)$$

Log Amplifier with a Diode When you place a diode in the feedback loop of an op-amp circuit, as shown in Figure 14–30, you have a basic log amplifier. Since the inverting input is at virtual ground (0 V), the output is at $-V_F$ when the input is positive. Since V_F is logarithmic, so is V_{out}. The output is limited to a maximum value of approximately −0.7 V because the diode's logarithmic characteristic is restricted to voltages below 0.7 V. Also, the input must be positive when the diode is connected in the direction shown in the figure. To handle negative inputs, you must turn the diode around.

▶ FIGURE 14–30

A basic log amplifier using a diode as the feedback element.



An analysis of the circuit in Figure 14–30 is as follows, beginning with the facts that $V_{out} = -V_F$ and $I_F = I_{in}$ because there is no current at the inverting input.

$$V_{out} = -V_F$$

$$I_F = I_{in} = \frac{V_{in}}{R_1}$$

Substituting into the formula for V_F,

$$V_{out} = -\left(\frac{kT}{q}\right)\ln\left(\frac{V_{in}}{I_R R_1}\right)$$

The term kT/q is a constant equal to approximately 25 mV at 25°C. Therefore, the output voltage can be expressed as

Equation 14–8

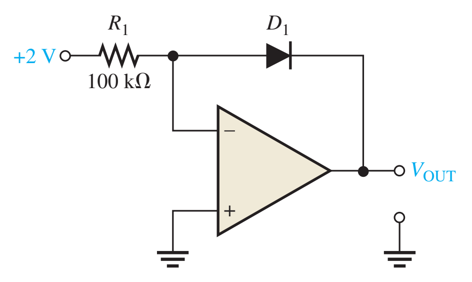
$$\boldsymbol{V_{out} \cong -(0.025\ \mathrm{V})\ln\left(\frac{V_{in}}{I_R R_1}\right)}$$

From Equation 14–8, you can see that the output voltage is the negative of a logarithmic function of the input voltage. The value of the output is controlled by the value of the input voltage and the value of the resistor R_1. The other factor, I_R, is a constant for a given diode.

EXAMPLE 14–8

Determine the output voltage for the log amplifier in Figure 14–31. Assume $I_R = 50$ nA.

▶ FIGURE 14–31



Solution The input voltage and the resistor value are given in Figure 14–31.

$$V_{\text{OUT}} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R_1}\right) = -(0.025\text{ V})\ln\left(\frac{2\text{ V}}{(50\text{ nA})(100\text{ k}\Omega)}\right)$$

$$= -(0.025\text{ V})\ln(400) = -(0.025\text{ V})(5.99) = \mathbf{-0.150\text{ V}}$$

Related Problem Calculate the output voltage of the log amplifier with a +4 V input.

Open the Multisim file E14-08 in the Examples folder on the companion website. Apply the specified input voltage and measure the output voltage.

Log Amplifier with a BJT The base-emitter junction of a bipolar junction transistor exhibits the same type of logarithmic characteristic as a diode because it is also a *pn* junction. A log amplifier with a BJT connected in a common-base form in the feedback loop is shown in Figure 14–32. Notice that V_{out} with respect to ground is equal to $-V_{\text{BE}}$.

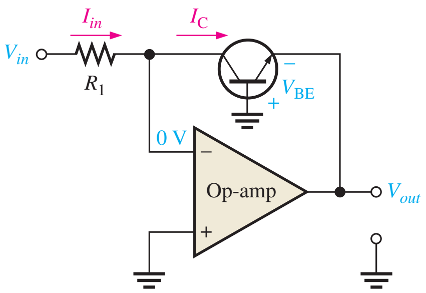


FIGURE 14–32

A basic log amplifier using a transistor as the feedback element.

The analysis for this circuit is the same as for the diode log amplifier except that V_{BE} replaces V_F, I_C replaces I_F, and I_{EBO} replaces I_R. The expression for the V_{BE} versus I_C characteristic curve is

$$I_C = I_{\text{EBO}}e^{qV_{\text{BE}}/kT}$$

where I_{EBO} is the emitter-to-base leakage current. The expression for the output voltage is

$$\mathbf{V_{out} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_{\text{EBO}}R_1}\right)}$$

Equation 14–9

EXAMPLE 14–9

What is V_{out} for a transistor log amplifier with $V_{in} = 3\text{ V}$ and $R_1 = 68\text{ k}\Omega$? Assume $I_{\text{EBO}} = 40\text{ nA}$.

Solution

$$V_{out} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_{\text{EBO}}R_1}\right) = -(0.025\text{ V})\ln\left(\frac{3\text{ V}}{(40\text{ nA})(68\text{ k}\Omega)}\right)$$

$$= -(0.025\text{ V})\ln(1103) = \mathbf{-175.1\text{ mV}}$$

Related Problem Calculate V_{out} if R_1 is changed to 33 kΩ.

The Basic Antilog Amplifier

The **antilogarithm** of a number is the result obtained when the base is raised to a power equal to the logarithm of that number. To get the antilogarithm, you must take the exponential of the logarithm (antilogarithm of $x = e^{\ln x}$).

An antilog amplifier is formed by connecting a transistor (or diode) as the input element as shown in Figure 14–33. The exponential formula still applies to the base-emitter *pn* junction. The output voltage is determined by the current (equal to the collector current) through the feedback resistor.

$$V_{out} = -R_f I_C$$

The characteristic equation of the *pn* junction is

$$I_C = I_{EBO} e^{qV_{BE}/kT}$$

Substituting into the equation for V_{out},

$$V_{out} = -R_f I_{EBO} e^{qV_{BE}/kT}$$

As you can see in Figure 14–33, $V_{in} = V_{BE}$.

$$V_{out} = -R_f I_{EBO} e^{qV_{in}/kT}$$

The exponential term can be expressed as an antilogarithm as follows:

$$V_{out} = -R_f I_{EBO} \text{antilog}\left(\frac{V_{in}q}{kT}\right)$$

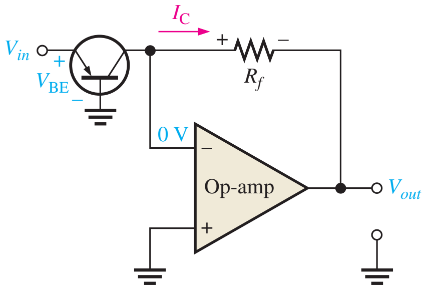
Since *kT/q* is approximately 25 mV,

Equation 14–10

$$\boldsymbol{V_{out} = -R_f I_{EBO} \textbf{antilog}\left(\frac{V_{in}}{25\text{ mV}}\right)}$$

▶ FIGURE 14–33

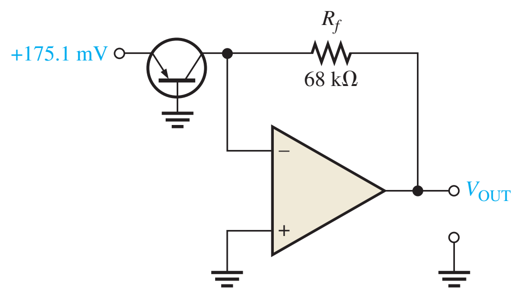
A basic antilog amplifier.



EXAMPLE 14–10

For the antilog amplifier in Figure 14–34, find the output voltage. Assume $I_{EBO} = 40$ nA.

▶ FIGURE 14–34



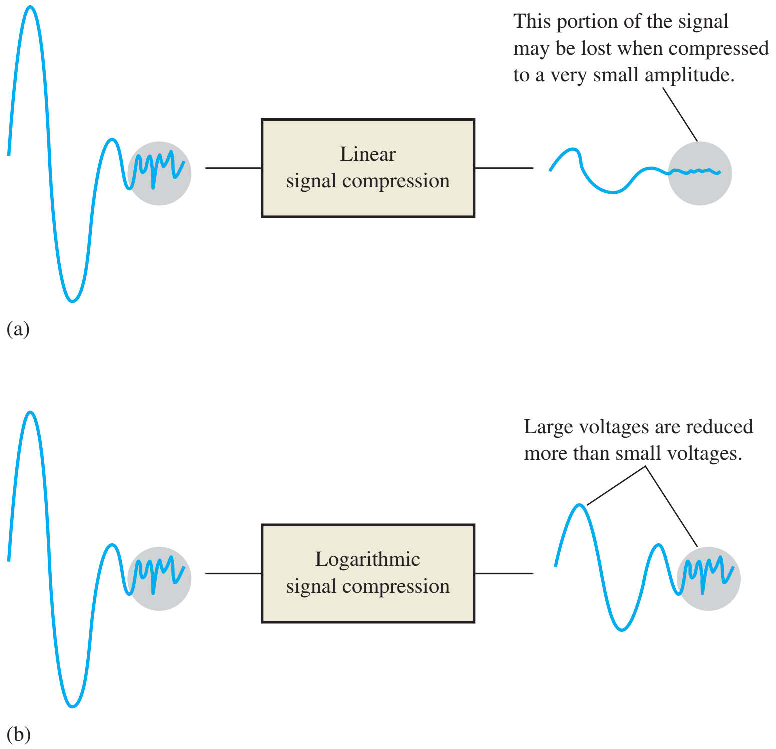
Solution First of all, notice that the input voltage in Figure 14–34 is the inverted output voltage of the log amplifier in Example 14–9, where the output voltage is proportional to the logarithm of the input voltage. In this case, the antilog amplifier reverses the process and produces an output that is proportional to the antilog of the input. Stated another way, the input of an antilog amplifier is proportional to the logarithm of the output. So, the output voltage of the antilog amplifier in Figure 14–34 should have the same magnitude as the input voltage of the log amplifier in Example 14–9 because all the constants are the same. Let's see if it does.

$$
\begin{aligned}
V_{out} &= -R_f I_{\mathrm{EBO}}\,\text{antilog}\left(\frac{V_{in}}{25\ \text{mV}}\right) = -(68\ \text{k}\Omega)(40\ \text{nA})\,\text{antilog}\left(\frac{175.1\ \text{mV}}{25\ \text{mV}}\right)\\
&= -(68\ \text{k}\Omega)(40\ \text{nA})(1101) = \mathbf{-3\ V}
\end{aligned}
$$

Related Problem Determine V_{out} for the amplifier in Figure 14–34 if the feedback resistor is changed to 100 kΩ.

Signal Compression with Logarithmic Amplifiers

In certain applications, a signal may be too large in magnitude for a particular system to handle. The term *dynamic range* is often used to describe the range of voltages contained in a signal. In these cases, the signal voltage must be scaled down by a process called **signal compression** so that it can be properly handled by the system. If a linear circuit is used to scale a signal down in amplitude, the lower voltages are reduced by the same percentage as the higher voltages. Linear signal compression often results in the lower voltages becoming obscured by noise and difficult to accurately distinguish, as illustrated in Figure 14–35(a). To overcome this problem, a signal with a large dynamic range can be compressed using a logarithmic response, as shown in Figure 14–35(b). In logarithmic signal compression, the higher voltages are reduced by a greater percentage than the lower voltages, thus keeping the lower voltage signals from being lost in noise.


This portion of the signal may be lost when compressed to a very small amplitude.
Linear signal compression
(a)
Large voltages are reduced more than small voltages.
Logarithmic signal compression
(b)

◄ FIGURE 14–35

The basic concept of signal compression with a logarithmic amplifier.

SECTION 14–4 CHECKUP

1. What purpose does the diode or transistor perform in the feedback loop of a log amplifier?
2. Why is the output of a log amplifier limited to about 0.7 V?
3. What are the factors that determine the output voltage of a basic log amplifier?
4. In terms of implementation, how does a basic antilog amplifier differ from a basic log amplifier?

14–5 CONVERTERS AND OTHER OP-AMP CIRCUITS

This section introduces a few more op-amp circuits that represent basic applications of the op-amp. You will learn about the constant-current source, the current-to-voltage converter, the voltage-to-current converter, and the peak detector. This is, of course, not a comprehensive coverage of all possible op-amp circuits but is intended only to introduce you to some common basic uses.

After completing this section, you should be able to

- ❑ **Explain and analyze other types of op-amp circuits**
- ❑ Describe a constant-current source
- ❑ Explain a current-to-voltage converter
- ❑ Discuss a voltage-to-current converter
- ❑ Explain how a peak detector works

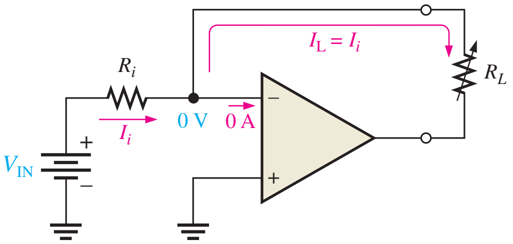
Constant-Current Source

A constant-current source delivers a load current that remains constant when the load resistance changes. Figure 14–36 shows a basic circuit in which a stable voltage source (V_{IN}) provides a constant current (I_i) through the input resistor (R_i). Since the inverting (−) input of the op-amp is at virtual ground (0 V), the value of I_i is determined by V_{IN} and R_i as

$$I_i = \frac{V_{IN}}{R_i}$$

▶ FIGURE 14–36

A basic constant-current source.



Now, since the internal input impedance of the op-amp is extremely high (ideally infinite), practically all of I_i is through R_L, which is connected in the feedback path. Since $I_i = I_L$,

Equation 14–11

$$\boldsymbol{I_L = \frac{V_{IN}}{R_i}}$$

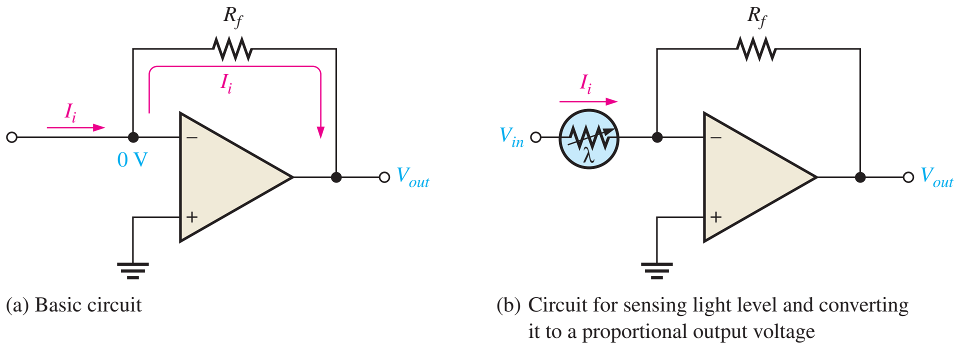
If R_L changes, I_L remains constant as long as V_{IN} and R_i are held constant.

Current-to-Voltage Converter

A current-to-voltage converter converts a variable input current to a proportional output voltage. A basic circuit that accomplishes this is shown in Figure 14–37(a). Since practically all of I_i is through the feedback path, the voltage dropped across R_f is I_iR_f. Because the left side of R_f is at virtual ground (0 V), the output voltage equals the voltage across R_f, which is proportional to I_i.

$$V_{out} = I_iR_f$$

Equation 14–12



(a) Basic circuit

(b) Circuit for sensing light level and converting it to a proportional output voltage

FIGURE 14–37

Current-to-voltage converter.

A specific application of this circuit is illustrated in Figure 14–37(b), where a photoconductive cell is used to sense changes in light level. As the amount of light changes, the current through the photoconductive cell varies because of the cell's change in resistance. This change in resistance produces a proportional change in the output voltage ($\Delta V_{out} = \Delta I_iR_f$).

Voltage-to-Current Converter

A basic voltage-to-current converter is shown in Figure 14–38. This circuit is used in applications where it is necessary to have an output (load) current that is controlled by an input voltage.

Neglecting the input offset voltage, both inverting and noninverting input terminals of the op-amp are at the same voltage, V_{in}. Therefore, the voltage across R_1 equals V_{in}. Since there is negligible current at the inverting input, the current through R_1 is the same as the current through R_L; thus

$$I_L = \frac{V_{in}}{R_1}$$

Equation 14–13

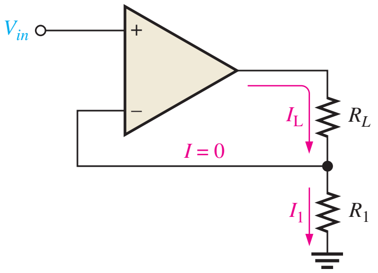


FIGURE 14–38

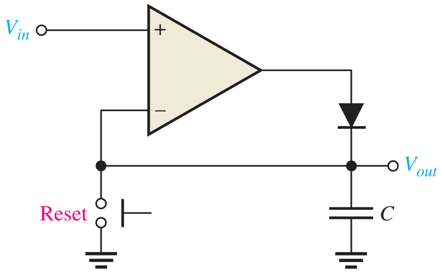
Voltage-to-current converter.

Peak Detector

An interesting application of the op-amp is in a peak detector circuit such as the one shown in Figure 14–39. In this case the op-amp is used as a comparator. This circuit is used to detect the peak of the input voltage and store that peak voltage on a capacitor. For example,

FIGURE 14–39

A basic peak detector.



this circuit can be used to detect and store the maximum value of a voltage surge; this value can then be measured at the output with a voltmeter or recording device. The basic operation is as follows. When a positive voltage is applied to the noninverting input of the op-amp, the high-level output voltage of the op-amp forward-biases the diode and charges the capacitor. The capacitor continues to charge until its voltage reaches a value equal to the input voltage and thus both op-amp inputs are at the same voltage. At this point, the op-amp comparator switches, and its output goes to the low level. The diode is now reverse-biased, and the capacitor stops charging. It has reached a voltage equal to the peak of V_{in} and will hold this voltage until the charge eventually leaks off or until it is reset with a switch as indicated. If a greater input peak occurs, the capacitor charges to the new peak.

SECTION 14–5 CHECKUP

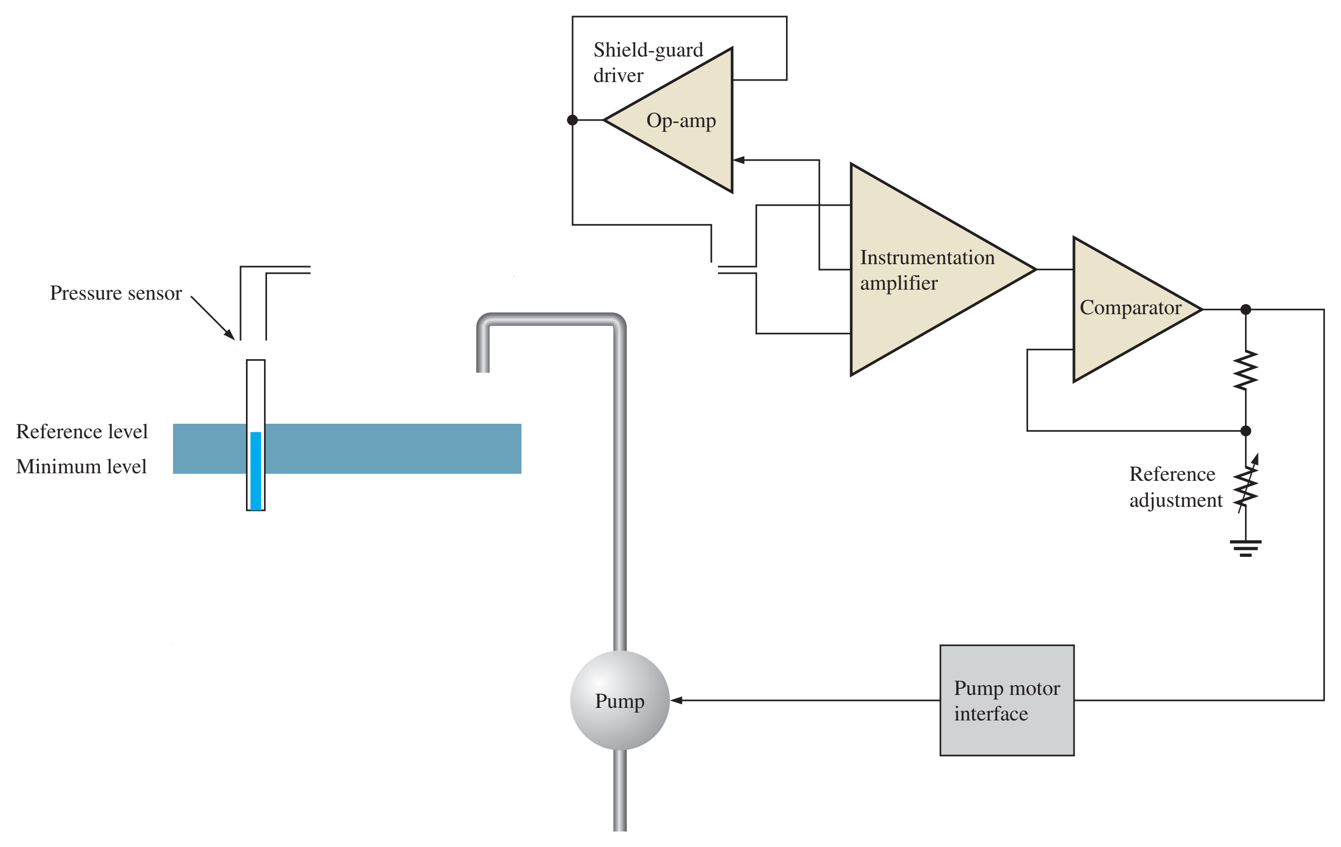
1. For the constant-current source in Figure 14–36, the input reference voltage is 6.8 V and R_i is 10 kΩ. What value of constant current does the circuit supply to a 1.0 kΩ load? To a 5 kΩ load?
2. What element determines the constant of proportionality that relates input current to output voltage in the current-to-voltage converter?

Application Activity: *Liquid Level Control*

The system in this application is designed to maintain a constant liquid level in a tank. The level is kept constant by an electric pump and a pressure sensor (transducer) that detects a change in the level of the liquid by sensing the pressure in a tube.

Level-Sensing Method

A tube with both ends open is placed vertically in a liquid so that one end is above the surface of the liquid. The level of liquid in the tube will be the same as the level in the tank. Now, if the upper end is closed, the pressure of the air trapped in the tube will vary proportional to a change in level of the liquid. For example, if the liquid is water and it rises in the tank by 20 mm, then the pressure in the tube will increase by 20 mm of water. A pressure sensor is placed on the upper end of the tube when the liquid is at its reference level, and the other side is exposed to atmospheric pressure. When the water level decreases, a negative change in pressure is measured by the pressure sensor and a small proportional voltage is produced. The voltage from the pressure sensor is connected to an instrumentation amplifier, which amplifies the small voltage to drive a comparator with hysteresis (Schmitt trigger). The comparator reference voltage is adjusted to the desired value; and when the level falls below the reference, the comparator switches states and



▲ **FIGURE 14–40**

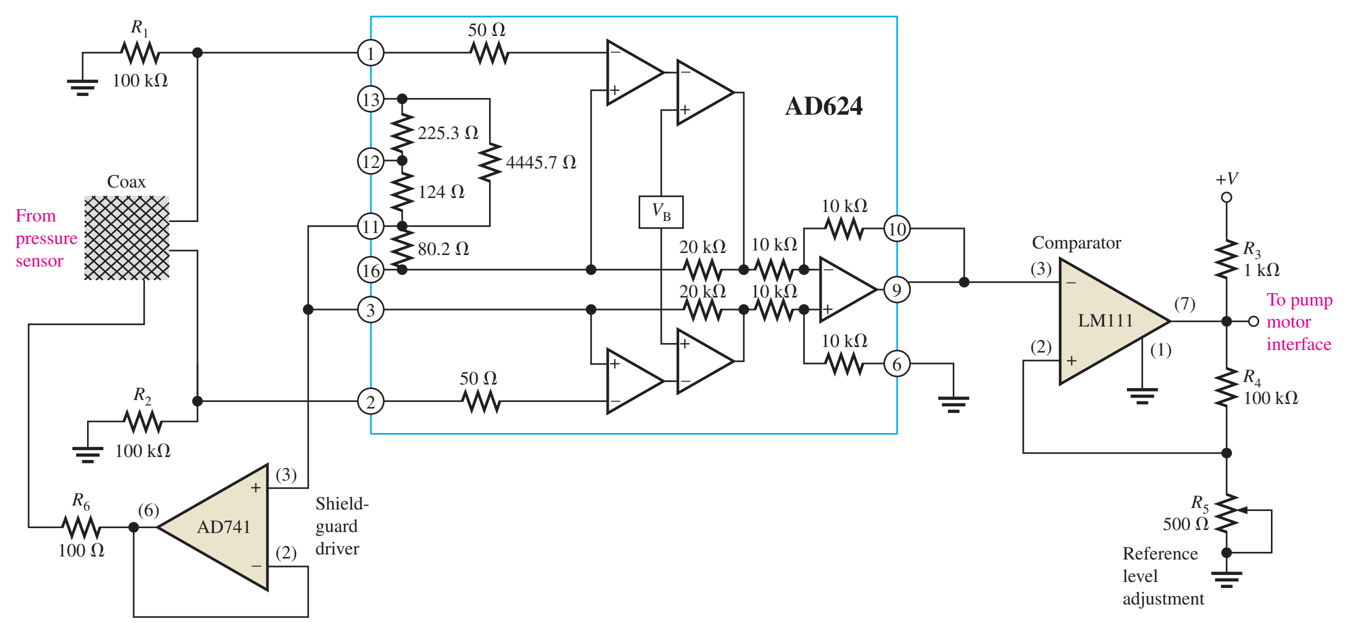
Block diagram of the liquid-level control system.

turns the pump *on* to refill the tank to the reference level. The pressure sensor detects when the reference level of the liquid is reached, and the comparator switches back to its other state, turning the pump *off.* A basic diagram of the system is shown in Figure 14–40.

The Circuit

This system will operate in an industrial environment with exposure to mostly 60 Hz electrical noise. Also, the circuit will be located some distance from the tank and connected to the pressure sensor with a long coaxial cable. The output voltage of the pressure sensor is very small ($100\ \mu V - 200\ \mu V$). For these reasons, a shield-guard driver is incorporated to minimize the effects of noise on the small signal. The AD624 instrumentation amplifier is used to drive an LM111 comparator with hysteresis controlled by a rheostat in the feedback circuit. An AD741 op-amp connected as a voltage-follower is used for the guard driver. The circuit diagram is shown in Figure 14–41. Power supply connections are omitted to simplify the drawing. Resistors R_1 and R_2 provide a return path for bias currents to prevent output drift. R_3 is a pull-up resistor for the comparator output, and R_4 and R_5 provide for the adjustable reference levels by varying the hysteresis. R_6 provides a resistance in series with the shield-guard driver to limit current.

As the liquid level in the tank decreases, the pressure in the tube decreases. This decrease in pressure is translated into a proportional decrease in voltage by the pressure sensor. This decrease in voltage is processed by the circuit to trigger the comparator to its HIGH state to

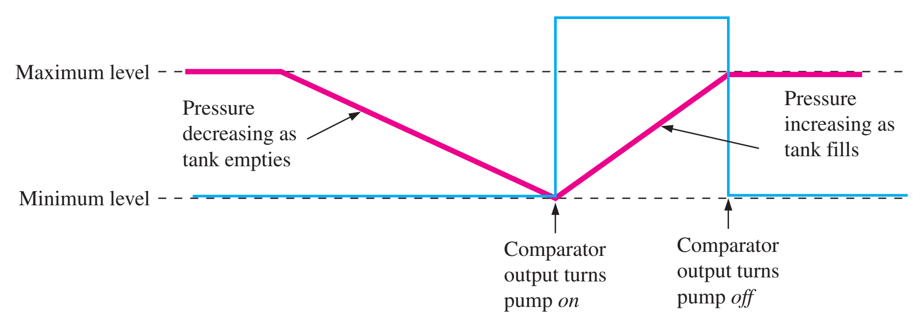


R_1
100 kΩ
50 Ω
AD624
225.3 Ω
4445.7 Ω
124 Ω
80.2 Ω
Coax
From pressure sensor
V_B
20 kΩ
20 kΩ
10 kΩ
10 kΩ
10 kΩ
10 kΩ
Comparator
LM111
+V
R_3
1 kΩ
To pump motor interface
R_4
100 kΩ
50 Ω
R_2
100 kΩ
R_6
100 Ω
AD741
Shield-guard driver
R_5
500 Ω
Reference level adjustment

▲ FIGURE 14–41

Schematic diagram of the liquid-level control circuit.

turn the pump *on* when a desired minimum level is reached. An increase in level occurs while the pump is running, causing a proportional increase in pressure. When the maximum level is reached, the circuit triggers the comparator to its LOW state to turn the pump *off*. This process is illustrated in Figure 14–42.



Maximum level
Minimum level
Pressure decreasing as tank empties
Pressure increasing as tank fills
Comparator output turns pump *on*
Comparator output turns pump *off*

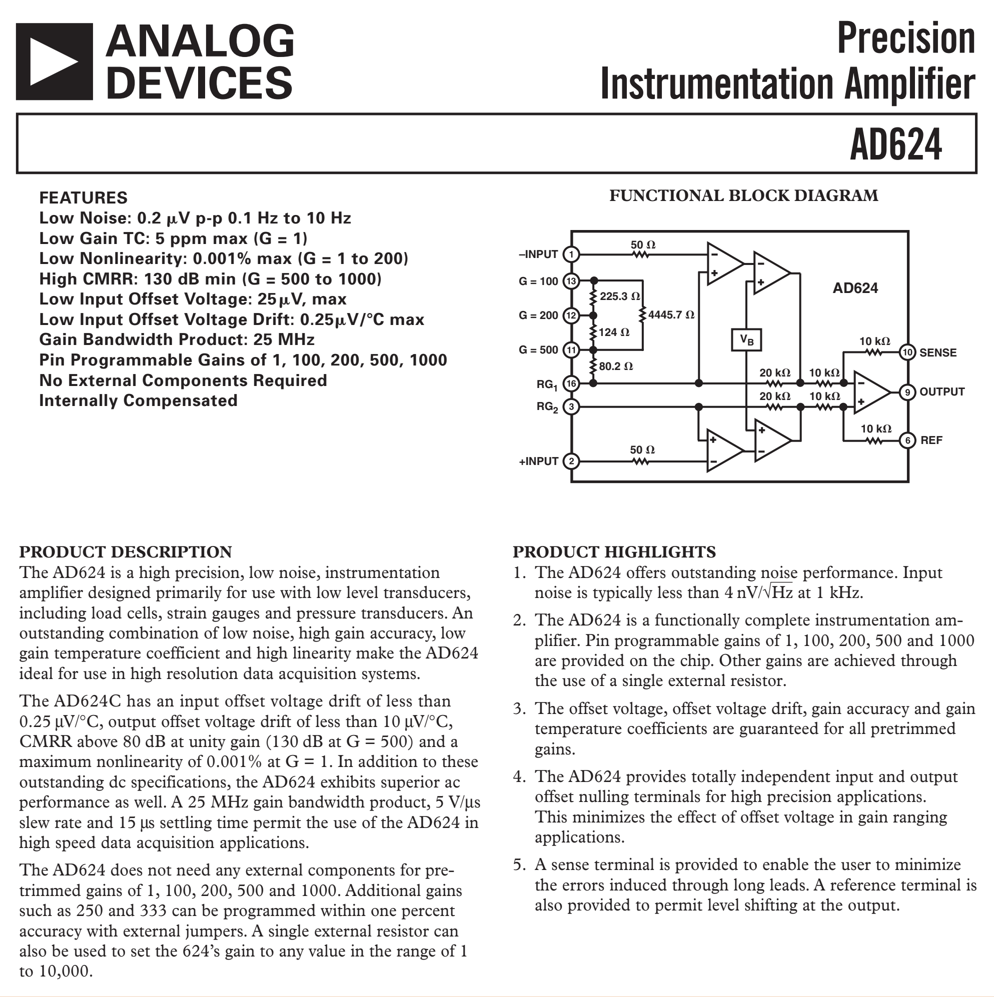
▲ FIGURE 14–42

System operation.

AD624 Datasheet

The front page of the datasheet for the AD624 instrumentation amplifier is shown in Figure 14–43.

1. Use the datasheet to determine the voltage gain of the AD624 in Figure 14–41 based on the connections. You will have to go on-line.
2. How would you change the gain?



ANALOG DEVICES

Precision Instrumentation Amplifier

AD624

FEATURES
Low Noise: 0.2 μV p-p 0.1 Hz to 10 Hz
Low Gain TC: 5 ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130 dB min (G = 500 to 1000)
Low Input Offset Voltage: 25 μV, max
Low Input Offset Voltage Drift: 0.25 μV/°C max
Gain Bandwidth Product: 25 MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

FUNCTIONAL BLOCK DIAGRAM

PRODUCT DESCRIPTION

The AD624 is a high precision, low noise, instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25 μV/°C, output offset voltage drift of less than 10 μV/°C, CMRR above 80 dB at unity gain (130 dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications, the AD624 exhibits superior ac performance as well. A 25 MHz gain bandwidth product, 5 V/μs slew rate and 15 μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pretrimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than 4 nV/$\sqrt{\text{Hz}}$ at 1 kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pretrimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

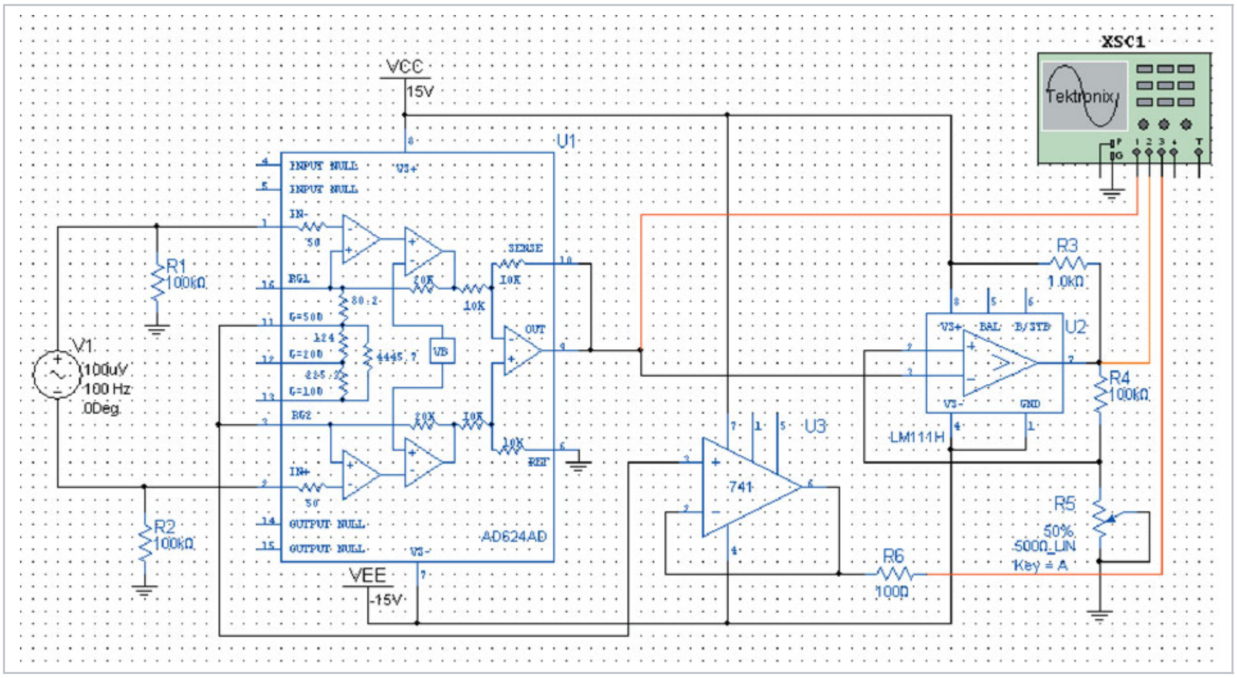
▲ FIGURE 14–43

AD624 datasheet (page l). Datasheet is courtesy of Analog Devices and is subject to revisions. To see the complete datasheet go to www.analog.com.

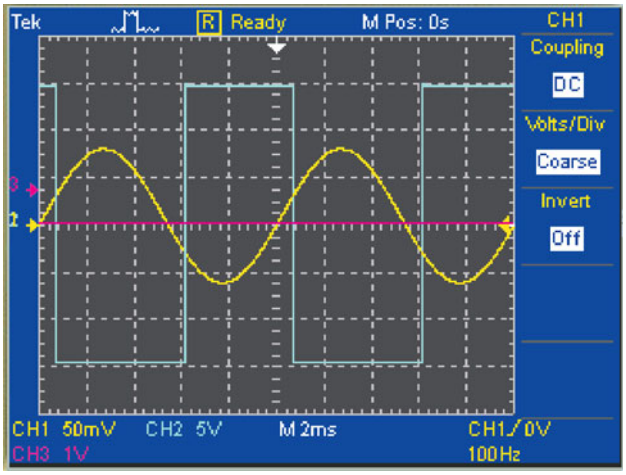
Simulation

The liquid-level control circuit is simulated using Multisim with an input signal of 100 mV at 100 Hz to represent the pressure sensor output. Although the sensor output will change very slowly (almost dc), we are using a higher frequency signal in order to observe the circuit operation. The simulated circuit is shown in Figure 14–44(a) for a differential input. The resulting outputs are shown in part (b). The comparator is triggered at two difference points, as indicated. Notice that there is no signal on the output of the shield-guard driver because there is no common-mode signal on the inputs.

3. Refer to Figure 14–44(b) to determine the voltage gain of the instrumentation amplifier and compare to the gain indicated by the pin connections. The input is 100 μV rms.
4. Determine the difference in mV (hysteresis) between the trigger points on the IA output waveform in Figure 14–44(b).


XSC1
Tektronix
VCC
15V
U1
INPUT NULL
INPUT NULL
IN-
RG1
G=500
G=200
G=100
RG2
IN+
OUTPUT NULL
OUTPUT NULL
VS+
VS-
SENSE
OUT
REF
10K
20K
VB
AD624AD
VEE
-15V
R1
100kΩ
R2
100kΩ
V1
100uV
100 Hz
0Deg
U3
741
U2
LM111H
BAL
B/STB
GND
R3
1.0kΩ
R4
100kΩ
R5
50%
500Ω_LIN
Key = A
R6
100Ω

(a) Circuit screen


Tek R Ready M Pos: 0s

CH1 Coupling DC

Volts/Div Coarse

Invert Off

CH1 50mV CH2 5V M 2ms CH1 ƒ 0V

CH3 1V 100Hz

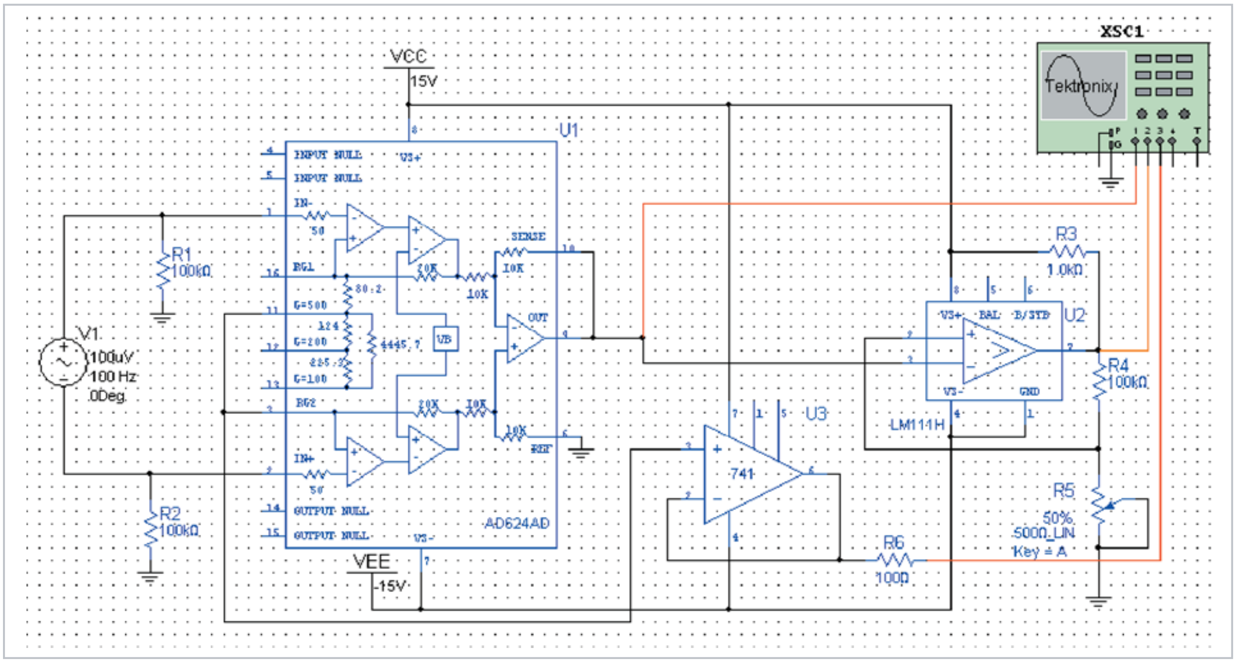
(b) Output of IA (yellow), output of comparator (blue), and output of guard driver (pink)

▲ FIGURE 14–44

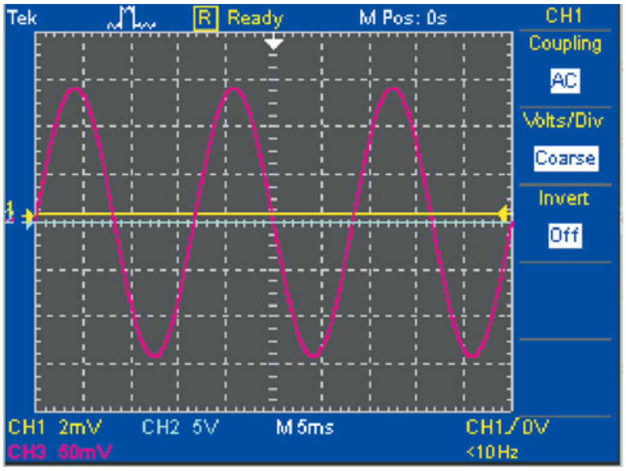
Simulation with a differential input.

Next, the input is changed to a 100 mV common-mode signal at a frequency of 60 Hz, and the simulation is run as shown in Figure 14–45. This simulates a low-frequency noise environment. Notice on the scope display that there is no output signal from the instrumentation amplifier, which indicates that it is rejecting the common-mode signal. The scope display also shows that the shield-guard driver correctly produces the common-mode signal.

5. Verify that the shield-guard driver output is equal to the common-mode signal.


XSC1
Tektronix
VCC
15V
U1
INPUT NULL
INPUT NULL
IN-
RG1
G=500
G=200
G=100
RG2
IN+
OUTPUT NULL
OUTPUT NULL
SENSE
OUT
REF
AD624AD
VEE
-15V
R1
100kΩ
R2
100kΩ
V1
100uV
100 Hz
0Deg
U3
741
R3
1.0kΩ
U2
LM111H
R4
100kΩ
R5
50%
500Ω_LIN
Key = A
R6
100Ω

(a) Circuit screen


Tek Ready M Pos: 0s

CH1 Coupling AC

Volts/Div Coarse

Invert Off

CH1 2mV CH2 5V M 5ms CH1 ╱ 0V

CH3 50mV <10Hz

(b) Output of IA (yellow), output of comparator (blue), and output of guard driver (pink)

▲ FIGURE 14–45

Simulation with a common-mode input.

Simulate the liquid-level control circuit using your Multisim software. Observe the operation with the virtual oscilloscope.

Prototyping and Testing

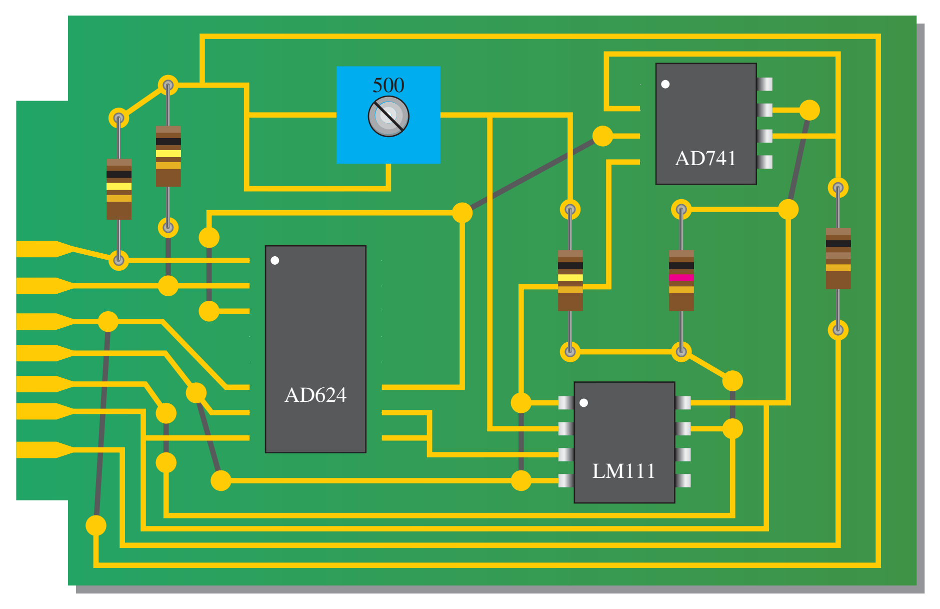
Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a similar circuit, go to Experiment 14–A in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The liquid-level control circuit is implemented on a printed circuit board as shown in Figure 14–46. The dark gray lines represent backside connections.



▲ FIGURE 14–46

Liquid-level control board.

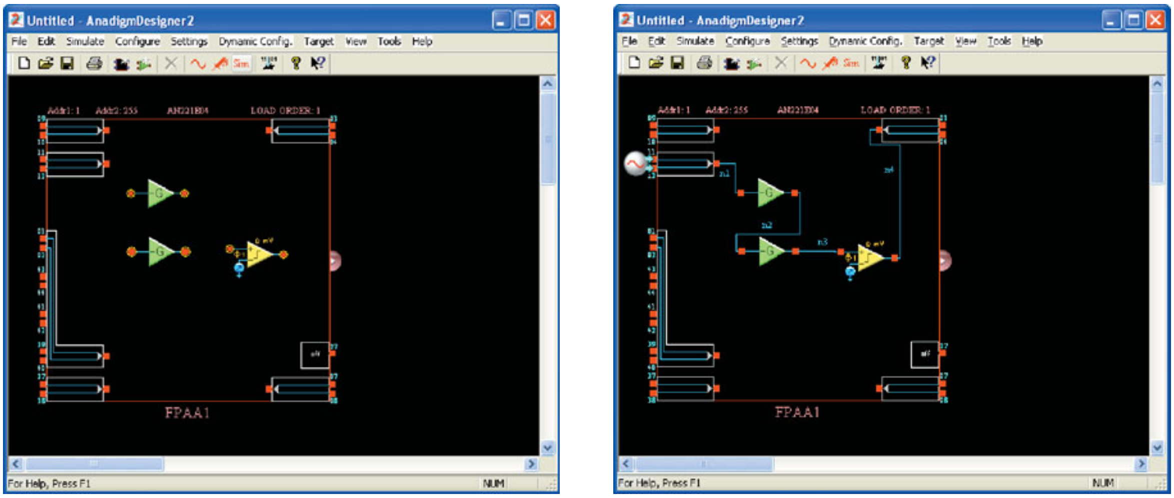
6. Check the printed circuit board and verify that it agrees with the schematic.
7. Label each input and output pin according to function.

Programmable Analog Technology

Assignment

Create a circuit to provide a function similar to that of the level-control circuit in the Application Activity.

Procedure: Open your Designer2 software and configure the CAMs as shown in Figure 14–47.

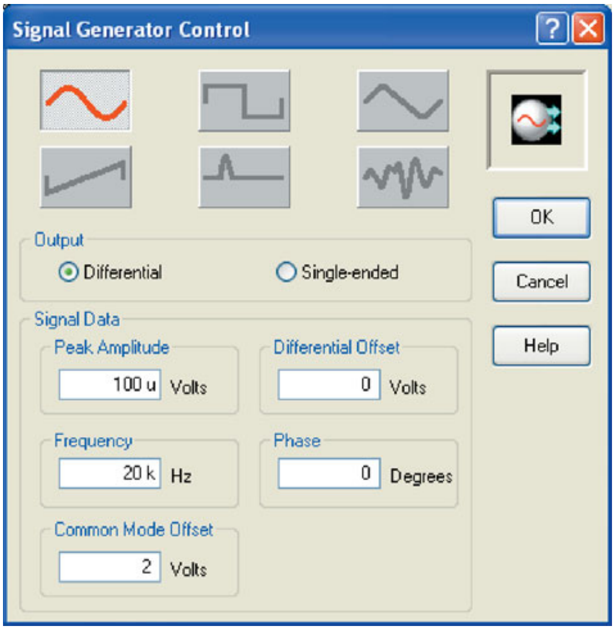

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
FPAA1
For Help, Press F1
NUM

(a) Select and place two inverting gain stage CAMs and one comparator CAM.

(b) Connect the CAMs and add a differential signal source.

▲ FIGURE 14–47

Configure the signal generator as shown in Figure 14–48. Set the signal generator to represent a pressure sensor with a differential output and an amplitude of 100 μV. Note that the frequency is selected only to facilitate viewing.


Signal Generator Control
OK
Cancel
Help

Output

● Differential ○ Single-ended

Signal Data

Peak Amplitude: 100 u Volts

Differential Offset: 0 Volts

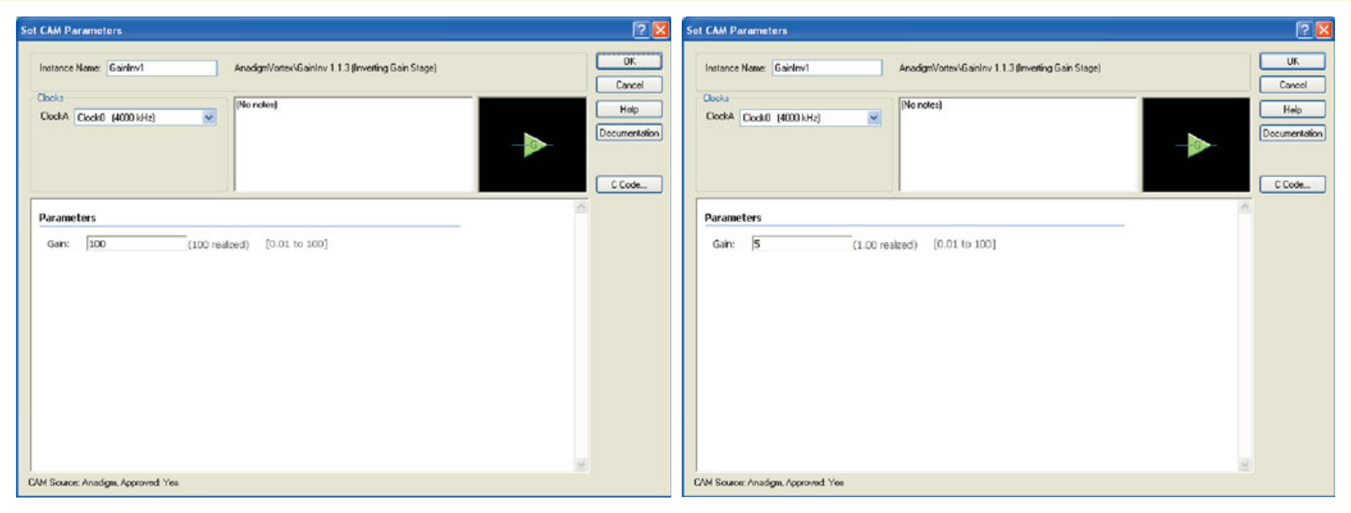
Frequency: 20 k Hz

Phase: 0 Degrees

Common Mode Offset: 2 Volts

▲ FIGURE 14–48

Configure the gain stages for a total gain of 500, as shown in Figure 14–49.


Set CAM Parameters
OK
Cancel
Help
Documentation
C Code...
Set CAM Parameters
OK
Cancel
Help
Documentation
C Code...
G

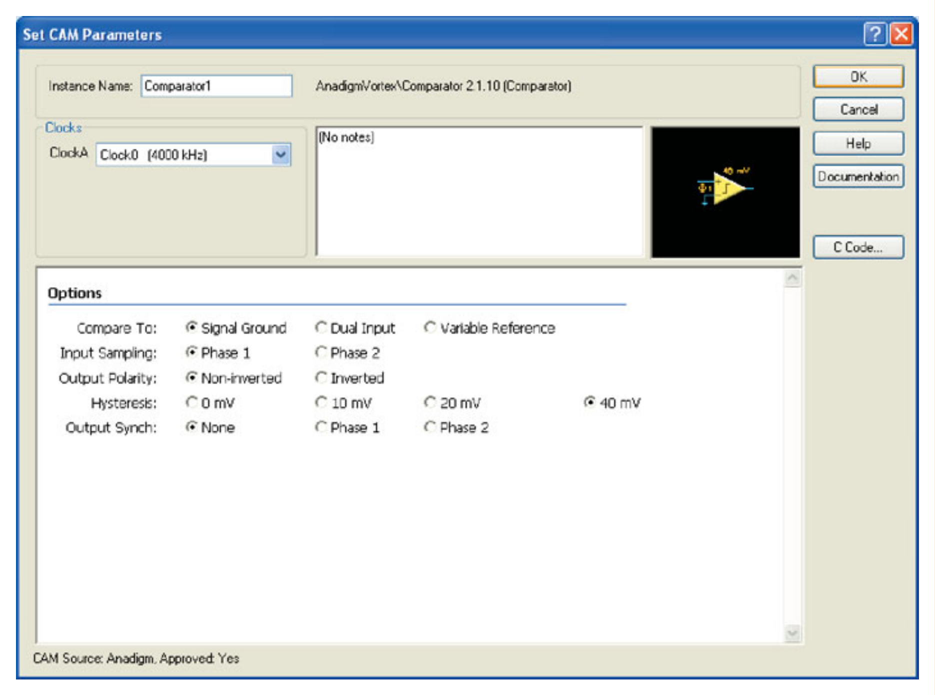
Instance Name: GainInv1
AnadigmVortex\GainInv 1.1.3 (Inverting Gain Stage)
Clocks
ClockA Clock0 (4000 kHz)
(No notes)
Parameters
Gain: 100 (100 realized) [0.01 to 100]
CAM Source: Anadigm, Approved: Yes

Instance Name: GainInv1
AnadigmVortex\GainInv 1.1.3 (Inverting Gain Stage)
Clocks
ClockA Clock0 (4000 kHz)
(No notes)
Parameters
Gain: 5 (1.00 realized) [0.01 to 100]
CAM Source: Anadigm, Approved: Yes

▲ FIGURE 14–49

First stage has gain of 100 and second stage has gain of 5.

Configure the comparator for a hysteresis of 40 mV, as shown in Figure 14–50.


Set CAM Parameters
OK
Cancel
Help
Documentation
C Code...
40 mV
Φ1

Instance Name: Comparator1
AnadigmVortex\Comparator 2.1.10 (Comparator)
Clocks
ClockA Clock0 (4000 kHz)
(No notes)

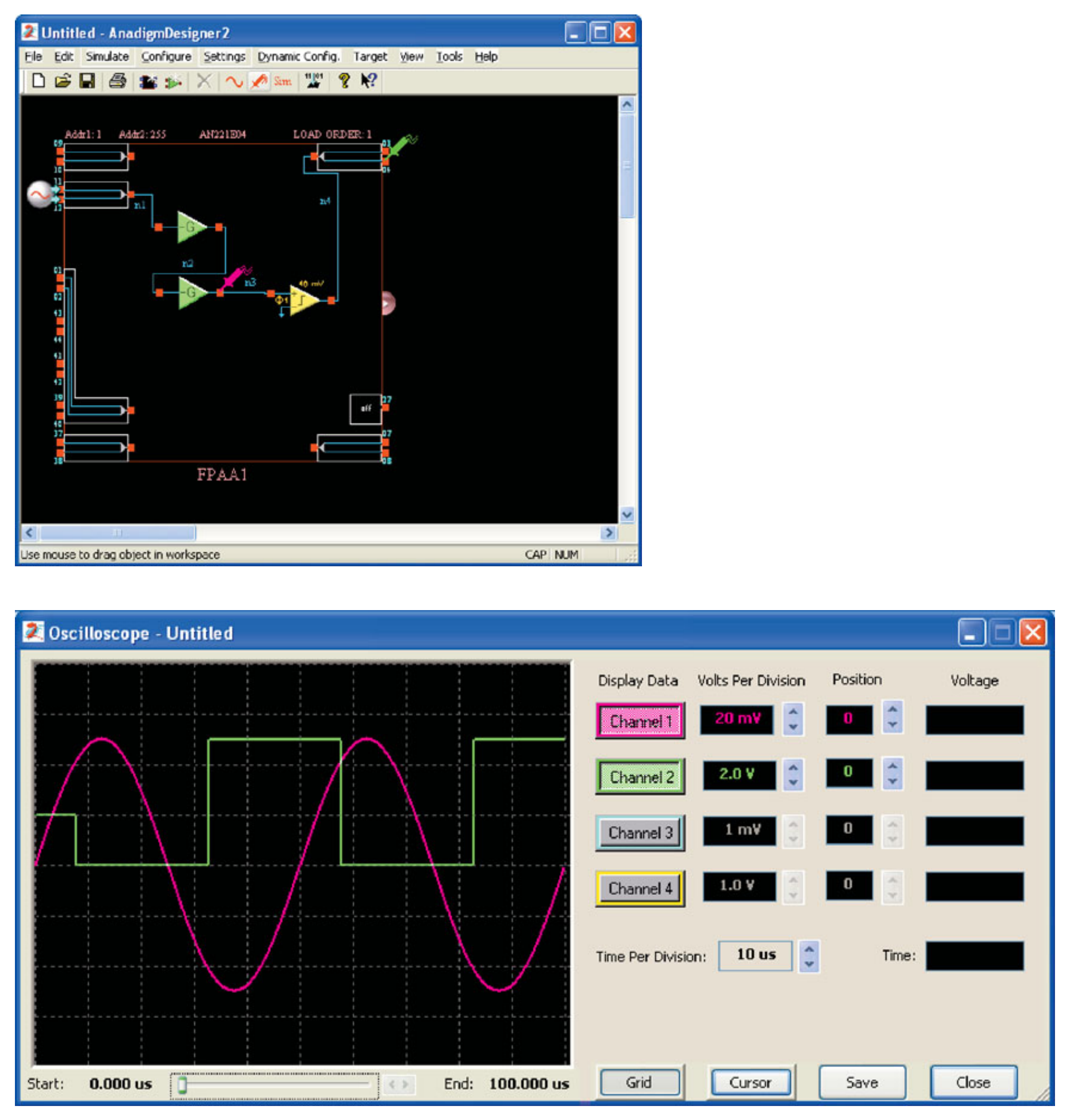
Options

Compare To: ● Signal Ground ○ Dual Input ○ Variable Reference
Input Sampling: ● Phase 1 ○ Phase 2
Output Polarity: ● Non-inverted ○ Inverted
Hysteresis: ○ 0 mV ○ 10 mV ○ 20 mV ● 40 mV
Output Synch: ● None ○ Phase 1 ○ Phase 2

CAM Source: Anadigm, Approved: Yes

▲ FIGURE 14–50

Analysis: Place probes as shown in Figure 14–51 (top) and run a simulation. The results are shown in Figure 14–51 (bottom).


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
40 mV
FPAA1
Use mouse to drag object in workspace
CAP NUM
Oscilloscope - Untitled
Display Data
Volts Per Division
Position
Voltage
Time:
Grid
Cursor
Save
Close

Channel 1 20 mV 0
Channel 2 2.0 V 0
Channel 3 1 mV 0
Channel 4 1.0 V 0
Time Per Division: 10 us
Start: 0.000 us End: 100.000 us

▲ FIGURE 14–51

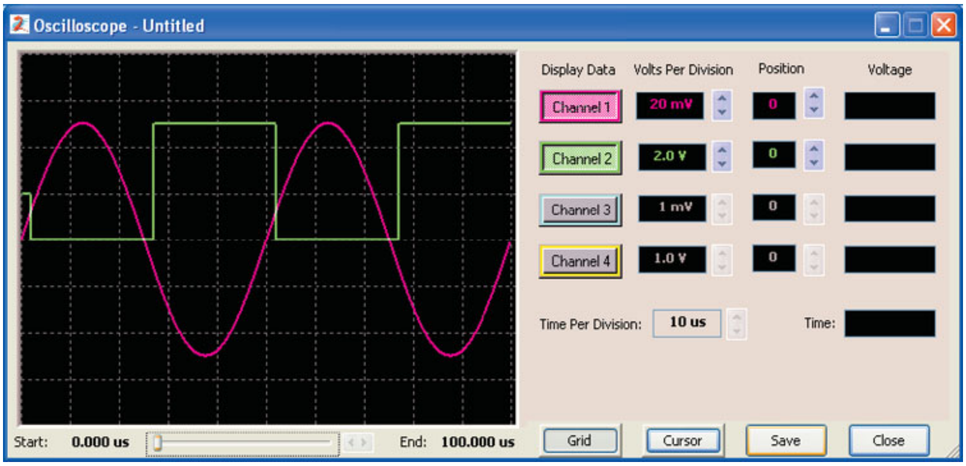
Waveform measurement with a 40 mV comparator hysteresis.

Change the comparator hysteresis to 10 mV, and you get the waveform shown in Figure 14–52. Notice how the trigger points change.

The comparator hysteresis sets the trigger points on the signal so that a minimum and a maximum level can be set to control the level in a tank. Once an FPAA/dpASP is programmed with this design, the levels can be changed by programming a different hysteresis.

Programming Exercises

1. Open your Designer2 software.
2. Implement the level control circuit described.
3. Observe the output for a comparator hyteresis of 0, 10 mV, 20 mV, and 40 mV.

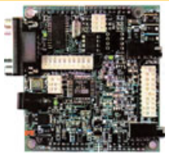


Channel 1: 20 mV, Position 0
Channel 2: 2.0 V, Position 0
Channel 3: 1 mV, Position 0
Channel 4: 1.0 V, Position 0
Time Per Division: 10 us
Time:
Start: 0.000 us
End: 100.000 us

▲ FIGURE 14–52

Waveform measurement with a 10 mV comparator hysteresis.

PAM Experiment



To program, download, and test a circuit using AnadigmDesigner2 software and the programmable analog module (PAM) board, go to Experiment 14–B in *Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling.

SUMMARY

Section 14–1

- A basic instrumentation amplifier is formed by three op-amps and seven resistors, including the gain-setting resistor R_G.
- An instrumentation amplifier has high input impedance, high CMRR, low output offset, and low output impedance.
- The voltage gain of a basic instrumentation amplifier is set by a single external resistor.
- An instrumentation amplifier is useful in applications where small signals are embedded in large common-mode noise.

Section 14–2

- A basic isolation amplifier has electrically isolated input and output stages.
- Isolation amplifiers use capacitive, optical, or transformer coupling for isolation.
- Isolation amplifiers are used to interface sensitive equipment with high-voltage environments and to provide protection from electrical shock in certain medical applications.

Section 14–3

- The operational transconductance amplifier (OTA) is a voltage-to-current amplifier.
- The output current of an OTA is the input voltage times the transconductance.
- In an OTA, transconductance varies with bias current; therefore, the gain of an OTA can be varied with a bias voltage or a variable resistor.

Section 14–4

- The operation of log and antilog amplifiers is based on the nonlinear (logarithmic) characteristics of a *pn* junction.
- A log amplifier has a *pn* junction in the feedback loop, and an antilog amplifier has a *pn* junction in series with the input.

Section 14–5

- A constant-current source delivers the same load current regardless of load resistance (within limits).
- In a peak detector, an op-amp is used as a comparator to charge a capacitor through a diode to the peak value of the input voltage. It is useful in measuring peak voltage surges.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Instrumentation amplifier An amplifier used for amplifying small signals riding on large common-mode voltages.

Isolation amplifier An amplifier with electrically isolated internal stages.

Natural logarithm The exponent to which the base e ($e = 2.71828$) must be raised in order to equal a given quantity.

Operational transconductance amplifier (OTA) A voltage-to-current amplifier.

Transconductance In an electronic device, the ratio of the output current to the input voltage.

KEY FORMULAS

Instrumentation Amplifier

14–1 $$A_{cl} = 1 + \frac{2R}{R_G}$$

14–2 $$R_G = \frac{2R}{A_{cl} - 1}$$

Isolation Amplifier

14–3 $$A_{v1} = \frac{R_{f1}}{R_{i1}} + 1$$

14–4 $$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1$$

Operational Transconductance Amplifier (OTA)

14–5 $$g_m = \frac{I_{out}}{V_{in}}$$

14–6 $$g_m = KI_{BIAS}$$

Log and Antilog Amplifiers

14–7 $$V_{out} = -K\ln(V_{in})$$

14–8 $$V_{out} \cong -(0.025\,\text{V})\ln\left(\frac{V_{in}}{I_R R_1}\right)$$

14–9 $$V_{out} = -(0.025\,\text{V})\ln\left(\frac{V_{in}}{I_{EBO} R_1}\right)$$

14–10 $$V_{out} = -R_f I_{EBO}\,\text{antilog}\left(\frac{V_{in}}{25\,\text{mV}}\right)$$

Converters and Other Op-Amp Circuits

14–11 $$I_L = \frac{V_{IN}}{R_i}$$ Constant-current source

14–12 $$V_{out} = I_i R_f$$ Current-to-voltage converter

14–13 $$I_L = \frac{V_{in}}{R_1}$$ Voltage-to-current converter

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. Instrumentation amplifiers are particularly useful for amplifying small signals in a noisy environment.
2. The gain of an instrumentation amplifier cannot be changed.
3. A basic instrumentation amplifier consists of three op-amps.
4. An isolation amplifier prefers to operate alone.
5. An isolation amplifier consists of two electrically isolated stages.
6. All isolation amplifiers use transformer coupling.
7. OTA stands for operational transistor amplifier.
8. The transconductance of an OTA is dependent on a bias current.
9. A log amplifier can be used for compression of large dynamic range signals.
10. A peak detector is a circuit that uses a diode and a capacitor to produce a dc voltage equal to the peak of the input signal voltage.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the value of R_G in Figure 14–7 is increased, the voltage gain will

   (a) increase **(b)** decrease **(c)** not change

2. If the voltage gain of the instrumentation amplifier in Figure 14–7 is set to 10 at 1 kHz and the frequency is increased to 100 kHz, the gain will

   (a) increase **(b)** decrease **(c)** not change

3. If the voltage gain of the instrumentation amplifier in Figure 14–7 is increased from 10 to 100, the bandwidth will

   (a) increase **(b)** decrease **(c)** not change

4. If R_{f1} in the isolation amplifier of Figure 14–15 is increased to 33 kΩ, the total voltage gain will

   (a) increase **(b)** decrease **(c)** not change

5. If the values of all the capacitors in Figure 14–15 are changed to 0.68 μF, the gain of the output stage will

   (a) increase **(b)** decrease **(c)** not change

6. If the value of R_L in the OTA of Figure 14–23 is reduced, the voltage gain will

   (a) increase **(b)** decrease **(c)** not change

7. If the bias current in the OTA of Figure 14–23 is increased, the voltage gain will

   (a) increase **(b)** decrease **(c)** not change

8. In the log amplifier of Figure 14–31, when the value of R_1 is decreased, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 14–1

1. To make a basic instrumentation amplifier, it takes
   - **(a)** one op-amp with a certain feedback arrangement
   - **(b)** two op-amps and seven resistors
   - **(c)** three op-amps and seven capacitors
   - **(d)** three op-amps and seven resistors
2. Typically, an instrumentation amplifier has an external resistor used for
   - **(a)** establishing the input impedance
   - **(b)** setting the voltage gain
   - **(c)** setting the current gain
   - **(d)** interfacing with an instrument

3. Instrumentation amplifiers are used primarily in
(a) high-noise environments **(b)** medical equipment
(c) test instruments **(d)** filter circuits

Section 14–2 **4.** Isolation amplifiers are used primarily in
(a) remote, isolated locations
(b) systems that isolate a single signal from many different signals
(c) applications where there are high voltages and sensitive equipment
(d) applications where human safety is a concern
(e) answers (c) and (d)

5. The two parts of a basic isolation amplifier are
(a) amplifier and filter **(b)** input stage and coupling stage
(c) input stage and output stage **(d)** gain stage and offset stage

6. The stages of many isolation amplifiers are connected by
(a) copper strips **(b)** a capacitor **(c)** microwave links **(d)** current loops

7. The characteristic that allows an isolation amplifier to amplify small signal voltages in the presence of much greater noise voltages is its
(a) CMRR **(b)** high gain
(c) high input impedance **(d)** magnetic coupling between input and output

Section 14–3 **8.** The term *OTA* means
(a) operational transistor amplifier **(b)** operational transformer amplifier
(c) operational transconductance amplifier **(d)** output transducer amplifier

9. In an OTA, the transconductance is controlled by
(a) the dc supply voltage **(b)** the input signal voltage
(c) the manufacturing process **(d)** a bias current

10. The voltage gain of an OTA circuit is set by
(a) a feedback resistor **(b)** the transconductance only
(c) the transconductance and the load resistor **(d)** the bias current and supply voltage

11. An OTA is basically a
(a) voltage-to-current amplifier **(b)** current-to-voltage amplifier
(c) current-to-current amplifier **(d)** voltage-to-voltage amplifier

Section 14–4 **12.** The operation of a logarithmic amplifier is based on
(a) the nonlinear operation of an op-amp
(b) the logarithmic characteristic of a *pn* junction
(c) the reverse breakdown characteristic of a *pn* junction
(d) the logarithmic charge and discharge of an *RC* circuit

13. If the input to a log amplifier is x, the output is proportional to
(a) e^x **(b)** $\ln x$ **(c)** $\log_{10}x$
(d) $2.3\log_{10}x$ **(e)** answers (a) and (c) **(f)** answers (b) and (d)

14. If the input to an antilog amplifier is x, the output is proportional to
(a) $e^{\ln x}$ **(b)** e^x **(c)** $\ln x$ **(d)** e^{-x}

Section 14–5 **15.** A constant-current source provides a nonchanging current to a load
(a) for all values of current
(b) for all values of load resistance
(c) for all values of load resistance within defined limits

16. A peak detector consists of
(a) a comparator, a transistor, and a capacitor **(b)** a comparator, a diode, and a capacitor
(c) a comparator, a diode, and an inductor **(d)** an integrator, a diode, and a capacitor

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

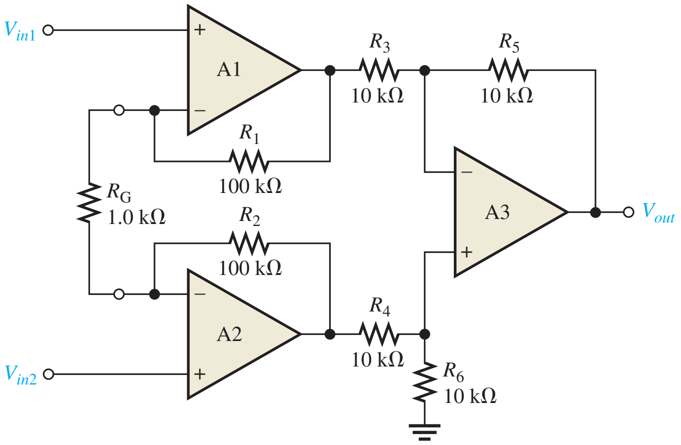
BASIC PROBLEMS

Section 14–1 **Instrumentation Amplifiers**

1. Determine the voltage gains of op-amps A1 and A2 for the instrumentation amplifier configuration in Figure 14–53.

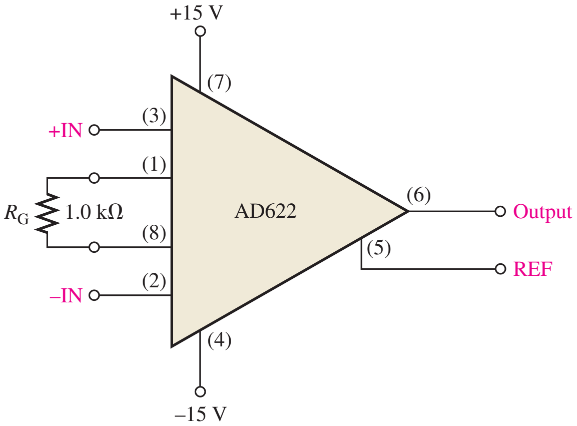
▶ **FIGURE 14–53**

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to Figure numbers (e.g., F14–53).



2. Find the overall voltage gain of the instrumentation amplifier in Figure 14–53.
3. The following voltages are applied to the instrumentation amplifier in Figure 14–53: $V_{in1} = 5$ mV, $V_{in2} = 10$ mV, and $V_{cm} = 225$ mV. Determine the final output voltage.
4. What value of R_G must be used to change the gain of the instrumentation amplifier in Figure 14–53 to 1000?
5. What is the voltage gain of the AD622 instrumentation amplifier in Figure 14–54?

▶ **FIGURE 14–54**

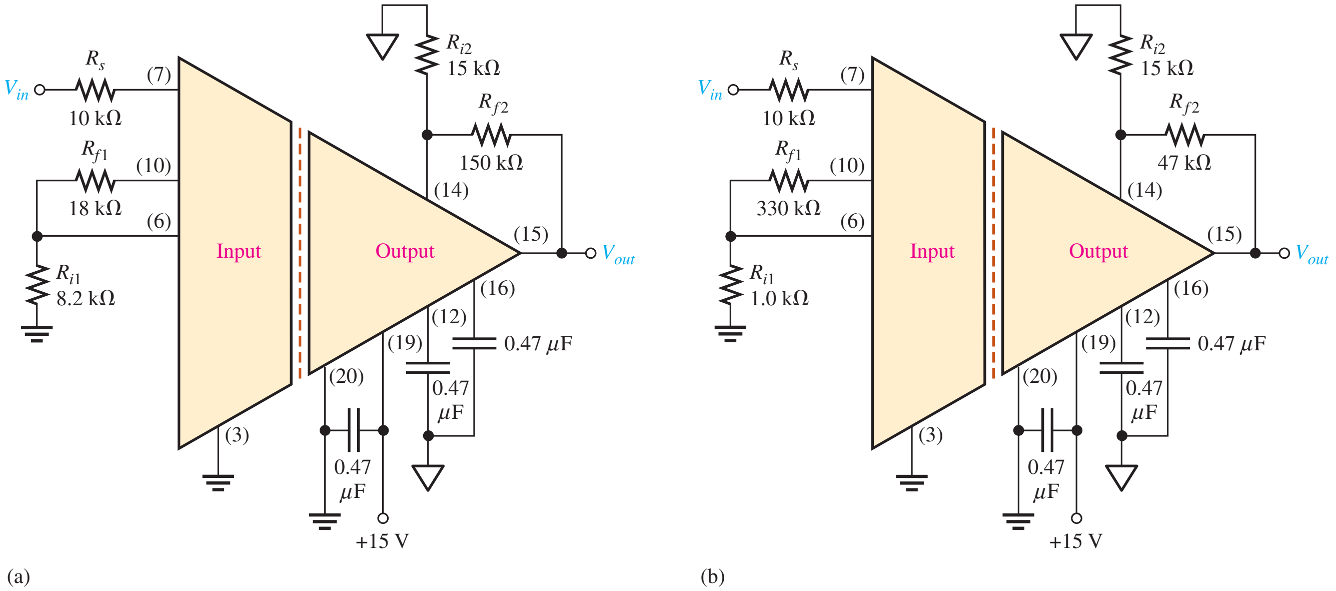


6. Determine the approximate bandwidth of the amplifier in Figure 14–54 if the voltage gain is set to 10. Use the graph in Figure 14–6.
7. Specify what you must do to change the gain of the amplifier in Figure 14–54 to approximately 24.
8. Determine the value of R_G in Figure 14–54 for a voltage gain of 20.

Section 14–2 **Isolation Amplifiers**

9. The op-amp in the input stage of a certain isolation amplifier has a voltage gain of 30. The output stage is set for a gain of 10. What is the total voltage gain of this device?

10. Determine the total voltage gain of each 3656KG in Figure 14–55.


V_{in}
R_s
10 kΩ
(7)
R_{f1}
18 kΩ
(10)
(6)
R_{i1}
8.2 kΩ
Input
Output
(3)
R_{i2}
15 kΩ
R_{f2}
150 kΩ
(14)
(15)
V_{out}
(16)
(12)
0.47 μF
(19)
(20)
0.47 μF
0.47 μF
+15 V
(a)
V_{in}
R_s
10 kΩ
(7)
R_{f1}
330 kΩ
(10)
(6)
R_{i1}
1.0 kΩ
Input
Output
(3)
R_{i2}
15 kΩ
R_{f2}
47 kΩ
(14)
(15)
V_{out}
(16)
(12)
0.47 μF
(19)
(20)
0.47 μF
0.47 μF
+15 V
(b)

▲ FIGURE 14–55

11. Specify how you would change the total gain of the amplifier in Figure 14–55(a) to approximately 100 by changing only the gain of the input stage.

12. Specify how you would change the total gain in Figure 14–55(b) to approximately 440 by changing only the gain of the output stage.

13. Specify how you would connect each amplifier in Figure 14–55 for unity gain.

Section 14–3 Operational Transconductance Amplifiers (OTAs)

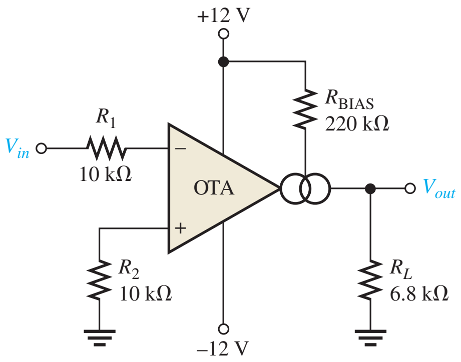
14. A certain OTA has an input voltage of 10 mV and an output current of 10 μA. What is the transconductance?

15. A certain OTA with a transconductance of 5000 μS has a load resistance of 10 kΩ. If the input voltage is 100 mV, what is the output current? What is the output voltage?

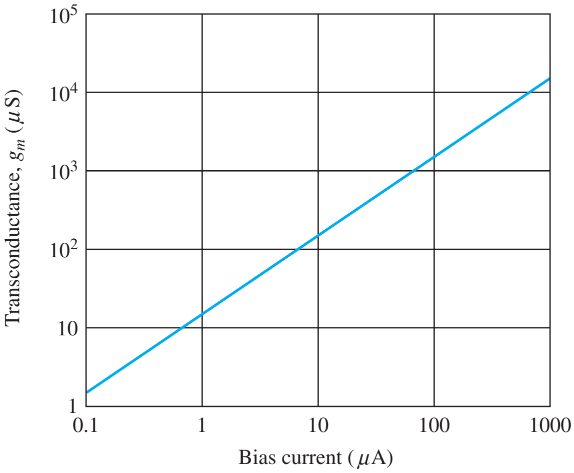
16. The output voltage of a certain OTA with a load resistance is determined to be 3.5 V. If its transconductance is 4000 μS and the input voltage is 100 mV, what is the value of the load resistance?

17. Determine the voltage gain of the OTA in Figure 14–56. Assume $K = 16\ \mu S/\mu A$ for the graph in Figure 14–57.

▶ FIGURE 14–56


+12 V
R_{BIAS}
220 kΩ
R_1
10 kΩ
V_{in}
–
+
OTA
V_{out}
R_2
10 kΩ
R_L
6.8 kΩ
–12 V

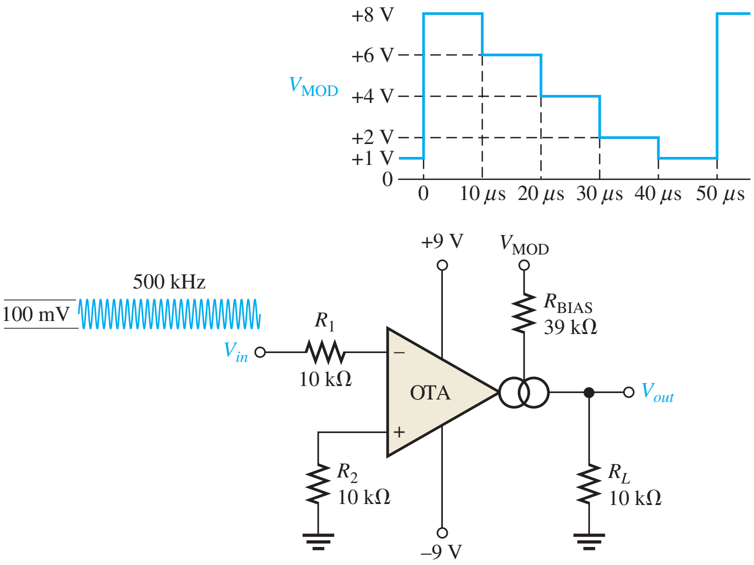
▶ FIGURE 14–57



18. If a 10 kΩ rheostat is added in series with the bias resistor in Figure 14–56, what are the minimum and maximum voltage gains?

19. The OTA in Figure 14–58 functions as an amplitude modulation circuit. Determine the output voltage waveform for the given input waveforms assuming $K = 16\ \mu\text{S}/\mu\text{A}$.

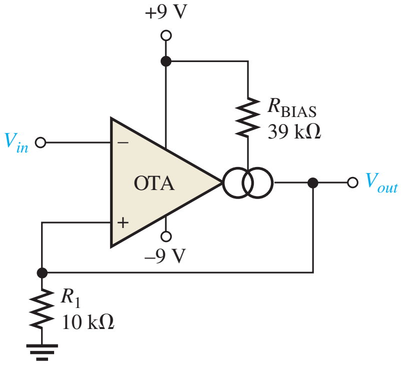
▶ FIGURE 14–58


+8 V
+6 V
V_{MOD}
+4 V
+2 V
+1 V
0
0
10 μs
20 μs
30 μs
40 μs
50 μs
500 kHz
100 mV
V_{in}
R_1
10 kΩ
+9 V
V_{MOD}
R_{BIAS}
39 kΩ
OTA
V_{out}
R_2
10 kΩ
R_L
10 kΩ
–9 V

20. Determine the trigger points for the Schmitt trigger in Figure 14–59.

21. Determine the output voltage waveform for the Schmitt trigger in Figure 14–59 in relation to a 1 kHz sine wave with peak values of ±10 V.

▶ FIGURE 14–59


+9 V
R_{BIAS}
39 kΩ
V_{in}
OTA
V_{out}
–9 V
R_1
10 kΩ

Section 14–4 Log and Antilog Amplifiers

22. Using your calculator, find the natural logarithm (ln) of each of the following numbers:

(a) 0.5 **(b)** 2 **(c)** 50 **(d)** 130

23. Repeat Problem 22 for $\log_{10}$.

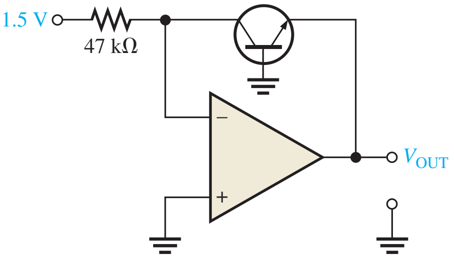
24. What is the antilog of 1.6?

25. Explain why the output of a log amplifier is limited to approximately 0.7 V.

26. What is the output voltage of a certain log amplifier with a diode in the feedback path when the input voltage is 3 V? The input resistor is 82 kΩ and the reverse leakage current is 100 nA.

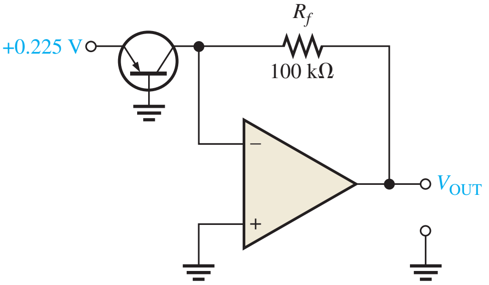
27. Determine the output voltage for the log amplifier in Figure 14–60. Assume $I_{EBO} = 60\,\text{nA}$.

▶ FIGURE 14–60



28. Determine the output voltage for the antilog amplifier in Figure 14–61. Assume $I_{EBO} = 60\,\text{nA}$.

▶ FIGURE 14–61

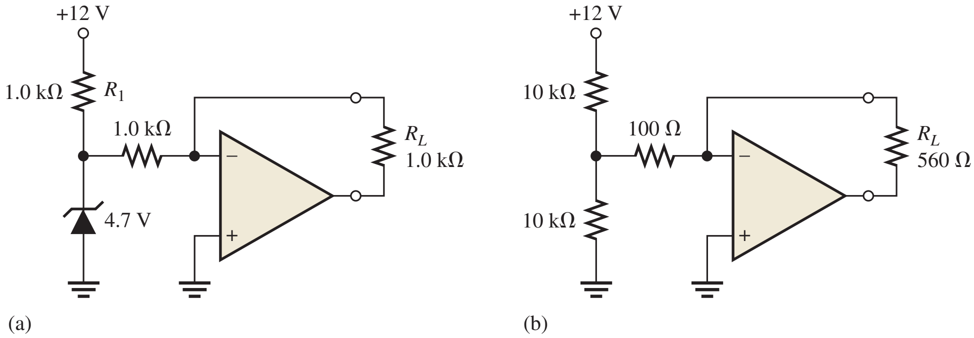


29. Signal compression is one application of logarithmic amplifiers. Suppose an audio signal with a maximum voltage of 1 V and a minimum voltage of 100 mV is applied to the log amplifier in Figure 14–60. What will be the maximum and minimum output voltages? What conclusion can you draw from this result?

Section 14–5 Converters and Other Op-Amp Circuits

30. Determine the load current in each circuit of Figure 14–62.

▶ FIGURE 14–62



31. Devise a circuit for remotely sensing temperature and producing a proportional voltage that can then be converted to digital form for display. A thermistor can be used as the temperature-sensing element.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

32. Open file TSP14-32 and determine the fault.

33. Open file TSP14-33 and determine the fault.

34. Open file TSP14-34 and determine the fault.

35. Open file TSP14-35 and determine the fault.

36. Open file TSP14-36 and determine the fault.

ACTIVE FILTERS

15

CHAPTER OUTLINE

15–1 Basic Filter Responses
15–2 Filter Response Characteristics
15–3 Active Low-Pass Filters
15–4 Active High-Pass Filters
15–5 Active Band-Pass Filters
15–6 Active Band-Stop Filters
15–7 Filter Response Measurements
Application Activity
Programmable Analog Technology

CHAPTER OBJECTIVES

- Describe and analyze the gain-versus-frequency responses of basic types of filters
- Describe three types of filter response characteristics and other parameters
- Identify and analyze active low-pass filters
- Identify and analyze active high-pass filters
- Analyze basic types of active band-pass filters
- Describe basic types of active band-stop filters
- Discuss two methods for measuring frequency response

KEY TERMS

- Filter
- Low-pass filter
- Pole
- Roll-off
- High-pass filter
- Band-pass filter
- Band-stop filter
- Damping factor

APPLICATION ACTIVITY PREVIEW

RFID stands for Radio Frequency Identification and is a technology that enables the tracking and/or identification of objects. Typically, an RFID system consists of an RF tag containing an IC chip that transmits data about the object, a reader that receives transmitted data from the tag, and a data-processing system that processes and stores the data passed to it by the reader. In this application, you will focus on the RFID reader. RFID systems are used in metering applications such as electronic toll collection, inventory control and tracking, merchandise control, asset tracking and recovery, tracking parts moving through a manufacturing process, and tracking goods in a supply chain.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

Power supply filters were introduced in Chapter 2. In this chapter, active filters that are used for signal processing are introduced. Filters are circuits that are capable of passing signals with certain selected frequencies while rejecting signals with other frequencies. This property is called *selectivity.*

Active filters use transistors or op-amps combined with passive *RC*, *RL*, or *RLC* circuits. The active devices provide voltage gain, and the passive circuits provide frequency selectivity. In terms of general response, the four basic categories of active filters are low-pass, high-pass, band-pass, and band-stop. In this chapter, you will study active filters using op-amps and *RC* circuits.

15–1 BASIC FILTER RESPONSES

Filters are usually categorized by the manner in which the output voltage varies with the frequency of the input voltage. The categories of active filters are low-pass, high-pass, band-pass, and band-stop. Each of these general responses are examined.

After completing this section, you should be able to

- ☐ **Describe and analyze the gain-versus-frequency responses of basic types of filters**
- ☐ Describe low-pass filter response
  - ◆ Define *passband* and *critical frequency* ◆ Determine the bandwidth ◆ Define *pole* ◆ Explain roll-off rate and define its unit ◆ Calculate the critical frequency
- ☐ Describe high-pass filter response
  - ◆ Explain how the passband is limited ◆ Calculate the critical frequency
- ☐ Describe band-pass filter response
  - ◆ Determine the bandwidth ◆ Determine the center frequency ◆ Calculate the quality factor (Q)
- ☐ Describe band-stop filter response
  - ◆ Determine the bandwidth

Low-Pass Filter Response

A **filter** is a circuit that passes certain frequencies and attenuates or rejects all other frequencies. The **passband** of a filter is the range of frequencies that are allowed to pass through the filter with minimum attenuation (usually defined as less than −3 dB of attenuation). The **critical frequency,** f_c, (also called the *cutoff frequency*) defines the end of the passband and is normally specified at the point where the response drops −3 dB (70.7%) from the passband response. Following the passband is a region called the *transition region* that leads into a region called the *stopband.* There is no precise point between the transition region and the stopband.

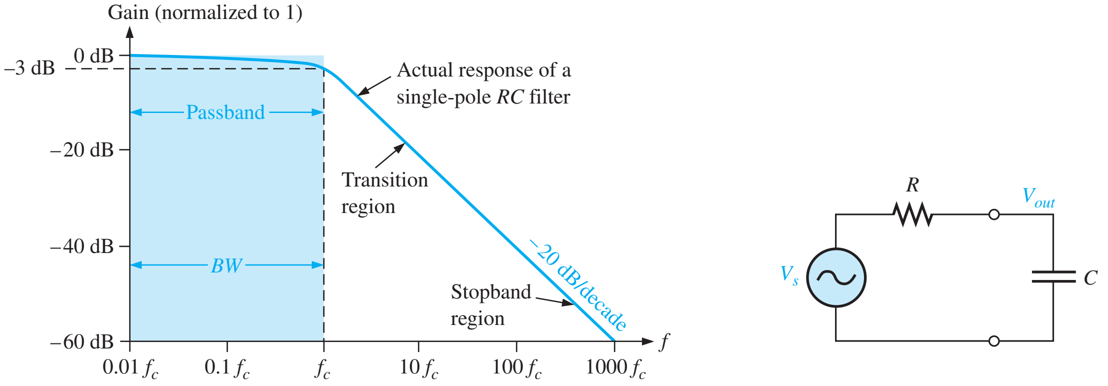
A **low-pass filter** is one that passes frequencies from dc to f_c and significantly attenuates all other frequencies. The passband of the ideal low-pass filter is shown in the blue-shaded area of Figure 15–1(a); the response drops to zero at frequencies beyond the passband. This ideal response is sometimes referred to as a “brick-wall” because nothing gets through beyond the wall. The bandwidth of an ideal low-pass filter is equal to f_c.

Equation 15–1

$$BW = f_c$$

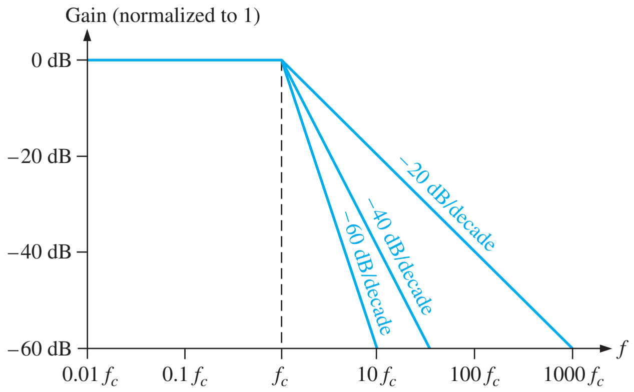
The ideal response shown in Figure 15–1(a) is not attainable by any practical filter. Actual filter responses depend on the number of **poles**, a term used with filters to describe the number of RC circuits contained in the filter. The most basic low-pass filter is a simple RC circuit consisting of just one resistor and one capacitor; the output is taken across the capacitor as shown in Figure 15–1(b). This basic RC filter has a single pole, and it rolls off at −20 dB/decade beyond the critical frequency. The actual response is indicated by the blue line in Figure 15–1(a). The response is plotted on a standard log plot that is used for filters to show details of the curve as the gain drops. Notice that the gain drops off slowly until the frequency is at the critical frequency; after this, the gain drops rapidly.

The −20 dB/decade **roll-off** rate for the gain of a basic RC filter means that at a frequency of $10f_c$, the output will be −20 dB (10%) of the input. This roll-off rate is not a particularly good filter characteristic because too much of the unwanted frequencies (beyond the passband) are allowed through the filter.



(a) Comparison of an ideal low-pass filter response (blue area) with actual response. Although not shown on log scale, response extends down to $f_c = 0$.

(b) Basic low-pass circuit



(c) Idealized low-pass filter responses

▲ **FIGURE 15–1**

Low-pass filter responses.

The critical frequency of a low-pass *RC* filter occurs when $X_C = R$, where

$$f_c = \frac{1}{2\pi RC}$$

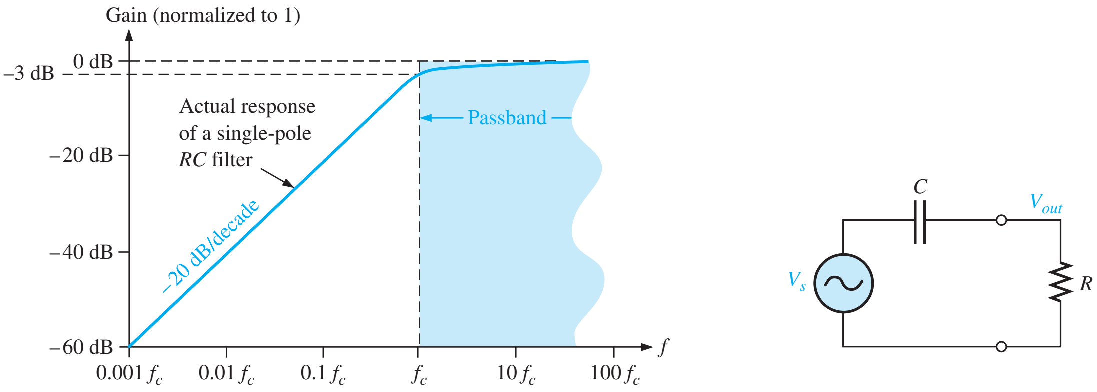
Recall from your basic dc/ac studies that the output at the critical frequency is 70.7% of the input. This response is equivalent to an attenuation of −3 dB.

Figure 15–1(c) illustrates three idealized low-pass response curves including the basic one-pole response (−20 dB/decade). The approximations show a flat response to the cutoff frequency and a roll-off at a constant rate after the cutoff frequency. Actual filters do not have a perfectly flat response up to the cutoff frequency but drop to −3 dB at this point as described previously.

In order to produce a filter that has a steeper transition region (and hence form a more effective filter), it is necessary to add additional circuitry to the basic filter. Responses that are steeper than −20 dB/decade in the transition region cannot be obtained by simply cascading identical *RC* stages (due to loading effects). However, by combining an op-amp with frequency-selective feedback circuits, filters can be designed with roll-off rates of −40, −60, or more dB/decade. Filters that include one or more op-amps in the design are called **active filters.** These filters can optimize the roll-off rate or other attribute (such as phase response) with a particular filter design. In general, the more poles the filter uses, the steeper its transition region will be. The exact response depends on the type of filter and the number of poles.

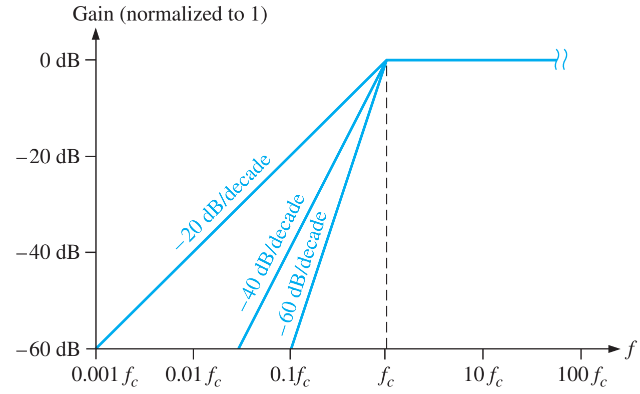
High-Pass Filter Response

A **high-pass filter** is one that significantly attenuates or rejects all frequencies below f_c and passes all frequencies above f_c. The critical frequency is, again, the frequency at which the output is 70.7% of the input (or -3 dB) as shown in Figure 15–2(a). The ideal response, indicated by the blue-shaded area, has an instantaneous drop at f_c, which, of course, is not achievable. Ideally, the passband of a high-pass filter is all frequencies above the critical frequency. The high-frequency response of practical circuits is limited by the op-amp or other components that make up the filter.



(a) Comparison of an ideal high-pass filter response (blue area) with actual response

(b) Basic high-pass circuit



(c) Idealized high-pass filter responses

▲ **FIGURE 15–2**

High-pass filter responses.

A simple *RC* circuit consisting of a single resistor and capacitor can be configured as a high-pass filter by taking the output across the resistor as shown in Figure 15–2(b). As in the case of the low-pass filter, the basic *RC* circuit has a roll-off rate of -20 dB/decade, as indicated by the blue line in Figure 15–2(a). Also, the critical frequency for the basic high-pass filter occurs when $X_C = R$, where

$$f_c = \frac{1}{2\pi RC}$$

Figure 15–2(c) illustrates three idealized high-pass response curves including the basic one-pole response (-20 dB/decade) for a high-pass *RC* circuit. As in the case of the low-pass filter, the approximations show a flat response to the cutoff frequency and a roll-off at a constant rate after the cutoff frequency. Actual high-pass filters do not have the perfectly flat response indicated or the precise roll-off rate shown. Responses that are steeper than -20 dB/decade in the transition region are also possible with active high-pass filters; the particular response depends on the type of filter and the number of poles.

Band-Pass Filter Response

A **band-pass filter** passes all signals lying within a band between a lower-frequency limit and an upper-frequency limit and essentially rejects all other frequencies that are outside this specified band. A generalized band-pass response curve is shown in Figure 15–3. The bandwidth (BW) is defined as the difference between the upper critical frequency (f_{c2}) and the lower critical frequency (f_{c1}).

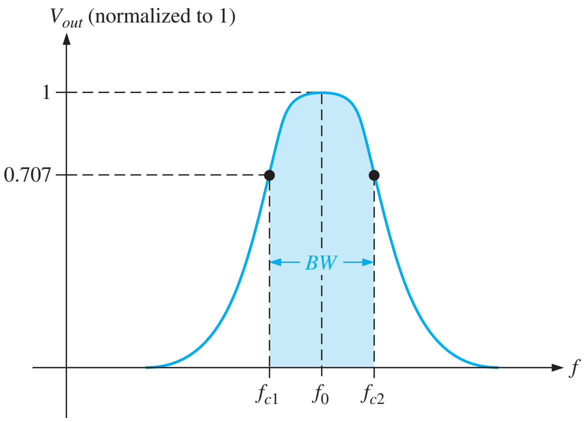
$$\boldsymbol{BW = f_{c2} - f_{c1}}$$

Equation 15–2

The critical frequencies are, of course, the points at which the response curve is 70.7% of its maximum. Recall from Chapter 12 that these critical frequencies are also called *3 dB frequencies.* The frequency about which the passband is centered is called the *center frequency,* f_0, defined as the geometric mean of the critical frequencies.

$$\boldsymbol{f_0 = \sqrt{f_{c1}f_{c2}}}$$

Equation 15–3



▲ FIGURE 15–3

General band-pass response curve.

Quality Factor The **quality factor (Q)** of a band-pass filter is the ratio of the center frequency to the bandwidth.

$$\boldsymbol{Q = \frac{f_0}{BW}}$$

Equation 15–4

The value of Q is an indication of the selectivity of a band-pass filter. The higher the value of Q, the narrower the bandwidth and the better the selectivity for a given value of f_0. Band-pass filters are sometimes classified as narrow-band ($Q > 10$) or wide-band ($Q < 10$). The quality factor (Q) can also be expressed in terms of the damping factor (DF) of the filter as

$$Q = \frac{1}{DF}$$

You will study the damping factor in Section 15–2.

EXAMPLE 15–1

A certain band-pass filter has a center frequency of 15 kHz and a bandwidth of 1 kHz. Determine Q and classify the filter as narrow-band or wide-band.

Solution

$$Q = \frac{f_0}{BW} = \frac{15\text{ kHz}}{1\text{ kHz}} = \mathbf{15}$$

Because $Q > 10$, this is a narrow-band filter.

Related Problem[*] If the quality factor of the filter is doubled, what will the bandwidth be?

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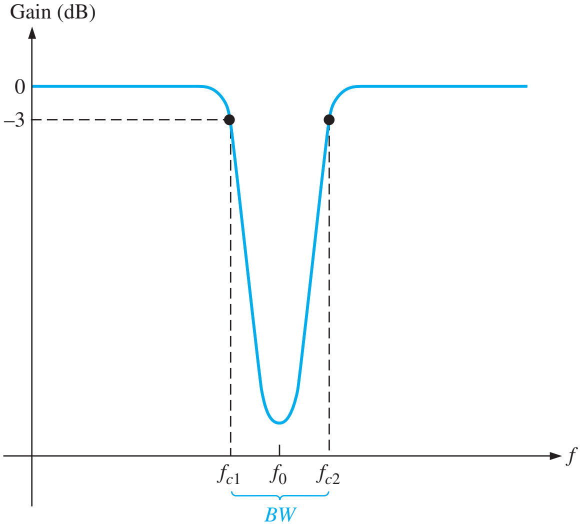
[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Band-Stop Filter Response

Another category of active filter is the **band-stop filter**, also known as *notch, band-reject,* or *band-elimination* filter. You can think of the operation as opposite to that of the band-pass filter because frequencies within a certain bandwidth are rejected, and frequencies outside the bandwidth are passed. A general response curve for a band-stop filter is shown in Figure 15–4. Notice that the bandwidth is the band of frequencies between the 3 dB points, just as in the case of the band-pass filter response.

▶ FIGURE 15–4

General band-stop filter response.



SECTION 15–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. What determines the bandwidth of a low-pass filter?
2. What limits the passband of an active high-pass filter?
3. How are the Q and the bandwidth of a band-pass filter related? Explain how the selectivity is affected by the Q of a filter.

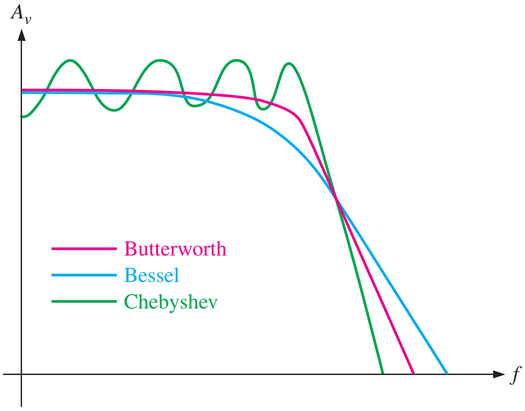
15–2 FILTER RESPONSE CHARACTERISTICS

Each type of filter response (low-pass, high-pass, band-pass, or band-stop) can be tailored by circuit component values to have either a Butterworth, Chebyshev, or Bessel characteristic. Each of these characteristics is identified by the shape of the response curve, and each has an advantage in certain applications.

After completing this section, you should be able to

- ❑ **Describe three types of filter response characteristics and other parameters**
- ❑ Discuss the Butterworth characteristic
- ❑ Describe the Chebyshev characteristic
- ❑ Discuss the Bessel characteristic
- ❑ Define *damping factor*
  - ◆ Calculate the damping factor
  - ◆ Show the block diagram of an active filter
- ❑ Analyze a filter for critical frequency and roll-off rate
  - ◆ Explain how to obtain multi-order filters
  - ◆ Describe the effects of cascading on roll-off rate

Butterworth, Chebyshev, or Bessel response characteristics can be realized with most active filter circuit configurations by proper selection of certain component values. A general comparison of the three response characteristics for a low-pass filter response curve is shown in Figure 15–5. High-pass and band-pass filters can also be designed to have any one of the characteristics.



◀ FIGURE 15–5

Comparative plots of three types of filter response characteristics.

The Butterworth Characteristic The **Butterworth** characteristic provides a very flat amplitude response in the passband and a roll-off rate of −20 dB/decade/pole. The phase response is not linear, however, and the phase shift (thus, time delay) of signals passing through the filter varies nonlinearly with frequency. Therefore, a pulse applied to a filter with a Butterworth response will cause overshoots on the output because each frequency component of the pulse's rising and falling edges experiences a different time delay. Filters with the Butterworth response are normally used when all frequencies in the passband must have the same gain. The Butterworth response is often referred to as a maximally flat response.

The Chebyshev Characteristic Filters with the **Chebyshev** response characteristic are useful when a rapid roll-off is required because it provides a roll-off rate greater than −20 dB/decade/pole. This is a greater rate than that of the Butterworth, so filters can be implemented with the Chebyshev response with fewer poles and less complex circuitry for a given roll-off rate. This type of filter response is characterized by overshoot or ripples in the passband (depending on the number of poles) and an even less linear phase response than the Butterworth.

The Bessel Characteristic The **Bessel** response exhibits a linear phase characteristic, meaning that the phase shift increases linearly with frequency. The result is almost no overshoot on the output with a pulse input. For this reason, filters with the Bessel response are used for filtering pulse waveforms without distorting the shape of the waveform.

The Damping Factor

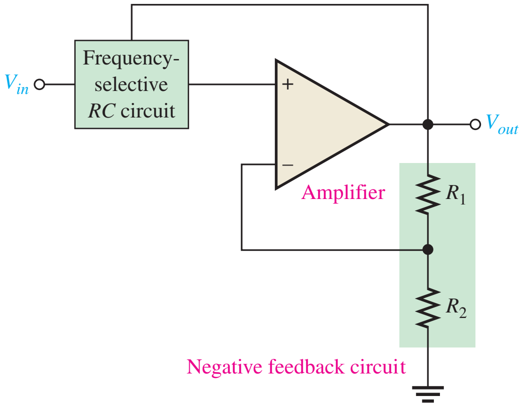
As mentioned, an active filter can be designed to have either a Butterworth, Chebyshev, or Bessel response characteristic regardless of whether it is a low-pass, high-pass, band-pass, or band-stop type. The **damping factor (*DF*)** of an active filter circuit determines which response characteristic the filter exhibits. To explain the basic concept, a generalized active filter is shown in Figure 15–6. It includes an amplifier, a negative feedback circuit, and a filter section. The amplifier and feedback are connected in a noninverting configuration. The damping factor is determined by the negative feedback circuit and is defined by the following equation:

Equation 15–5

$$DF = 2 - \frac{R_1}{R_2}$$

▶ FIGURE 15–6

General diagram of an active filter.



Basically, the damping factor affects the filter response by negative feedback action. Any attempted increase or decrease in the output voltage is offset by the opposing effect of the negative feedback. This tends to make the response curve flat in the passband of the filter if the value for the damping factor is precisely set. By advanced mathematics, which we will not cover, values for the damping factor have been derived for various orders of filters to achieve the maximally flat response of the Butterworth characteristic.

The value of the damping factor required to produce a desired response characteristic depends on the **order** (number of poles) of the filter. A *pole,* for our purposes, is simply a circuit with one resistor and one capacitor. The more poles a filter has, the faster its roll-off rate is. To achieve a second-order Butterworth response, for example, the damping factor must be 1.414. To implement this damping factor, the feedback resistor ratio must be

$$\frac{R_1}{R_2} = 2 - DF = 2 - 1.414 = 0.586$$

This ratio gives the closed-loop gain of the noninverting amplifier portion of the filter, $A_{cl(\mathrm{NI})}$, a value of 1.586, derived as follows:

$$A_{cl(\mathrm{NI})} = \frac{1}{B} = \frac{1}{R_2/(R_1 + R_2)} = \frac{R_1 + R_2}{R_2} = \frac{R_1}{R_2} + 1 = 0.586 + 1 = 1.586$$

EXAMPLE 15–2

If resistor R_2 in the feedback circuit of an active single-pole filter of the type in Figure 15–6 is $10\ \text{k}\Omega$, what value must R_1 be to obtain a maximally flat Butterworth response?

Solution

$$\frac{R_1}{R_2} = 0.586$$

$$R_1 = 0.586R_2 = 0.586(10\ \text{k}\Omega) = \mathbf{5.86\ k\Omega}$$

Using the nearest standard 5 percent value of $5.6\ \text{k}\Omega$ will get very close to the ideal Butterworth response.

Related Problem What is the damping factor for $R_2 = 10\ \text{k}\Omega$ and $R_1 = 5.6\ \text{k}\Omega$?

Critical Frequency and Roll-Off Rate

The critical frequency is determined by the values of the resistors and capacitors in the frequency-selective *RC* circuit shown in Figure 15–6. For a single-pole (first-order) filter, as shown in Figure 15–7, the critical frequency is

$$f_c = \frac{1}{2\pi RC}$$

Although we show a low-pass configuration, the same formula is used for the f_c of a single-pole high-pass filter. The number of poles determines the roll-off rate of the filter. A Butterworth response produces -20 dB/decade/pole. So, a first-order (one-pole) filter has a roll-off of -20 dB/decade; a second-order (two-pole) filter has a roll-off rate of -40 dB/decade; a third-order (three-pole) filter has a roll-off rate of -60 dB/decade; and so on.

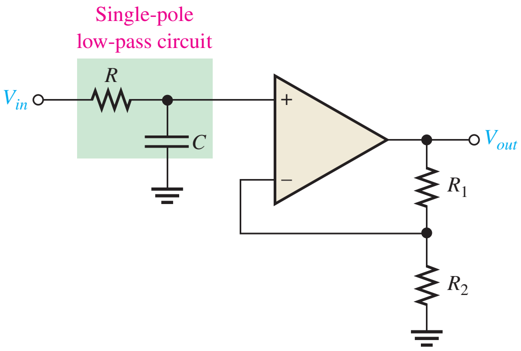
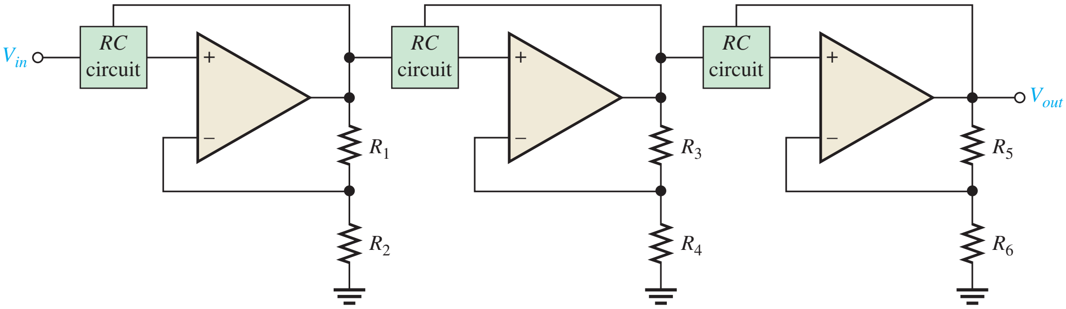


FIGURE 15–7

First-order (one-pole) low-pass filter.

Generally, to obtain a filter with three poles or more, one-pole or two-pole filters are cascaded, as shown in Figure 15–8. To obtain a third-order filter, for example, cascade a second-order and a first-order filter; to obtain a fourth-order filter, cascade two second-order filters; and so on. Each filter in a cascaded arrangement is called a *stage* or *section.*

Because of its maximally flat response, the Butterworth characteristic is the most widely used. Therefore, we will limit our coverage to the Butterworth response to illustrate basic filter concepts. Table 15–1 lists the roll-off rates, damping factors, and feedback resistor ratios for up to sixth-order Butterworth filters. Resistor designations correspond to the gain-setting resistors in Figure 15–8 and may be different on other circuit diagrams.



▲ FIGURE 15–8

The number of filter poles can be increased by cascading.

▼ TABLE 15–1

Values for the Butterworth response.

		1ST STAGE			2ND STAGE			3RD STAGE		
ORDER	ROLL-OFF DB/DECADE	POLES	*DF*	R_1/R_2	POLES	*DF*	R_3/R_4	POLES	*DF*	R_5/R_6
1	−20	1	Optional							
2	−40	2	1.414	0.586						
3	−60	2	1.00	1	1	1.00	1			
4	−80	2	1.848	0.152	2	0.765	1.235			
5	−100	2	1.00	1	2	1.618	0.382	1	0.618	1.382
6	−120	2	1.932	0.068	2	1.414	0.586	2	0.518	1.482

SECTION 15–2 CHECKUP

1. Explain how Butterworth, Chebyshev, and Bessel responses differ.
2. What determines the response characteristic of a filter?
3. Name the basic parts of an active filter.

15–3 ACTIVE LOW-PASS FILTERS

Filters that use op-amps as the active element provide several advantages over passive filters (*R*, *L*, and *C* elements only). The op-amp provides gain, so the signal is not attenuated as it passes through the filter. The high input impedance of the op-amp prevents excessive loading of the driving source, and the low output impedance of the op-amp prevents the filter from being affected by the load that it is driving. Active filters are also easy to adjust over a wide frequency range without altering the desired response.

After completing this section, you should be able to

- ☐ **Identify and analyze active low-pass filters**
- ☐ Identify a single-pole low-pass filter circuit
  - Determine the closed-loop voltage gain
  - Determine the critical frequency
- ☐ Identify a Sallen-Key low-pass filter circuit
  - Describe the filter operation
  - Calculate the critical frequency
- ☐ Analyze cascaded low-pass filters
  - Explain how the roll-off rate is affected

A Single-Pole Filter

Figure 15–9(a) shows an active filter with a single low-pass *RC* frequency-selective circuit that provides a roll-off of −20 dB/decade above the critical frequency, as indicated by the response curve in Figure 15–9(b). The critical frequency of the single-pole filter is $f_c = 1/(2\pi RC)$. The op-amp in this filter is connected as a noninverting amplifier with the closed-loop voltage gain in the passband set by the values of R_1 and R_2.

$$A_{cl(\mathrm{NI})} = \frac{R_1}{R_2} + 1$$

Equation 15–6

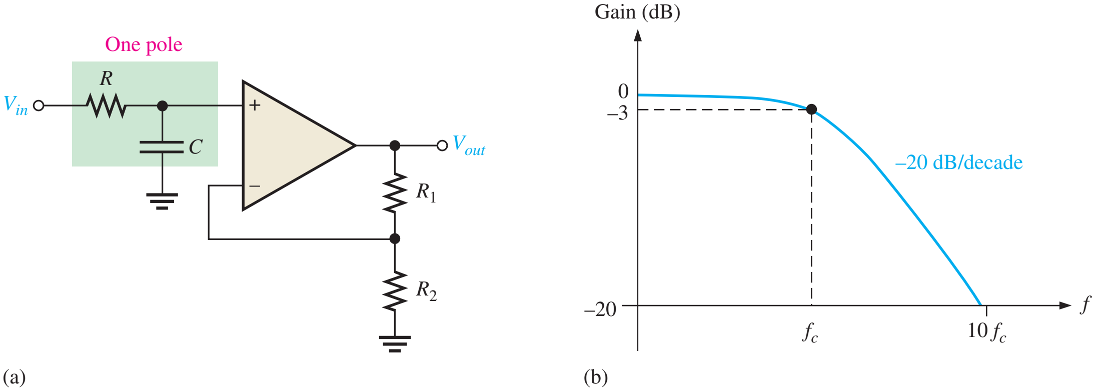


FIGURE 15–9

Single-pole active low-pass filter and response curve.

The Sallen-Key Low-Pass Filter

The Sallen-Key is one of the most common configurations for a second-order (two-pole) filter. It is also known as a VCVS (voltage-controlled voltage source) filter. A low-pass version of the Sallen-Key filter is shown in Figure 15–10. Notice that there are two low-pass *RC* circuits that provide a roll-off of −40 dB/decade above the critical frequency (assuming a Butterworth characteristic). One *RC* circuit consists of R_A and C_A, and the second circuit consists of R_B and C_B. A unique feature of the Sallen-Key low-pass filter is the capacitor C_A that provides feedback for shaping the response near the edge of the passband. The critical frequency for the Sallen-Key filter is

$$f_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$$

Equation 15–7

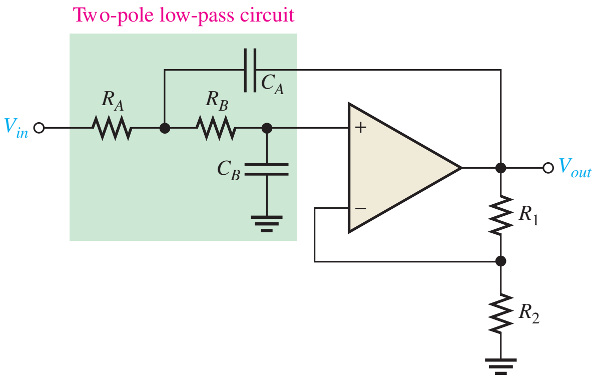


FIGURE 15–10

Basic Sallen-Key low-pass filter.

The component values can be made equal so that $R_A = R_B = R$ and $C_A = C_B = C$. In this case, the expression for the critical frequency simplifies to

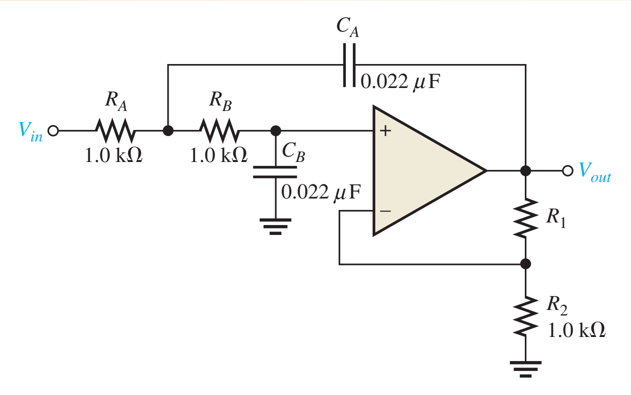
$$f_c = \frac{1}{2\pi RC}$$

As in the single-pole filter, the op-amp in the second-order Sallen-Key filter acts as a noninverting amplifier with the negative feedback provided by resistors R_1 and R_2. As you have learned, the damping factor is set by the values of R_1 and R_2, thus making the filter response either Butterworth, Chebyshev, or Bessel. For example, from Table 15–1, the R_1/R_2 ratio must be 0.586 to produce the damping factor of 1.414 required for a second-order Butterworth response.

EXAMPLE 15–3

Determine the critical frequency of the Sallen-Key low-pass filter in Figure 15–11, and set the value of R_1 for an approximate Butterworth response.

▶ FIGURE 15–11



Solution Since $R_A = R_B = R = 1.0\,\text{k}\Omega$ and $C_A = C_B = C = 0.022\,\mu\text{F}$,

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(1.0\,\text{k}\Omega)(0.022\,\mu\text{F})} = \mathbf{7.23\,kHz}$$

For a Butterworth response, $R_1/R_2 = 0.586$.

$$R_1 = 0.586R_2 = 0.586(1.0\,\text{k}\Omega) = \mathbf{586\,\Omega}$$

Select a standard value as near as possible to this calculated value.

Related Problem Determine f_c for Figure 15–11 if $R_A = R_B = R_2 = 2.2\,\text{k}\Omega$ and $C_A = C_B = 0.01\,\mu\text{F}$. Also determine the value of R_1 for a Butterworth response.

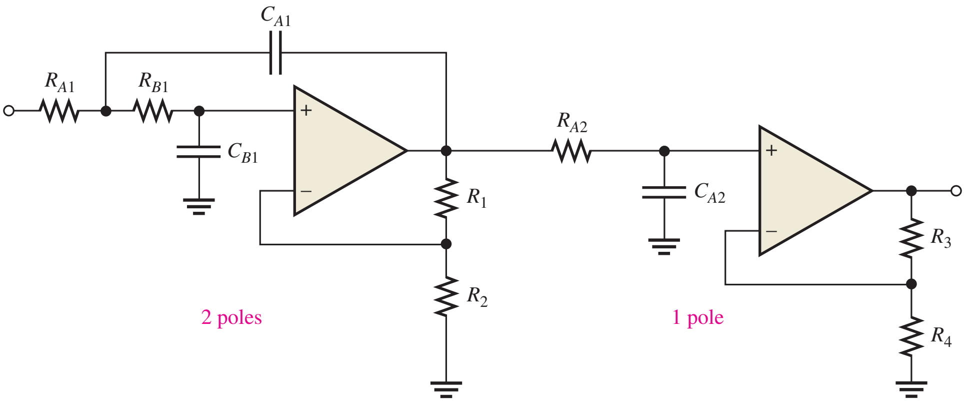
Open the Multisim file E15-03 in the Examples folder on the companion website. Determine the critical frequency and compare with the calculated value.

Cascaded Low-Pass Filters

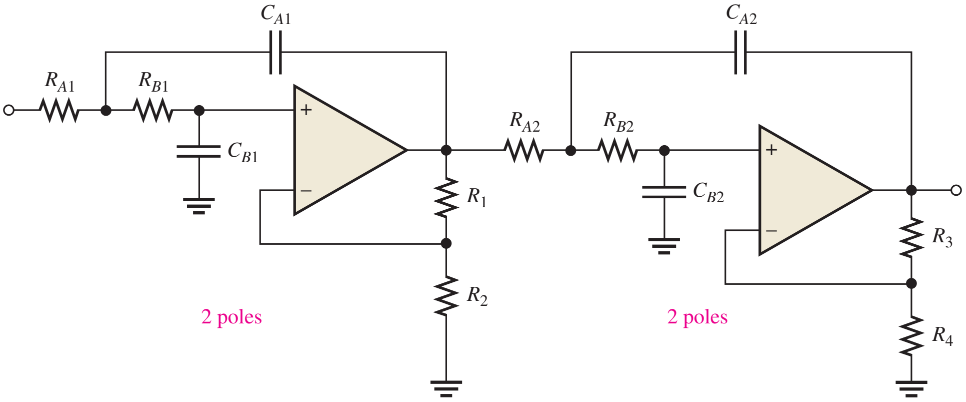
A three-pole filter is required to get a third-order low-pass response (−60 dB/decade). This is done by cascading a two-pole Sallen-Key low-pass filter and a single-pole low-pass filter, as shown in Figure 15–12(a). Figure 15–12(b) shows a four-pole configuration obtained by cascading two Sallen-Key (2-pole) low-pass filters. In general, a four-pole filter is preferred because it uses the same number of op-amps to achieve a faster roll-off.

FIGURE 15–12

Cascaded low-pass filters.



(a) Third-order configuration



(b) Fourth-order configuration

EXAMPLE 15–4

For the four-pole filter in Figure 15–12(b), determine the capacitance values required to produce a critical frequency of 2680 Hz if all the resistors in the *RC* low-pass circuits are 1.8 kΩ. Also select values for the feedback resistors to get a Butterworth response.

Solution Both stages must have the same f_c. Assuming equal-value capacitors,

$$f_c = \frac{1}{2\pi RC}$$

$$C = \frac{1}{2\pi R f_c} = \frac{1}{2\pi(1.8\text{ k}\Omega)(2680\text{ Hz})} = 0.033\ \mu\text{F}$$

$$C_{A1} = C_{B1} = C_{A2} = C_{B2} = \mathbf{0.033\ \boldsymbol{\mu}F}$$

Also select $R_2 = R_4 = 1.8\text{ k}\Omega$ for simplicity. Refer to Table 15–1. For a Butterworth response in the first stage, $DF = 1.848$ and $R_1/R_2 = 0.152$. Therefore,

$$R_1 = 0.152R_2 = 0.152(1800\ \Omega) = \mathbf{274\ \Omega}$$

Choose $R_1 = 270\ \Omega$.

In the second stage, $DF = 0.765$ and $R_3/R_4 = 1.235$. Therefore,

$$R_3 = 1.235R_4 = 1.235(1800\ \Omega) = \mathbf{2.22\ k\Omega}$$

Choose $R_3 = 2.2\text{ k}\Omega$.

Related Problem For the filter in Figure 15–12(b), determine the capacitance values for $f_c = 1\text{ kHz}$ if all the filter resistors are 680 Ω. Also specify the values for the feedback resistors to produce a Butterworth response.

SECTION 15–3 CHECKUP

1. How many poles does a second-order low-pass filter have? How many resistors and how many capacitors are used in the frequency-selective circuit?
2. Why is the damping factor of a filter important?
3. What is the primary purpose of cascading low-pass filters?

15–4 ACTIVE HIGH-PASS FILTERS

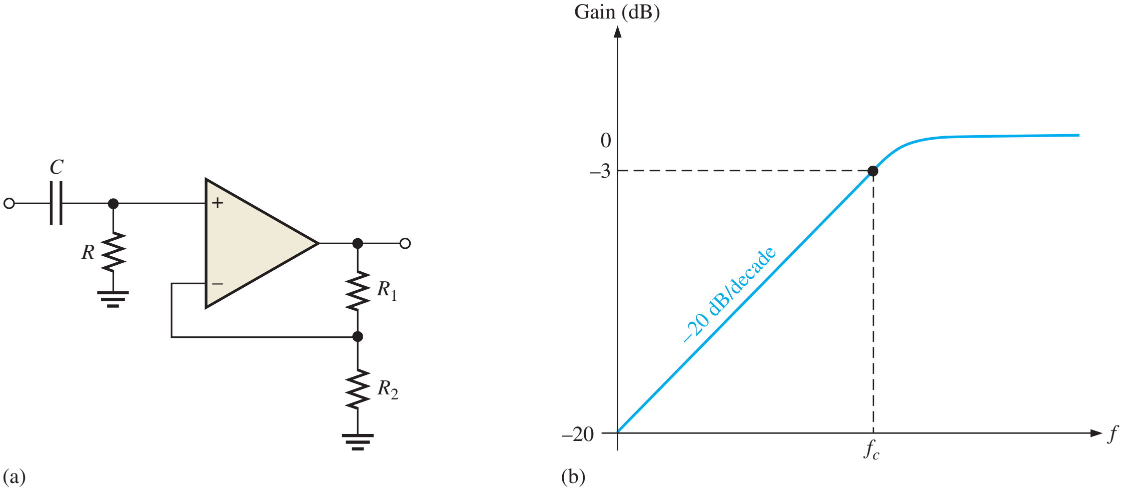
In high-pass filters, the roles of the capacitor and resistor are reversed in the *RC* circuits. Otherwise, the basic parameters are the same as for the low-pass filters.

After completing this section, you should be able to

- ❑ **Identify and analyze active high-pass filters**
- ❑ Identify a single-pole high-pass filter circuit
  - ◆ Explain limitations at higher pass-band frequencies
- ❑ Identify a Sallen-Key high-pass filter circuit
  - ◆ Describe the filter operation
  - ◆ Calculate component values
- ❑ Discuss cascaded high-pass filters
  - ◆ Describe a six-pole filter

A Single-Pole Filter

A high-pass active filter with a −20 dB/decade roll-off is shown in Figure 15–13(a). Notice that the input circuit is a single high-pass *RC* circuit. The negative feedback circuit is the same as for the low-pass filters previously discussed. The high-pass response curve is shown in Figure 15–13(b).



▲ FIGURE 15–13

Single-pole active high-pass filter and response curve.

Ideally, a high-pass filter passes all frequencies above f_c without limit, as indicated in Figure 15–14(a), although in practice, this is not the case. As you have learned, all op-amps inherently have internal *RC* circuits that limit the amplifier's response at high frequencies.

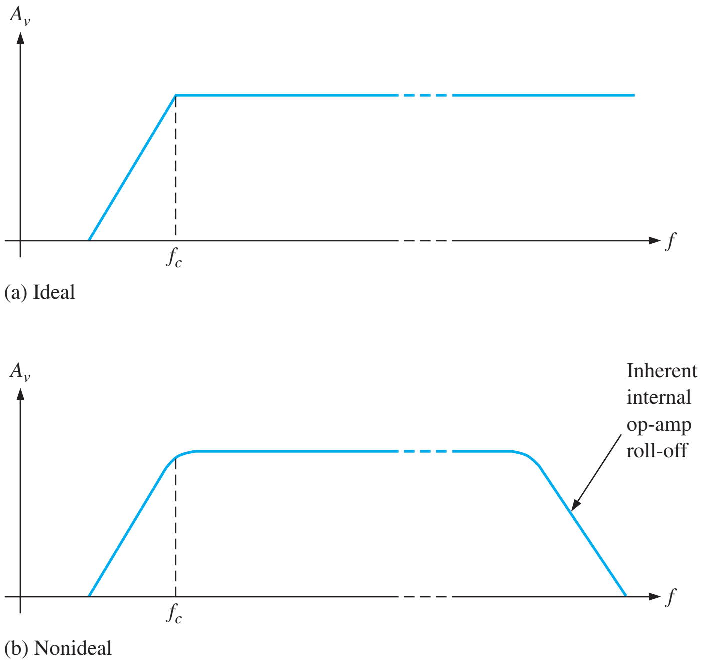


FIGURE 15–14

High-pass filter response.

Therefore, there is an upper-frequency limit on the high-pass filter's response which, in effect, makes it a band-pass filter with a very wide bandwidth. In the majority of applications, the internal high-frequency limitation is so much greater than that of the filter's critical frequency that the limitation can be neglected. In some applications, discrete transistors are used for the gain element to increase the high-frequency limitation beyond that realizable with available op-amps.

The Sallen-Key High-Pass Filter

A high-pass Sallen-Key configuration is shown in Figure 15–15. The components R_A, C_A, R_B, and C_B form the two-pole frequency-selective circuit. Notice that the positions of the resistors and capacitors in the frequency-selective circuit are opposite to those in the low-pass configuration. As with the other filters, the response characteristic can be optimized by proper selection of the feedback resistors, R_1 and R_2.

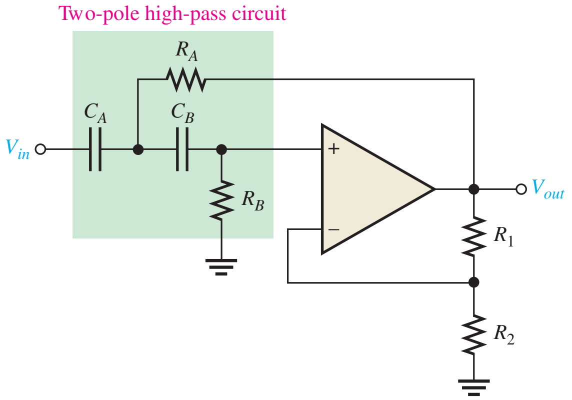


FIGURE 15–15

Basic Sallen-Key high-pass filter.

EXAMPLE 15–5

Choose values for the Sallen-Key high-pass filter in Figure 15–15 to implement an equal-value second-order Butterworth response with a critical frequency of approximately 10 kHz.

Solution Start by selecting a value for R_A and R_B (R_1 or R_2 can also be the same value as R_A and R_B for simplicity).

$$R = R_A = R_B = R_2 = \mathbf{3.3\,k\Omega} \text{ (an arbitrary selection)}$$

Next, calculate the capacitance value from $f_c = 1/(2\pi RC)$.

$$C = C_A = C_B = \frac{1}{2\pi R f_c} = \frac{1}{2\pi(3.3\,\text{k}\Omega)(10\,\text{kHz})} = \mathbf{0.0048\,\mu F}$$

For a Butterworth response, the damping factor must be 1.414 and $R_1/R_2 = 0.586$.

$$R_1 = 0.586R_2 = 0.586(3.3\,\text{k}\Omega) = \mathbf{1.93\,k\Omega}$$

If you had chosen $R_1 = 3.3\,\text{k}\Omega$, then

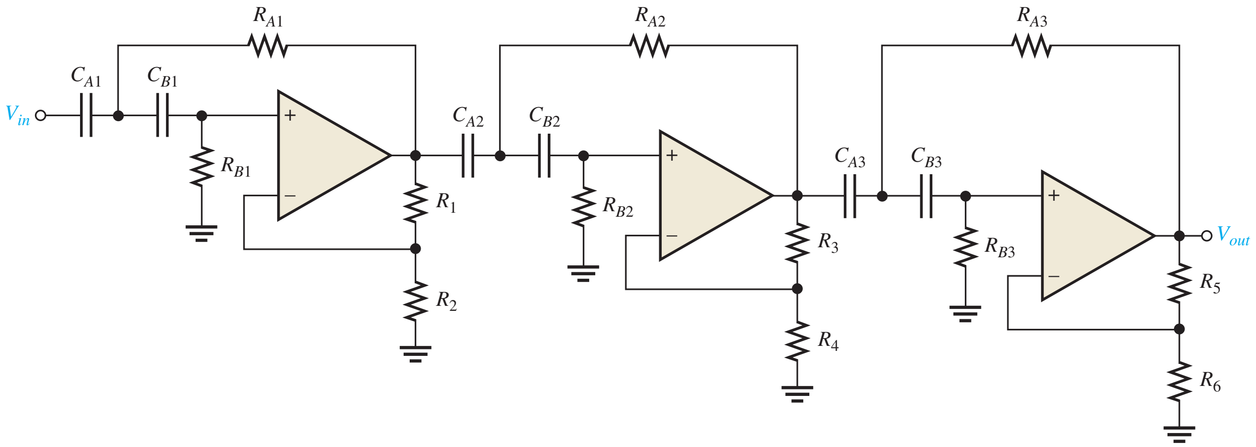
$$R_2 = \frac{R_1}{0.586} = \frac{3.3\,\text{k}\Omega}{0.586} = 5.63\,\text{k}\Omega$$

Either way, an approximate Butterworth response is realized by choosing the nearest standard values.

Related Problem Select values for all the components in the high-pass filter of Figure 15–15 to obtain an $f_c = 300$ Hz. Use equal-value components with $R = 10\,\text{k}\Omega$ and optimize for a Butterworth response.

Cascading High-Pass Filters

As with the low-pass configuration, first- and second-order high-pass filters can be cascaded to provide three or more poles and thereby create faster roll-off rates. Figure 15–16 shows a six-pole high-pass filter consisting of three Sallen-Key two-pole stages. With this configuration optimized for a Butterworth response, a roll-off of −120 dB/decade is achieved.



▲ FIGURE 15–16

Sixth-order high-pass filter.

SECTION 15–4 CHECKUP

1. How does a high-pass Sallen-Key filter differ from the low-pass configuration?
2. To increase the critical frequency of a high-pass filter, would you increase or decrease the resistor values?
3. If three two-pole high-pass filters and one single-pole high-pass filter are cascaded, what is the resulting roll-off?

15–5 ACTIVE BAND-PASS FILTERS

As mentioned, band-pass filters pass all frequencies bounded by a lower-frequency limit and an upper-frequency limit and reject all others lying outside this specified band. A band-pass response can be thought of as the overlapping of a low-frequency response curve and a high-frequency response curve.

After completing this section, you should be able to

- ❑ **Analyze basic types of active band-pass filters**
- ❑ Describe how to cascade low-pass and high-pass filters to create a band-pass filter
  - ◆ Calculate the critical frequencies and the center frequency
- ❑ Identify and analyze a multiple-feedback band-pass filter
  - ◆ Determine the center frequency, quality factor (Q), and bandwidth ◆ Calculate the voltage gain
- ❑ Identify and describe the state-variable filter
  - ◆ Explain the basic filter operation ◆ Determine the Q
- ❑ Identify and discuss the biquad filter

Cascaded Low-Pass and High-Pass Filters

One way to implement a band-pass filter is a cascaded arrangement of a high-pass filter and a low-pass filter, as shown in Figure 15–17(a), as long as the critical frequencies are sufficiently separated. Each of the filters shown is a Sallen-Key Butterworth configuration so that the roll-off rates are −40 dB/decade, indicated in the composite response curve of Figure 15–17(b). The critical frequency of each filter is chosen so that the response curves overlap sufficiently, as indicated. The critical frequency of the high-pass filter must be sufficiently lower than that of the low-pass stage. This filter is generally limited to wide bandwidth applications.

The lower frequency f_{c1} of the passband is the critical frequency of the high-pass filter. The upper frequency f_{c2} is the critical frequency of the low-pass filter. Ideally, as discussed earlier, the center frequency f_0 of the passband is the geometric mean of f_{c1} and f_{c2}. The following formulas express the three frequencies of the band-pass filter in Figure 15–17.

$$f_{c1} = \frac{1}{2\pi\sqrt{R_{A1}R_{B1}C_{A1}C_{B1}}}$$

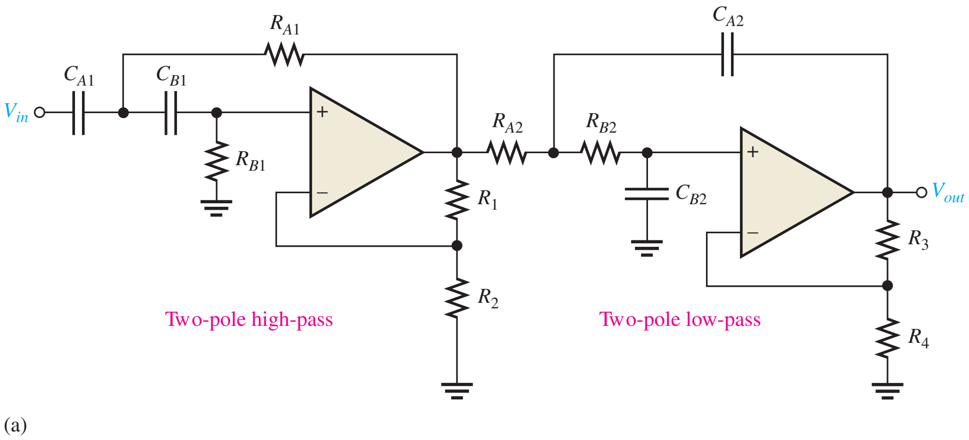
$$f_{c2} = \frac{1}{2\pi\sqrt{R_{A2}R_{B2}C_{A2}C_{B2}}}$$

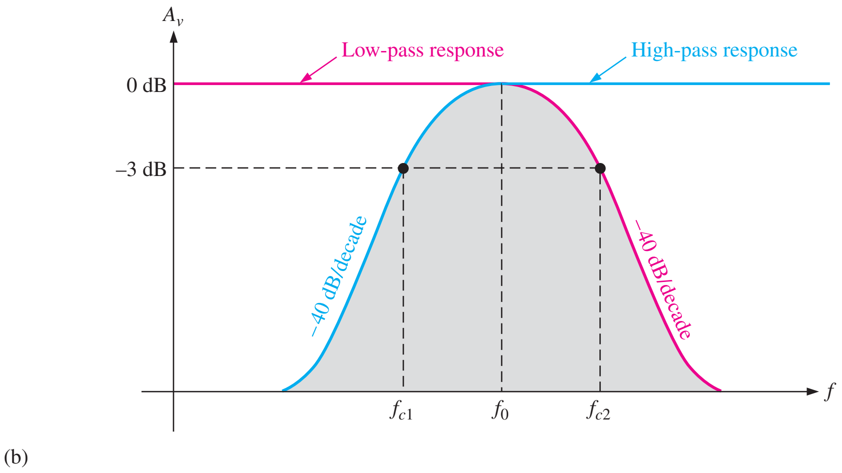
$$f_0 = \sqrt{f_{c1}f_{c2}}$$

Of course, if equal-value components are used in implementing each filter, the critical frequency equations simplify to the form $f_c = 1/(2\pi RC)$.

FIGURE 15–17

Band-pass filter formed by cascading a two-pole high-pass and a two-pole low-pass filter (it does not matter in which order the filters are cascaded).


R_{A1}
C_{A2}
C_{A1}
C_{B1}
V_{in}
R_{B1}
R_{A2}
R_{B2}
R_1
C_{B2}
V_{out}
R_3
R_2
R_4
Two-pole high-pass
Two-pole low-pass
(a)

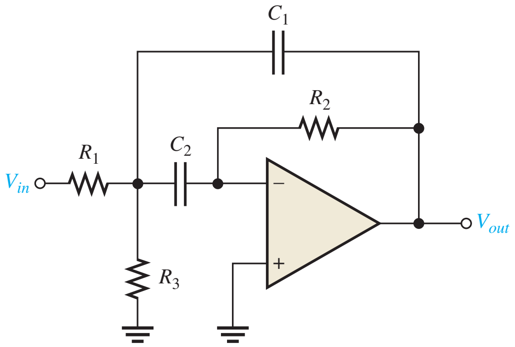


Multiple-Feedback Band-Pass Filter

Another type of filter configuration, shown in Figure 15–18, is a multiple-feedback band-pass filter. The two feedback paths are through R_2 and C_1. Components R_1 and C_1 provide the low-pass response, and R_2 and C_2 provide the high-pass response. The maximum gain, A_0, occurs at the center frequency. Q values of less than 10 are typical in this type of filter.

FIGURE 15–18

Multiple-feedback band-pass filter.


C_1
R_2
R_1
C_2
V_{in}
V_{out}
R_3

An expression for the center frequency is developed as follows, recognizing that R_1 and R_3 appear in parallel as viewed from the C_1 feedback path (with the V_{in} source replaced by a short).

$$f_0 = \frac{1}{2\pi\sqrt{(R_1 \| R_3)R_2C_1C_2}}$$

Making $C_1 = C_2 = C$ yields

$$f_0 = \frac{1}{2\pi\sqrt{(R_1 \| R_3)R_2C^2}} = \frac{1}{2\pi C\sqrt{(R_1 \| R_3)R_2}}$$

$$= \frac{1}{2\pi C}\sqrt{\frac{1}{R_2(R_1 \| R_3)}} = \frac{1}{2\pi C}\sqrt{\left(\frac{1}{R_2}\right)\left(\frac{1}{R_1R_3/R_1 + R_3}\right)}$$

$$\boldsymbol{f_0 = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1R_2R_3}}}$$

Equation 15–8

A value for the capacitors is chosen and then the three resistor values are calculated to achieve the desired values for f_0, BW, and A_0. As you know, the Q can be determined from the relation $Q = f_0/BW$. The resistor values can be found using the following formulas (stated without derivation):

$$R_1 = \frac{Q}{2\pi f_0 CA_0}$$

$$R_2 = \frac{Q}{\pi f_0 C}$$

$$R_3 = \frac{Q}{2\pi f_0 C(2Q^2 - A_0)}$$

To develop a gain expression, solve for Q in the R_1 and R_2 formulas as follows:

$$Q = 2\pi f_0 A_0 CR_1$$
$$Q = \pi f_0 CR_2$$

Then,

$$2\pi f_0 A_0 CR_1 = \pi f_0 CR_2$$

Cancelling yields

$$2A_0R_1 = R_2$$

$$\boldsymbol{A_0 = \frac{R_2}{2R_1}}$$

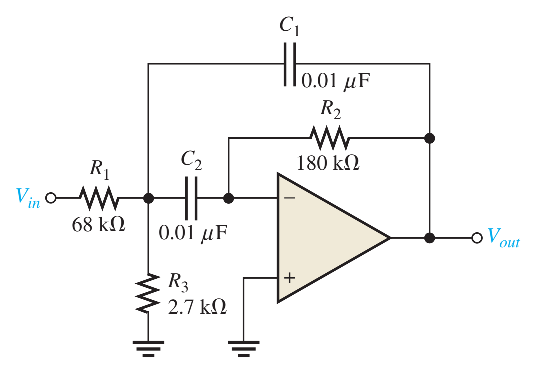
Equation 15–9

In order for the denominator of the equation $R_3 = Q/[2\pi f_0 C(2Q^2 - A_0)]$ to be positive, $A_0 < 2Q^2$, which imposes a limitation on the gain.

EXAMPLE 15–6

Determine the center frequency, maximum gain, and bandwidth for the filter in Figure 15–19.

▶ **FIGURE 15–19**



Solution

$$f_0 = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1R_2R_3}} = \frac{1}{2\pi(0.01\ \mu\text{F})}\sqrt{\frac{68\ \text{k}\Omega + 2.7\ \text{k}\Omega}{(68\ \text{k}\Omega)(180\ \text{k}\Omega)(2.7\ \text{k}\Omega)}} = \mathbf{736\ Hz}$$

$$A_0 = \frac{R_2}{2R_1} = \frac{180\ \text{k}\Omega}{2(68\ \text{k}\Omega)} = \mathbf{1.32}$$

$$Q = \pi f_0 C R_2 = \pi(736\ \text{Hz})(0.01\ \mu\text{F})(180\ \text{k}\Omega) = 4.16$$

$$BW = \frac{f_0}{Q} = \frac{736\ \text{Hz}}{4.16} = \mathbf{177\ Hz}$$

Related Problem If R_2 in Figure 15–19 is increased to 330 kΩ, determine the gain, center frequency, and bandwidth of the filter?

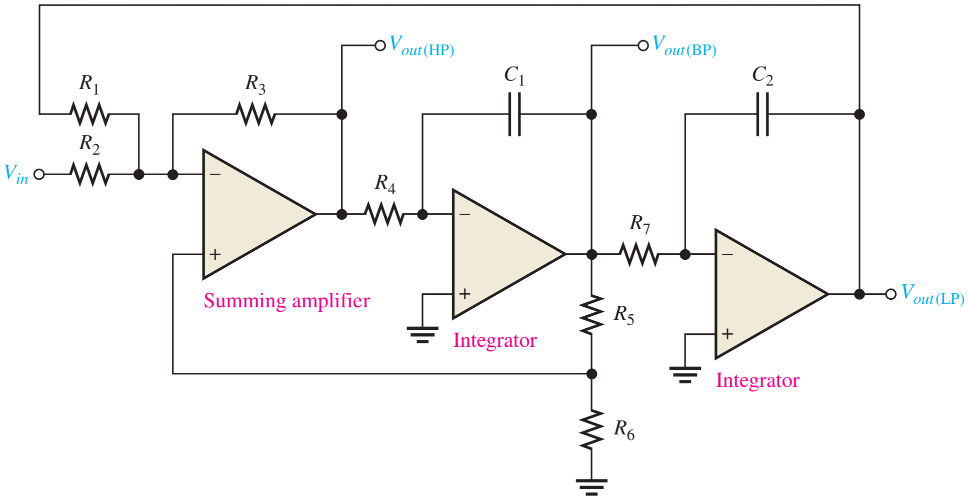
Open the Multisim file E15-06 in the Examples folder on the companion website. Measure the center frequency and the bandwidth and compare to the calculated values.

State-Variable Filter

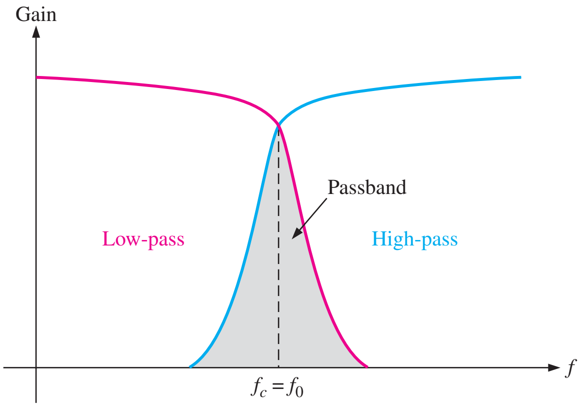
The state-variable or universal active filter is widely used for band-pass applications. As shown in Figure 15–20, it consists of a summing amplifier and two op-amp integrators (which act as single-pole low-pass filters) that are combined in a cascaded arrangement to form a second-order filter. Although used primarily as a band-pass (BP) filter, the state-variable configuration also provides low-pass (LP) and high-pass (HP) outputs. The center frequency is set by the *RC* circuits in both integrators. When used as a band-pass filter, the critical frequencies of the integrators are usually made equal, thus setting the center frequency of the passband.

▶ FIGURE 15–20

State-variable filter.



Basic Operation At input frequencies below f_c, the input signal passes through the summing amplifier and integrators and is fed back 180° out of phase. Thus, the feedback signal and input signal cancel for all frequencies below approximately f_c. As the low-pass response of the integrators rolls off, the feedback signal diminishes, thus allowing the input to pass through to the band-pass output. Above f_c, the low-pass response disappears, thus preventing the input signal from passing through the integrators. As a result, the band-pass filter output peaks sharply at f_c, as indicated in Figure 15–21. Stable Qs up to 100 can be obtained with



▲ FIGURE 15–21

General state-variable response curves.

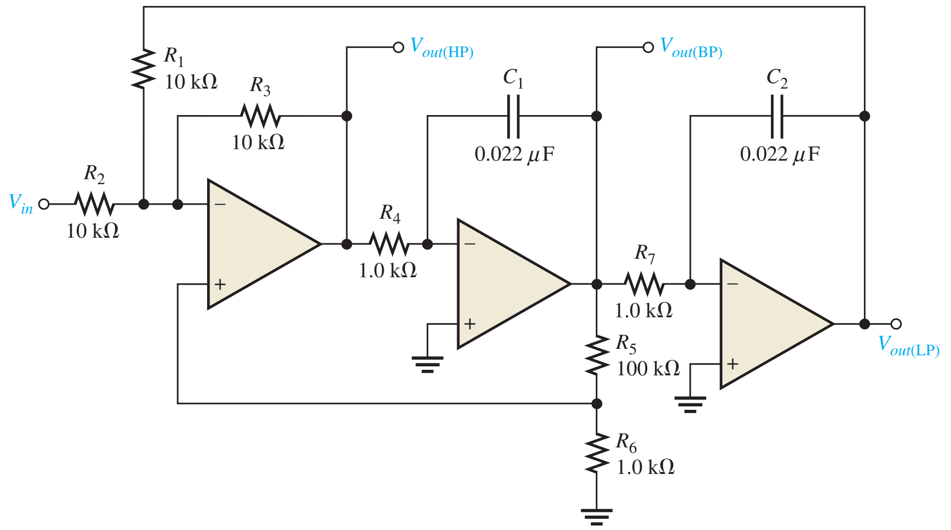
this type of filter. The Q is set by the feedback resistors R_5 and R_6 according to the following equation:

$$Q = \frac{1}{3}\left(\frac{R_5}{R_6} + 1\right)$$

The state-variable filter cannot be optimized for low-pass, high-pass, and narrow band-pass performance simultaneously for this reason: To optimize for a low-pass or a high-pass Butterworth response, DF must equal 1.414. Since $Q = 1/DF$, a Q of 0.707 will result. Such a low Q provides a very wide band-pass response (large BW and poor selectivity). For optimization as a narrow band-pass filter, the Q must be set high.

EXAMPLE 15–7

Determine the center frequency, Q, and BW for the passband of the state-variable filter in Figure 15–22.


R_1
10 kΩ
R_3
10 kΩ
$V_{out(HP)}$
C_1
0.022 μF
$V_{out(BP)}$
C_2
0.022 μF
V_{in}
R_2
10 kΩ
R_4
1.0 kΩ
R_7
1.0 kΩ
R_5
100 kΩ
R_6
1.0 kΩ
$V_{out(LP)}$

▲ FIGURE 15–22

Solution For each integrator,

$$f_c = \frac{1}{2\pi R_4 C_1} = \frac{1}{2\pi R_7 C_2} = \frac{1}{2\pi(1.0\text{ k}\Omega)(0.022\ \mu\text{F})} = 7.23\text{ kHz}$$

The center frequency is approximately equal to the critical frequencies of the integrators.

$$f_0 = f_c = \mathbf{7.23\ kHz}$$

$$Q = \frac{1}{3}\left(\frac{R_5}{R_6} + 1\right) = \frac{1}{3}\left(\frac{100\text{ k}\Omega}{1.0\text{ k}\Omega} + 1\right) = \mathbf{33.7}$$

$$BW = \frac{f_0}{Q} = \frac{7.23\text{ kHz}}{33.7} = \mathbf{215\ Hz}$$

Related Problem Determine f_0, Q, and BW for the filter in Figure 15–22 if $R_4 = R_6 = R_7 = 330\ \Omega$ with all other component values the same as shown on the schematic.

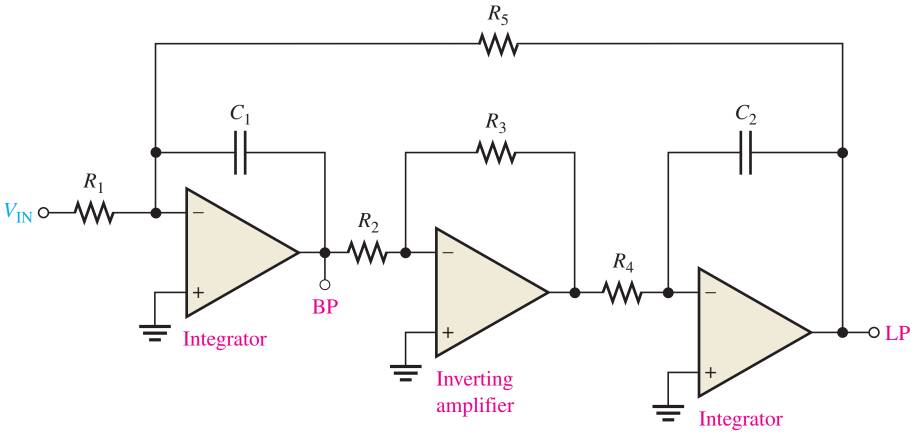
Open the Multisim file E15-07 in the Examples folder on the companion website. Measure the center frequency and the bandwidth and compare to the calculated values.

The Biquad Filter

The biquad filter is similar to the state-variable filter except that it consists of an integrator, followed by an inverting amplifier, and then another integrator, as shown in Figure 15–23. These differences in the configuration between a biquad and a state-variable filter result in some operational differences although both allow a very high Q value. In a biquad filter, the bandwidth is independent and the Q is dependent on the critical frequency; however, in the state-variable filter it is just the opposite: the bandwidth is dependent and the Q is independent on the critical frequency. Also, the biquad filter provides only band-pass and low-pass outputs.

▶ FIGURE 15–23

A biquad filter.



SECTION 15–5 CHECKUP

1. What determines selectivity in a band-pass filter?
2. One filter has a $Q = 5$ and another has a $Q = 25$. Which has the narrower bandwidth?
3. List the active elements that make up a state-variable filter.
4. List the active elements that make up a biquad filter.

15–6 ACTIVE BAND-STOP FILTERS

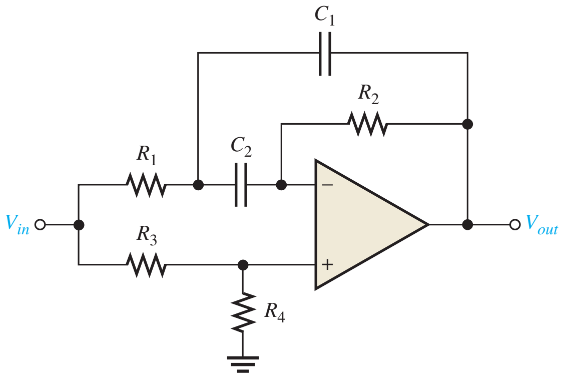
Band-stop filters reject a specified band of frequencies and pass all others. The response is opposite to that of a band-pass filter. Band-stop filters are sometimes referred to as notch filters.

After completing this section, you should be able to

- **Describe basic types of active band-stop filters**
- Identify and describe a multiple-feedback band-stop filter
- Identify and analyze the state-variable filter

Multiple-Feedback Band-Stop Filter

Figure 15–24 shows a multiple-feedback band-stop filter. Notice that this configuration is similar to the band-pass version in Figure 15–18 except that R_3 has been moved and R_4 has been added.

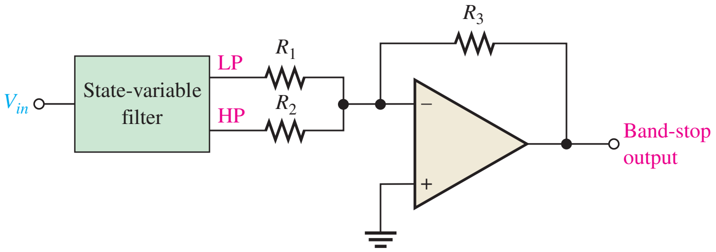


◀ FIGURE 15–24

Multiple-feedback band-stop filter.

State-Variable Band-Stop Filter

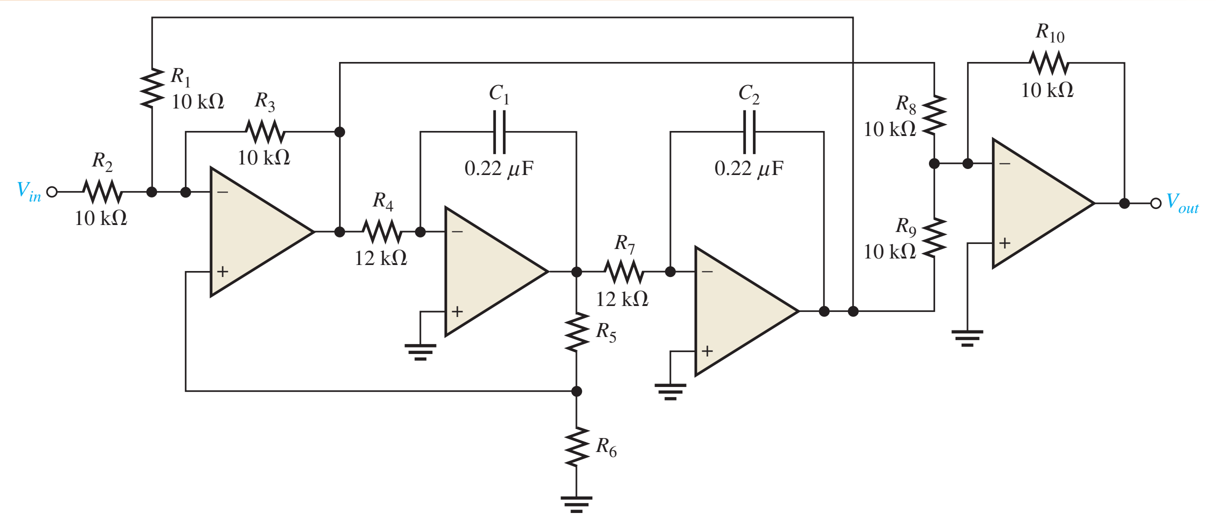
Summing the low-pass and the high-pass responses of the state-variable filter covered in Section 15–5 with a summing amplifier creates a band-stop filter, as shown in Figure 15–25. One important application of this filter is minimizing the 60 Hz “hum” in audio systems by setting the center frequency to 60 Hz.



▲ FIGURE 15–25

State-variable band-stop filter.

EXAMPLE 15–8 Verify that the band-stop filter in Figure 15–26 has a center frequency of 60 Hz, and optimize the filter for a Q of 10.



▲ FIGURE 15–26

Solution f_0 equals the f_c of the integrator stages. (In practice, component values are critical.)

$$f_0 = \frac{1}{2\pi R_4 C_1} = \frac{1}{2\pi R_7 C_2} = \frac{1}{2\pi(12\text{ k}\Omega)(0.22\ \mu\text{F})} = \mathbf{60\ Hz}$$

You can obtain a $Q = 10$ by choosing R_6 and then calculating R_5.

$$Q = \frac{1}{3}\left(\frac{R_5}{R_6} + 1\right)$$

$$R_5 = (3Q - 1)R_6$$

Choose $R_6 = \mathbf{3.3\ k\Omega}$. Then

$$R_5 = [3(10) - 1]3.3\text{ k}\Omega = \mathbf{95.7\ k\Omega}$$

Use the nearest standard value of 100 kΩ.

Related Problem How would you change the center frequency to 120 Hz in Figure 15–26?

Open the Multisim file E15-08 in the Examples folder on the companion website and verify that the center frequency is approximately 60 Hz.

SECTION 15–6 CHECKUP

1. How does a band-stop response differ from a band-pass response?
2. How is a state-variable band-pass filter converted to a band-stop filter?

15–7 FILTER RESPONSE MEASUREMENTS

Two methods of determining a filter's response by measurement are discrete point measurement and swept frequency measurement.

After completing this section, you should be able to

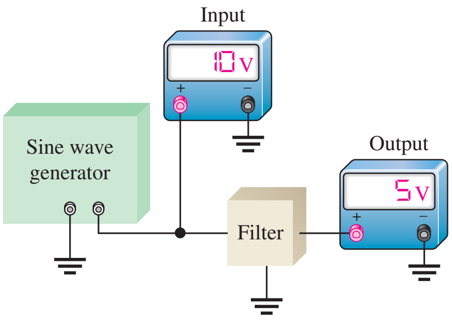
- **Discuss two methods for measuring frequency response**
- Explain discrete-point measurement
  - List the steps in the procedure
  - Show a test setup
- Explain swept frequency measurement
  - Show a test setup for this method using a spectrum analyzer
  - Show a test setup for this method using an oscilloscope

Discrete Point Measurement

Figure 15–27 shows an arrangement for taking filter output voltage measurements at discrete values of input frequency using common laboratory instruments. The general procedure is as follows:

1. Set the amplitude of the sine wave generator to a desired voltage level.
2. Set the frequency of the sine wave generator to a value well below the expected critical frequency of the filter under test. For a low-pass filter, set the frequency as near as possible to 0 Hz. For a band-pass filter, set the frequency well below the expected lower critical frequency.
3. Increase the frequency in predetermined steps sufficient to allow enough data points for an accurate response curve.
4. Maintain a constant input voltage amplitude while varying the frequency.
5. Record the output voltage at each value of frequency.
6. After recording a sufficient number of points, plot a graph of output voltage versus frequency.

If the frequencies to be measured exceed the frequency response of the DMM, an oscilloscope may have to be used instead.

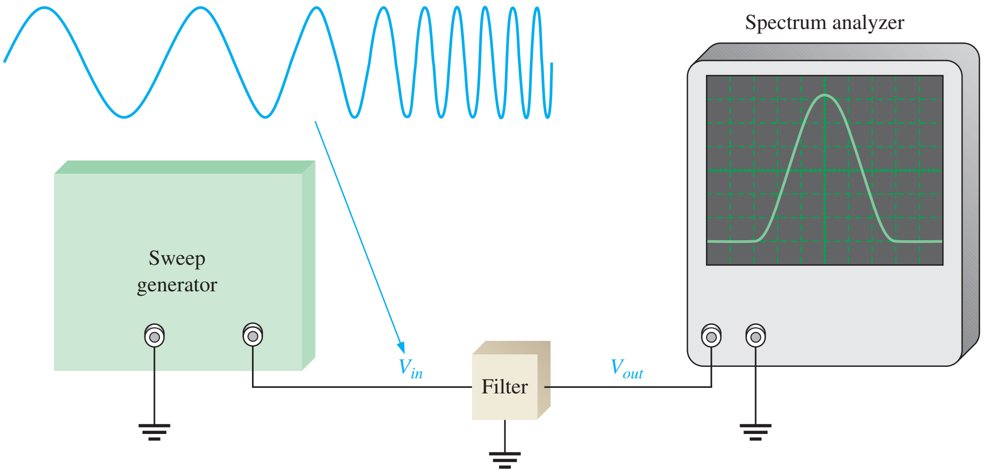


◀ FIGURE 15–27

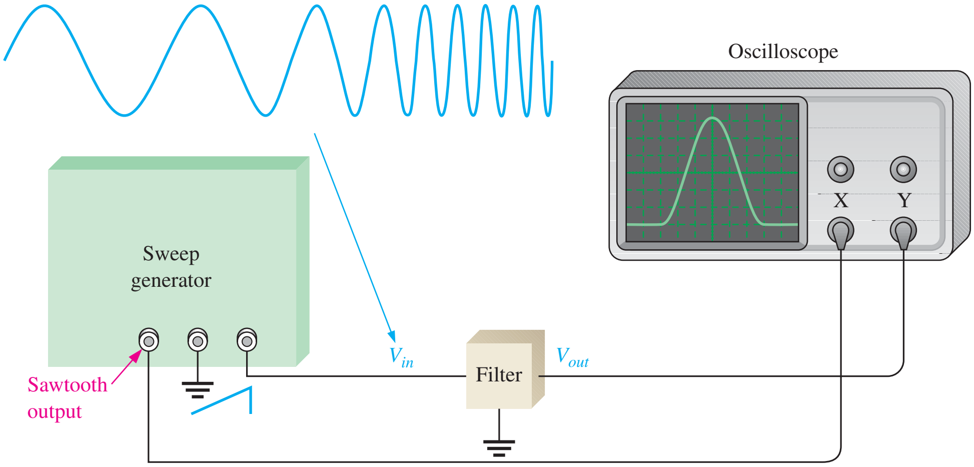
Test setup for discrete point measurement of the filter response. (Readings are arbitrary and for display only.)

Swept Frequency Measurement

The swept frequency method requires more elaborate test equipment than does the discrete point method, but it is much more efficient and can result in a more accurate response curve. A general test setup is shown in Figure 15–28(a) using a swept frequency



(a) Test setup for a filter response using a spectrum analyzer



(b) Test setup for a filter response using an oscilloscope. The scope is placed in X-Y mode. The sawtooth waveform from the sweep generator drives the X-channel of the oscilloscope.

▲ **FIGURE 15–28**

Test setup for swept frequency measurement of the filter response.

generator and a spectrum analyzer. Figure 15–28(b) shows how the test can be made with an oscilloscope.

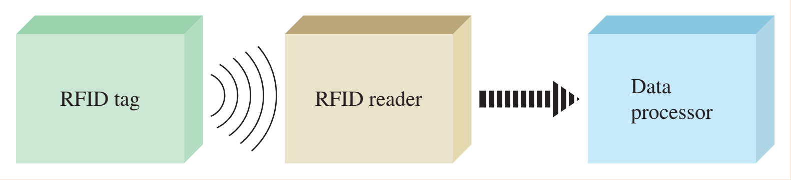
The swept frequency generator produces a constant amplitude output signal whose frequency increases linearly between two preset limits, as indicated in Figure 15–28. The spectrum analyzer is essentially an elaborate oscilloscope that can be calibrated for a desired *frequency span/division* rather than for the usual *time/division* setting. Therefore, as the input frequency to the filter sweeps through a preselected range, the response curve is traced out on the screen of the spectrum analyzer or an oscilloscope.

SECTION 15–7 CHECKUP

1. What is the purpose of the two tests discussed in this section?
2. Name one disadvantage and one advantage of each test method.

Application Activity: *RFID System*

RFID (radio frequency identification) is a technology that enables the tracking and/or identification of objects. Typically, an RFID system contains an *RFID tag* that consists of an IC chip that transmits data about the object, an *RFID reader* that receives transmitted data from the tag, and a *data-processing system* that processes and stores the data passed to it by the reader. A basic block diagram is shown in Figure 15–29.



▲ FIGURE 15–29

Basic block diagram of an RFID system.

The RFID Tag

RFID tags are tiny, very thin microchips with memory and a coil antenna. The tags listen for a radio signal sent by an RFID reader. When a tag receives a signal, it responds by transmitting its unique ID code and other data back to the reader.

Passive RFID Tag This type of tag does not require batteries. The tag is inactive until powered by the energy from the electromagnetic field of an RFID reader. Passive tags can be read from distances up to about 20 feet and are generally read-only, meaning the data they contain cannot be altered or written over.

Active RFID Tag This type of tag is powered by a battery and is capable of communicating up to 100 feet or more from the RFID reader. Generally, the active tag is larger and more expensive than a passive tag, but can hold more data about the product and is commonly used for identification of high-value assets. Active tags may be read-write, meaning the data they contain can be written over.

Tags are available in a variety of shapes. Depending on the application, they may be embedded in glass or epoxy, or they may be in label or card form. Another type of tag, often called the *smart label,* is a paper (or similar material) label with printing, but also with the RF circuitry and antenna embedded in it.

Some advantages of RFID tags compared to bar codes are

- Non-line-of-sight identification
- More information can be stored
- Coverage at greater distances
- Unattended operations are possible
- Ability to identify moving objects that have tags embedded
- Can be used in diverse environments

Disadvantages of RFID tags are that they are expensive compared to the bar code and they are bulkier because the electronics is embedded in the tag.

RFID tags and readers must be tuned to the same frequency to communicate. RFID systems use many different frequencies, but generally the most common are low frequency

(125 kHz), high frequency (13.56 MHz), and ultra-high frequency, or UHF (850–900 MHz). Microwave (2.45 GHz) is also used in some applications. The frequency used depends on the particular type of application.

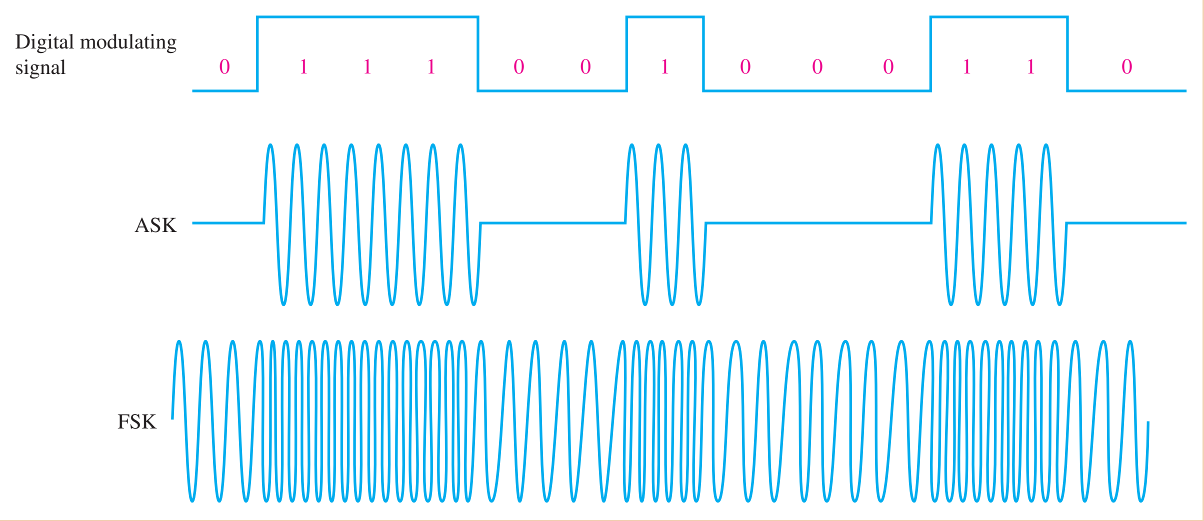
Low-frequency systems are the least expensive and have the shortest range. They are most commonly used in security access, asset tracking, and animal identification applications. High-frequency systems are used for applications such as railroad car tracking and automated toll collection.

Some typical RFID application areas are

- Metering applications such as electronic toll collection
- Inventory control and tracking such as merchandise control
- Asset tracking and recovery
- Tracking parts moving through a manufacturing process
- Tracking goods in a supply chain

The RFID Reader

Data is stored on the RFID tag in digital form and is transmitted to the reader as a modulated signal. Many RFID systems use ASK (amplitude shift keying) or FSK (frequency shift keying). In ASK, the amplitude of a carrier signal is varied by the digital data. In FSK, the frequency of a carrier signal is varied by the digital data. Examples of these forms of modulation are shown Figure 15–30. In this system, the carrier is 125 kHz, and the modulating signal is a digital waveform at the rate of 10 kHz, representing a stream of 1s and 0s.

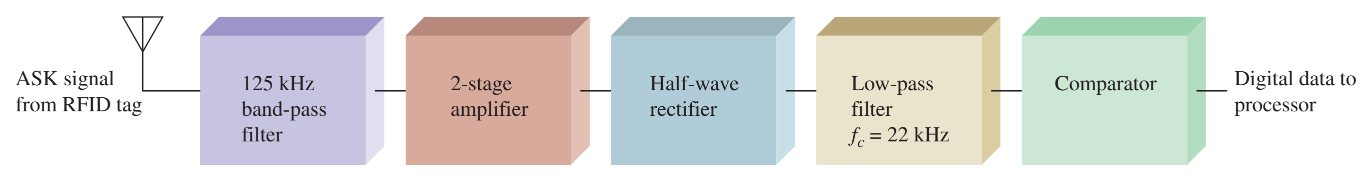


▲ FIGURE 15–30

Examples of ASK and FSK modulation transmitted by an RFID tag.

Project

Your company is developing a new RFID reader using ASK modulation at a carrier frequency of 125 kHz. A block diagram is shown in Figure 15–31. The purpose of each block is as follows. The band-pass filter passes the 125 kHz signal and reduces signals and noise from other sources; the 2-stage amplifier increases the very small signal from the tag to a usable level; the rectifier eliminates the negative portions of the modulated signal; the low-pass filter eliminates the 125 kHz carrier frequency but passes the 10 kHz


ASK signal from RFID tag
125 kHz band-pass filter
2-stage amplifier
Half-wave rectifier
Low-pass filter f_c = 22 kHz
Comparator
Digital data to processor

▲ **FIGURE 15–31**

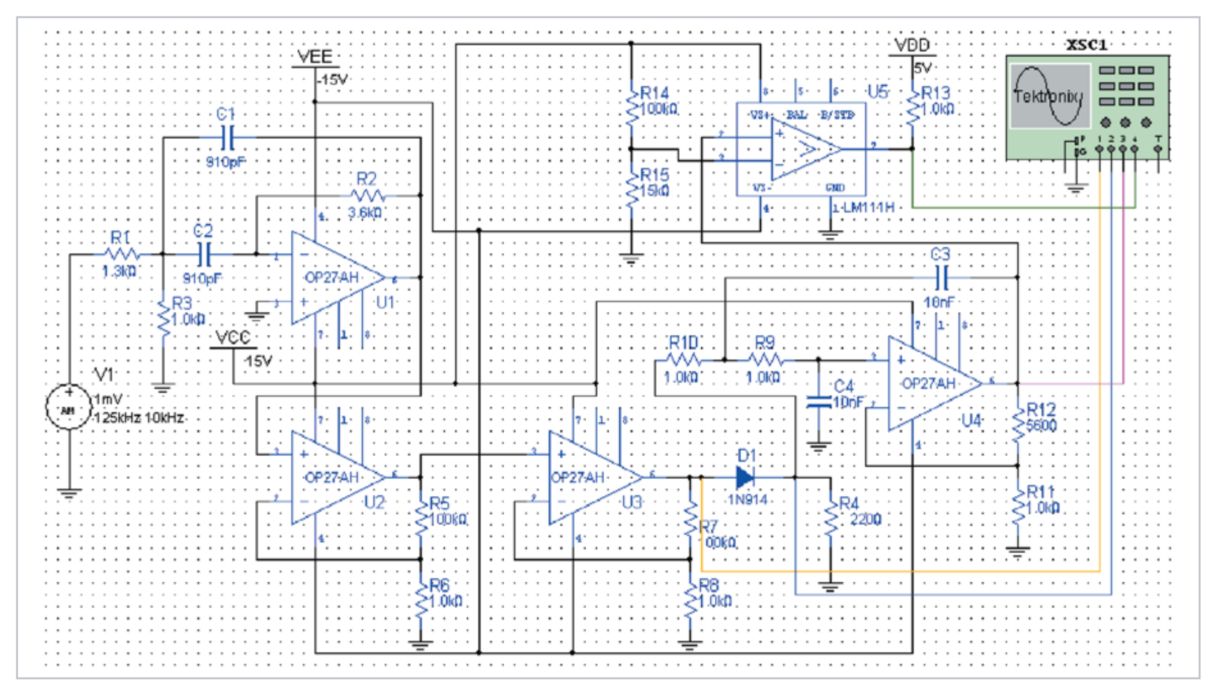
Block diagram of RFID reader.

modulating signal; and the comparator restores the digital signal to a usable stream of digital data.

1. In general, what are RFID systems used for?
2. Name the three basic components of an RFID system.
3. Explain the purpose of an RFID tag.
4. Explain the purpose of an RFID reader.

Simulation

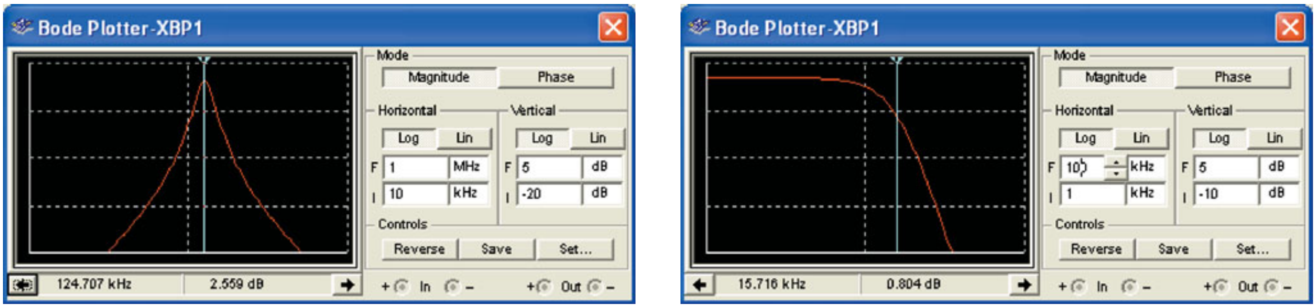
The RFID reader is simulated with Multisim using an input signal of 1 mV at 125 kHz to represent the output of the RFID tag. For purposes of simulation, the 125 kHz carrier is modulated with a 10 kHz sine wave although the actual modulating signal will be a pulse waveform containing digital data. In Multisim it is difficult to produce a sinusoidal carrier signal modulated with a pulse signal, so the sinusoidal modulating signal serves to verify system operation. The simulated circuit is shown in Figure 15–32. The band-pass filter is U1, the amplifier stages are U2 and U3, the half-wave rectifier is D1, the low-pass filter is U4, and the comparator is U5. Datasheets for the OP27AH op-amp and the LM111H comparator are available at www.analog.com.


VEE
-15V
C1
910pF
R2
3.6kΩ
C2
910pF
R1
1.3kΩ
R3
1.0kΩ
OP27AH
U1
VCC
15V
V1
1mV
125kHz 10kHz
OP27AH
U2
R5
100kΩ
R6
1.0kΩ
OP27AH
U3
R7
100kΩ
R8
1.0kΩ
D1
1N914
R4
220Ω
R10
1.0kΩ
R9
1.0kΩ
C4
10nF
C3
10nF
OP27AH
U4
R12
560Ω
R11
1.0kΩ
R14
100kΩ
R15
15kΩ
U5
LM111H
VDD
5V
R13
1.0kΩ
XSC1
Tektronix

▲ **FIGURE 15–32**

Multisim circuit screen for the RFID reader.

The frequency responses of the band-pass filter and the low-pass filter are shown on the Bode plotters in Figure 15–33. As you can see, the peak response of the band-pass filter is approximately 125 kHz and the critical frequency of the low-pass filter is approximately 16 kHz.


Bode Plotter-XBP1
Mode: Magnitude
Horizontal: Log; F 1 MHz; I 10 kHz
Vertical: Log; F 5 dB; I -20 dB
124.707 kHz 2.559 dB

Bode Plotter-XBP1
Mode: Magnitude
Horizontal: Log; F 10 kHz; I 1 kHz
Vertical: Log; F 5 dB; I -10 dB
15.716 kHz 0.804 dB
Mode
Magnitude
Phase
Horizontal
Vertical
Log
Lin
Controls
Reverse
Save
Set...
In
Out

(a) Band-pass response

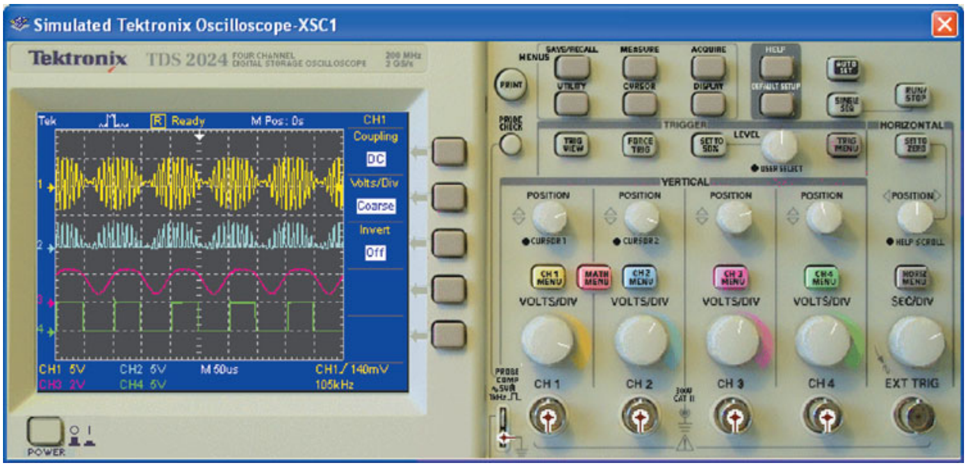
(b) Low-pass response

▲ FIGURE 15–33

Bode plots for the RFID reader filters.

5. What is the purpose of the band-pass filter in the RFID reader?
6. What is the purpose of the low-pass filter in the RFID reader?
7. Calculate the gain of each amplifier in the reader in Figure 15–32.
8. Use the formula for a multiple-feedback band-pass filter to verify the center frequency of the band-pass filter in the reader.
9. What type of response characteristic is the low-pass filter set up for?
10. Calculate the critical frequency of the low-pass filter and compare to the measured value.
11. Calculate the reference voltage for the comparator and explain why a reference above ground is necessary.

Measurements at points on the reader circuit are shown on the oscilloscope in Figure 15–34. The top waveform is the modulated carrier at the output of amplifier U3. The second waveform is the output of the rectifier D1. The third waveform is the output of the low-pass filter (notice that the carrier frequency has been removed by the filter). The bottom waveform is the output of the comparator and represents the digital data sent to the processor.


Simulated Tektronix Oscilloscope-XSC1
CH1 Coupling DC
Volts/Div Coarse
Invert Off
CH1 5V CH2 5V M 50us CH1 ∕ 140mV
CH3 2V CH4 5V 105kHz
Tektronix
TDS 2024
Tek
Ready
M Pos: 0s
1
2
3
4
MENUS
SAVE/RECALL
MEASURE
ACQUIRE
HELP
UTILITY
CURSOR
DISPLAY
DEFAULT SETUP
PRINT
PROBE CHECK
TRIGGER
LEVEL
TRIG VIEW
FORCE TRIG
SET TO 50%
TRIG MENU
RUN/STOP
SINGLE SEQ
AUTO SET
HORIZONTAL
SET TO ZERO
VERTICAL
POSITION
CURSOR 1
CURSOR 2
HELP SCROLL
CH 1 MENU
MATH MENU
CH 2 MENU
CH 3 MENU
CH 4 MENU
HORIZ MENU
VOLTS/DIV
SEC/DIV
CH 1
CH 2
CH 3
CH 4
EXT TRIG
POWER

▲ FIGURE 15–34

RFID reader waveforms.

Simulate the RFID reader circuit using your Multisim software. Observe the operation with the oscilloscope and Bode plotter.

Prototyping and Testing

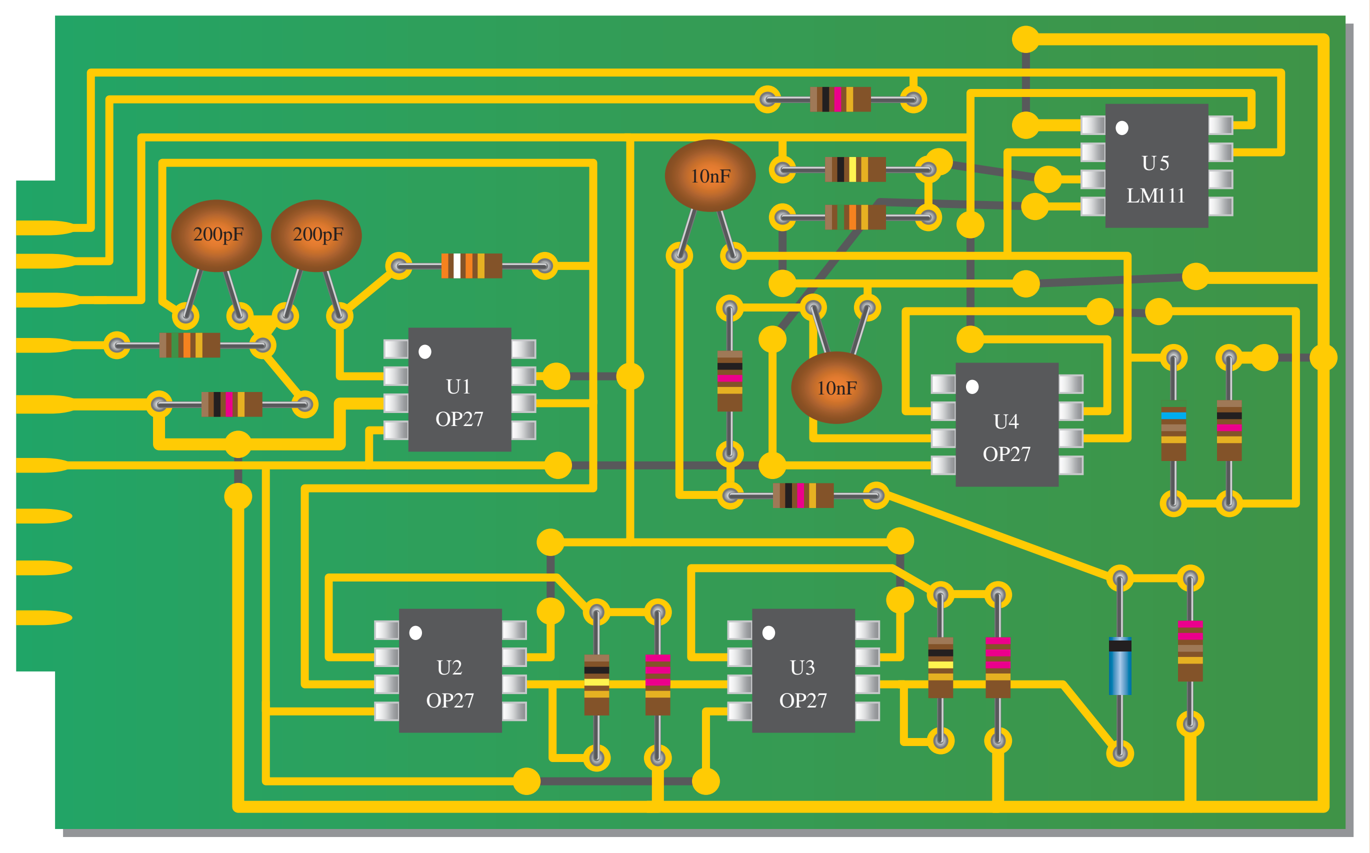
Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

Lab Experiment

To build and test a low-pass filter similar to one used in the RFID reader, go to Experiment 15–A in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The RFID reader circuit is implemented on a printed circuit board as shown in Figure 15–35. The dark gray lines represent backside traces.



▲ FIGURE 15–35

RFID reader board.

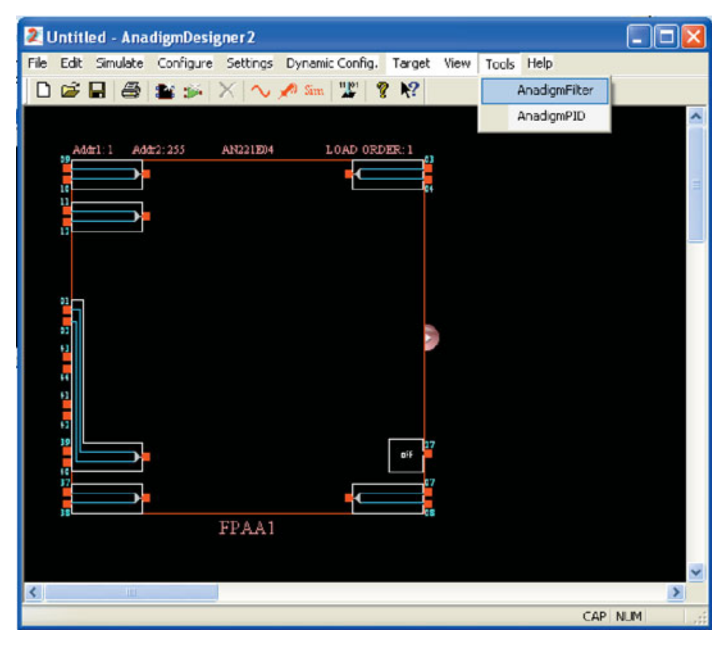
12. Check the printed circuit board and verify that it agrees with the simulation schematic in Figure 15–32.
13. Label each input and output pin according to function.

Programmable Analog Technology

The material you have learned in this chapter is necessary to give you a basic understanding of active filters. However, filter design can be quite complex mathematically. To avoid tedious calculations and trial-and-error breadboarding, the preferred method for development of many filters is to use computer software and then download the design to a programmable analog array. AnadigmDesigner2 software is used in this section to illustrate the ease with which active filters can be developed and implemented in hardware. If you have checked out the optional *Programmable Analog Technology* feature, which appeared first in Chapter 12, you are aware that this software is available and can be downloaded free from www.anadigm.com. You can easily implement a filter design in an FPAA or dpASP chip if you have an evaluation board and interface cable connected to your computer.

Filter Specification

Once you have downloaded the AnadigmDesigner2 software, the first thing you see when opening it is an outline representation of the blank FPAA chip, as shown in Figure 15–36. Under the Tools menu, select *AnadigmFilter,* as shown, and you will get the screen shown in Figure 15–37.


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
AnadigmFilter
AnadigmPID
Addr1:1
Addr2:255
AN221E04
LOAD ORDER:1
FPAA1
CAP NUM

▲ FIGURE 15–36

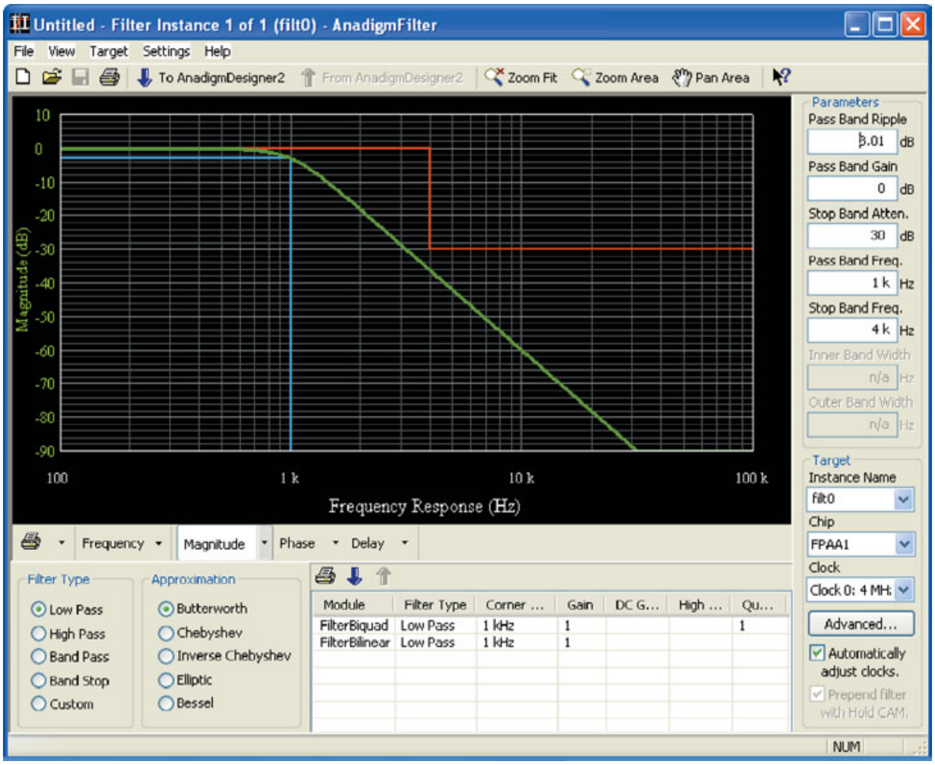
FPAA chip outline screen showing AnadigmFilter selection.

You are now ready to specify a filter. For example, select a filter type and approximation and enter the desired parameters, as shown in Figure 15–38, for a band-pass Butterworth filter. Note that you can use your mouse to drag the limits, shown in red and blue on the screen, to set the desired response.

When the filter has been completely specified, click on “To AnadigmDesigner2” and the filter components will be placed in the FPAA chip screen, as shown in Figure 15–39(a). Notice that the filter consists of three stages, in this case. Now use the connection tool to connect the filter to an input and output, as shown in part (b).

▶ FIGURE 15–37

Filter default screen.


Untitled - Filter Instance 1 of 1 (filt0) - AnadigmFilter
File View Target Settings Help
To AnadigmDesigner2
From AnadigmDesigner2
Zoom Fit
Zoom Area
Pan Area
Magnitude (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
100
1 k
10 k
100 k
Frequency Response (Hz)
Frequency
Magnitude
Phase
Delay
NUM

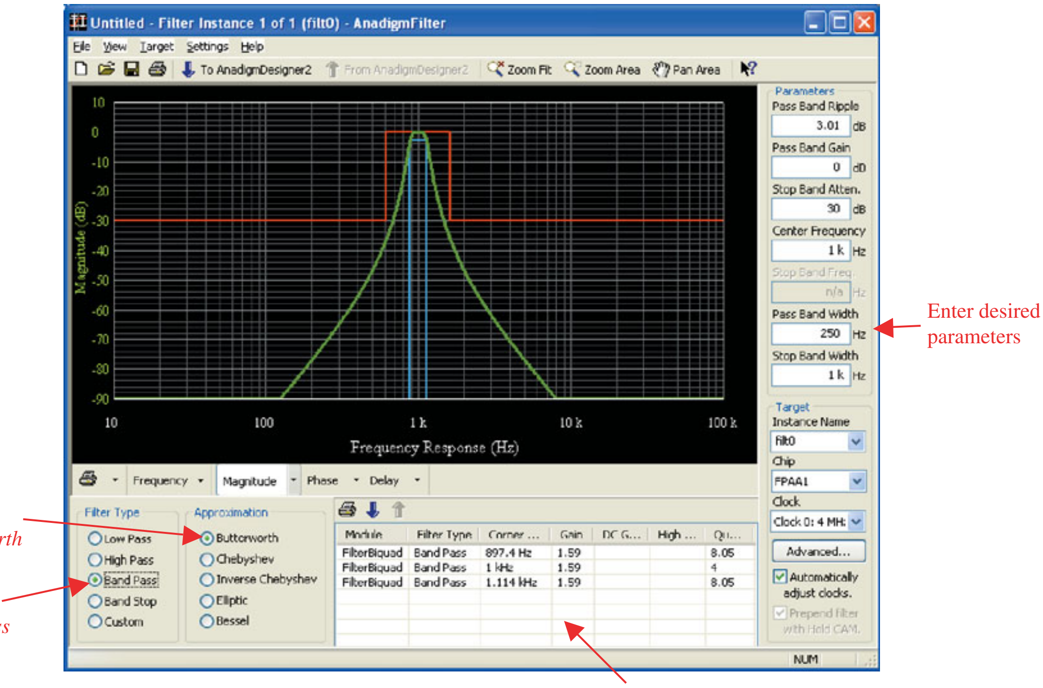
Filter Type
● Low Pass
○ High Pass
○ Band Pass
○ Band Stop
○ Custom

Approximation
● Butterworth
○ Chebyshev
○ Inverse Chebyshev
○ Elliptic
○ Bessel

Module	Filter Type	Corner ...	Gain	DC G...	High ...	Qu...
FilterBiquad	Low Pass	1 kHz	1			1
FilterBilinear	Low Pass	1 kHz	1			

Parameters
Pass Band Ripple 3.01 dB
Pass Band Gain 0 dB
Stop Band Atten. 30 dB
Pass Band Freq. 1 k Hz
Stop Band Freq. 4 k Hz
Inner Band Width n/a Hz
Outer Band Width n/a Hz

Target
Instance Name filt0
Chip FPAA1
Clock Clock 0: 4 MH:
Advanced...
☑ Automatically adjust clocks.
☑ Prepend filter with Hold CAM.


Untitled - Filter Instance 1 of 1 (filt0) - AnadigmFilter
File View Target Settings Help
To AnadigmDesigner2
From AnadigmDesigner2
Zoom Fit
Zoom Area
Pan Area
Magnitude (dB)
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
10
100
1 k
10 k
100 k
Frequency Response (Hz)
Frequency
Magnitude
Phase
Delay
NUM

Filter Type
○ Low Pass
○ High Pass
● Band Pass
○ Band Stop
○ Custom

Approximation
● Butterworth
○ Chebyshev
○ Inverse Chebyshev
○ Elliptic
○ Bessel

Module	Filter Type	Corner ...	Gain	DC G...	High ...	Qu...
FilterBiquad	Band Pass	897.4 Hz	1.59			8.05
FilterBiquad	Band Pass	1 kHz	1.59			4
FilterBiquad	Band Pass	1.114 kHz	1.59			8.05

Parameters
Pass Band Ripple 3.01 dB
Pass Band Gain 0 dB
Stop Band Atten. 30 dB
Center Frequency 1 k Hz
Stop Band Freq. n/a Hz
Pass Band Width 250 Hz
Stop Band Width 1 k Hz

Target
Instance Name filt0
Chip FPAA1
Clock Clock 0: 4 MH:
Advanced...
☑ Automatically adjust clocks.
☑ Prepend filter with Hold CAM.

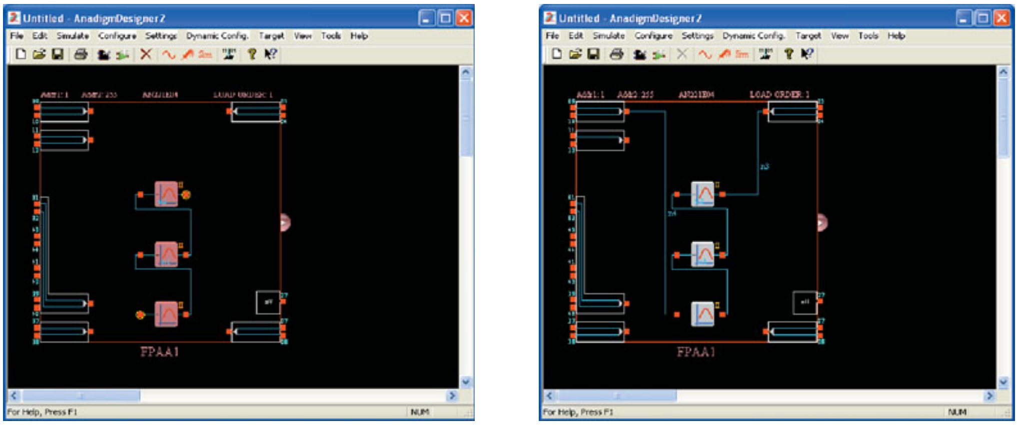
Enter desired parameters

Select *Butterworth*

Select *Band Pass*

Filter description is shown here

▲ FIGURE 15–38


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
FPAA1
For Help, Press F1
NUM

(a)

(b)

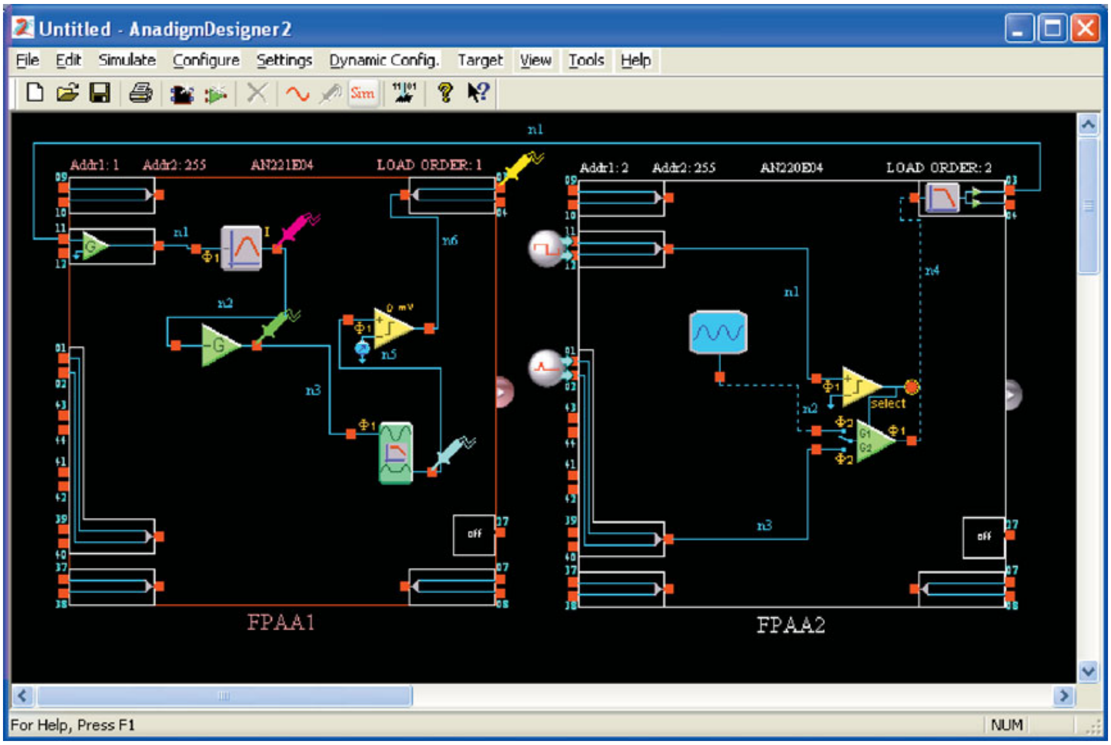
▲ FIGURE 15–39

By attaching actual signal generators and oscilloscope probes to the board, you can verify that the downloaded circuit is behaving just as the simulator indicated it would. Note that an FPAA or dpASP is reprogrammable so you can make circuit changes, download, and test indefinitely.

Design Assignment

Implement the RFID reader circuit using AnadigmDesigner2 software.

Procedure: Figure 15–40 shows a version of the circuit implemented in FPAA1. Because of limitations on implementing the ASK input signal, modifications have been made. Since the input cell

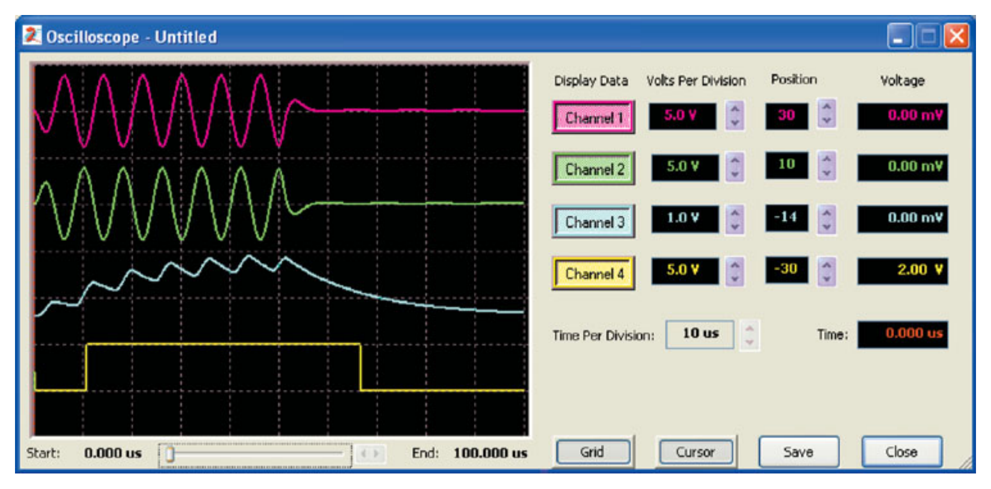

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Sim
n1
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
Addr1: 2 Addr2: 255 AN220E04 LOAD ORDER: 2
n1
n2
n3
n5
n6
G
0 mV
n1
n2
n3
n4
select
off
FPAA1
FPAA2
For Help, Press F1
NUM

▲ FIGURE 15–40

Design screen showing the RFID reader in FPAA1 and an ASK generator representing the RFID tag in FPAA2.

contains an amplifier with gain, the amplifier in the RFID reader circuit has less gain than if a 1 mV ASK signal were available. Also, the rectifier and low-pass filter are combined in one CAM. FPAA2 is used as a signal source to replicate a 125 kHz carrier modulated with a 10 kHz square wave. This chip is for test purposes only and is not part of the RFID reader.

Analysis: The simulation of the RFID reader is shown in Figure 15–41. The top waveform is the output of the 125 kHz band-pass filter CAM and is an ASK input signal representing a digital 1 followed by a 0. The second waveform is the output of the inverting gain stage CAM with a unity gain. The third waveform is the output of the half-wave rectifier/low-pass filter CAM. The bottom output is the digital signal from the comparator.



Display Data	Volts Per Division	Position	Voltage
Channel 1	5.0 V	30	0.00 mV
Channel 2	5.0 V	10	0.00 mV
Channel 3	1.0 V	-14	0.00 mV
Channel 4	5.0 V	-30	2.00 V

Time Per Division: 10 us

Time: 0.000 us

Start: 0.000 us

End: 100.000 us

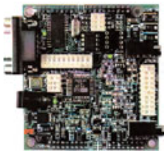
▲ **FIGURE 15–41**

Simulation waveforms for the RFID reader.

Programming Exercises

1. Why is a software program the best way to specify and implement active filters?
2. List the filter types available in the AnadigmFilter software.
3. List the filter approximations available in the AnadigmFilter software.

PAM Experiment



To program, download, and test a circuit using AnadigmDesigner2 software and the programmable analog module (PAM) board, go to Experiment 15–B in *Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling.

SUMMARY

Section 15–1

- In filter terminology, a single *RC* circuit is called a *pole.*
- The bandwidth in a low-pass filter equals the critical frequency because the response extends to 0 Hz.
- The passband of a high-pass filter extends above the critical frequency and is limited only by the inherent frequency limitation of the active circuit.

- A band-pass filter passes all frequencies within a band between a lower and an upper critical frequency and rejects all others outside this band.
- The bandwidth of a band-pass filter is the difference between the upper critical frequency and the lower critical frequency.
- The quality factor Q of a band-pass filter determines the filter's selectivity. The higher the Q, the narrower the bandwidth and the better the selectivity.
- A band-stop filter rejects all frequencies within a specified band and passes all those outside this band.

Section 15–2

- Filters with the Butterworth response characteristic have a very flat response in the passband, exhibit a roll-off of −20 dB/decade/pole, and are used when all the frequencies in the passband must have the same gain.
- Filters with the Chebyshev characteristic have ripples or overshoot in the passband and exhibit a faster roll-off per pole than filters with the Butterworth characteristic.
- Filters with the Bessel characteristic are used for filtering pulse waveforms. Their linear phase characteristic results in minimal waveshape distortion. The roll-off rate per pole is slower than for the Butterworth.
- Each pole in a Butterworth filter causes the output to roll off at a rate of −20 dB/decade.
- The damping factor determines the filter response characteristic (Butterworth, Chebyshev, or Bessel).

Section 15–3

- Single-pole low-pass filters have a −20 dB/decade roll-off.
- The Sallen-Key low-pass filter has two poles (second order) and has a −40 dB/decade roll-off.
- Each additional filter in a cascaded arrangement adds −20 dB to the roll-off rate.

Section 15–4

- Single-pole high-pass filters have a −20 dB/decade roll-off.
- The Sallen-Key high-pass filter has two poles (second order) and has a −40 dB/deacde roll-off.
- Each additional filter in a cascaded arrangement adds −20 dB to the roll-off rate.
- The response of an active high-pass filter is limited by the internal op-amp roll-off.

Section 15–5

- Band-pass filters pass a specified band of frequencies.
- A band-pass filter can be achieved by cascading a low-pass and a high-pass filter.
- The multiple-feedback band-pass filter uses two feedback paths to achieve its response characteristic.
- The state-variable band-pass filter uses a summing amplifier and two integrators.
- The biquad filter consists of an integrator followed by an inverting amplifier and a second integrator.

Section 15–6

- Band-stop filters reject a specified band of frequencies.
- Multiple-feedback and state-variable are common types of band-stop filters.

Section 15–7

- Filter response can be measured using discrete point measurement or swept frequency measurement.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Band-pass filter A type of filter that passes a range of frequencies lying between a certain lower frequency and a certain higher frequency.

Band-stop filter A type of filter that blocks or rejects a range of frequencies lying between a certain lower frequency and a certain higher frequency.

Damping factor A filter characteristic that determines the type of response.

Filter A circuit that passes certain frequencies and attenuates or rejects all other frequencies.

High-pass filter A type of filter that passes frequencies above a certain frequency while rejecting lower frequencies.

Low-pass filter A type of filter that passes frequencies below a certain frequency while rejecting higher frequencies.

Pole A circuit containing one resistor and one capacitor that contributes −20 dB/decade to a filter's roll-off rate.

Roll-off The rate of decrease in gain, below or above the critical frequencies of a filter.

KEY FORMULAS

15–1	$BW = f_c$	Low-pass bandwidth
15–2	$BW = f_{c2} - f_{c1}$	Filter bandwidth of a band-pass filter
15–3	$f_0 = \sqrt{f_{c1} f_{c2}}$	Center frequency of a band-pass filter
15–4	$Q = \dfrac{f_0}{BW}$	Quality factor of a band-pass filter
15–5	$DF = 2 - \dfrac{R_1}{R_2}$	Damping factor
15–6	$A_{cl(\mathrm{NI})} = \dfrac{R_1}{R_2} + 1$	Closed-loop voltage gain
15–7	$f_c = \dfrac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$	Critical frequency for a second-order Sallen-Key filter
15–8	$f_0 = \dfrac{1}{2\pi C}\sqrt{\dfrac{R_1 + R_3}{R_1 R_2 R_3}}$	Center frequency of a multiple-feedback filter
15–9	$A_0 = \dfrac{R_2}{2R_1}$	Gain of a multiple-feedback filter

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. The response of a filter can be identified by its passband.
2. A filter pole is the cutoff frequency of a filter.
3. A single-pole filter has one *RC* circuit.
4. A single-pole filter produces a roll-off of −25 dB/decade.
5. A low-pass filter can pass a dc voltage.
6. A high-pass filter passes any frequency above dc.
7. The critical frequency of a filter depends only on *R* and *C* values.
8. The band-pass filter has two critical frequencies.
9. The quality factor of a band-pass filter is the ratio of bandwidth to the center frequency.
10. The higher the *Q*, the narrower the bandwidth of a band-pass filter.
11. The Butterworth characteristic provides a flat response in the passband.
12. Filters with a Chebyshev response have a slow roll-off.
13. A Chebyshev response has ripples in the passband.
14. Bessel filters are useful in filtering pulse waveforms.
15. The order of a filter is the number of poles it contains.
16. A Sallen-Key filter is also known as a VCVS filter.
17. Multiple feedback is used in low-pass filters.
18. A state-variable filter uses differentiators.
19. A band-stop filter rejects certain frequencies.
20. Filter response can be measured using a sweep generator.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the critical frequency of a low-pass filter is increased, the bandwidth will

(a) increase **(b)** decrease **(c)** not change

2. If the critical frequency of a high-pass filter is increased, the bandwidth will

(a) increase **(b)** decrease **(c)** not change

3. If the Q of a band-pass filter is increased, the bandwidth will

(a) increase **(b)** decrease **(c)** not change

4. If the value of C_A and C_B in Figure 15–11 are increased by the same amount, the critical frequency will

(a) increase **(b)** decrease **(c)** not change

5. If the the value of R_2 in Figure 15–11 is increased, the bandwidth will

(a) increase **(b)** decrease **(c)** not change

6. If two filters like the one in Figure 15–15 are cascaded, the roll-off rate of the frequency response will

(a) increase **(b)** decrease **(c)** not change

7. If the value of R_2 in Figure 15–19 is decreased, the Q will

(a) increase **(b)** decrease **(c)** not change

8. If the capacitors in Figure 15–19 are changed to 0.022 μF, the center frequency will

(a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 15–1

1. The term *pole* in filter terminology refers to

(a) a high-gain op-amp **(b)** one complete active filter

(c) a single *RC* circuit **(d)** the feedback circuit

2. A single resistor and a single capacitor can be connected to form a filter with a roll-off rate of

(a) -20 dB/decade **(b)** -40 dB/decade

(c) -6 dB/octave **(d)** answers (a) and (c)

3. A band-pass response has

(a) two critical frequencies **(b)** one critical frequency

(c) a flat curve in the passband **(d)** a wide bandwidth

4. The lowest frequency passed by a low-pass filter is

(a) 1 Hz **(b)** 0 Hz **(c)** 10 Hz **(d)** dependent on the critical frequency

5. The quality factor (Q) of a band-pass filter depends on

(a) the critical frequencies **(b)** only the bandwidth

(c) the center frequency and the bandwidth **(d)** only the center frequency

Section 15–2

6. The damping factor of an active filter determines

(a) the voltage gain **(b)** the critical frequency

(c) the response characteristic **(d)** the roll-off rate

7. A maximally flat frequency response is known as

(a) Chebyshev **(b)** Butterworth **(c)** Bessel **(d)** Colpitts

8. The damping factor of a filter is set by

(a) the negative feedback circuit **(b)** the positive feedback circuit

(c) the frequency-selective circuit **(d)** the gain of the op-amp

9. The number of poles in a filter affect the

(a) voltage gain **(b)** bandwidth

(c) center frequency **(d)** roll-off rate

Section 15–3

10. Sallen-Key low-pass filters are

(a) single-pole filters **(b)** second-order filters

(c) Butterworth filters **(d)** band-pass filters

11. When low-pass filters are cascaded, the roll-off rate

(a) increases **(b)** decreases **(c)** does not change

Section 15–4

12. In a high-pass filter, the roll-off occurs

(a) above the critical frequency **(b)** below the critical frequency

(c) during the mid range **(d)** at the center frequency

13. A two-pole Sallen-Key high-pass filter contains

(a) one capacitor and two resistors **(b)** two capacitors and two resistors

(c) a feedback circuit **(d)** answers (b) and (c)

Section 15–5

14. When a low-pass and a high-pass filter are cascaded to get a band-pass filter, the critical frequency of the low-pass filter must be

(a) equal to the critical frequency of the high-pass filter

(b) less than the critical frequency of the high-pass filter

(c) greater than the critical frequency of the high-pass filter

15. A state-variable filter consists of

(a) one op-amp with multiple-feedback paths

(b) a summing amplifier and two integrators

(c) a summing amplifier and two differentiators

(d) three Butterworth stages

Section 15–6

16. When the gain of a filter is minimum at its center frequency, it is

(a) a band-pass filter **(b)** a band-stop filter

(c) a notch filter **(d)** answers (b) and (c)

PROBLEMS

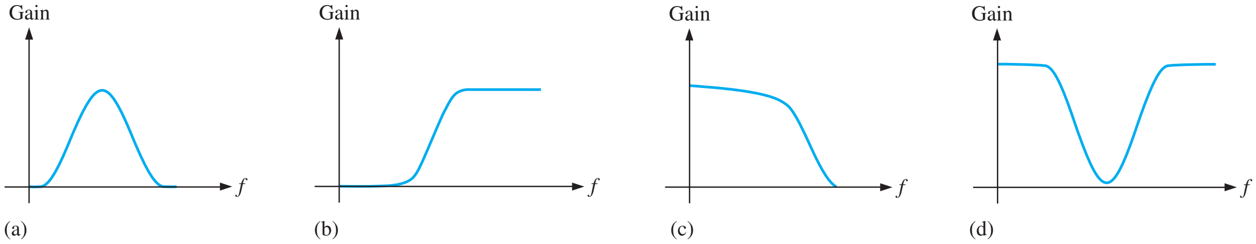
Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 15–1

Basic Filter Responses

1. Identify each type of filter response (low-pass, high-pass, band-pass, or band-stop) in Figure 15–42.



▲ FIGURE 15–42

2. A certain low-pass filter has a critical frequency of 800 Hz. What is its bandwidth?

3. A single-pole high-pass filter has a frequency-selective circuit with $R = 2.2\text{ k}\Omega$ and $C = 0.0015\ \mu\text{F}$. What is the critical frequency? Can you determine the bandwidth from the available information?

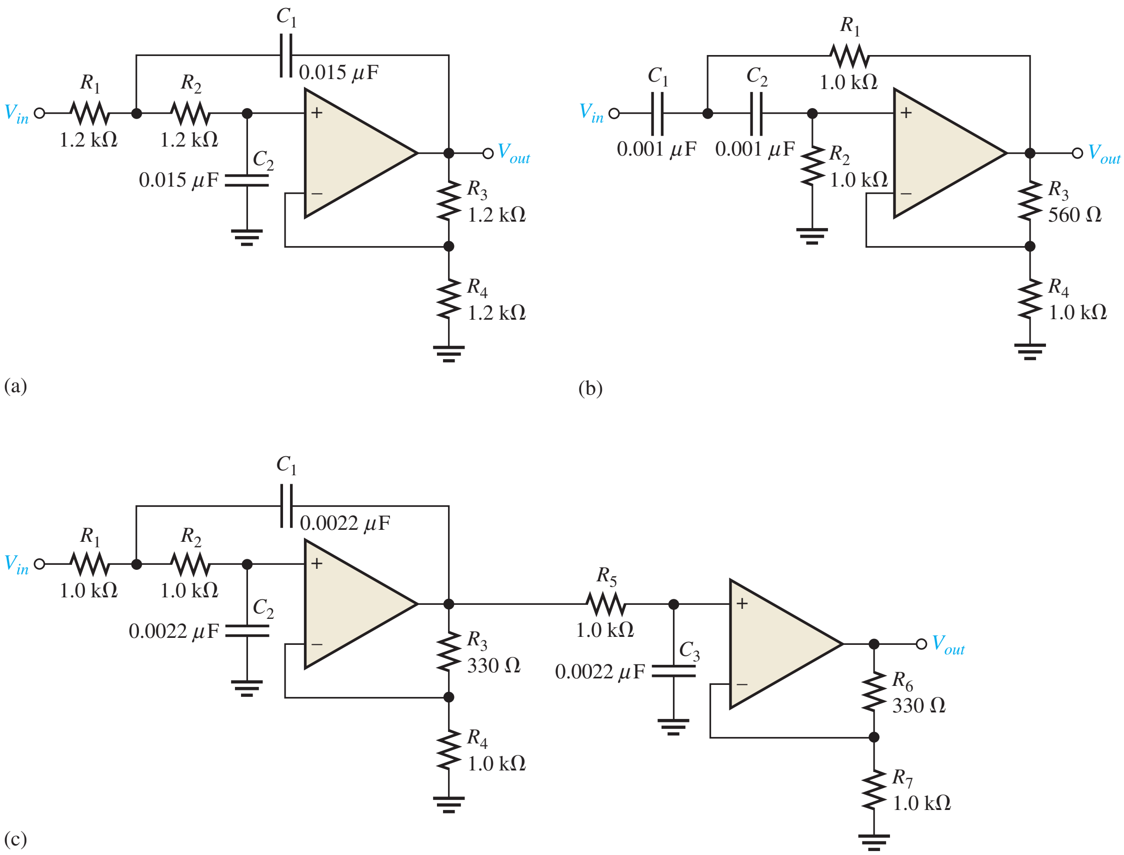
4. What is the roll-off rate of the filter described in Problem 3?

5. What is the bandwidth of a band-pass filter whose critical frequencies are 3.2 kHz and 3.9 kHz? What is the Q of this filter?

6. What is the center frequency of a filter with a Q of 15 and a bandwidth of 1 kHz?

Section 15–2 Filter Response Characteristics

7. What is the damping factor in each active filter shown in Figure 15–43? Which filters are approximately optimized for a Butterworth response characteristic?



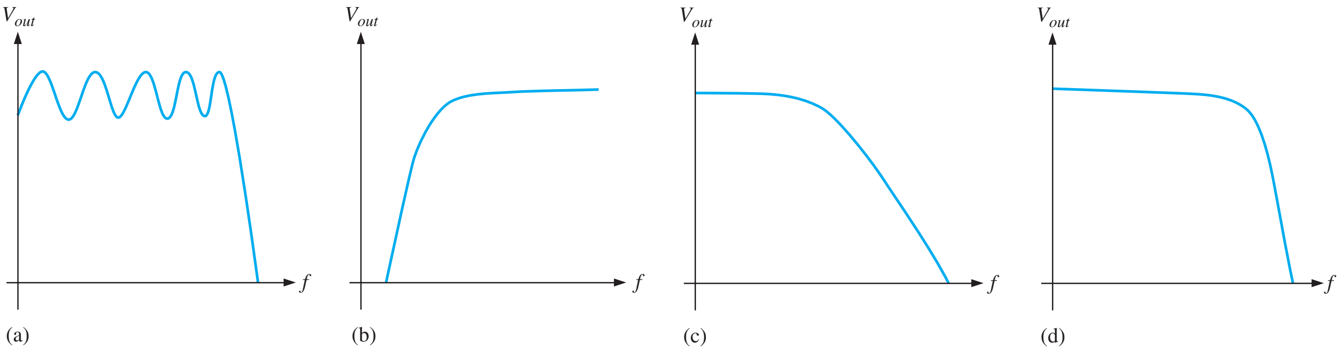
C_1
0.015 μF
V_{in}
R_1
1.2 kΩ
R_2
1.2 kΩ
C_2
0.015 μF
+
−
V_{out}
R_3
1.2 kΩ
R_4
1.2 kΩ
(a)
R_1
1.0 kΩ
V_{in}
C_1
0.001 μF
C_2
0.001 μF
R_2
1.0 kΩ
V_{out}
R_3
560 Ω
R_4
1.0 kΩ
(b)
C_1
0.0022 μF
V_{in}
R_1
1.0 kΩ
R_2
1.0 kΩ
C_2
0.0022 μF
R_3
330 Ω
R_4
1.0 kΩ
R_5
1.0 kΩ
C_3
0.0022 μF
V_{out}
R_6
330 Ω
R_7
1.0 kΩ
(c)

▲ FIGURE 15–43

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F15-43).

8. For the filters in Figure 15–43 that do not have a Butterworth response, specify the changes necessary to convert them to Butterworth responses. (Use nearest standard values.)

9. Response curves for second-order filters are shown in Figure 15–44. Identify each as Butterworth. Chebyshev, or Bessel.



▲ FIGURE 15–44

Section 15–3 Active Low-Pass Filters

10. Is the four-pole filter in Figure 15–45 approximately optimized for a Butterworth response? What is the roll-off rate?

11. Determine the critical frequency in Figure 15–45.

12. Without changing the response curve, adjust the component values in the filter of Figure 15–45 to make it an equal-value filter. Select $C = 0.22\ \mu F$ for both stages.

13. Modify the filter in Figure 15–45 to increase the roll-off rate to −120 dB/decade while maintaining an approximate Butterworth response.

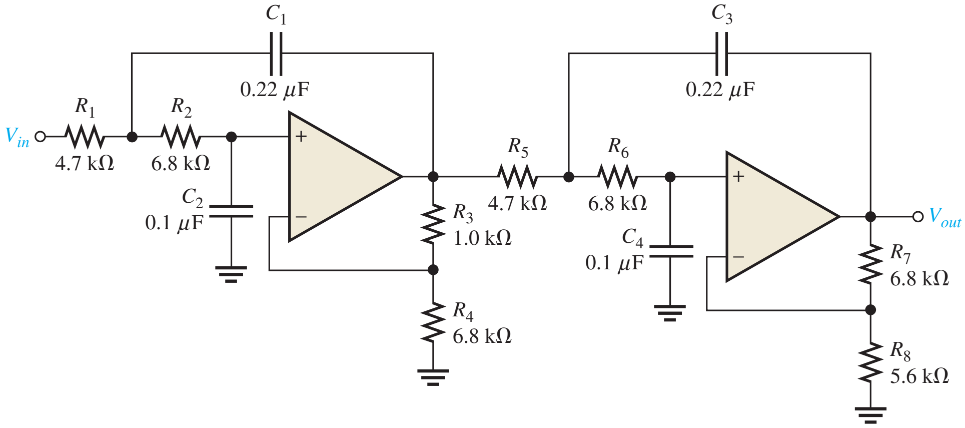
14. Using a block diagram format, show how to implement the following roll-off rates using single-pole and two-pole low-pass filters with Butterworth responses.

(a) −40 dB/decade **(b)** −20 dB/decade

(c) −60 dB/decade **(d)** −100 dB/decade

(e) −120 dB/decade

▶ FIGURE 15–45



C_1
0.22 μF
C_3
0.22 μF
V_{in}
R_1
4.7 kΩ
R_2
6.8 kΩ
C_2
0.1 μF
+
−
R_3
1.0 kΩ
R_4
6.8 kΩ
R_5
4.7 kΩ
R_6
6.8 kΩ
C_4
0.1 μF
+
−
V_{out}
R_7
6.8 kΩ
R_8
5.6 kΩ

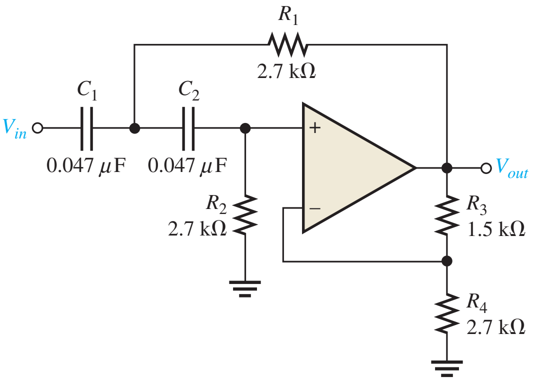
Section 15–4 Active High-Pass Filters

15. Convert the filter in Problem 12 to a high-pass with the same critical frequency and response characteristic.

16. Make the necessary circuit modification to reduce by half the critical frequency in Problem 15.

17. For the filter in Figure 15–46, **(a)** how would you increase the critical frequency? (b) How would you increase the gain?

▶ FIGURE 15–46

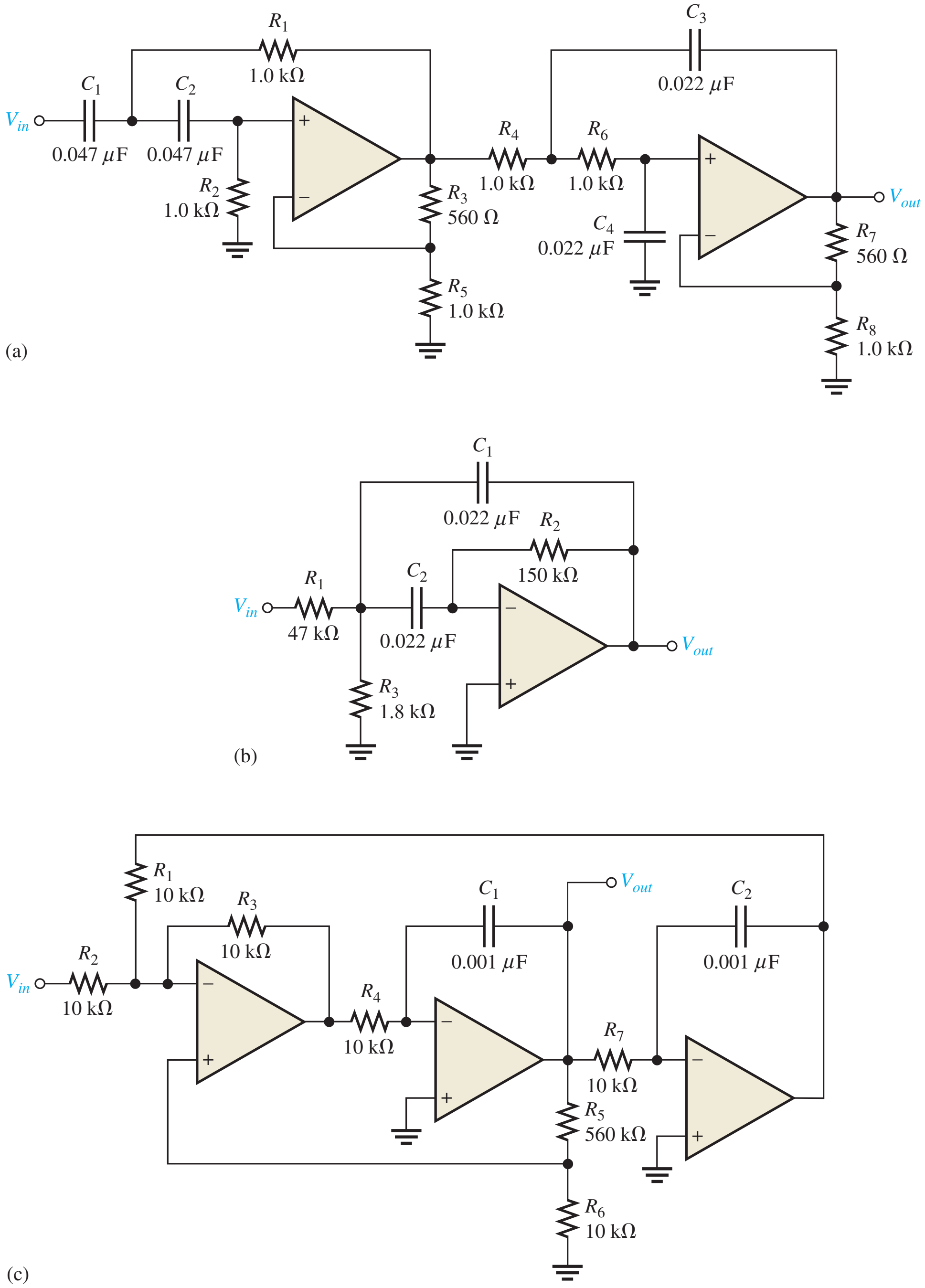


R_1
2.7 kΩ
C_1
C_2
V_{in}
0.047 μF
0.047 μF
R_2
2.7 kΩ
+
−
V_{out}
R_3
1.5 kΩ
R_4
2.7 kΩ

Section 15–5 Active Band-Pass Filters

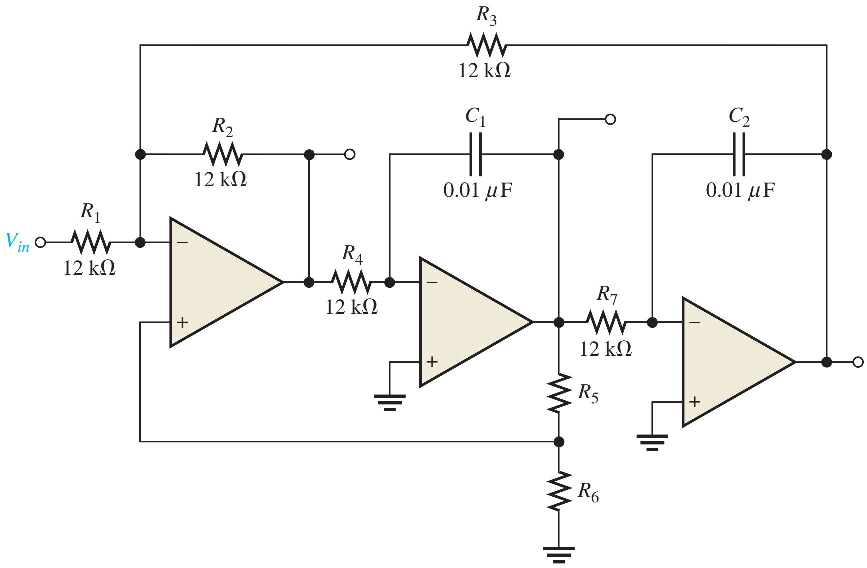
18. Identify each band-pass filter configuration in Figure 15–47.

19. Determine the center frequency and bandwidth for each filter in Figure 15–47.


R_1
1.0 kΩ
C_3
0.022 μF
C_1
C_2
V_{in}
0.047 μF
0.047 μF
R_2
1.0 kΩ
R_4
1.0 kΩ
R_6
1.0 kΩ
R_3
560 Ω
C_4
0.022 μF
R_5
1.0 kΩ
V_{out}
R_7
560 Ω
R_8
1.0 kΩ
(a)
C_1
0.022 μF
R_2
150 kΩ
R_1
47 kΩ
C_2
0.022 μF
V_{in}
V_{out}
R_3
1.8 kΩ
(b)
R_1
10 kΩ
R_3
10 kΩ
C_1
0.001 μF
V_{out}
C_2
0.001 μF
R_2
10 kΩ
V_{in}
R_4
10 kΩ
R_7
10 kΩ
R_5
560 kΩ
R_6
10 kΩ
(c)

▲ FIGURE 15–47

▶ FIGURE 15–48



20. Optimize the state-variable filter in Figure 15–48 for $Q = 50$. What bandwidth is achieved?

Section 15–6

Active Band-Stop Filters

21. Show how to make a notch (band-stop) filter using the basic circuit in Figure 15–48.

22. Modify the band-stop filter in Problem 21 for a center frequency of 120 Hz.

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

23. Open file TSP15-23 and determine the fault.

24. Open file TSP15-24 and determine the fault.

25. Open file TSP15-25 and determine the fault.

26. Open file TSP15-26 and determine the fault.

27. Open file TSP15-27 and determine the fault.

28. Open file TSP15-28 and determine the fault.

29. Open file TSP15-29 and determine the fault.

30. Open file TSP15-30 and determine the fault.

31. Open file TSP15-31 and determine the fault.

16

OSCILLATORS

CHAPTER OUTLINE

16–1 The Oscillator
16–2 Feedback Oscillators
16–3 Oscillators with *RC* Feedback Circuits
16–4 Oscillators with *LC* Feedback Circuits
16–5 Relaxation Oscillators
16–6 The 555 Timer as an Oscillator
Application Activity
Programmable Analog Technology

CHAPTER OBJECTIVES

- Describe the operating principles of an oscillator
- Discuss the principle on which feedback oscillators is based
- Describe and analyze the operation of *RC* feedback oscillators
- Describe and analyze the operation of *LC* feedback oscillators
- Describe and analyze the operation of relaxation oscillators
- Discuss and analyze the 555 timer and use it in oscillator applications

KEY TERMS

- Oscillator
- Positive feedback
- Voltage-controlled oscillator (VCO)
- Astable

APPLICATION ACTIVITY PREVIEW

The application in this chapter is a circuit that produces an ASK signal for testing the RFID reader developed in the last chapter. The ASK test generator uses an oscillator, a 555 timer, and a JFET analog switch to produce a 125 kHz carrier signal modulated at 10 kHz by a digital signal. The output amplitude is adjustable down to a low level to simulate the RFID tag signal.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

Oscillators are electronic circuits that generate an output signal without the necessity of an input signal. They are used as signal sources in all sorts of applications. Different types of oscillators produce various types of outputs including sine waves, square waves, triangular waves, and sawtooth waves. In this chapter, several types of basic oscillator circuits using both discrete transistors and op-amps as the gain element are introduced. Also, a popular integrated circuit, the 555 timer, is discussed in relation to its oscillator applications.

Sinusoidal oscillator operation is based on the principle of positive feedback, where a portion of the output signal is fed back to the input in a way that causes it to reinforce itself and thus sustain a continuous output signal. Oscillators are widely used in most communications systems as well as in digital systems, including computers, to generate required frequencies and timing signals. Also, oscillators are found in many types of test instruments like those used in the laboratory.

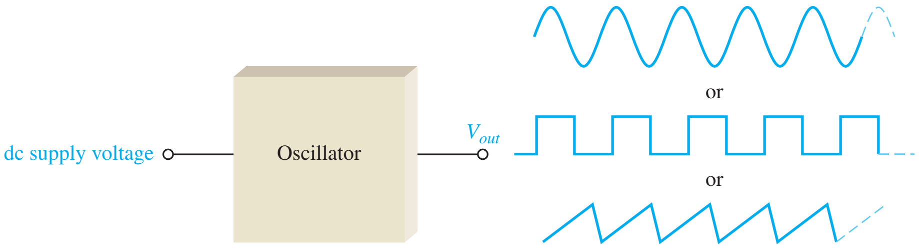
16–1 THE OSCILLATOR

An **oscillator** is a circuit that produces a periodic waveform on its output with only the dc supply voltage as an input. A repetitive input signal is not required except to synchronize oscillations in some applications. The output voltage can be either sinusoidal or nonsinusoidal, depending on the type of oscillator. Two major classifications for oscillators are feedback oscillators and relaxation oscillators.

After completing this section, you should be able to

- ❑ **Describe the operating principles of an oscillator**
- ❑ Discuss feedback oscillators
  - ◆ List the basic elements of a feedback oscillator
  - ◆ Show a test setup
- ❑ Briefly describe a relaxation oscillator
  - ◆ State the difference between a feedback oscillator and a relaxation oscillator

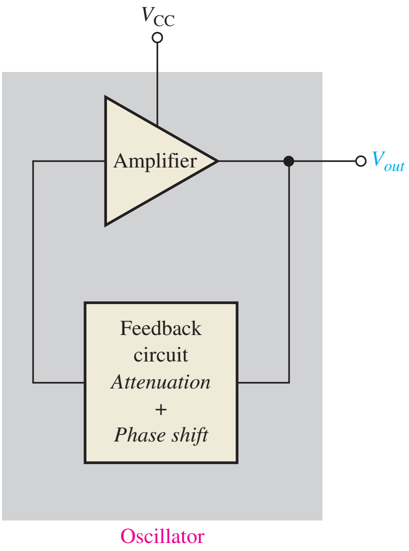
Essentially, an oscillator converts electrical energy from the dc power supply to periodic waveforms. A basic oscillator is shown in Figure 16–1.



◀ FIGURE 16–1

The basic oscillator concept showing three common types of output waveforms: sine wave, square wave, and sawtooth.

Feedback Oscillators One type of oscillator is the **feedback oscillator**, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Figure 16–2.



◀ FIGURE 16–2

Basic elements of a feedback oscillator.

Relaxation Oscillators A second type of oscillator is the **relaxation oscillator**. Instead of feedback, a relaxation oscillator uses an *RC* timing circuit to generate a waveform that is generally a square wave or other nonsinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor. Relaxation oscillators are discussed in Section 16–5.

SECTION 16–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What is an oscillator?
2. What type of feedback does a feedback oscillator require?
3. What is the purpose of the feedback circuit?
4. Name the two types of oscillators.

16–2 FEEDBACK OSCILLATORS

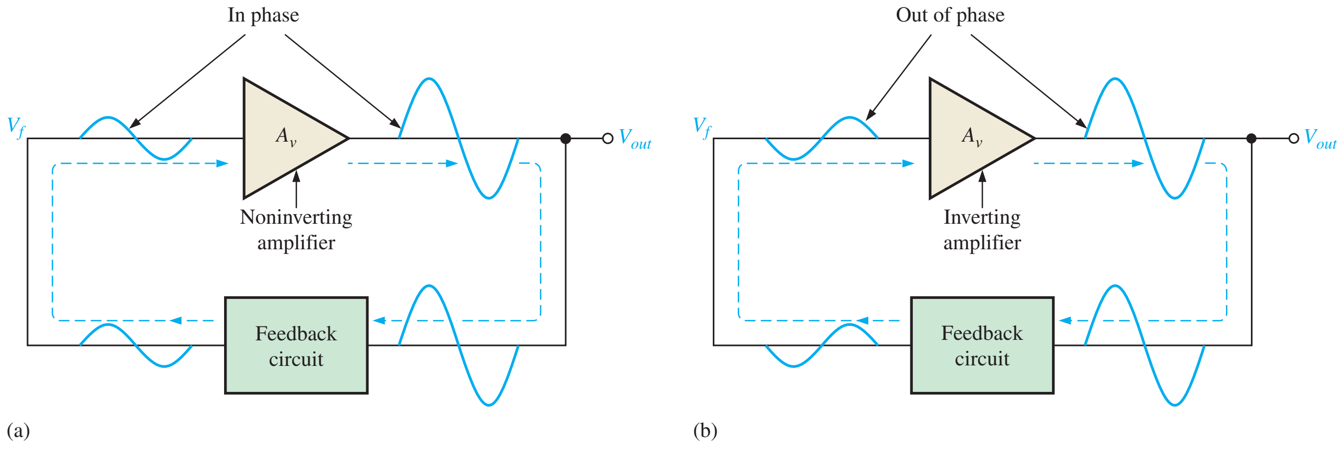
Feedback oscillator operation is based on the principle of positive feedback. In this section, we will examine this concept and look at the general conditions required for oscillation to occur. Feedback oscillators are widely used to generate sinusoidal waveforms.

After completing this section, you should be able to

- **Discuss the principle on which feedback oscillators is based**
- Explain positive feedback
  - Define *oscillation*
- Describe the conditions for oscillation
  - Define *closed loop gain*
- Discuss the conditions required for oscillator start-up

Positive Feedback

Positive feedback is characterized by the condition wherein a portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a reinforcement of the output signal. This basic idea is illustrated in Figure 16–3(a). As you can see, the in-phase feedback voltage, V_f, is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal sustains itself and



▲ FIGURE 16–3

Positive feedback produces oscillation.

a continuous sinusoidal output is produced. This phenomenon is called *oscillation.* In some types of amplifiers, the feedback circuit shifts the phase 180° and an inverting amplifier is required to provide another 180° phase shift so that there is no net phase shift. This is illustrated in Figure 16–3(b).

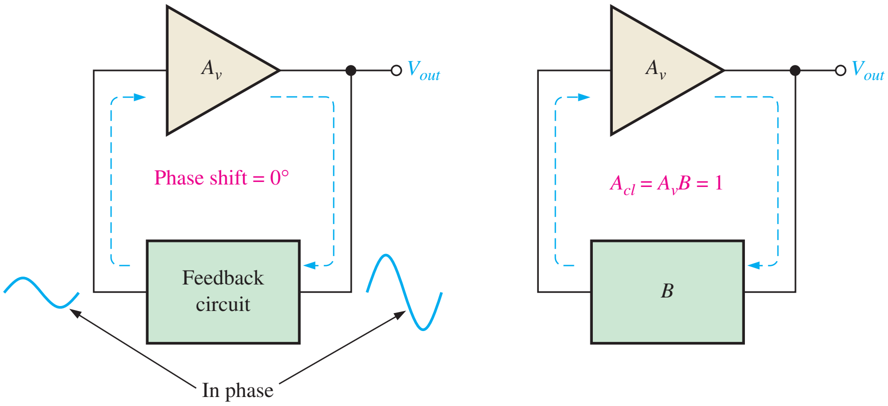
Conditions for Oscillation

Two conditions, illustrated in Figure 16–4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively 0°.
2. The voltage gain, A_{cl}, around the closed feedback loop (loop gain) must equal 1 (unity).

FIGURE 16–4

General conditions to sustain oscillation.



(a) The phase shift around the loop is 0°.

(b) The closed loop gain is 1.

The voltage gain around the closed feedback loop, A_{cl}, is the product of the amplifier gain, A_v, and the attenuation, B, of the feedback circuit.

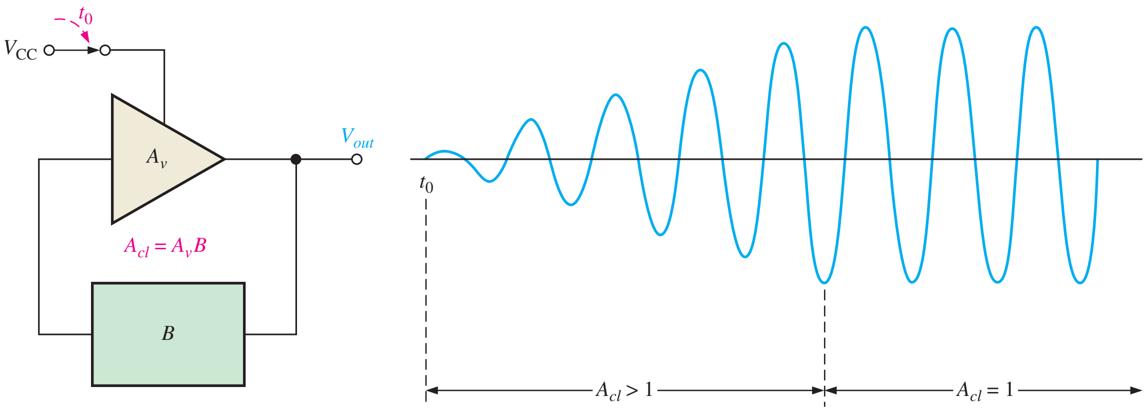
$$A_{cl} = A_v B$$

If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output to saturate at both peaks of the waveform, producing unacceptable distortion. To avoid this, some form of gain control must be used to keep the loop gain at exactly 1 once oscillations have started. For example, if the attenuation of the feedback circuit is 0.01, the amplifier must have a gain of exactly 100 to overcome this attenuation and not create unacceptable distortion ($0.01 \times 100 = 1$). An amplifier gain of greater than 100 will cause the oscillator to limit both peaks of the waveform.

Start-Up Conditions

So far, you have seen what it takes for an oscillator to produce a continuous sinusoidal output. Now let's examine the requirements for the oscillation to start when the dc supply voltage is first turned on. As you know, the unity-gain condition must be met for oscillation to be sustained. For oscillation to *begin,* the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained. Ways that certain amplifiers achieve this reduction in gain after start-up are discussed in later sections of this chapter. The voltage gain conditions for both starting and sustaining oscillation are illustrated in Figure 16–5.

A question that normally arises is this: If the oscillator is initially off and there is no output voltage, how does a feedback signal originate to start the positive feedback buildup process? Initially, a small positive feedback voltage develops from thermally produced broad-band noise in the resistors or other components or from power supply turn-on transients. The feedback circuit permits only a voltage with a frequency equal to the selected oscillation frequency to appear in phase on the amplifier's input. This initial feedback



▲ FIGURE 16–5

When oscillation starts at t_0, the condition $A_{cl} > 1$ causes the sinusoidal output voltage amplitude to build up to a desired level. Then A_{cl} decreases to 1 and maintains the desired amplitude.

voltage is amplified and continually reinforced, resulting in a buildup of the output voltage as previously discussed.

SECTION 16–2 CHECKUP

1. What are the conditions required for a circuit to oscillate?
2. Define *positive feedback.*
3. What is the voltage gain condition for oscillator start-up?

16–3 OSCILLATORS WITH *RC* FEEDBACK CIRCUITS

Three types of feedback oscillators that use *RC* circuits to produce sinusoidal outputs are the Wien-bridge oscillator, the phase-shift oscillator, and the twin-T oscillator. Generally, *RC* feedback oscillators are used for frequencies up to about 1 MHz. The Wien-bridge is by far the most widely used type of *RC* feedback oscillator for this range of frequencies.

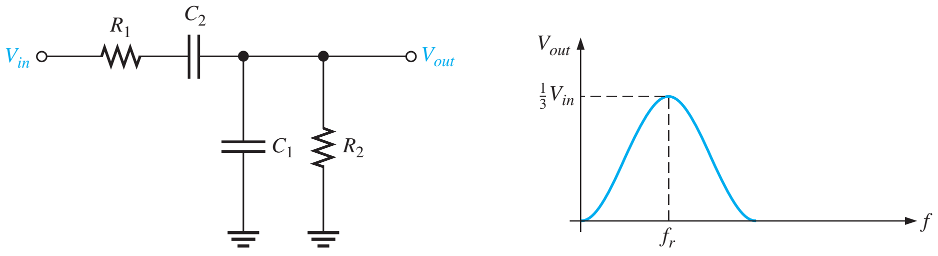
After completing this section, you should be able to

- ❑ **Describe and analyze the operation of *RC* feedback oscillators**
- ❑ Identify and describe the Wien-bridge oscillator
  ◆ Discuss the response of a lead-lag circuit ◆ Discuss the attenuation of the lead-lag circuit ◆ Calculate the resonant frequency ◆ Discuss the positive feedback conditions for oscillation ◆ Describe the start-up conditions ◆ Discuss a JFET stabilized Wien-bridge oscillator
- ❑ Describe and analyze the phase-shift oscillator
  ◆ Discuss the required value of feedback attenuation ◆ Calculate the resonant frequency
- ❑ Discuss the twin-T oscillator

The Wien-Bridge Oscillator

One type of sinusoidal feedback oscillator is the **Wien-bridge oscillator**. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 16–6(a).

R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion. The operation of this lead-lag circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C_2. As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.



(a) Circuit (b) Response curve

FIGURE 16–6

A lead-lag circuit and its response curve.

The response curve for the lead-lag circuit shown in Figure 16–6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point, the attenuation (V_{out}/V_{in}) of the circuit is $1/3$ if $R_1 = R_2$ and $X_{C1} = X_{C2}$ as stated by the following equation (derived in “Derivations of Selected Equations” at www.pearsonhighered.com/floyd):

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

Equation 16–1

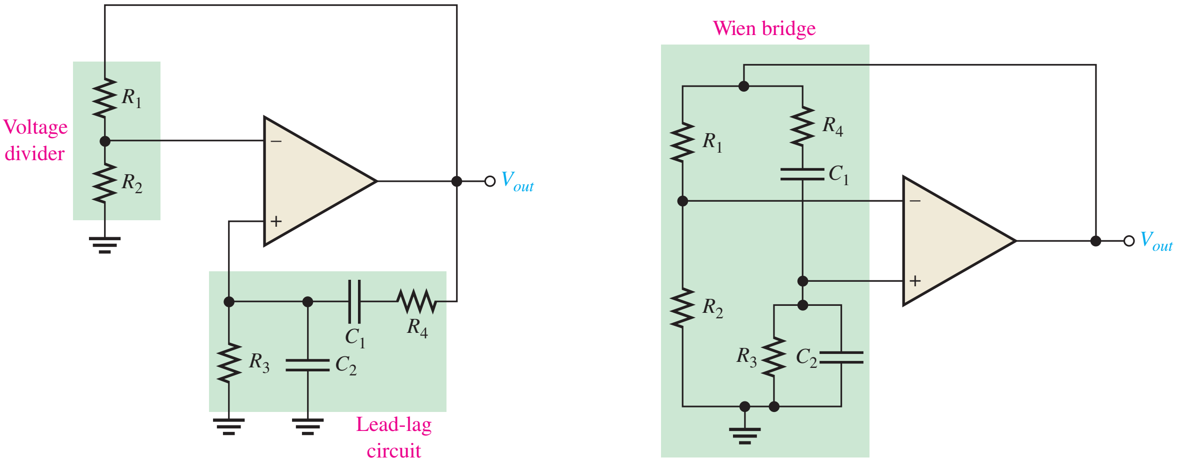
The formula for the resonant frequency (also derived on the companion website) is

$$f_r = \frac{1}{2\pi RC}$$

Equation 16–2

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, f_r, at which the phase shift through the circuit is 0° and the attenuation is 1/3. Below f_r, the lead circuit dominates and the output leads the input. Above f_r, the lag circuit dominates and the output lags the input.

The Basic Circuit The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Figure 16–7(a). A voltage divider is used in the negative feedback loop.



(a) (b) Wien bridge circuit combines a voltage divider and a lead-lag circuit.

FIGURE 16–7

The Wien-bridge oscillator schematic drawn in two different but equivalent ways.

The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the voltage divider determines the closed-loop gain of the amplifier.

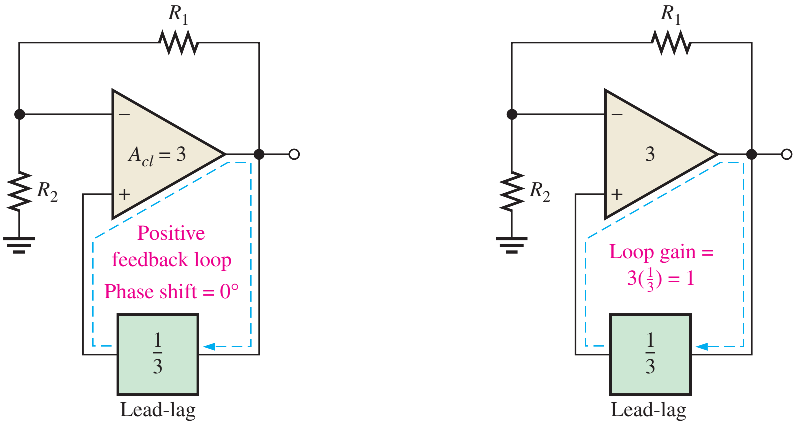
$$A_{cl} = \frac{1}{B} = \frac{1}{R_2/(R_1 + R_2)} = \frac{R_1 + R_2}{R_2}$$

The circuit is redrawn in Figure 16–7(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.

Positive Feedback Conditions for Oscillation As you know, for the circuit to produce a sustained sinusoidal output (oscillate), the phase shift around the positive feedback loop must be 0° and the gain around the loop must equal unity (1). The 0° phase-shift condition is met when the frequency is f_r because the phase shift through the lead-lag circuit is 0° and there is no inversion from the noninverting (+) input of the op-amp to the output. This is shown in Figure 16–8(a).

▶ FIGURE 16–8

Conditions for sustained oscillation.



(a) The phase shift around the loop is 0°.

(b) The voltage gain around the loop is 1.

The unity-gain condition in the feedback loop is met when

$$A_{cl} = 3$$

This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1, as depicted in Figure 16–8(b). To achieve a closed-loop gain of 3,

$$R_1 = 2R_2$$

Then

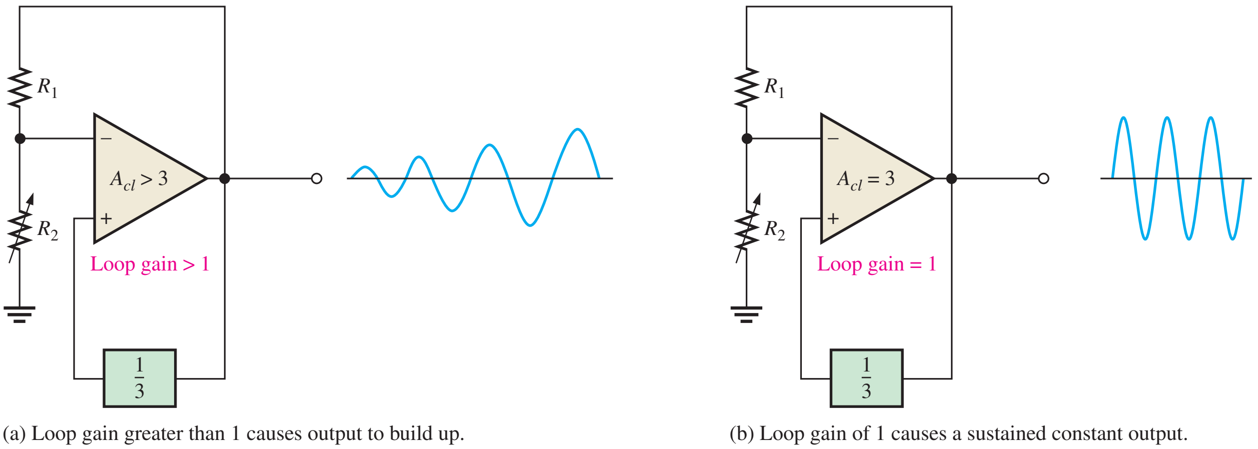
$$A_{cl} = \frac{R_1 + R_2}{R_2} = \frac{2R_2 + R_2}{R_2} = \frac{3R_2}{R_2} = 3$$

Start-Up Conditions Initially, the closed-loop gain of the amplifier itself must be more than 3 ($A_{cl} > 3$) until the output signal builds up to a desired level. Ideally, the gain of the amplifier must then decrease to 3 so that the total gain around the loop is 1 and the output signal stays at the desired level, thus sustaining oscillation. This is illustrated in Figure 16–9.

The circuit in Figure 16–10 illustrates a method for achieving sustained oscillations. Notice that the voltage-divider circuit has been modified to include an additional resistor R_3 in parallel with a back-to-back zener diode arrangement. When dc power is first applied,

HISTORY NOTE

Max Wien (1866–1938) was a German physicist. He theoretically developed the concept of the Wien-bridge oscillator in 1891. At that time, Wien did not have a means of developing electronic gain, so a workable oscillator could not be achieved. Based on Wien's work, William Hewlett, co-founder of Hewlett-Packard, was successful in building a practical Wien-bridge oscillator in 1939.

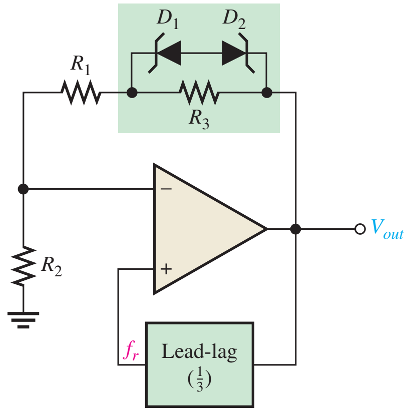


(a) Loop gain greater than 1 causes output to build up.

(b) Loop gain of 1 causes a sustained constant output.

▲ **FIGURE 16–9**

Conditions for start-up and sustained oscillations.



◀ **FIGURE 16–10**

Self-starting Wien-bridge oscillator using back-to-back zener diodes.

both zener diodes appear as opens. This places R_3 in series with R_1, thus increasing the closed-loop gain of the amplifier as follows ($R_1 = 2R_2$):

$$A_{cl} = \frac{R_1 + R_2 + R_3}{R_2} = \frac{3R_2 + R_3}{R_2} = 3 + \frac{R_3}{R_2}$$

Initially, a small positive feedback signal develops from noise or turn-on transients. The lead-lag circuit permits only a signal with a frequency equal to f_r to appear in phase on the noninverting input. This feedback signal is amplified and continually reinforced, resulting in a buildup of the output voltage. When the output signal reaches the zener breakdown voltage, the zeners conduct and effectively short out R_3. This lowers the amplifier's closed-loop gain to 3. At this point, the total loop gain is 1 and the output signal levels off and the oscillation is sustained.

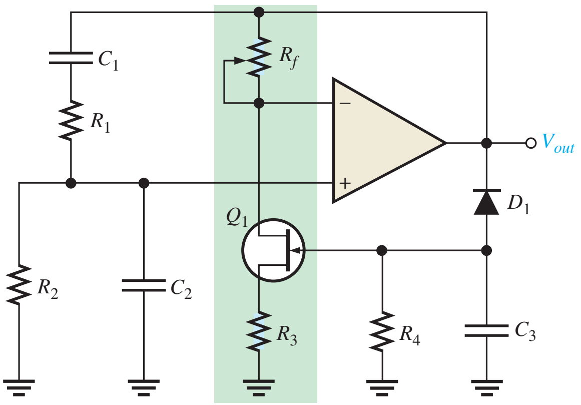
All practical methods to achieve stability for feedback oscillators require the gain to be self-adjusting. This requirement is a form of automatic gain control (AGC). The zener diodes in Figure 16–10 limit the gain at the onset of nonlinearity, in this case, zener conduction. Although the zener feedback is simple, it suffers from the nonlinearity of the zener diodes that occurs in order to control gain. It is difficult to achieve an undistorted sinusoidal output waveform. In some older designs, a tungsten lamp was used in the feedback circuit to achieve stability.

A better method to control the gain uses a JFET as a voltage-controlled resistor in a negative feedback path. This method can produce an excellent sinusoidal waveform that is stable. A JFET operating with a small or zero V_{DS} is operating in the ohmic region. As the gate voltage increases, the drain-source resistance increases. If the JFET is placed in the negative feedback path, automatic gain control can be achieved because of this voltage-controlled resistance.

A JFET stabilized Wien bridge is shown in Figure 16–11. The gain of the op-amp is controlled by the components shown in the green box, which include the JFET. The JFET's drain-source resistance depends on the gate voltage. With no output signal, the gate is at zero volts, causing the drain-source resistance to be at the minimum. With this condition, the loop gain is greater than 1. Oscillations begin and rapidly build to a large output signal. Negative excursions of the output signal forward-bias D_1, causing capacitor C_3 to charge to a negative voltage. This voltage increases the drain-source resistance of the JFET and reduces the gain (and hence the output). This is classic negative feedback at work. With the proper selection of components, the gain can be stabilized at the required level. Example 16–1 illustrates a JFET stabilized Wien-bridge oscillator.

▶ FIGURE 16–11

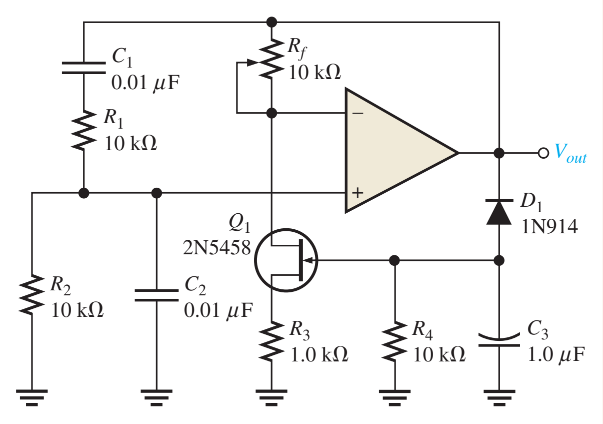
Self-starting Wien-bridge oscillator using a JFET in the negative feedback loop.



EXAMPLE 16–1

Determine the resonant frequency for the Wien-bridge oscillator in Figure 16–12. Also, calculate the setting for R_f assuming the internal drain-source resistance, r'_{ds}, of the JFET is 500 Ω when oscillations are stable.

▶ FIGURE 16–12



Solution For the lead-lag circuit, $R_1 = R_2 = R = 10\,\text{k}\Omega$ and $C_1 = C_2 = C = 0.01\,\mu\text{F}$. The frequency is

$$f_r = \frac{1}{2\pi RC} = \frac{1}{2\pi(10\,\text{k}\Omega)(0.01\,\mu\text{F})} = \mathbf{1.59\,kHz}$$

The closed-loop gain must be 3.0 for oscillations to be sustained. For an inverting amplifier, the gain expression is the same as for a noninverting amplifier.

$$A_v = \frac{R_f}{R_i} + 1$$

R_i is composed of R_3 (the source resistor) and r'_{ds}. Substituting,

$$A_v = \frac{R_f}{R_3 + r'_{ds}} + 1$$

Rearranging and solving for R_f,

$$R_f = (A_v - 1)(R_3 + r'_{ds}) = (3 - 1)(1.0\text{ k}\Omega + 500\ \Omega) = \mathbf{3.0\text{ k}\Omega}$$

*Related Problem** What happens to the oscillations if the setting of R_f is too high? What happens if the setting is too low?

***Answers can be found at www.pearsonhighered.com/floyd.**

Open the Multisim file E16-01 in the Examples folder on the companion website. Determine the frequency of oscillation and compare with the calculated value.

The Phase-Shift Oscillator

Figure 16–13 shows a sinusoidal feedback oscillator called the **phase-shift oscillator**. Each of the three *RC* circuits in the feedback loop can provide a *maximum* phase shift approaching 90°. Oscillation occurs at the frequency where the total phase shift through the three *RC* circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop.

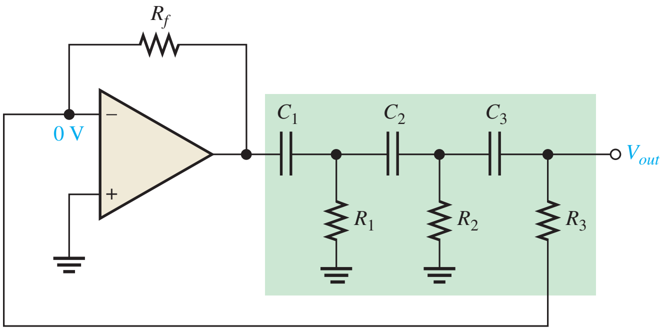


FIGURE 16–13

Phase-shift oscillator.

The attenuation, B, of the three-section *RC* feedback circuit is

$$\mathbf{B = \frac{1}{29}} \qquad \text{Equation 16–3}$$

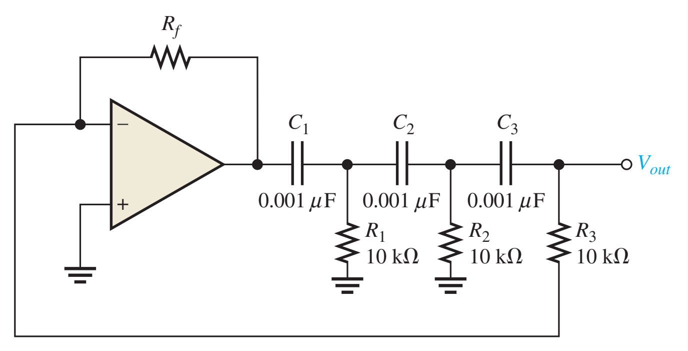
where $B = R_3/R_f$. The derivation of this unusual result is given in "Derivations of Selected Equations" at www.pearsonhighered.com/floyd. To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by R_f and R_3). The frequency of oscillation (f_r) is also derived on the companion website and is stated in the following equation, where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

$$\mathbf{f_r = \frac{1}{2\pi\sqrt{6}RC}} \qquad \text{Equation 16–4}$$

EXAMPLE 16–2

(a) Determine the value of R_f necessary for the circuit in Figure 16–14 to operate as an oscillator.

(b) Determine the frequency of oscillation.



▲ FIGURE 16–14

Solution

(a) $A_{cl} = 29$, and $B = 1/29 = R_3/R_f$. Therefore,

$$\frac{R_f}{R_3} = 29$$

$$R_f = 29R_3 = 29(10\text{ k}\Omega) = \mathbf{290\text{ k}\Omega}$$

(b) $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$. Therefore,

$$f_r = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6}(10\text{ k}\Omega)(0.001\ \mu\text{F})} \cong \mathbf{6.5\text{ kHz}}$$

Related Problem

(a) If R_1, R_2, and R_3 in Figure 16–14 are changed to 8.2 kΩ, what value must R_f be for oscillation?

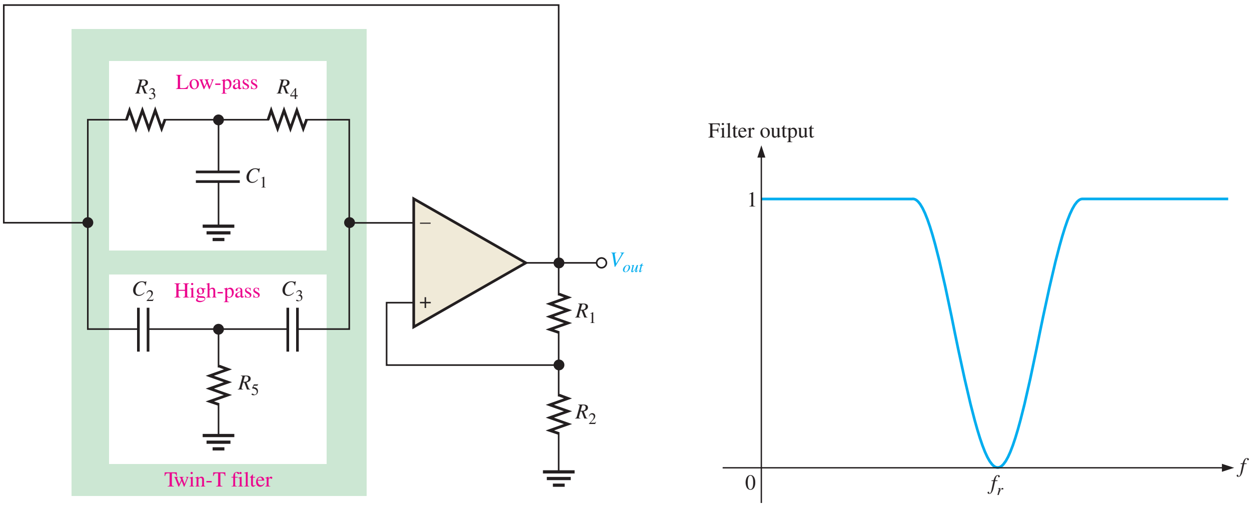
(b) What is the value of f_r?

Open the Multisim file E16-02 in the Examples folder on the companion website. Measure the frequency of oscillation and compare to the calculated value.

Twin-T Oscillator

Another type of *RC* feedback oscillator is called the *twin-T* because of the two T-type *RC* filters used in the feedback loop, as shown in Figure 16–15(a). One of the twin-T filters has a low-pass response, and the other has a high-pass response. The combined parallel filters produce a band-stop or notch response with a center frequency equal to the desired frequency of oscillation, f_r, as shown in Figure 16–15(b).

Oscillation cannot occur at frequencies above or below f_r because of the negative feedback through the filters. At f_r, however, there is negligible negative feedback; thus, the positive feedback through the voltage divider (R_1 and R_2) allows the circuit to oscillate.



(a) Oscillator circuit

(b) Twin-T filter's frequency response curve

▲ **FIGURE 16–15**

Twin-T oscillator and twin-T filter response.

SECTION 16–3 CHECKUP

1. There are two feedback loops in the Wien-bridge oscillator. What is the purpose of each?
2. A certain lead-lag circuit has $R_1 = R_2$ and $C_1 = C_2$. An input voltage of 5 V rms is applied. The input frequency equals the resonant frequency of the circuit. What is the rms output voltage?
3. Why is the phase shift through the *RC* feedback circuit in a phase-shift oscillator 180°?

16–4 OSCILLATORS WITH *LC* FEEDBACK CIRCUITS

Although the *RC* feedback oscillators, particularly the Wien bridge, are generally suitable for frequencies up to about 1 MHz, *LC* feedback elements are normally used in oscillators that require higher frequencies of oscillation. Also, because of the frequency limitation (lower unity-gain frequency) of most op-amps, discrete transistors (BJT or FET) are often used as the gain element in *LC* oscillators. This section introduces several types of resonant *LC* feedback oscillators: the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled oscillators.

After completing this section, you should be able to

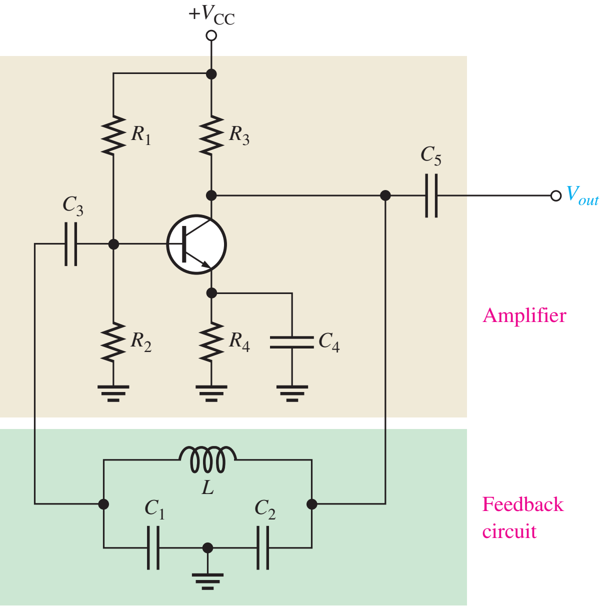
- ❑ **Describe and analyze the operation of *LC* feedback oscillators**
- ❑ Identify and analyze a Colpitts oscillator
  ◆ Determine the resonant frequency ◆ Describe the conditions for oscillation and start-up ◆ Discuss and analyze loading of the feedback circuit
- ❑ Identify and analyze a Clapp oscillator
  ◆ Determine the resonant frequency
- ❑ Identify and analyze a Hartley oscillator
  ◆ Determine the resonant frequency and attenuation of the feedback circuit
- ❑ Identify and analyze an Armstrong oscillator
  ◆ Determine the resonant frequency
- ❑ Describe the operation of crystal-controlled oscillators
  ◆ Define *piezoelectric effect* ◆ Discuss the quartz crystal ◆ Discuss the modes of operation in the crystal

The Colpitts Oscillator

One basic type of resonant circuit feedback oscillator is the Colpitts, named after its inventor—as are most of the others we cover here. As shown in Figure 16–16, this type of oscillator uses an *LC* circuit in the feedback loop to provide the necessary phase shift and to act as a resonant filter that passes only the desired frequency of oscillation.

▶ FIGURE 16–16

A basic Colpitts oscillator with a BJT as the gain element.



The approximate frequency of oscillation is the resonant frequency of the *LC* circuit and is established by the values of C_1, C_2, and *L* according to this familiar formula:

Equation 16–5

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}}$$

where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

$$C_T = \frac{C_1C_2}{C_1 + C_2}$$

Conditions for Oscillation and Start-Up The attenuation, *B*, of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 and C_2.

Figure 16–17 shows that the circulating tank current is through both C_1 and C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage (V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (*B*) is

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)}$$

Cancelling the $2\pi f_r$ terms gives

$$B = \frac{C_2}{C_1}$$

As you know, a condition for oscillation is $A_vB = 1$. Since $B = C_2/C_1$,

Equation 16–6

$$A_v = \frac{C_1}{C_2}$$

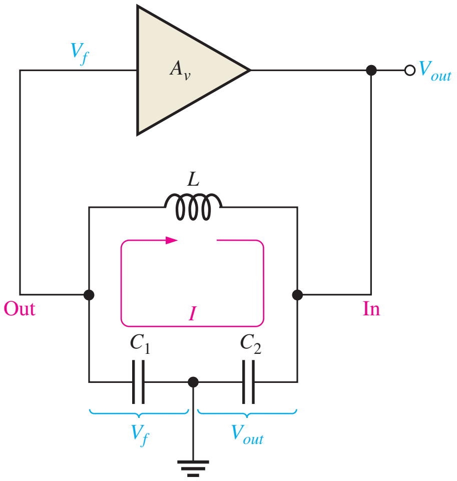


FIGURE 16–17

The attenuation of the tank circuit is the output of the tank (V_f) divided by the input to the tank (V_{out}). $B = V_f/V_{out} = C_2/C_1$. For $A_vB > 1$, A_v must be greater than C_1/C_2.

HISTORY NOTE

Edwin H. Colpitts was involved in the development of oscillators and vacuum tube push-pull amplifiers at Western Electric in the early 1900s. Western Electric research laboratories became part of Bell Laboratories in 1925, and Colpitts became vice-president of Bell Labs before retirement. The Colpitts oscillator is named in his honor.

where A_v is the voltage gain of the amplifier, which is represented by the triangle in Figure 16–17. With this condition met, $A_vB = (C_1/C_2)(C_2/C_1) = 1$. Actually, for the oscillator to be self-starting, A_vB must be greater than 1 (that is, $A_vB > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2.

$$A_v > \frac{C_1}{C_2}$$

Loading of the Feedback Circuit Affects the Frequency of Oscillation As indicated in Figure 16–18, the input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q of the circuit. The resonant frequency of a parallel resonant circuit depends on the Q, according to the following formula:

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2 + 1}}$$

Equation 16–7

As a rule of thumb, for a Q greater than 10, the frequency is approximately $1/(2\pi\sqrt{LC_T})$, as stated in Equation 16–5. When Q is less than 10, however, f_r is reduced significantly.

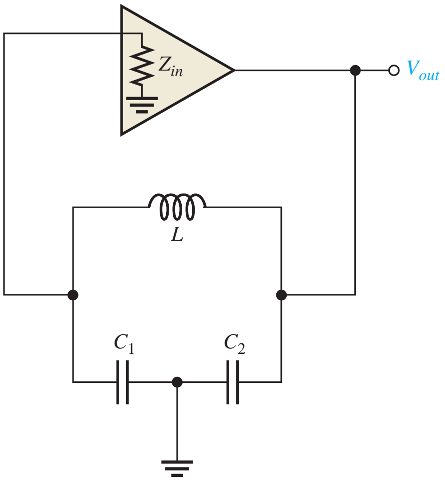
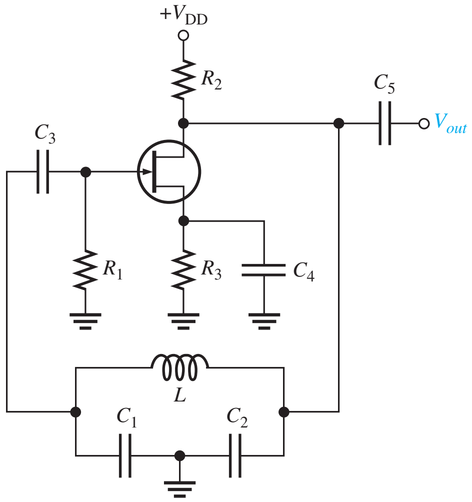


FIGURE 16–18

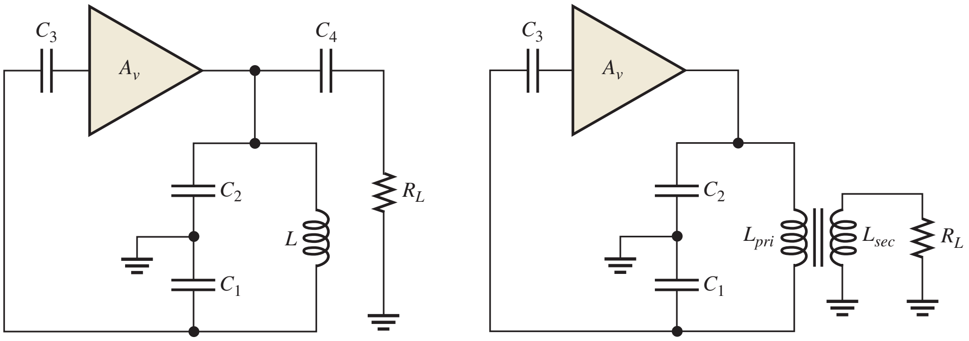
Z_{in} of the amplifier loads the feedback circuit and lowers its Q, thus lowering the resonant frequency.

A FET can be used in place of a BJT, as shown in Figure 16–19, to minimize the loading effect of the transistor's input impedance. Recall that FETs have much higher input impedances than do bipolar junction transistors. Also, when an external load is connected to the oscillator output, as shown in Figure 16–20(a), f_r may decrease, again because of a reduction in Q. This happens if the load resistance is too small. In some cases, one way to eliminate the effects of a load resistance is by transformer coupling, as indicated in Figure 16–20(b).



▲ **FIGURE 16–19**

A basic FET Colpitts oscillator.



(a) A load capacitively coupled to oscillator output can reduce circuit Q and f_r.

(b) Transformer coupling of load can reduce loading effect by impedance transformation.

▲ **FIGURE 16–20**

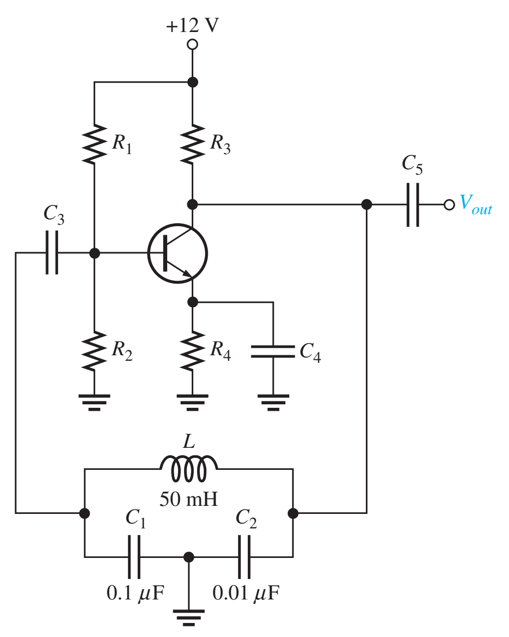
Oscillator loading.

EXAMPLE 16–3

(a) Determine the frequency for the oscillator in Figure 16–21. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10.

(b) Find the frequency if the oscillator is loaded to a point where the Q drops to 8.

FIGURE 16–21



Solution (a) $$C_T = \frac{C_1C_2}{C_1 + C_2} = \frac{(0.1\ \mu\text{F})(0.01\ \mu\text{F})}{0.11\ \mu\text{F}} = 0.0091\ \mu\text{F}$$

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} = \frac{1}{2\pi\sqrt{(50\text{ mH})(0.0091\ \mu\text{F})}} = \mathbf{7.46\ kHz}$$

(b) $$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2 + 1}} = (7.46\text{ kHz})(0.9923) = \mathbf{7.40\ kHz}$$

Related Problem What frequency does the oscillator in Figure 16–21 produce if it is loaded to a point where $Q = 4$?

The Clapp Oscillator

The Clapp oscillator is a variation of the Colpitts. The basic difference is an additional capacitor, C_3, in series with the inductor in the resonant feedback circuit, as shown in Figure 16–22. Since C_3 is in series with C_1 and C_2 around the tank circuit, the total capacitance is

$$C_T = \frac{1}{\dfrac{1}{C_1} + \dfrac{1}{C_2} + \dfrac{1}{C_3}}$$

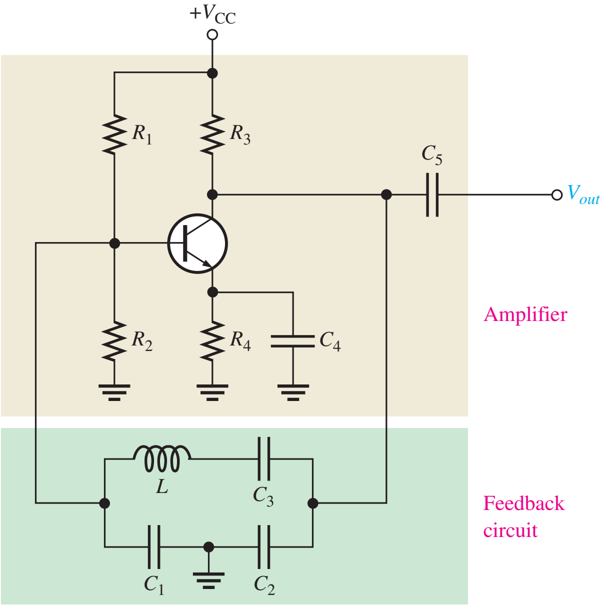
and the approximate frequency of oscillation ($Q > 10$) is

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}}$$

If C_3 is much smaller than C_1 and C_2, then C_3 almost entirely controls the resonant frequency ($f_r \cong 1/(2\pi\sqrt{LC_3})$). Since C_1 and C_2 are both connected to ground at one end, the junction capacitance of the transistor and other stray capacitances appear in parallel with C_1 and C_2 to ground, altering their effective values. C_3 is not affected, however, and thus provides a more accurate and stable frequency of oscillation.

FIGURE 16–22

A basic Clapp oscillator.

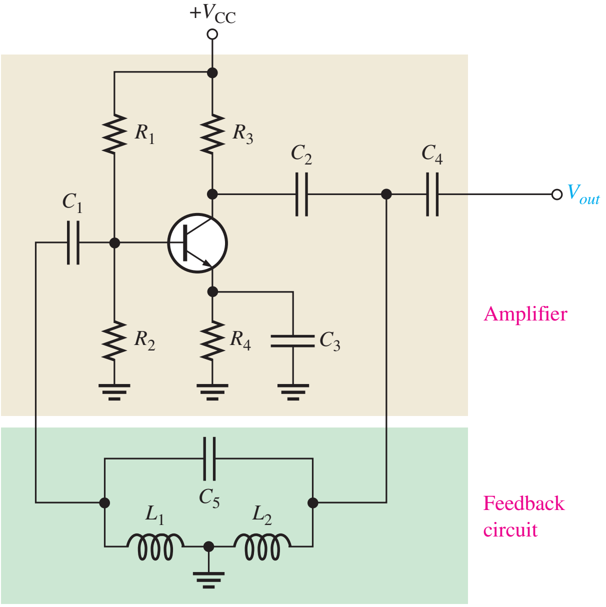

+V_{CC}
R_1
R_3
C_5
V_{out}
R_2
R_4
C_4
Amplifier
L
C_3
C_1
C_2
Feedback circuit

The Hartley Oscillator

The Hartley oscillator is similar to the Colpitts except that the feedback circuit consists of two series inductors and a parallel capacitor as shown in Figure 16–23.

FIGURE 16–23

A basic Hartley oscillator.


+V_{CC}
R_1
R_3
C_2
C_4
V_{out}
C_1
R_2
R_4
C_3
Amplifier
C_5
L_1
L_2
Feedback circuit

HISTORY NOTE

Ralph Vinton Lyon Hartley (1888–1970) invented the Hartley oscillator and the Hartley transform, a mathematical analysis method, which contributed to the foundations of information theory. In 1915 he was in charge of radio receiver development for the Bell System transatlantic radiotelephone tests. During this time he developed the Hartley oscillator. A patent for the oscillator was filed in 1915 and awarded in 1920.

In this circuit, the frequency of oscillation for $Q > 10$ is

$$f_r \cong \frac{1}{2\pi\sqrt{L_T C}}$$

where $L_T = L_1 + L_2$. The inductors act in a role similar to C_1 and C_2 in the Colpitts to determine the attenuation, B, of the feedback circuit.

$$B \cong \frac{L_1}{L_2}$$

To assure start-up of oscillation, A_v must be greater than $1/B$.

$$A_v \cong \frac{L_2}{L_1}$$

Equation 16–8

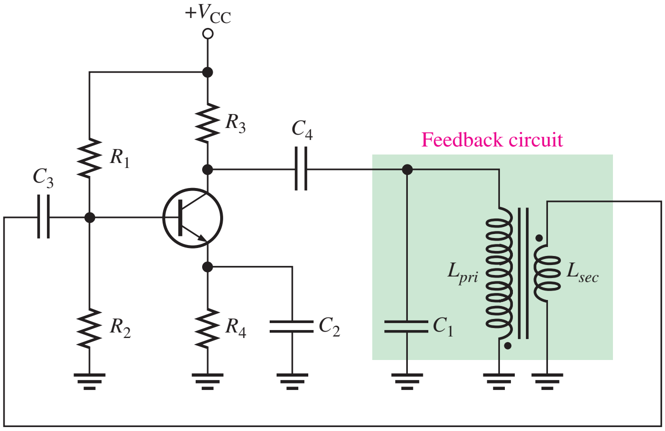
Loading of the tank circuit has the same effect in the Hartley as in the Colpitts; that is, the Q is decreased and thus f_r decreases.

The Armstrong Oscillator

This type of *LC* feedback oscillator uses transformer coupling to feed back a portion of the signal voltage, as shown in Figure 16–24. It is sometimes called a "tickler" oscillator in reference to the transformer secondary or "tickler coil" that provides the feedback to keep the oscillation going. The Armstrong is less common than the Colpitts, Clapp, and Hartley, mainly because of the disadvantage of transformer size and cost. The frequency of oscillation is set by the inductance of the primary winding (L_{pri}) in parallel with C_1.

$$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}}$$

Equation 16–9



◀ FIGURE 16–24

A basic Armstrong oscillator.

Crystal-Controlled Oscillators

The most stable and accurate type of feedback oscillator uses a piezoelectric **crystal** in the feedback loop to control the frequency.

The Piezoelectric Effect Quartz is one type of crystalline substance found in nature that exhibits a property called the **piezoelectric effect**. When a changing mechanical stress is applied across the crystal to cause it to vibrate, a voltage develops at the frequency of mechanical vibration. Conversely, when an ac voltage is applied across the crystal, it vibrates at the frequency of the applied voltage. The greatest vibration occurs at the crystal's natural resonant frequency, which is determined by the physical dimensions and by the way the crystal is cut.

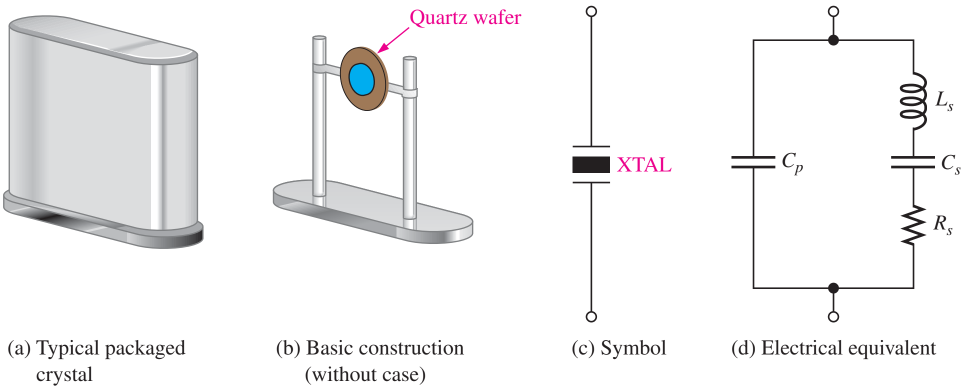
Crystals used in electronic applications typically consist of a quartz wafer mounted between two electrodes and enclosed in a protective "can" as shown in Figure 16–25(a) and (b). A schematic symbol for a crystal is shown in Figure 16–25(c), and an equivalent *RLC* circuit for the crystal appears in Figure 16–25(d). As you can see, the crystal's equivalent circuit is a series-parallel *RLC* circuit and can operate in either series resonance or parallel resonance. At the series resonant frequency, the inductive reactance is cancelled by the reactance of C_s. The remaining series resistor, R_s, determines the impedance of the crystal. Parallel resonance occurs when the inductive reactance and the reactance of the parallel capacitance, C_p, are equal. The parallel resonant frequency is usually at least 1 kHz higher

HISTORY NOTE

Edwin Howard Armstrong (1890–1954) was an American electrical engineer and inventor. He was the inventor of the FM radio. Armstrong also invented the regenerative circuit (patented 1914), the superheterodyne receiver (patented 1918) and the superregenerative circuit (patented 1922). Many of Armstrong's inventions were ultimately claimed by others in patent lawsuits. The Armstrong oscillator is named in his honor.

FIGURE 16–25

A quartz crystal.



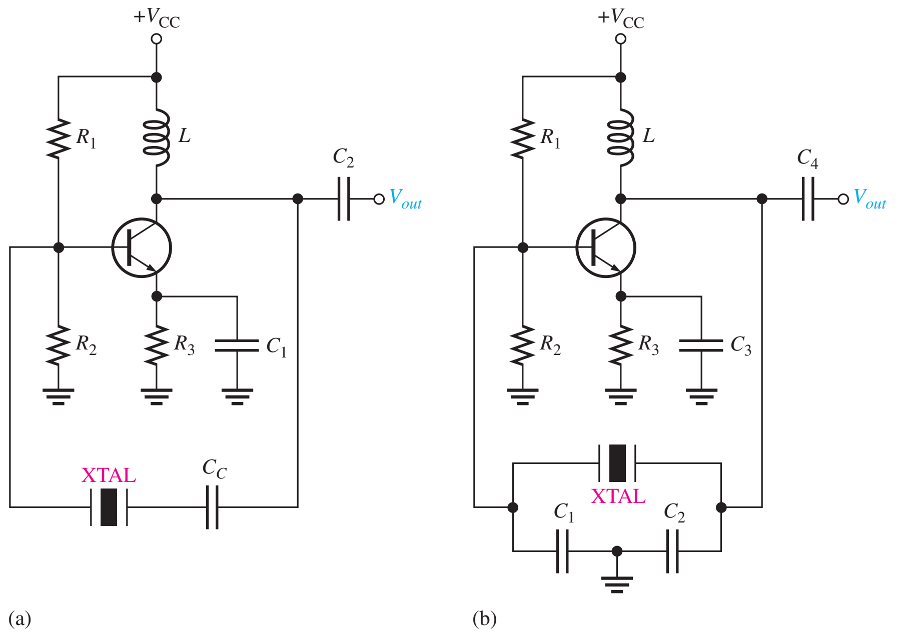
(a) Typical packaged crystal (b) Basic construction (without case) (c) Symbol (d) Electrical equivalent

than the series resonant frequency. A great advantage of the crystal is that it exhibits a very high Q (Qs with values of several thousand are typical).

An oscillator that uses a crystal as a series resonant tank circuit is shown in Figure 16–26(a). The impedance of the crystal is minimum at the series resonant frequency, thus providing maximum feedback. The crystal tuning capacitor, C_C, is used to "fine tune" the oscillator frequency by "pulling" the resonant frequency of the crystal slightly up or down.

FIGURE 16–26

Basic crystal oscillators.



A modified Colpitts configuration is shown in Figure 16–26(b) with a crystal acting as a parallel resonant tank circuit. The impedance of the crystal is maximum at parallel resonance, thus developing the maximum voltage across the capacitors. The voltage across C_1 is fed back to the input.

Modes of Oscillation in the Crystal

Piezoelectric crystals can oscillate in either of two modes—fundamental or overtone. The fundamental frequency of a crystal is the lowest frequency at which it is naturally resonant. The fundamental frequency depends on the crystal's mechanical dimensions, type of cut, and other factors, and is inversely proportional to the thickness of the crystal slab. Because a slab of crystal cannot be cut too thin without fracturing, there is an upper limit on the fundamental frequency. For most crystals, this upper limit is less than 20 MHz. For higher frequencies, the crystal must be operated in the overtone mode. Overtones are approximate integer multiples of the fundamental frequency. The overtone frequencies are usually, but not always, odd multiples (3, 5, 7, . . .) of the fundamental. Many crystal oscillators are available in integrated circuit packages.

SECTION 16–4 CHECKUP

1. What is the basic difference between the Colpitts and the Hartley oscillators?
2. What is the advantage of a FET amplifier in a Colpitts or Hartley oscillator?
3. How can you distinguish a Colpitts oscillator from a Clapp oscillator?

16–5 RELAXATION OSCILLATORS

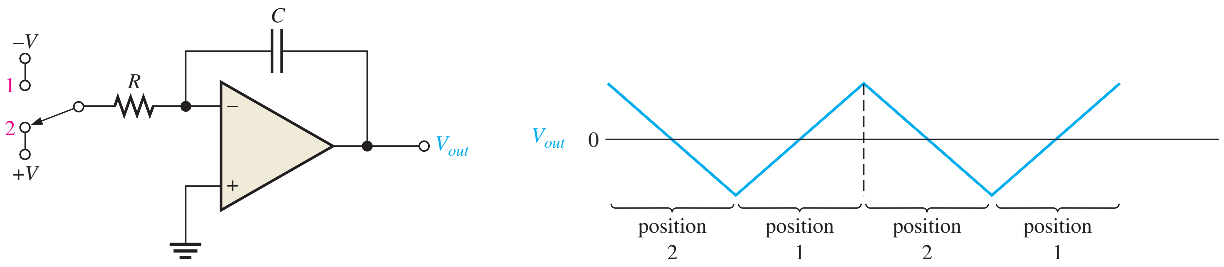
The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an *RC* timing circuit and a device that changes states to generate a periodic waveform. In this section, you will learn about several circuits that are used to produce nonsinusoidal waveforms.

After completing this section, you should be able to

- **Describe and analyze the operation of relaxation oscillators**
- Describe the operation of a triangular-wave oscillator
  - Discuss a practical triangular-wave oscillator
  - Define *function generator*
  - Determine the UTP, LTP, and frequency of oscillation
- Describe a sawtooth voltage-controlled oscillator (VCO)
  - Explain the purpose of the PUT in this circuit
  - Determine the frequency of oscillation
- Describe a square-wave oscillator

A Triangular-Wave Oscillator

The op-amp integrator covered in Chapter 13 can be used as the basis for a triangular-wave oscillator. The basic idea is illustrated in Figure 16–27(a) where a dual-polarity, switched input is used. We use the switch only to introduce the concept; it is not a practical way to implement this circuit. When the switch is in position 1, the negative voltage is applied, and the output is a positive-going ramp. When the switch is thrown into position 2, a negative-going ramp is produced. If the switch is thrown back and forth at fixed intervals, the output is a triangular wave consisting of alternating positive-going and negative-going ramps, as shown in Figure 16–27(b).



(a)

(b) Output voltage as the switch is thrown back and forth at regular intervals

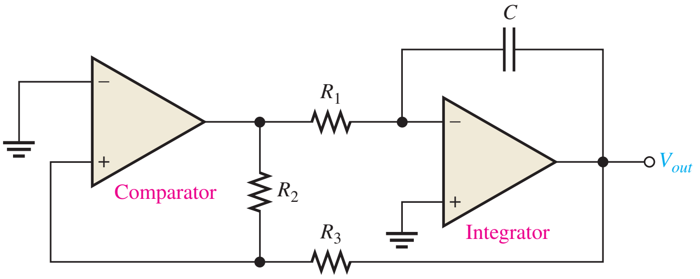
▲ FIGURE 16–27

Basic triangular-wave oscillator.

A Practical Triangular-Wave Oscillator One practical implementation of a triangular-wave oscillator utilizes an op-amp comparator with hysteresis to perform the switching function, as shown in Figure 16–28. The operation is as follows. To begin, assume that the output voltage of the comparator is at its maximum negative level. This output is connected to the inverting input of the integrator through R_1, producing a positive-going ramp on the output of the integrator. When the ramp voltage reaches the upper trigger point (UTP), the comparator switches to its maximum positive level. This positive level causes the integrator ramp to change to a negative-going direction. The ramp continues in this direction until the lower trigger point (LTP) of the comparator is reached. At this point, the comparator output switches back to the maximum negative level and the cycle repeats. This action is illustrated in Figure 16–29.

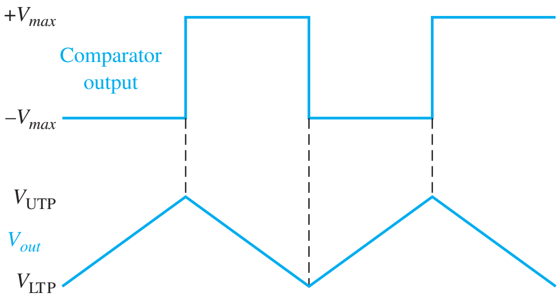
▶ **FIGURE 16–28**

A triangular-wave oscillator using two op-amps.



▶ **FIGURE 16–29**

Waveforms for the circuit in Figure 16–28.



Since the comparator produces a square-wave output, the circuit in Figure 16–28 can be used as both a triangular-wave oscillator and a square-wave oscillator. Devices of this type are commonly known as **function generators** because they produce more than one output function. The output amplitude of the square wave is set by the output swing of the comparator, and the resistors R_2 and R_3 set the amplitude of the triangular output by establishing the UTP and LTP voltages according to the following formulas:

$$V_{\text{UTP}} = +V_{max}\left(\frac{R_3}{R_2}\right)$$

$$V_{\text{LTP}} = -V_{max}\left(\frac{R_3}{R_2}\right)$$

where the comparator output levels, $+V_{max}$ and $-V_{max}$, are equal. The frequency of both waveforms depends on the R_1C time constant as well as the amplitude-setting resistors, R_2 and R_3. By varying R_1, the frequency of oscillation can be adjusted without changing the output amplitude.

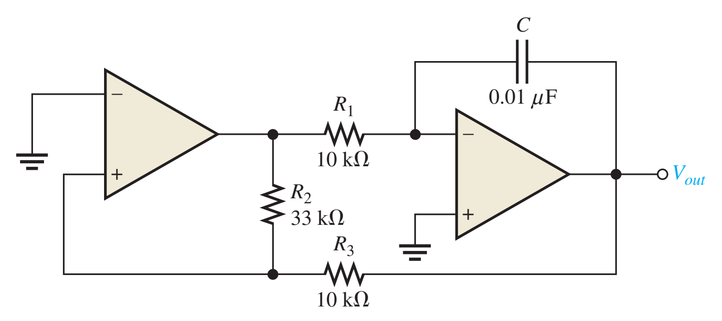
Equation 16–10

$$\boldsymbol{f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right)}$$

EXAMPLE 16–4

Determine the frequency of oscillation of the circuit in Figure 16–30. To what value must R_1 be changed to make the frequency 20 kHz?

▶ FIGURE 16–30



Solution

$$f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right) = \left(\frac{1}{4(10\,\text{k}\Omega)(0.01\,\mu\text{F})}\right)\left(\frac{33\,\text{k}\Omega}{10\,\text{k}\Omega}\right) = \mathbf{8.25\,kHz}$$

To make $f = 20$ kHz,

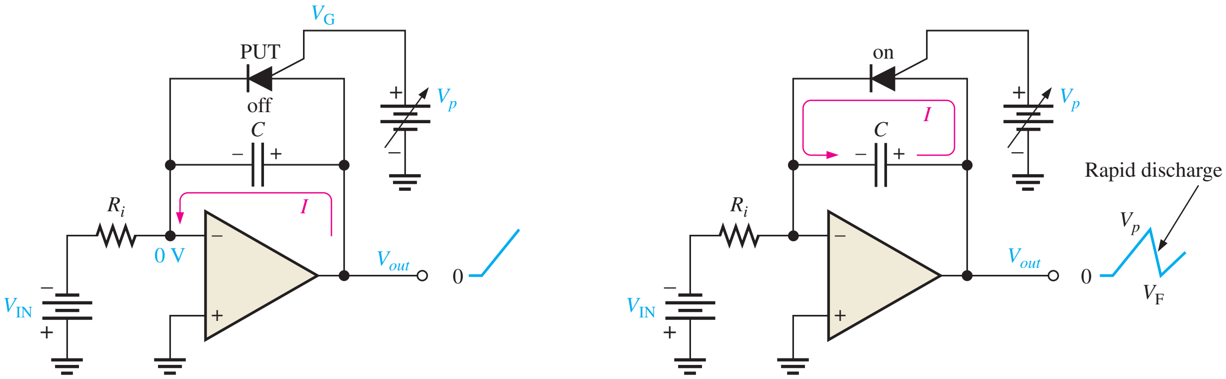
$$R_1 = \frac{1}{4fC}\left(\frac{R_2}{R_3}\right) = \left(\frac{1}{4(20\,\text{kHz})(0.01\,\mu\text{F})}\right)\left(\frac{33\,\text{k}\Omega}{10\,\text{k}\Omega}\right) = \mathbf{4.13\,k\Omega}$$

Related Problem What is the amplitude of the triangular wave in Figure 16–30 if the comparator output is ±10 V?

A Sawtooth Voltage-Controlled Oscillator (VCO)

The **voltage-controlled oscillator (VCO)** is a relaxation oscillator whose frequency can be changed by a variable dc control voltage. VCOs can be either sinusoidal or nonsinusoidal. One way to build a sawtooth VCO is with an op-amp integrator that uses a switching device (PUT) in parallel with the feedback capacitor to terminate each ramp at a prescribed level and effectively "reset" the circuit. Figure 16–31(a) shows the implementation.

As you learned in Chapter 11, the PUT is a programmable unijunction transistor with an anode, a cathode, and a gate terminal. The gate is always biased positively with respect to



(a) Initially, the capacitor charges, the output ramp begins, and the PUT is off.

(b) The capacitor rapidly discharges when the PUT momentarily turns on.

▲ FIGURE 16–31

Sawtooth VCO operation.

the cathode. When the anode voltage exceeds the gate voltage by approximately 0.7 V, the PUT turns on and acts as a forward-biased diode. When the anode voltage falls below this level, the PUT turns off. Also, the current must be above the holding value to maintain conduction.

The operation of the sawtooth VCO begins when the negative dc input voltage, $-V_{IN}$, produces a positive-going ramp on the output. During the time that the ramp is increasing, the circuit acts as a regular integrator. The PUT triggers on when the output ramp (at the anode) exceeds the gate voltage by 0.7 V. The gate is set to the approximate desired sawtooth peak voltage. When the PUT turns on, the capacitor rapidly discharges, as shown in Figure 16–31(b). The capacitor does not discharge completely to zero because of the PUT's forward voltage, V_F. Discharge continues until the PUT current falls below the holding value. At this point, the PUT turns off and the capacitor begins to charge again, thus generating a new output ramp. The cycle continually repeats, and the resulting output is a repetitive sawtooth waveform, as shown. The sawtooth amplitude and period can be adjusted by varying the PUT gate voltage.

The frequency of oscillation is determined by the R_iC time constant of the integrator and the peak voltage set by the PUT. Recall that the charging rate of a capacitor is V_{IN}/R_iC. The time it takes a capacitor to charge from V_F to V_p is the period, T, of the sawtooth waveform (neglecting the rapid discharge time).

$$T = \frac{V_p - V_F}{|V_{IN}|/R_iC}$$

From $f = 1/T$,

Equation 16–11

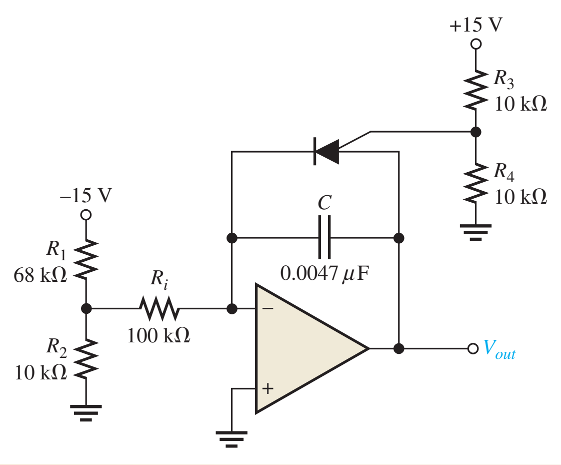
$$\boldsymbol{f = \frac{|V_{IN}|}{R_iC}\left(\frac{1}{V_p - V_F}\right)}$$

EXAMPLE 16–5

(a) Find the amplitude and frequency of the sawtooth output in Figure 16–32. Assume that the forward PUT voltage, V_F, is approximately 1 V.

(b) Sketch the output waveform.

▶ FIGURE 16–32



Solution

(a) First, find the gate voltage in order to establish the approximate voltage at which the PUT turns on.

$$V_G = \frac{R_4}{R_3 + R_4}(+V) = \frac{10\ \text{k}\Omega}{20\ \text{k}\Omega}(15\ \text{V}) = 7.5\ \text{V}$$

This voltage sets the approximate maximum peak value of the sawtooth output (neglecting the 0.7 V).

$$V_p \cong 7.5\text{ V}$$

The minimum peak value (low point) is

$$V_{\text{F}} \cong 1\text{ V}$$

So the peak-to-peak amplitude is

$$V_{pp} = V_p - V_{\text{F}} = 7.5\text{ V} - 1\text{ V} = \mathbf{6.5\text{ V}}$$

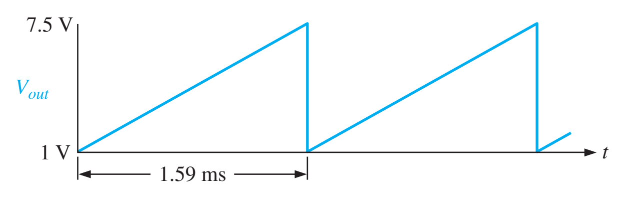
Determine the frequency as follows:

$$V_{\text{IN}} = \frac{R_2}{R_1 + R_2}(-V) = \frac{10\text{ k}\Omega}{78\text{ k}\Omega}(-15\text{ V}) = -1.92\text{ V}$$

$$f = \frac{|V_{\text{IN}}|}{R_iC}\left(\frac{1}{V_p - V_{\text{F}}}\right) = \left(\frac{1.92\text{ V}}{(100\text{ k}\Omega)(0.0047\mu\text{F})}\right)\left(\frac{1}{7.5\text{ V} - 1\text{ V}}\right) = \mathbf{628\text{ Hz}}$$

(b) The output waveform is shown in Figure 16–33, where the period is determined as follows:

$$T = \frac{1}{f} = \frac{1}{628\text{ Hz}} = 1.59\text{ ms}$$



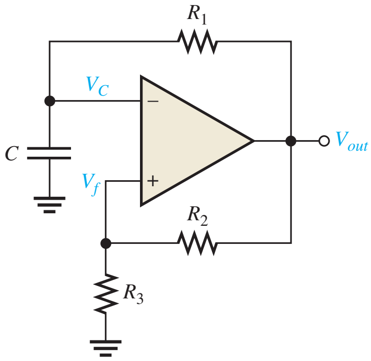
▲ FIGURE 16–33

Output of the circuit in Figure 16–32.

Related Problem If R_i is changed to 56 kΩ in Figure 16–32, what is the frequency?

A Square-Wave Oscillator

The basic square-wave oscillator shown in Figure 16–34 is a type of relaxation oscillator because its operation is based on the charging and discharging of a capacitor. Notice that the op-amp's inverting input is the capacitor voltage and the noninverting input is a portion of the output fed back through resistors R_2 and R_3 to provide hysteresis. When the circuit is first turned on, the capacitor is uncharged, and thus the inverting input is at 0 V. This makes the output a positive maximum, and the capacitor begins to charge toward V_{out} through R_1. When the capacitor voltage (V_C) reaches a value equal to the feedback voltage (V_f) on the noninverting input, the op-amp switches to the maximum negative state. At this point, the capacitor begins to discharge from $+V_f$ toward $-V_f$. When the capacitor voltage reaches $-V_f$, the op-amp switches back to the maximum positive state. This action continues to repeat, as shown in Figure 16–35, and a square-wave output voltage is obtained.



▲ FIGURE 16–34

A square-wave relaxation oscillator.

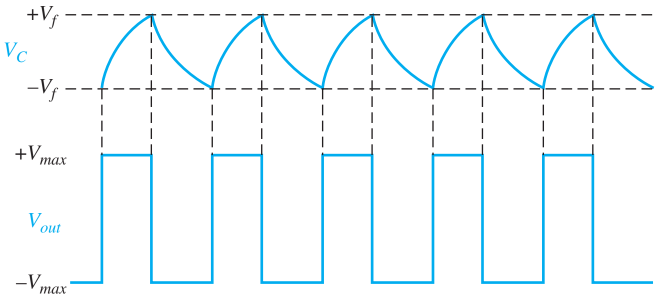


FIGURE 16–35

Waveforms for the square-wave relaxation oscillator.

SECTION 16–5 CHECKUP

1. What is a VCO, and basically, what does it do?
2. Upon what principle does a relaxation oscillator operate?

16–6 THE 555 TIMER AS AN OSCILLATOR

The 555 timer is a versatile integrated circuit with many applications. In this section, you will see how the 555 is configured as an astable or free-running multivibrator, which is essentially a square-wave oscillator. The use of the 555 timer as a voltage-controlled oscillator (VCO) is also discussed.

After completing this section, you should be able to

- ❑ **Discuss and analyze the 555 timer and use it in oscillator applications**
- ❑ Describe the astable operation of a 555 timer
  - ◆ Determine the frequency of oscillation ◆ Determine the duty cycle
- ❑ Discuss the 555 timer as a voltage-controlled oscillator
  - ◆ Describe the connections

The 555 timer consists basically of two comparators, a flip-flop, a discharge transistor, and a resistive voltage divider, as shown in Figure 16–36. The flip-flop (bistable multivibrator) is a digital device that may be unfamiliar to you at this point unless you already have taken a digital fundamentals course. Briefly, it is a two-state device whose output can be at either a high voltage level (set, *S*) or a low voltage level (reset, *R*). The state of the output can be changed with proper input signals.

The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value; therefore, the upper comparator has a reference of $\frac{2}{3}V_{CC}$, and the lower comparator has a reference of $\frac{1}{3}V_{CC}$. The comparators' outputs control the state of the flip-flop. When the trigger voltage goes below $\frac{1}{3}V_{CC}$, the flip-flop sets and the output jumps to its high level. The threshold input is normally connected to an external *RC* timing circuit. When the external capacitor voltage exceeds $\frac{2}{3}V_{CC}$, the upper comparator resets the flip-flop, which in turn switches the output back to its low level. When the device output is low, the discharge transistor (Q_d) is turned on and provides a path for rapid discharge of the external timing capacitor. This basic operation allows the timer to be configured with external components as an oscillator, a one-shot, or a time-delay element.

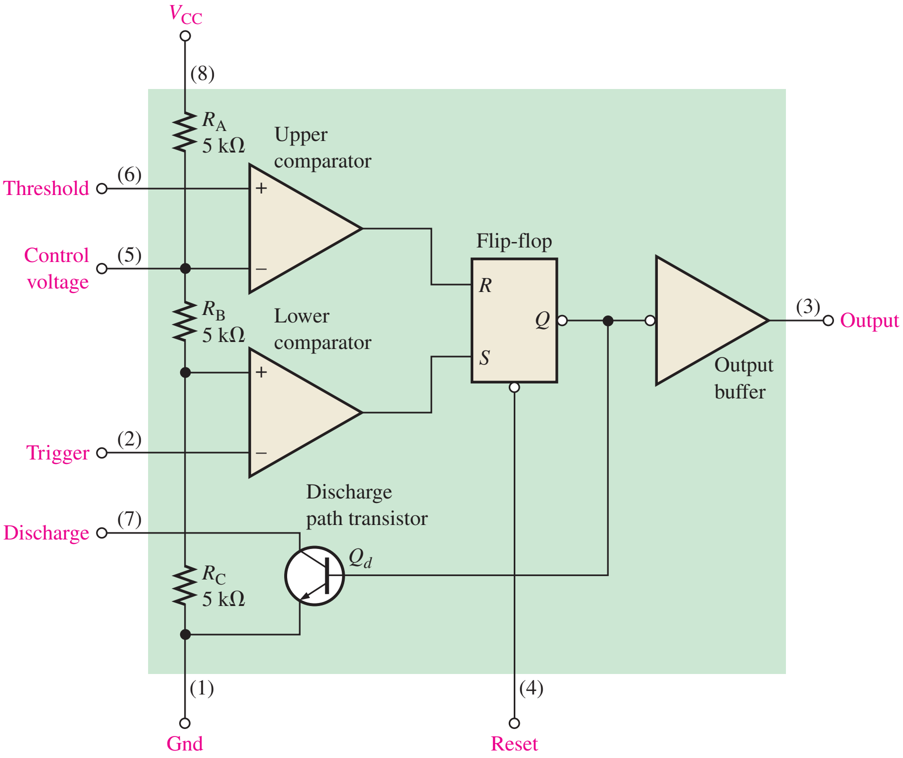

V_{CC}
(8)
R_A 5 kΩ
Upper comparator
Threshold (6)
+
Control voltage (5)
−
Flip-flop
R
Q
S
R_B 5 kΩ
Lower comparator
+
(3) Output
Output buffer
Trigger (2)
−
Discharge path transistor
Discharge (7)
Q_d
R_C 5 kΩ
(1)
Gnd
(4)
Reset

FIGURE 16–36

Internal diagram of a 555 integrated circuit timer. (IC pin numbers are in parentheses.)

Astable Operation

A 555 timer connected to operate in the **astable** mode as a free-running relaxation oscillator (astable multivibrator) is shown in Figure 16–37. Notice that the threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1, R_2, and C_{ext} form the timing circuit that sets the frequency of oscillation. The 0.01 μF capacitor connected to the control (CONT) input is strictly for decoupling and has no effect on the operation.

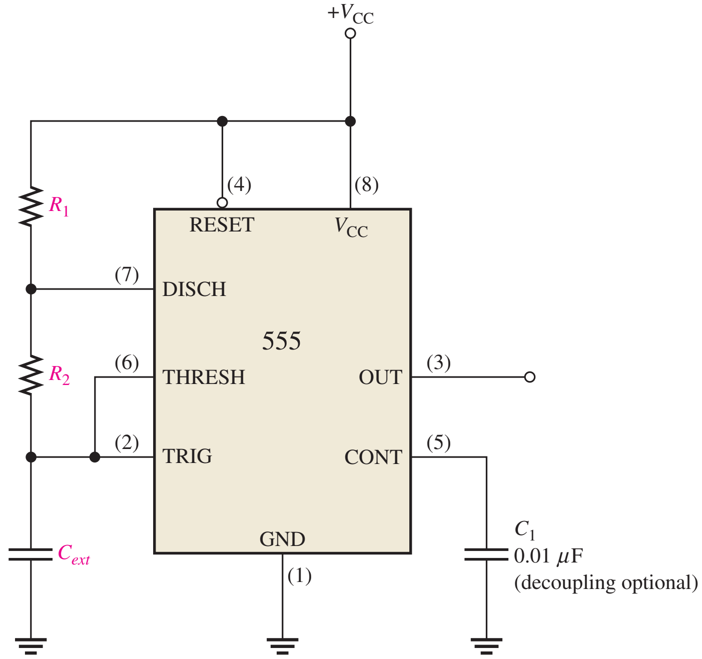
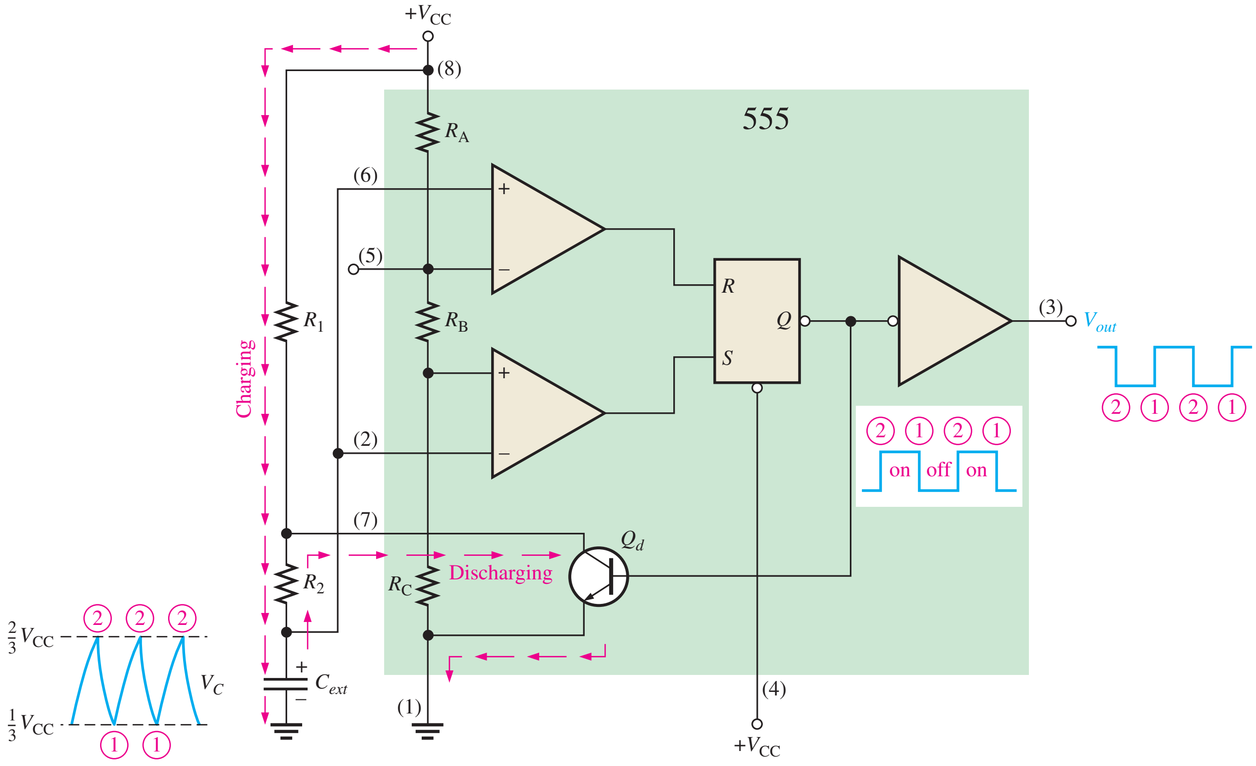

$+V_{CC}$
(4)
(8)
RESET
V_{CC}
R_1
(7)
DISCH
555
R_2
(6)
THRESH
OUT
(3)
(2)
TRIG
CONT
(5)
C_{ext}
GND
(1)
C_1
0.01 μF
(decoupling optional)

FIGURE 16–37

The 555 timer connected as an astable multivibrator.

Initially, when the power is turned on, the capacitor C_{ext} is uncharged and thus the trigger voltage (pin 2) is at 0 V. This causes the output of the lower comparator to be high and the output of the upper comparator to be low, forcing the output of the flip-flop, and thus the base of Q_d, low and keeping the transistor off. Now, C_{ext} begins charging through R_1 and R_2 as indicated in Figure 16–38. When the capacitor voltage reaches $\frac{1}{3}V_{CC}$, the lower comparator switches to its low output state, and when the capacitor voltage reaches $\frac{2}{3}V_{CC}$, the upper comparator switches to its high output state. This resets the flip-flop, causes the base of Q_d to go high, and turns on the transistor. This sequence creates a discharge path for the capacitor through R_2 and the transistor, as indicated. The capacitor now begins to discharge, causing the upper comparator to go low. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, the lower comparator switches high, setting the flip-flop, which makes the base of Q_d low and turns off the transistor. Another charging cycle begins, and the entire process repeats. The result is a rectangular wave output whose duty cycle depends on the values of R_1 and R_2.



▲ FIGURE 16–38

Operation of the 555 timer in the astable mode.

The frequency of oscillation is given by Equation 16–12, or it can be found using the graph in Figure 16–39.

Equation 16–12

$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$$

By selecting R_1 and R_2, the duty cycle of the output can be adjusted. Since C_{ext} charges through $R_1 + R_2$ and discharges only through R_2, duty cycles approaching a minimum of 50 percent can be achieved if $R_2 >> R_1$ so that the charging and discharging times are approximately equal.

A formula to calculate the duty cycle is developed as follows. The time that the output is high (t_H) is how long it takes C_{ext} to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$. It is expressed as

$$t_H = 0.694(R_1 + R_2)C_{ext}$$

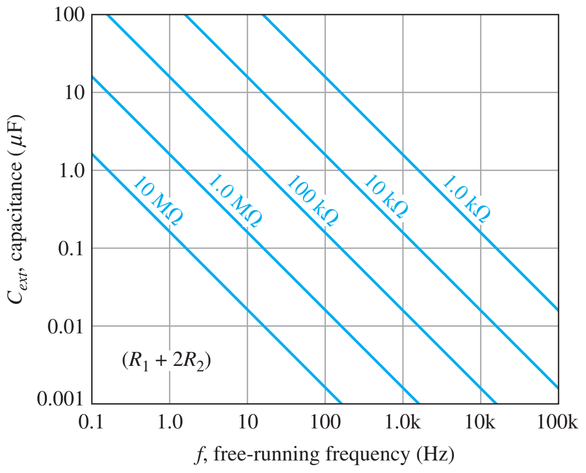


FIGURE 16–39

Frequency of oscillation (free-running frequency) of a 555 timer in the astable mode as a function of C_{ext} and $R_1 + 2R_2$. The sloped lines are values of $R_1 + 2R_2$.

The time that the output is low (t_L) is how long it takes C_{ext} to discharge from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$. It is expressed as

$$t_L = 0.694R_2C_{ext}$$

The period, T, of the output waveform is the sum of t_H and t_L. The following formula for T is the reciprocal of f in Equation 16–12.

$$T = t_H + t_L = 0.694(R_1 + 2R_2)C_{ext}$$

Finally, the percent duty cycle is

$$\text{Duty cycle} = \left(\frac{t_H}{T}\right)100\% = \left(\frac{t_H}{t_H + t_L}\right)100\%$$

$$\textbf{Duty cycle} = \left(\frac{\boldsymbol{R_1 + R_2}}{\boldsymbol{R_1 + 2R_2}}\right)\mathbf{100\%}$$

Equation 16–13

To achieve duty cycles of less than 50 percent, the circuit in Figure 16–37 can be modified so that C_{ext} charges through only R_1 and discharges through R_2. This is achieved with a diode, D_1, placed as shown in Figure 16–40. The duty cycle can be made less than 50

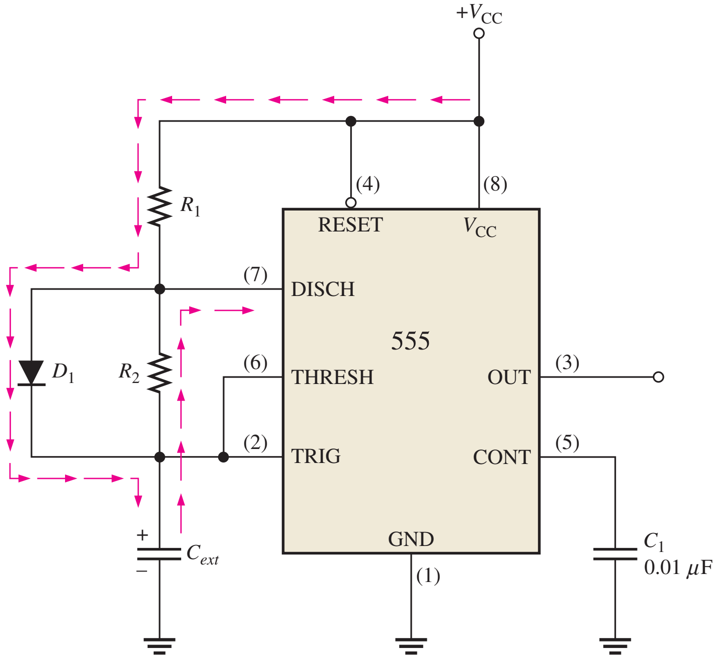


FIGURE 16–40

The addition of diode D_1 allows the duty cycle of the output to be adjusted to less than 50 percent by making $R_1 < R_2$.

percent by making R_1 less than R_2. Under this condition, the formulas for the frequency and percent duty cycle are (assuming an ideal diode)

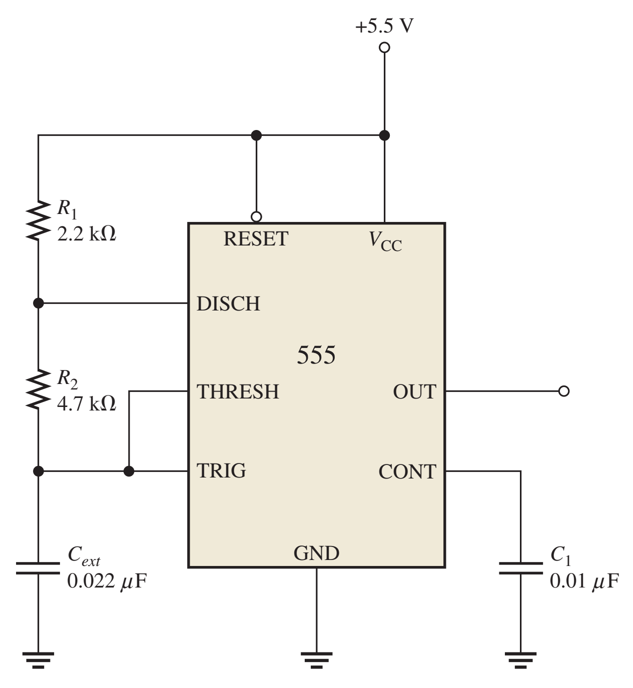
$$f_r \cong \frac{1.44}{(R_1 + R_2)\,C_{ext}}$$

$$\text{Duty cycle} \cong \left(\frac{R_1}{R_1 + R_2}\right)100\%$$

EXAMPLE 16–6

A 555 timer configured to run in the astable mode (oscillator) is shown in Figure 16–41. Determine the frequency of the output and the duty cycle.

▶ FIGURE 16–41



Solution

$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}} = \frac{1.44}{(2.2\text{ k}\Omega + 9.4\text{ k}\Omega)0.022\ \mu\text{F}} = \mathbf{5.64\ kHz}$$

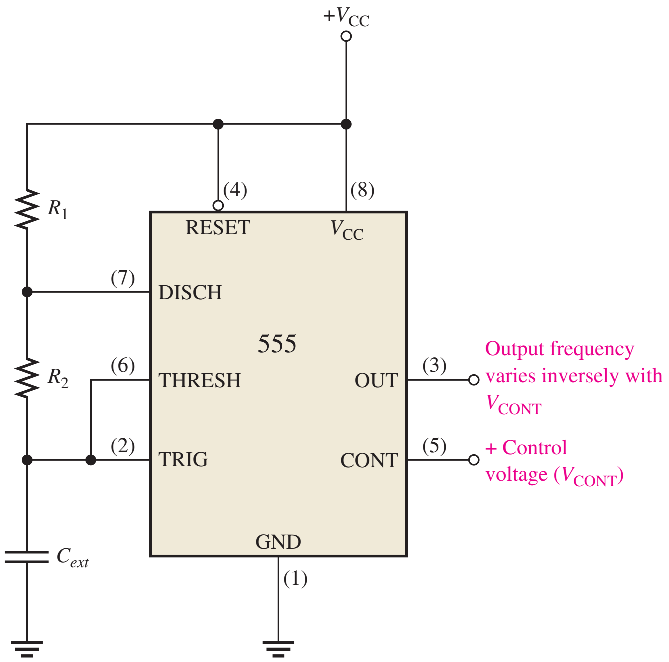
$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\% = \left(\frac{2.2\text{ k}\Omega + 4.7\text{ k}\Omega}{2.2\text{ k}\Omega + 9.4\text{ k}\Omega}\right)100\% = \mathbf{59.5\%}$$

Related Problem Determine the duty cycle in Figure 16–41 if a diode is connected across R_2 as indicated in Figure 16–40.

Operation as a Voltage-Controlled Oscillator (VCO)

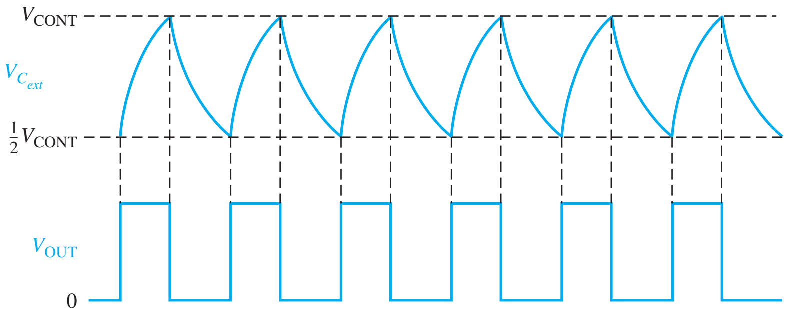
A 555 timer can be set up to operate as a VCO by using the same external connections as for astable operation, with the exception that a variable control voltage is applied to the CONT input (pin 5), as indicated in Figure 16–42.

As shown in Figure 16–43, the control voltage (V_{CONT}) changes the threshold values of $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ for the internal comparators. With the control voltage, the upper value is V_{CONT} and the lower value is $\frac{1}{2}V_{CONT}$, as you can see by examining the internal diagram of the 555 timer. When the control voltage is varied, the output frequency also varies. An


$+V_{CC}$
(4)
(8)
R_1
RESET
V_{CC}
(7)
DISCH
555
R_2
(6)
THRESH
OUT
(3)
Output frequency varies inversely with V_{CONT}
(2)
TRIG
CONT
(5)
+ Control voltage (V_{CONT})
C_{ext}
GND
(1)

▲ **FIGURE 16–42**

The 555 timer connected as a voltage-controlled oscillator (VCO). Note the variable control voltage input on pin 5.



▲ **FIGURE 16–43**

The VCO output frequency varies inversely with V_{CONT} because the charging and discharging time of C_{ext} is directly dependent on the control voltage.

increase in V_{CONT} increases the charging and discharging time of the external capacitor and causes the frequency to decrease. A decrease in V_{CONT} decreases the charging and discharging time of the capacitor and causes the frequency to increase.

An interesting application of the VCO is in phase-locked loops, which are used in various types of communication receivers to track variations in the frequency of incoming signals.

SECTION 16–6 CHECKUP

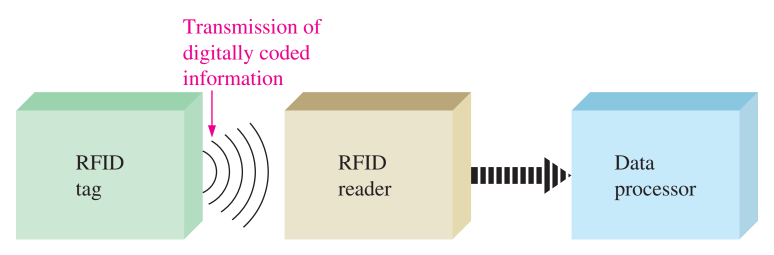
1. Name the five basic elements in a 555 timer IC.
2. When the 555 timer is configured as an astable multivibrator, how is the duty cycle determined?

Application Activity: *ASK Test Generator*

The RFID reader board that was developed in the Chapter 15 Application Activity requires an ASK modulated source to test it. Recall that the RFID tag transmits a 125 kHz ASK (amplitude shift keyed) signal modulated with coded information represented by a digital waveform. The basic block diagram is shown in Figure 16–44.

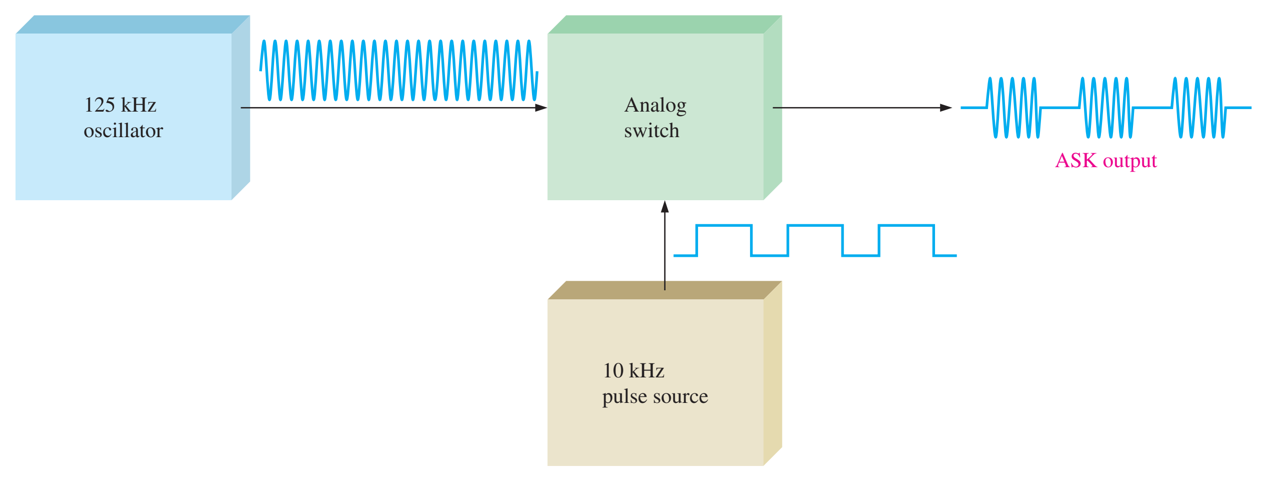
▶ FIGURE 16–44

Basic block diagram of an RFID system.



The ASK Test Generator

The purpose of this application is to develop a signal source for testing the RFID reader circuit board. The source must produce a 125 kHz signal that is modulated with a 10 kHz pulse signal to simulate the RFID tag. An oscillator is used to generate the 125 kHz carrier signal, and a 555 timer produces the modulating pulse signal. The modulating device is an analog switch that allows the carrier signal to be turned on and off by the modulating pulse signal. A basic block diagram is shown in Figure 16–45.



▲ FIGURE 16–45

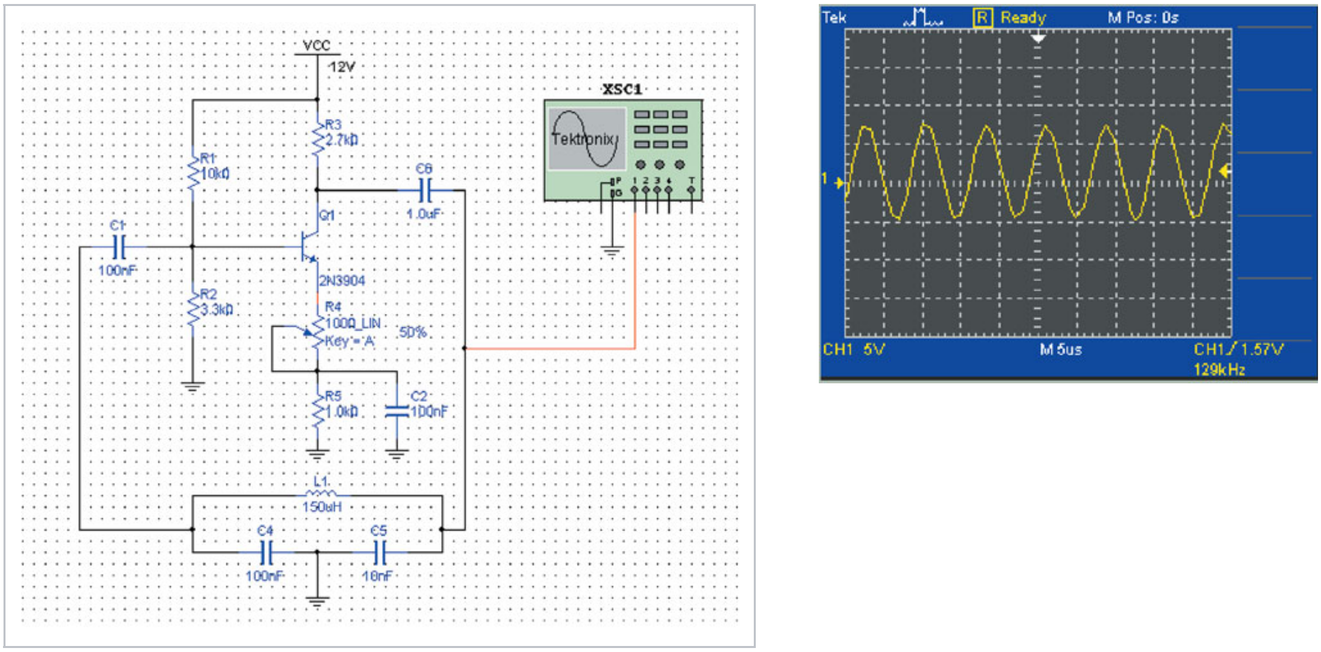
Basic block diagram of the ASK test generator.

Simulation

The first step is to design the 125 kHz oscillator circuit. The type of oscillator chosen for this application is the Colpitts oscillator. The simulated circuit is shown in Figure 16–46(a), and the output waveform is shown in part (b).

1. Calculate the gain of the Colpitts oscillator in Figure 16–46.
2. Calculate the frequency of the Colpitts oscillator and compare to the frequency measured in the simulation.

In the second step, the 10 kHz pulse oscillator is designed using a 555 timer. The simulated circuit and output waveform are shown in Figure 16–47.

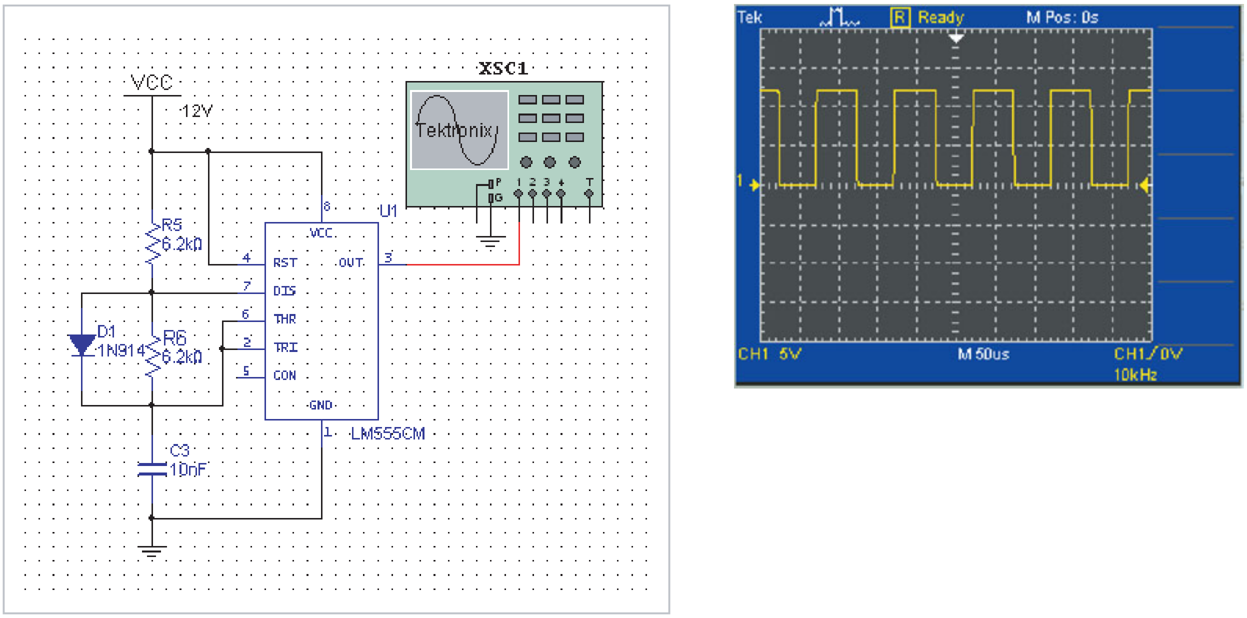

VCC
12V
XSC1
Tektronix
R3
2.7kΩ
R1
10kΩ
C6
1.0uF
C1
100nF
Q1
2N3904
R2
3.3kΩ
R4
100Ω_LIN
Key = A
50%
R5
1.0kΩ
C2
100nF
L1
150uH
C4
100nF
C5
10nF
Tek
Ready
M Pos: 0s
1
CH1 5V
M 5us
CH1 ╱ 1.57V
129kHz

(a)

(b)

▲ **FIGURE 16–46**

Colpitts oscillator for generating the 125 kHz carrier signal.


XSC1
Tektronix
VCC
12V
U1
R5
6.2kΩ
8
VCC
4
RST
OUT
3
7
DIS
6
THR
D1
1N914
R6
6.2kΩ
2
TRI
5
CON
GND
1
LM555CM
C3
10nF
Tek
Ready
M Pos: 0s
1
CH1 5V
M 50us
CH1 ╱ 0V
10kHz

(a)

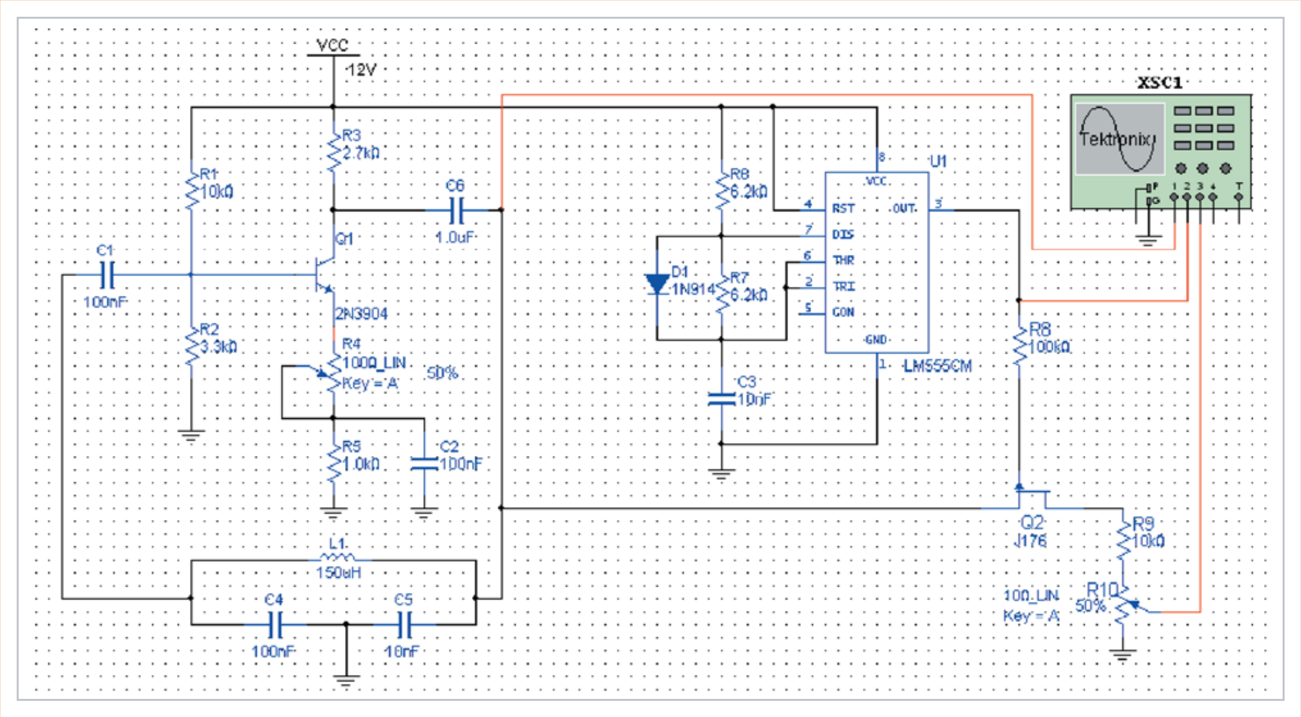
(b)

▲ **FIGURE 16–47**

555 timer configured for generating a 10 kHz square wave.

3. Calculate the frequency of the pulse oscillator in Figure 16–47 and compare to the measured frequency in the simulation.
4. Describe a possible reason for the difference in the calculated and the simulated value of frequency.

The third step in the simulation of the ASK test generator is to combine the Colpitts oscillator with the 555 timer and add an analog switch. For the purpose of switching the carrier signal on and off, a *p*-channel JFET is used. When the timer output is low, the JFET turns on and passes the carrier signal to the ASK output. When the timer output is high, the JFET turns off and blocks the signal from the output. The complete circuit is shown in Figure 16–48, and the resulting waveforms are shown in Figure 16–49.


VCC
12V
XSC1
Tektronix
R3
2.7kΩ
R1
10kΩ
C6
1.0uF
Q1
C1
100nF
2N3904
R2
3.3kΩ
R4
100Ω_LIN
Key = A
50%
R5
1.0kΩ
C2
100nF
L1
150uH
C4
100nF
C5
10nF
R8
6.2kΩ
D1
1N914
R7
6.2kΩ
C3
10nF
U1
8
VCC
4
RST
OUT
3
7
DIS
6
THR
2
TRI
5
CON
GND
1
LM555CM
R8
100kΩ
Q2
J176
R9
10kΩ
R10
100_LIN
Key = A
50%
1 2 3 4
T

▲ **FIGURE 16–48**

The complete ASK test generator.

5. What is the purpose of Q_2 in the ASK test generator circuit?

Finally, a simulation is run with the ASK test generator driving the RFID reader. This is shown in Figure 16–50.

6. Identify each waveform in Figure 16–50.

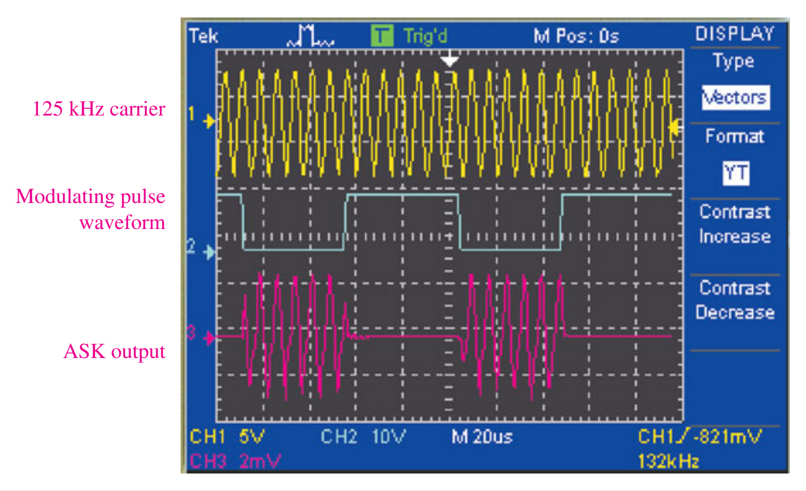
Simulate the ASK test generator using your Multisim software. Observe the operation with the oscilloscope.

Prototyping and Testing

Now that the circuit has been simulated, the prototype circuit is constructed and tested. After the circuit is successfully tested on a protoboard, it is ready to be finalized on a printed circuit board.

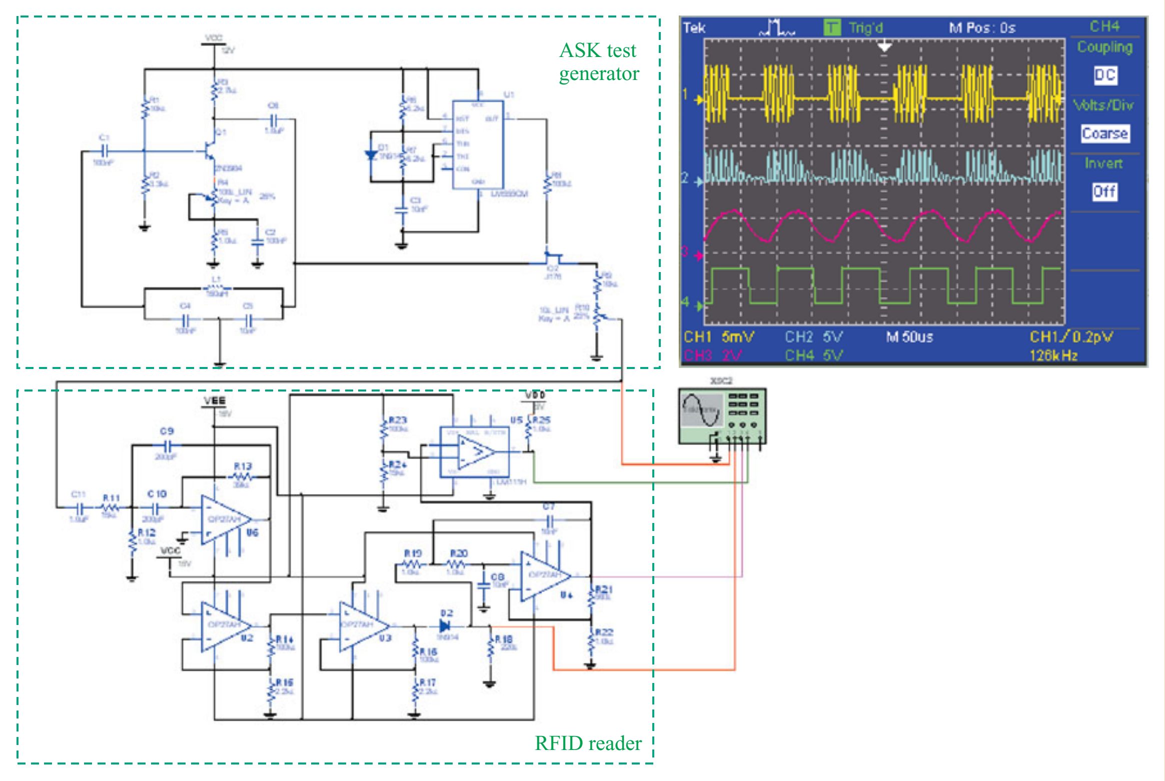
▶ FIGURE 16–49

Waveforms for the ASK test generator.


125 kHz carrier

Modulating pulse waveform

ASK output
Tek
Trig'd
M Pos: 0s
DISPLAY
Type
Vectors
Format
YT
Contrast Increase
Contrast Decrease
1
2
3
CH1 5V
CH2 10V
M 20us
CH1 ∕ -821mV
CH3 2mV
132kHz


ASK test generator
RFID reader
Tek
Trig'd
M Pos: 0s
CH4
Coupling
DC
Volts/Div
Coarse
Invert
Off
1
2
3
4
CH1 5mV
CH2 5V
M 50us
CH1 ∕ 0.2pV
CH3 2V
CH4 5V
126kHz
XSC2
VCC
VEE
VDD
U1
LM555CM
OP27AH
U2
U3
U4
U6
U5
LM111H
Q1
2N3904
Q2
J176
D1
D2
1N914

▲ FIGURE 16–50

Simulation of the ASK test generator driving the RFID reader.

Lab Experiment

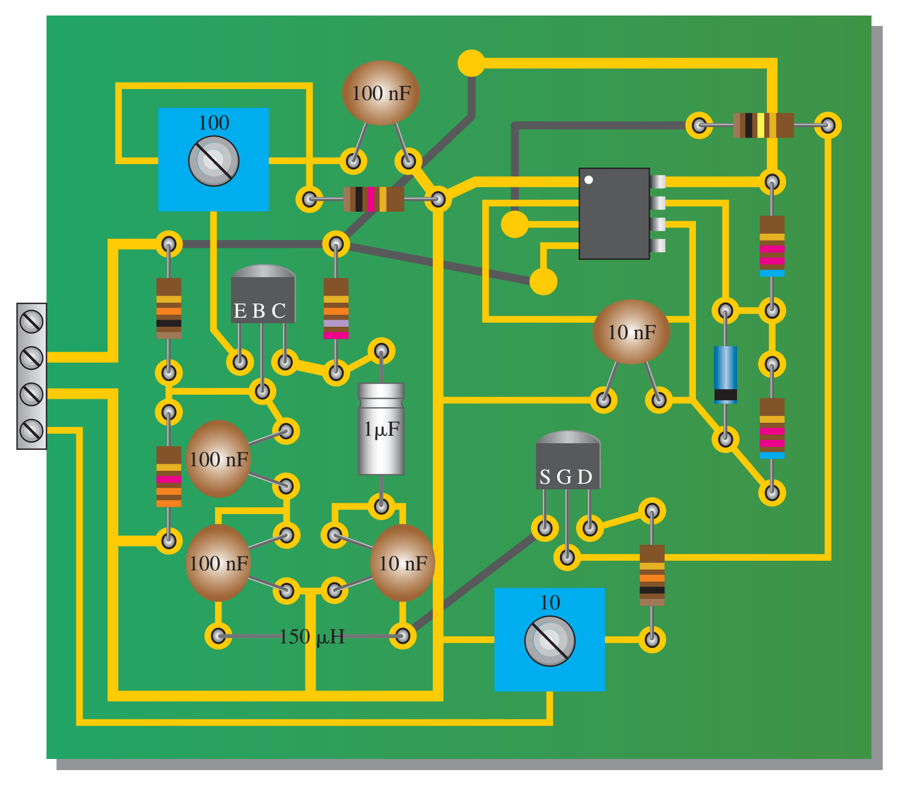
To build and test a circuit similar to one used in the ASK test generator, go to Experiment 16–A in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Circuit Board

The ASK test generator is implemented on a printed circuit board as shown in Figure 16–51 and will be housed in a unit for use in testing RFID readers on the assembly line. The dark gray lines represent backside connections.

FIGURE 16–51

ASK test generator board.



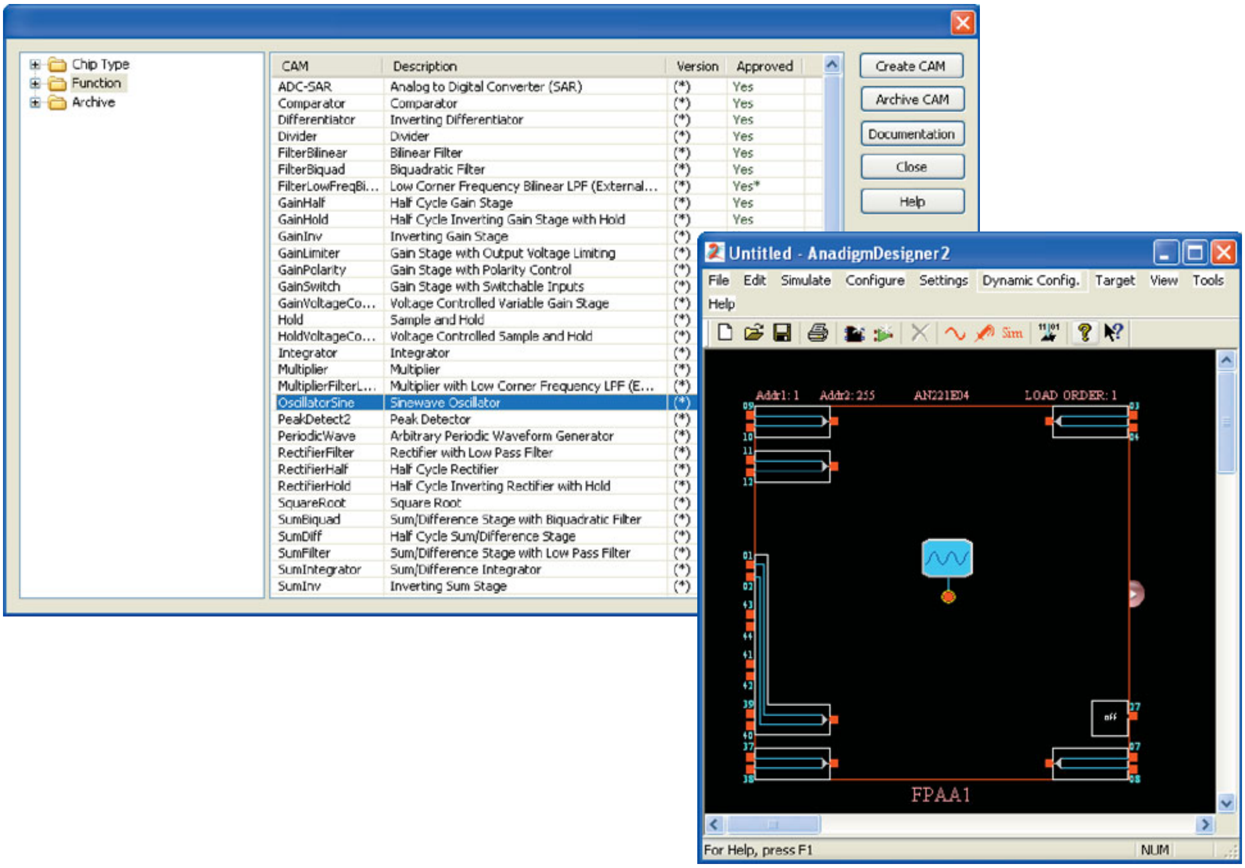
7. Check the printed circuit board and verify that it agrees with the simulation schematic in Figure 16–48.
8. Label each input and output pin according to function.

Programmable Analog Technology

Oscillators with various types of outputs can be programmed into an FPAA or a dpASP. These are described as follows.

Sine-Wave Oscillator

Oscillators can be implemented in programmable analog arrays using software. A sine-wave oscillator is shown in Figure 16–52 using AnadigmDesigner2.



CAM	Description	Version	Approved
ADC-SAR	Analog to Digital Converter (SAR)	(*)	Yes
Comparator	Comparator	(*)	Yes
Differentiator	Inverting Differentiator	(*)	Yes
Divider	Divider	(*)	Yes
FilterBilinear	Bilinear Filter	(*)	Yes
FilterBiquad	Biquadratic Filter	(*)	Yes
FilterLowFreqBi...	Low Corner Frequency Bilinear LPF (External...	(*)	Yes*
GainHalf	Half Cycle Gain Stage	(*)	Yes
GainHold	Half Cycle Inverting Gain Stage with Hold	(*)	Yes
GainInv	Inverting Gain Stage	(*)	
GainLimiter	Gain Stage with Output Voltage Limiting	(*)	
GainPolarity	Gain Stage with Polarity Control	(*)	
GainSwitch	Gain Stage with Switchable Inputs	(*)	
GainVoltageCo...	Voltage Controlled Variable Gain Stage	(*)	
Hold	Sample and Hold	(*)	
HoldVoltageCo...	Voltage Controlled Sample and Hold	(*)	
Integrator	Integrator	(*)	
Multiplier	Multiplier	(*)	
MultiplierFilterL...	Multiplier with Low Corner Frequency LPF (E...	(*)	
OscillatorSine	Sinewave Oscillator	(*)	
PeakDetect2	Peak Detector	(*)	
PeriodicWave	Arbitrary Periodic Waveform Generator	(*)	
RectifierFilter	Rectifier with Low Pass Filter	(*)	
RectifierHalf	Half Cycle Rectifier	(*)	
RectifierHold	Half Cycle Inverting Rectifier with Hold	(*)	
SquareRoot	Square Root	(*)	
SumBiquad	Sum/Difference Stage with Biquadratic Filter	(*)	
SumDiff	Half Cycle Sum/Difference Stage	(*)	
SumFilter	Sum/Difference Stage with Low Pass Filter	(*)	
SumIntegrator	Sum/Difference Integrator	(*)	
SumInv	Inverting Sum Stage	(*)	

▲ FIGURE 16–52

Selection and placement of the sine-wave oscillator CAM.

The frequency and peak amplitude of the oscillator can be programmed, and the oscillator CAM can be connected to an output as shown in Figure 16–53(a). Running the simulation produces the results shown in part (b).

Square-Wave Oscillator

A square-wave oscillator can be programmed using the sine-wave oscillator CAM and the comparator CAM, as illustrated in Figure 16–54. The frequency of the square wave can be changed by reprogramming the frequency of the sine-wave oscillator.

Variable Duty Cycle Pulse Oscillator

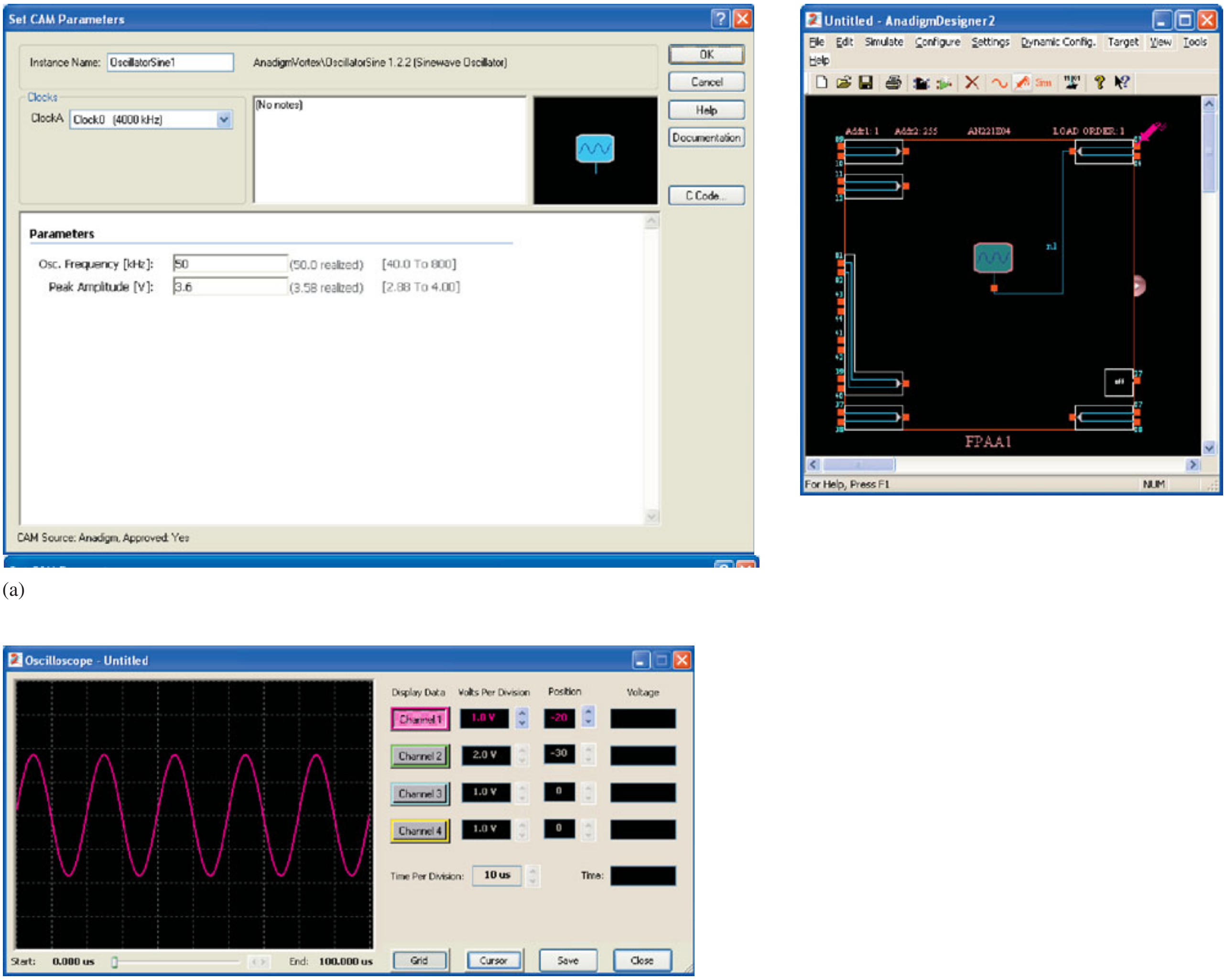
By adding a variable reference to the comparator CAM and by changing its value, the duty cycle as well as the frequency of the pulse waveform can be varied, as shown in Figure 16–55.

Triangular-Wave Oscillator

One way to program a triangular-wave oscillator is shown in Figure 16–56. A sine-wave oscillator is used to drive an inverting gain stage into nonlinear operation. This is followed by an integrator with a properly selected integration constant. A comparator could have been used instead of the over-driven gain stage except that Designer2 does not allow the output of a comparator to be connected to anything but a chip output.

Programming Exercises

1. How do you adjust the duty cycle of the variable duty cycle pulse oscillator?
2. To change the frequency of the triangular-wave oscillator, what parameters must be changed by programming?


Set CAM Parameters
OK
Cancel
Help
Documentation
C Code...
Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
n1
FPAA1
For Help, Press F1
NUM
Oscilloscope - Untitled
Grid
Cursor
Save
Close

Instance Name: OscillatorSine1
AnadigmVortex\OscillatorSine 1.2.2 (Sinewave Oscillator)

Clocks
ClockA Clock0 (4000 kHz)

(No notes)

Parameters
Osc. Frequency [kHz]: 50 (50.0 realized) [40.0 To 800]
Peak Amplitude [V]: 3.6 (3.58 realized) [2.88 To 4.00]

CAM Source: Anadigm, Approved: Yes

(a)

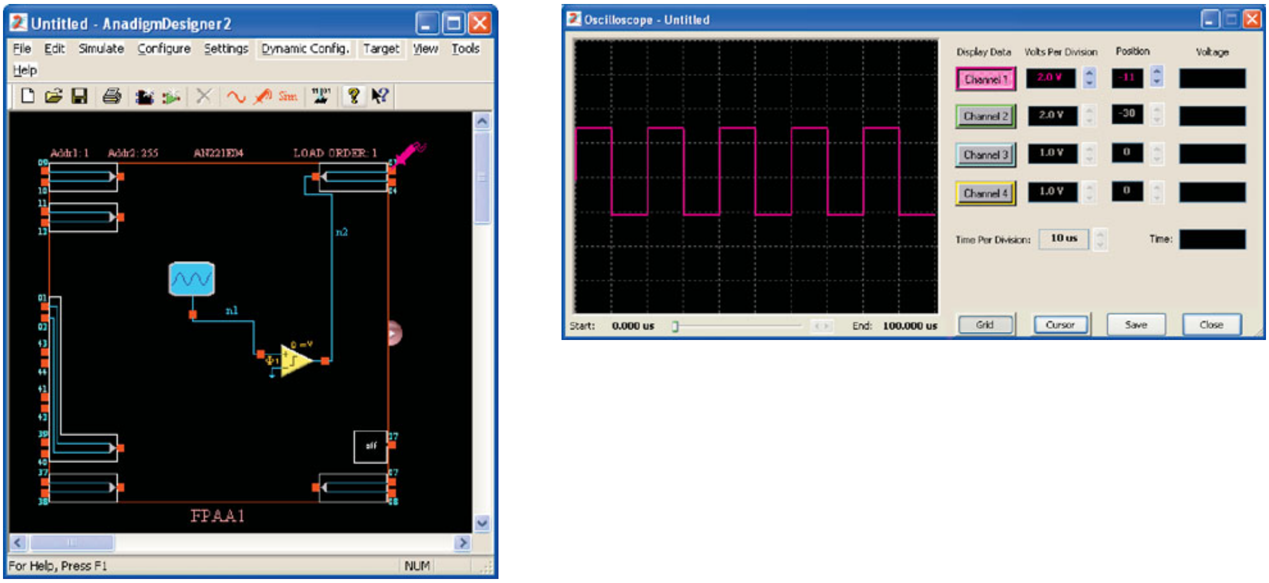
Display Data	Volts Per Division	Position	Voltage
Channel 1	1.0 V	-20	
Channel 2	2.0 V	-30	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

Time Per Division: 10 us
Time:
Start: 0.000 us
End: 100.000 us

(b)

▲ **FIGURE 16–53**

Programming a chip as a sine-wave oscillator.

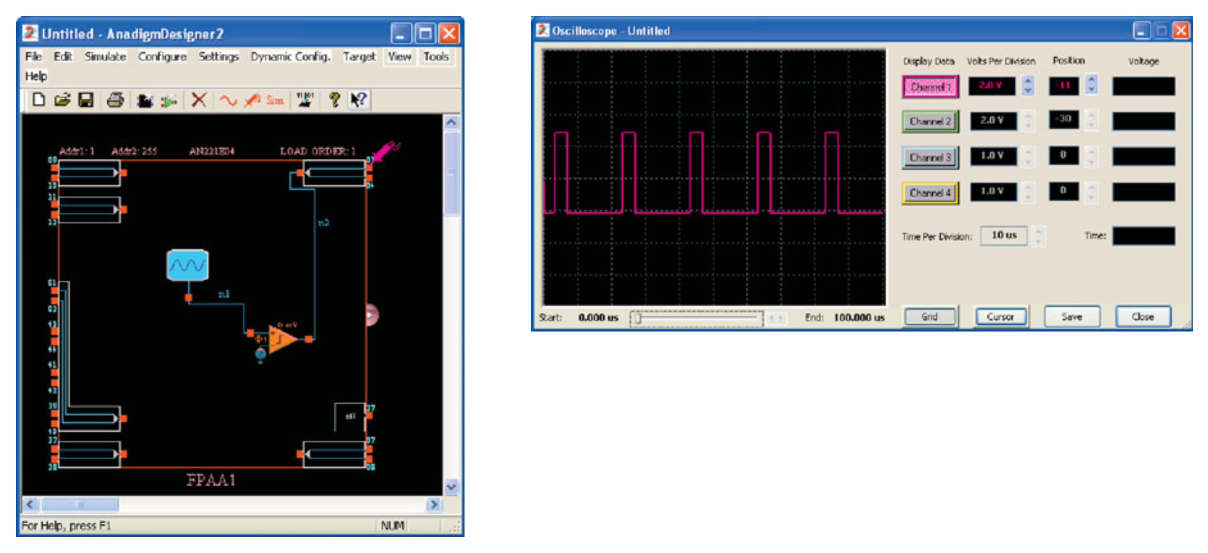

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
n1
n2
FPAA1
For Help, Press F1
NUM
Oscilloscope - Untitled
Grid
Cursor
Save
Close

Display Data	Volts Per Division	Position	Voltage
Channel 1	2.0 V	-11	
Channel 2	2.0 V	-30	
Channel 3	1.0 V	0	
Channel 4	1.0 V	0	

Time Per Division: 10 us
Time:
Start: 0.000 us
End: 100.000 us

▲ **FIGURE 16–54**

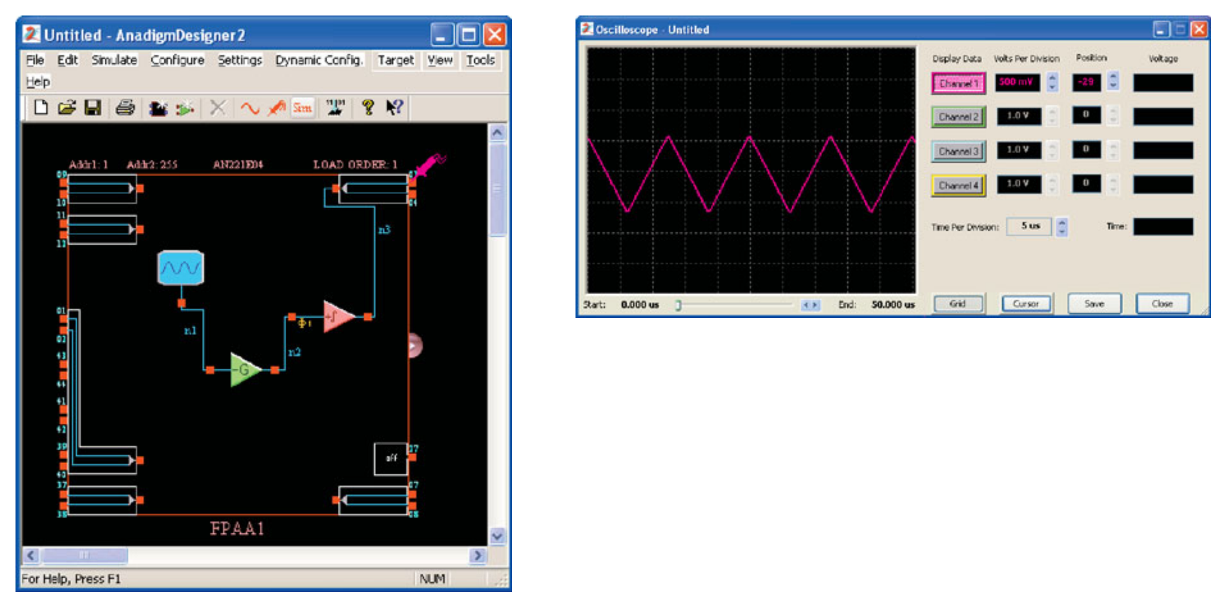
A square-wave oscillator.


Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
n1
n2
FPAA1
For Help, press F1
NUM
Oscilloscope - Untitled
Display Data
Volts Per Division
Position
Voltage
Channel 1
Channel 2
Channel 3
Channel 4
Time Per Division:
Time:
Grid
Cursor
Save
Close

Channel 1: 2.0 V, -11
Channel 2: 2.0 V, -30
Channel 3: 1.0 V, 0
Channel 4: 1.0 V, 0
Time Per Division: 10 us
Start: 0.000 us
End: 100.000 us

▲ **FIGURE 16–55**

A variable duty cycle pulse oscillator.

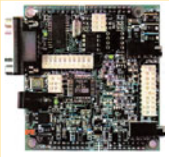

Untitled - AnadigmDesigner2
File Edit Simulate Configure Settings Dynamic Config. Target View Tools Help
Addr1: 1 Addr2: 255 AN221E04 LOAD ORDER: 1
n1
n2
n3
G
FPAA1
For Help, Press F1
NUM
Oscilloscope - Untitled
Display Data
Volts Per Division
Position
Voltage
Channel 1
Channel 2
Channel 3
Channel 4
Time Per Division:
Time:
Grid
Cursor
Save
Close

Channel 1: 500 mV, -28
Channel 2: 1.0 V, 0
Channel 3: 1.0 V, 0
Channel 4: 1.0 V, 0
Time Per Division: 5 us
Start: 0.000 us
End: 50.000 us

▲ **FIGURE 16–56**

A triangular-wave oscillator.

PAM Experiment



To program, download, and test a circuit using AnadigmDesigner2 software and the programmable analog module (PAM) board, go to Experiment 16–B in *Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling.

SUMMARY

Section 16–1

- Sinusoidal feedback oscillators operate with positive feedback.
- Relaxation oscillators use an *RC* timing circuit.

Section 16–2

- The two conditions for positive feedback are the phase shift around the feedback loop must be 0° and the voltage gain around the feedback loop must equal 1.
- For initial start-up, the voltage gain around the feedback loop must be greater than 1.

Section 16–3

- Sinusoidal *RC* oscillators include the Wien-bridge, phase-shift, and twin-T.

Section 16–4

- Sinusoidal *LC* oscillators include the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled.
- The feedback signal in a Colpitts oscillator is derived from a capacitive voltage divider in the *LC* circuit.
- The Clapp oscillator is a variation of the Colpitts with a capacitor added in series with the inductor.
- The feedback signal in a Hartley oscillator is derived from an inductive voltage divider in the *LC* circuit.
- The feedback signal in an Armstrong oscillator is derived by transformer coupling.
- Crystal oscillators are the most stable type of feedback oscillator.

Section 16–5

- A relaxation oscillator uses an *RC* timing circuit and a device that changes states to generate a periodic waveform.
- The frequency in a voltage-controlled oscillator (VCO) can be varied with a dc control voltage.

Section 16–6

- The 555 timer is an integrated circuit that can be used as an oscillator, in addition to many other applications.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Astable Characterized by having no stable states.

Oscillator An electronic circuit that produces a periodic waveform on its output with only the dc supply voltage as an input.

Positive feedback The return of a portion of the output signal to the input such that it reinforces and sustains the output.

Voltage-controlled oscillator (VCO) A type of relaxation oscillator whose frequency can be varied by a dc control voltage.

KEY FORMULAS

16–1	$\dfrac{V_{out}}{V_{in}} = \dfrac{1}{3}$	Wien-bridge positive feedback attenuation
16–2	$f_r = \dfrac{1}{2\pi RC}$	Wien-bridge resonant frequency
16–3	$B = \dfrac{1}{29}$	Phase-shift feedback attenuation
16–4	$f_r = \dfrac{1}{2\pi\sqrt{6}RC}$	Phase-shift oscillator frequency
16–5	$f_r \cong \dfrac{1}{2\pi\sqrt{LC_{\mathrm{T}}}}$	Colpitts, Clapp, and Hartley approximate resonant frequency
16–6	$A_v = \dfrac{C_1}{C_2}$	Colpitts amplifier gain

16–7	$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2 + 1}}$	Colpitts resonant frequency
16–8	$A_v > \frac{L_2}{L_1}$	Hartley self-starting gain
16–9	$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}}$	Armstrong resonant frequency
16–10	$f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right)$	Triangular-wave oscillator frequency
16–11	$f = \frac{\lvert V_{IN}\rvert}{R_iC}\left(\frac{1}{V_p - V_F}\right)$	Sawtooth VCO frequency
16–12	$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$	555 astable frequency
16–13	$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\%$	555 astable

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. Two categories of oscillators are feedback and relaxation.
2. A feedback oscillator uses only negative feedback.
3. Positive feedback is never used in an oscillator.
4. The net phase shift around the oscillator feedback loop must be zero.
5. The voltage gain around the closed feedback loop must be greater than 1 to sustain oscillations.
6. For start-up, the loop gain must be greater than 1.
7. A Wien-bridge oscillator uses an *RC* circuit in the positive feedback loop.
8. The phase-shift oscillator utilizes *RC* circuits.
9. The twin-T oscillator contains an *LC* feedback circuit.
10. Colpitts, Clapp, Hartley, and Armstrong are examples of *LC* oscillators.
11. The crystal oscillator is based on the photoelectric effect.
12. A relaxation oscillator uses no positive feedback.
13. Most relaxation oscillators produce sinusoidal outputs.
14. VCO stands for variable-capacitance oscillator.
15. The 555 timer can be used as an oscillator.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If R_1 and R_2 are increased to 18 kΩ in Figure 16–12, the frequency of oscillation will
   (a) increase **(b)** decrease **(c)** not change
2. If the feedback potentiometer R_f is adjusted to a higher value, the voltage gain in Figure 16–12 will
   (a) increase **(b)** decrease **(c)** not change
3. In Figure 16–14, if the R_f is decreased, the feedback attenuation will
   (a) increase **(b)** decrease **(c)** not change
4. If the capacitors in Figure 16–14 are increased to 0.01 μF, the frequency of oscillation will
   (a) increase **(b)** decrease **(c)** not change
5. In order to increase V_{UTP} in Figure 16–30, R_3 must
   (a) increase **(b)** decrease **(c)** not change
6. If the capacitor in Figure 16–30 opens, the frequency of oscillation will
   (a) increase **(b)** decrease **(c)** not change

7. If the value of R_1 in Figure 16–32 is decreased, the peak value of the sawtooth output will
   (a) increase **(b)** decrease **(c)** not change
8. If the diode in Figure 16–40 opens, the duty cycle will
   (a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 16–1

1. An oscillator differs from an amplifier because the oscillator
   (a) has more gain **(b)** requires no input signal
   (c) requires no dc supply **(d)** always has the same output

Section 16–2

2. One condition for oscillation is
   (a) a phase shift around the feedback loop of 180°
   (b) a gain around the feedback loop of one-third
   (c) a phase shift around the feedback loop of 0°
   (d) a gain around the feedback loop of less than 1
3. A second condition for oscillation is
   (a) no gain around the feedback loop
   (b) a gain of 1 around the feedback loop
   (c) the attenuation of the feedback circuit must be one-third
   (d) the feedback circuit must be capacitive
4. In a certain oscillator, $A_v = 50$. The attenuation of the feedback circuit must be
   (a) 1 **(b)** 0.01 **(c)** 10 **(d)** 0.02
5. For an oscillator to properly start, the gain around the feedback loop must initially be
   (a) 1 **(b)** less than 1 **(c)** greater than 1 **(d)** equal to B

Section 16–3

6. Wien-bridge oscillators are based on
   (a) positive feedback **(b)** negative feedback
   (c) the piezoelectric effect **(d)** high gain
7. In a Wien-bridge oscillator, if the resistances in the positive feedback circuit are decreased, the frequency
   (a) decreases **(b)** increases **(c)** remains the same
8. The Wien-bridge oscillator's positive feedback circuit is
   (a) an *RL* circuit **(b)** an *LC* circuit
   (c) a voltage divider **(d)** a lead-lag circuit
9. A phase-shift oscillator has
   (a) three *RC* circuits **(b)** three *LC* circuits
   (c) a T-type circuit **(d)** a π-type circuit

Section 16–4

10. Colpitts, Clapp, and Hartley are names that refer to
    (a) types of *RC* oscillators **(b)** inventors of the transistor
    (c) types of *LC* oscillators **(d)** types of filters
11. The main feature of a crystal oscillator is
    (a) economy **(b)** reliability **(c)** stability **(d)** high frequency

Section 16–5

12. An oscillator whose frequency is changed by a variable dc voltage is known as
    (a) a crystal oscillator **(b)** a VCO
    (c) an Armstrong oscillator **(d)** a piezoelectric device
13. The operation of a relaxation oscillator is based on
    (a) the charging and discharging of a capacitor **(b)** a highly selective resonant circuit
    (c) a very stable supply voltage **(d)** low power consumption

Section 16–6 **14.** Which one of the following is *not* an input or output of the 555 timer?

(a) Threshold **(b)** Control voltage **(c)** Clock
(d) Trigger **(e)** Discharge **(f)** Reset

PROBLEMS

Answers to odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 16–1 **The Oscillator**

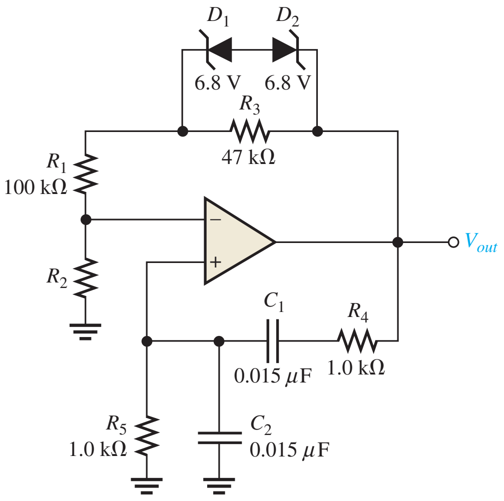
1. What type of input is required for an oscillator?
2. What are the basic components of an oscillator circuit?

Section 16–2 **Feedback Oscillators**

3. If the voltage gain of the amplifier portion of an oscillator is 75, what must be the attenuation of the feedback circuit to sustain the oscillation?
4. Generally describe the change required in the oscillator of Problem 3 in order for oscillation to begin when the power is initially turned on.

Section 16–3 **Oscillators with *RC* Feedback Circuits**

5. A certain lead-lag circuit has a resonant frequency of 3.5 kHz. What is the rms output voltage if an input signal with a frequency equal to f_r and with an rms value of 2.2 V is applied to the input?
6. Calculate the resonant frequency of a lead-lag circuit with the following values: $R_1 = R_2 = 6.2\ \text{k}\Omega$, and $C_1 = C_2 = 0.02\ \mu\text{F}$.
7. Determine the necessary value of R_2 in Figure 16–57 so that the circuit will oscillate. Neglect the forward resistance of the zener diodes. (*Hint:* The total gain of the circuit must be 3 when the zener diodes are conducting.)
8. Explain the purpose of R_3 in Figure 16–57.

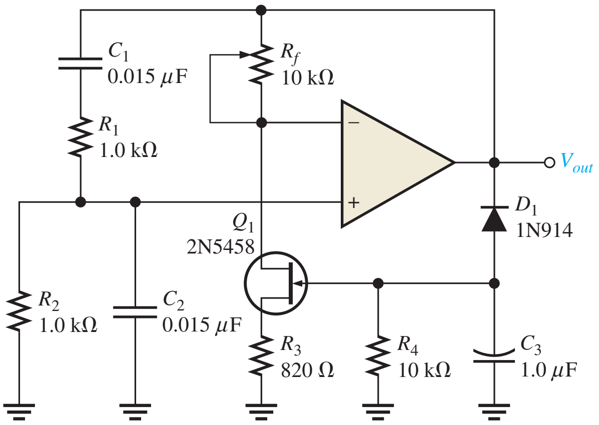


▲ FIGURE 16–57

9. For the Wien-bridge oscillator in Figure 16–58, calculate the setting for R_f, assuming the internal drain-source resistance, r'_{ds}, of the JFET is 350 Ω when oscillations are stable.
10. Find the frequency of oscillation for the Wien-bridge oscillator in Figure 16–58.

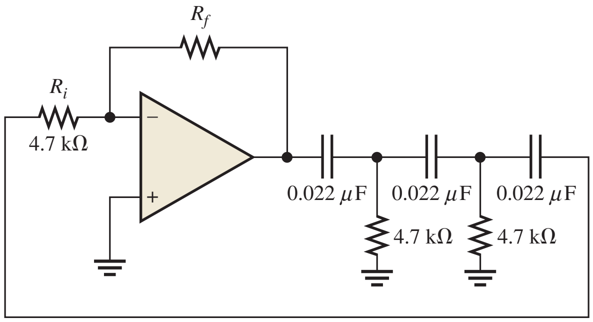
FIGURE 16–58

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F16-58).


C_1
0.015 μF
R_f
10 kΩ
R_1
1.0 kΩ
–
+
V_{out}
D_1
1N914
Q_1
2N5458
R_2
1.0 kΩ
C_2
0.015 μF
R_3
820 Ω
R_4
10 kΩ
C_3
1.0 μF

11. What value of R_f is required in Figure 16–59? What is f_r?

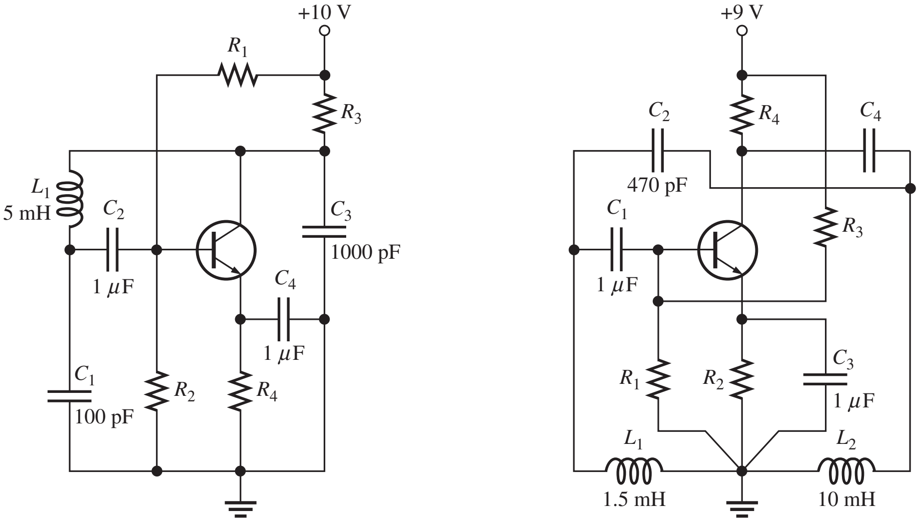
FIGURE 16–59


R_f
R_i
4.7 kΩ
–
+
0.022 μF
0.022 μF
0.022 μF
4.7 kΩ
4.7 kΩ

Section 16–4 Oscillators with LC Feedback Circuits

12. Calculate the frequency of oscillation for each circuit in Figure 16–60 and identify the type of oscillator. Assume $Q > 10$ in each case.

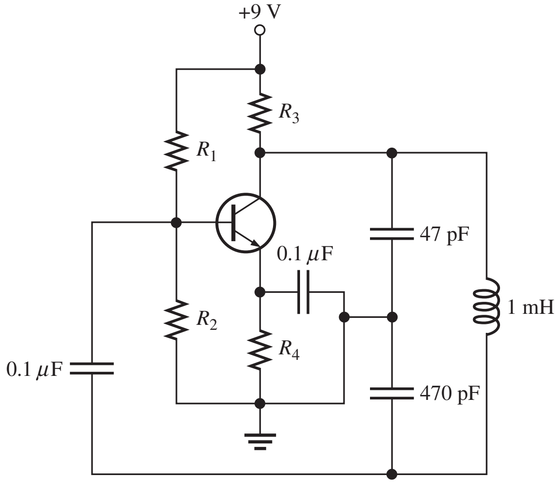
FIGURE 16–60


+10 V
R_1
R_3
L_1
5 mH
C_2
1 μF
C_3
1000 pF
C_4
1 μF
C_1
100 pF
R_2
R_4
+9 V
C_2
470 pF
R_4
C_4
C_1
1 μF
R_3
R_1
R_2
C_3
1 μF
L_1
1.5 mH
L_2
10 mH

(a) (b)

13. Determine what the gain of the amplifier stage must be in Figure 16–61 in order to have sustained oscillation.

▶ FIGURE 16–61


+9 V
R_3
R_1
47 pF
0.1 μF
1 mH
R_2
R_4
0.1 μF
470 pF

Section 16–5 Relaxation Oscillators

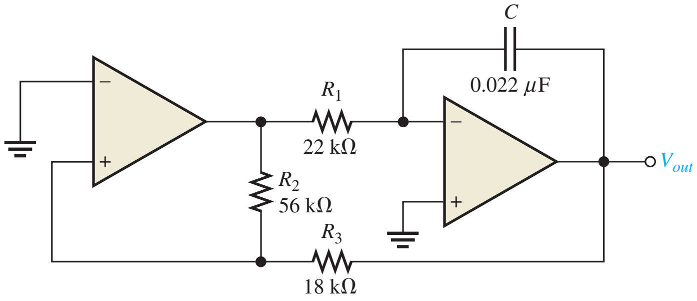
14. What type of signal does the circuit in Figure 16–62 produce? Determine the frequency of the output.

15. Show how to change the frequency of oscillation in Figure 16–62 to 10 kHz.

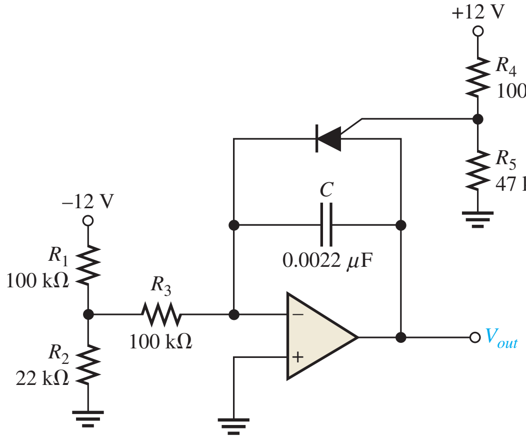
16. Determine the amplitude and frequency of the output voltage in Figure 16–63. Use 1 V as the forward PUT voltage.

17. Modify the sawtooth generator in Figure 16–63 so that its peak-to-peak output is 4 V.

▶ FIGURE 16–62


C
0.022 μF
−
+
R_1
22 kΩ
R_2
56 kΩ
R_3
18 kΩ
−
+
V_{out}

▶ FIGURE 16–63


+12 V
R_4
100 kΩ
R_5
47 kΩ
C
0.0022 μF
−12 V
R_1
100 kΩ
R_3
100 kΩ
R_2
22 kΩ
−
+
V_{out}

18. A certain sawtooth generator has the following parameter values: $V_{IN} = 3$ V, $R = 4.7$ kΩ, $C = 0.001$ μF. Determine its peak-to-peak output voltage if the period is 10 μs.

Section 16–6 The 555 Timer as an Oscillator

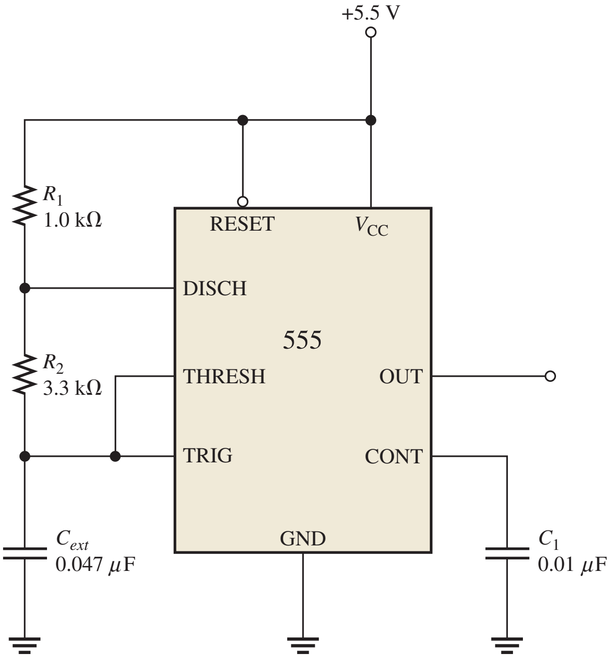
19. What are the two comparator reference voltages in a 555 timer when $V_{CC} = 10$ V?

20. Determine the frequency of oscillation for the 555 astable oscillator in Figure 16–64.

21. To what value must C_{ext} be changed in Figure 16–64 to achieve a frequency of 25 kHz?

22. In an astable 555 configuration, the external resistor $R_1 = 3.3\text{ k}\Omega$. What must R_2 equal to produce a duty cycle of 75 percent?

▶ FIGURE 16–64



MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

23. Open file TSP16-23 and determine the fault.

24. Open file TSP16-24 and determine the fault.

25. Open file TSP16-25 and determine the fault.

26. Open file TSP16-26 and determine the fault.

27. Open file TSP16-27 and determine the fault.

28. Open file TSP16-28 and determine the fault.

VOLTAGE REGULATORS

17

CHAPTER OUTLINE

17–1 Voltage Regulation
17–2 Basic Linear Series Regulators
17–3 Basic Linear Shunt Regulators
17–4 Basic Switching Regulators
17–5 Integrated Circuit Voltage Regulators
17–6 Integrated Circuit Voltage Regulator Configurations
Application Activity

CHAPTER OBJECTIVES

- Describe the concept of voltage regulation
- Describe and analyze the operation of linear series regulators
- Describe and analyze the operation of linear shunt regulators
- Discuss the principles of switching regulators
- Discuss integrated circuit voltage regulators
- Describe applications of IC voltage regulators

KEY TERMS

- Regulator
- Line regulation
- Load regulation
- Linear regulator
- Switching regulator
- Thermal overload

APPLICATION ACTIVITY PREVIEW

In the Application Activity, the dc power supply from Chapter 3 is redesigned to produce a regulated variable output voltage from 9 V to 30 V. The company that manufactures the power supply will introduce it as a new line that can be preset to a specified voltage at the factory or adjusted by the customer to any desired value in the output voltage range.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

A voltage regulator provides a constant dc output voltage that is essentially independent of the input voltage, output load current, and temperature. The voltage regulator is one part of a power supply. Its input voltage comes from the filtered output of a rectifier derived from an ac voltage or from a battery in the case of portable systems.

Most voltage regulators fall into two broad categories: linear regulators and switching regulators. In the linear regulator category, two general types are the series regulator and the shunt regulator. These are normally available for either positive or negative output voltages. A dual regulator provides both positive and negative outputs. In the switching regulator category, three general configurations are step-down, step-up, and inverting.

Many types of integrated circuit (IC) regulators are available. The most popular types of linear regulator are the three-terminal fixed voltage regulator and the three-terminal adjustable voltage regulator. Switching regulators are also widely used. In this chapter, specific IC devices are introduced as representative of the wide range of available devices.

17–1 VOLTAGE REGULATION

Two basic categories of voltage regulation are line regulation and load regulation. The purpose of line regulation is to maintain a nearly constant output voltage when the input voltage varies. The purpose of load regulation is to maintain a nearly constant output voltage when the load varies.

After completing this section, you should be able to

- **Describe the concept of voltage regulation**
- Explain line regulation
  - Calculate line regulation
- Explain load regulation
  - Calculate load regulation

Line Regulation

When the ac input (line) voltage of a power supply changes, an electronic circuit called a **regulator** maintains a nearly constant output voltage, as illustrated in Figure 17–1. **Line regulation** can be defined as the percentage change in the output voltage for a given change in the input voltage. When taken over a range of input voltage values, line regulation is expressed as a percentage by the following formula:

Equation 17–1

$$\textbf{Line regulation} = \left(\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}\right)100\%$$

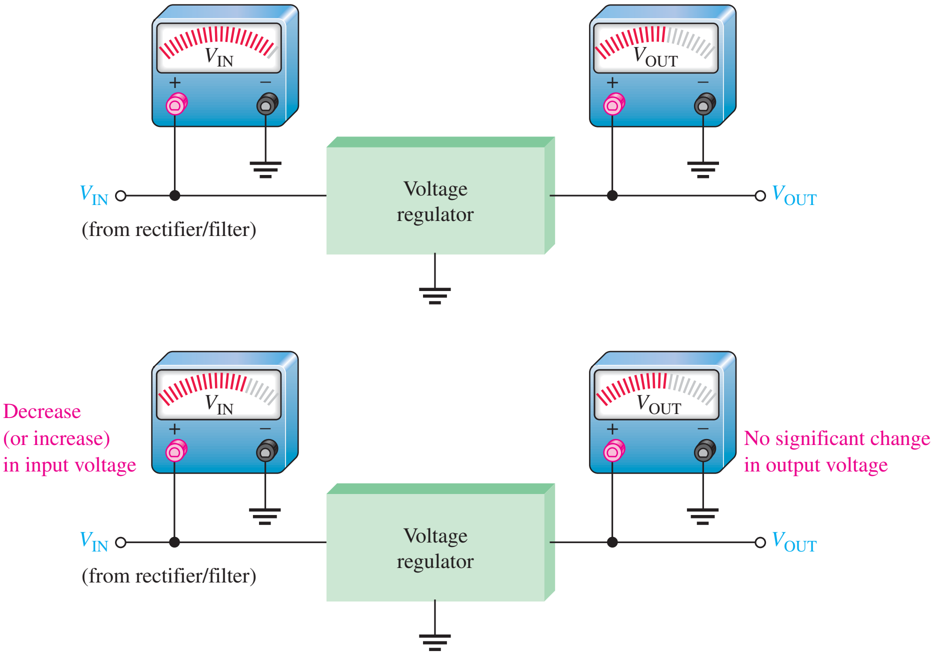
Line regulation can also be expressed in units of %/V. For example, a line regulation of 0.05%/V means that the output voltage changes 0.05 percent when the input voltage increases or decreases by one volt. Line regulation can be calculated using the following formula (Δ means "a change in"):

Equation 17–2

$$\textbf{Line regulation} = \frac{(\Delta V_{\text{OUT}}/V_{\text{OUT}})100\%}{\Delta V_{\text{IN}}}$$

FIGURE 17–1

Line regulation. A change in input (line) voltage does not significantly affect the output voltage of a regulator (within certain limits).


V_{IN}
V_{OUT}
+
−
V_{IN}
(from rectifier/filter)
Voltage regulator
V_{OUT}
Decrease (or increase) in input voltage
No significant change in output voltage
V_{IN}
(from rectifier/filter)
Voltage regulator
V_{OUT}

EXAMPLE 17–1 When the ac input voltage of a certain power supply changes, the input to the voltage regulator decreases by 5 V as a result, and the output of the regulator decreases by 0.25 V. The nominal output is 15 V. Determine the line regulation in %/V.

Solution The line regulation as a percentage change per volt is

$$\text{line regulation} = \frac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}} = \frac{(0.25\text{ V}/15\text{ V})100\%}{5\text{ V}} = \mathbf{0.333\%/V}$$

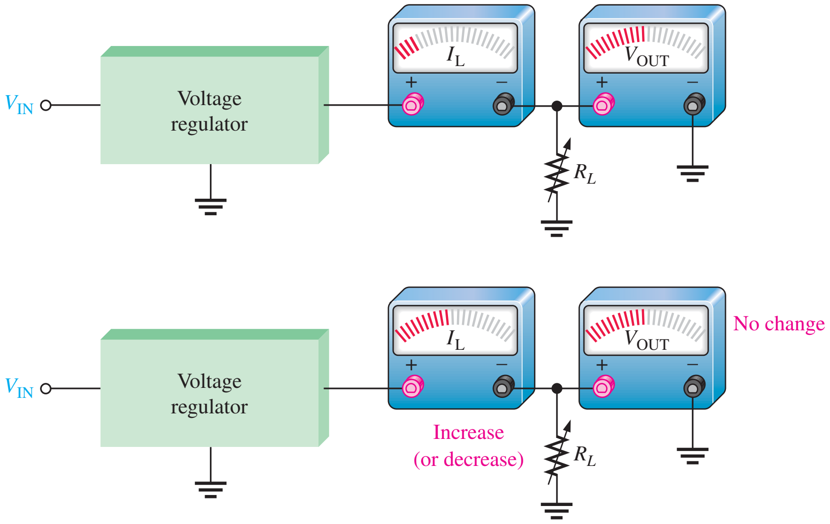
Related Problem[*] The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.42 V. The nominal output is 20 V. Determine the regulation in %/V.

---

[*] **Answers can be found at www.pearsonhighered.com/floyd.**

Load Regulation

When the amount of current through a load changes due to a varying load resistance, the voltage regulator must maintain a nearly constant output voltage across the load, as illustrated in Figure 17–2.



▲ FIGURE 17–2

Load regulation. A change in load current has practically no effect on the output voltage of a regulator (within certain limits).

Load regulation can be defined as the percentage change in output voltage for a given change in load current. One way to express load regulation is as a percentage change in output voltage from no-load (NL) to full-load (FL).

$$\textbf{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\% \qquad \text{Equation 17–3}$$

Alternately, the load regulation can be expressed as a percentage change in output voltage for each mA change in load current. For example, a load regulation of 0.01%/mA means that the output voltage changes 0.01 percent when the load current increases or decreases 1 mA.

EXAMPLE 17–2 A certain voltage regulator has a 12 V output when there is no load ($I_L = 0$). When there is a full-load current of 10 mA, the output voltage is 11.9 V. Express the voltage regulation as a percentage change from no-load to full-load and also as a percentage change for each mA change in load current.

Solution The no-load output voltage is

$$V_{NL} = 12\text{V}$$

The full-load output voltage is

$$V_{FL} = 11.9\text{ V}$$

The load regulation as a percentage change from no-load to full-load is

$$\text{load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\% = \left(\frac{12\text{ V} - 11.9\text{ V}}{11.9\text{ V}}\right)100\% = \mathbf{0.840\%}$$

The load regulation can also be expressed as a percentage change per milliamp as

$$\text{load regulation} = \frac{0.840\%}{10\text{ mA}} = \mathbf{0.084\%/mA}$$

where the change in load current from no-load to full-load is 10 mA.

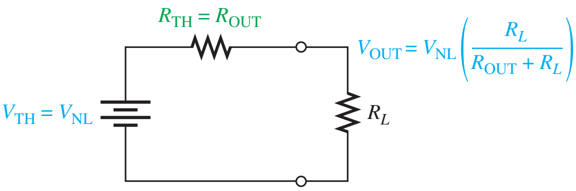
Related Problem A regulator has a no-load output voltage of 18 V and a full-load output of 17.8 V at a load current of 50 mA. Determine the voltage regulation as a percentage change from no-load to full-load and also as a percentage change for each mA change in load current.

Sometimes power supply manufacturers specify the equivalent output resistance of a power supply (R_{OUT}) instead of its load regulation. Recall that an equivalent Thevenin circuit can be drawn for any two-terminal linear circuit. Figure 17–3 shows the equivalent Thevenin circuit for a power supply with a load resistor. The Thevenin voltage is the voltage from the supply with no load (V_{NL}), and the Thevenin resistance is the specified output resistance, R_{OUT}. Ideally, R_{OUT} is zero, corresponding to 0% load regulation, but in practical power supplies R_{OUT} is a small value. With the load resistor in place, the output voltage is found by applying the voltage-divider rule:

$$V_{OUT} = V_{NL}\left(\frac{R_L}{R_{OUT} + R_L}\right)$$

▶ FIGURE 17–3

Thevenin equivalent circuit for a power supply with a load resistor.



If we let R_{FL} equal the smallest-rated load resistance (largest-rated current), then the full-load output voltage (V_{FL}) is

$$V_{FL} = V_{NL}\left(\frac{R_{FL}}{R_{OUT} + R_{FL}}\right)$$

By rearranging and substituting into Equation 17–3,

$$V_{NL} = V_{FL}\left(\frac{R_{OUT} + R_{FL}}{R_{FL}}\right)$$

$$\text{Load regulation} = \frac{V_{FL}\left(\frac{R_{OUT} + R_{FL}}{R_{FL}}\right) - V_{FL}}{V_{FL}} \times 100\%$$

$$= \left(\frac{R_{OUT} + R_{FL}}{R_{FL}} - 1\right)100\%$$

$$\textbf{Load regulation} = \left(\frac{R_{OUT}}{R_{FL}}\right)100\% \qquad \text{Equation 17–4}$$

Equation 17–4 is a useful way of finding the percent load regulation when the output resistance and minimum load resistance are specified.

SECTION 17–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. Define *line regulation.*
2. Define *load regulation.*
3. The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.042 V. The nominal output is 20 V. Determine the line regulation in both % and in %/V.
4. If a 5.0 V power supply has an output resistance of 80 mΩ and a specified maximum output current of 1.0 A, what is the load regulation? Give the result as a % and as a %/mA.

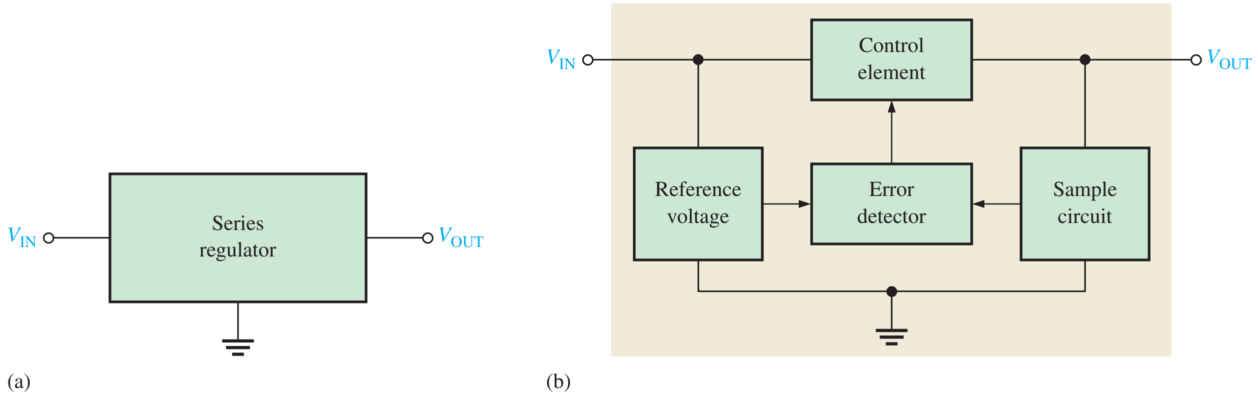
17–2 BASIC LINEAR SERIES REGULATORS

The fundamental classes of voltage regulators are linear regulators and switching regulators. Both of these are available in integrated circuit form. Two basic types of linear regulator are the series regulator and the shunt regulator.

After completing this section, you should be able to

- **Describe and analyze the operation of linear series regulators**
- Explain regulating action
  - Determine the closed-loop gain
  - Determine the output voltage
- Discuss overload protection
  - Explain constant-current limiting
  - Determine the maximum load current
- Discuss fold-back current limiting

A simple representation of a series type of **linear regulator** is shown in Figure 17–4(a), and the basic components are shown in the block diagram in Figure 17–4(b). The control element is a pass transistor in series with the load between the input and output. The output sample circuit senses a change in the output voltage. The error detector compares the sample voltage with a reference voltage and causes the control element to



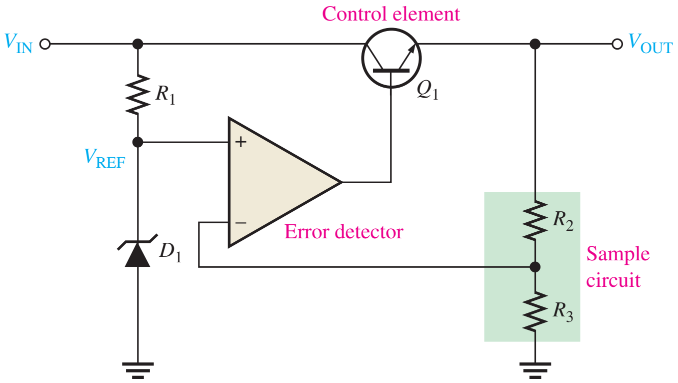
▲ **FIGURE 17–4**

Simple series voltage regulator and block diagram.

compensate in order to maintain a constant output voltage. A basic op-amp series regulator is shown in Figure 17–5.

▶ **FIGURE 17–5**

Basic op-amp series regulator.

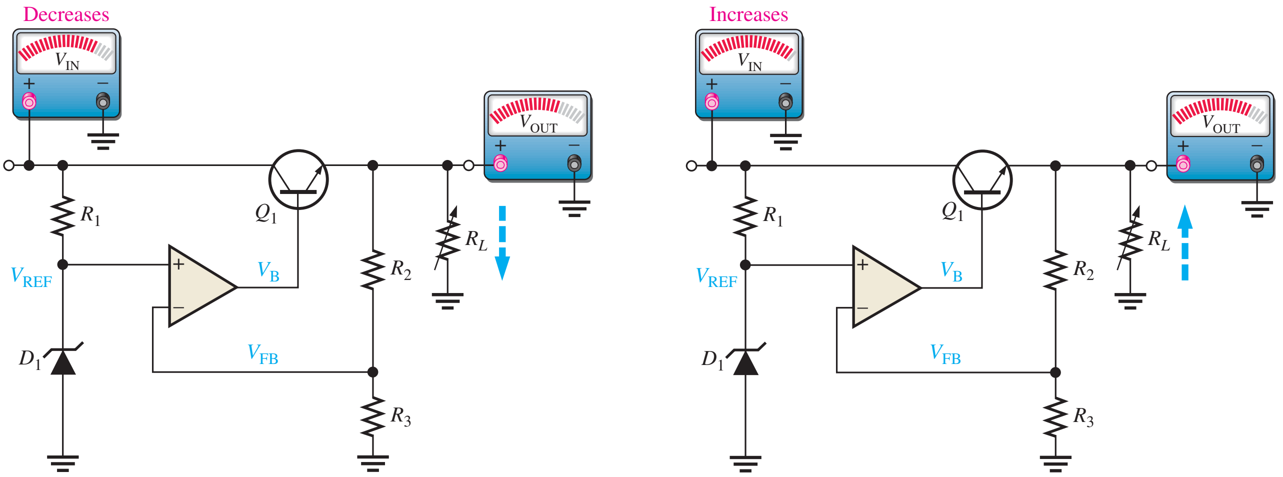


Regulating Action

The operation of the series regulator is illustrated in Figure 17–6 and is as follows. The resistive voltage divider formed by R_2 and R_3 senses any change in the output voltage. When the output tries to decrease, as indicated in Figure 17–6(a), because of a decrease in V_{IN} or because of an increase in I_L caused by a decrease in R_L, a proportional voltage decrease is applied to the op-amp's inverting input by the voltage divider. Since the zener diode (D_1) holds the other op-amp input at a nearly constant reference voltage, V_{REF}, a small difference voltage (error voltage) is developed across the op-amp's inputs. This difference voltage is amplified, and the op-amp's output voltage, V_B, increases. This increase is applied to the base of Q_1, causing the emitter voltage V_{OUT} to increase until the voltage to the inverting input again equals the reference (zener) voltage. This action offsets the attempted decrease in output voltage, thus keeping it nearly constant. The power transistor, Q_1, is usually used with a heat sink because it must handle all of the load current.

The opposite action occurs when the output tries to increase, as indicated in Figure 17–6(b). The op-amp in the series regulator is actually connected as a noninverting amplifier where the reference voltage V_{REF} is the input at the noninverting terminal, and the R_2/R_3 voltage divider forms the negative feedback circuit. The closed-loop voltage gain is

$$A_{cl} = 1 + \frac{R_2}{R_3}$$



(a) When V_{IN} or R_L decreases, V_{OUT} attempts to decrease. The feedback voltage, V_{FB}, also attempts to decrease, and as a result, the op-amp's output voltage V_B attempts to increase, thus compensating for the attempted decrease in V_{OUT} by increasing the Q_1 emitter voltage. Changes in V_{OUT} are exaggerated for illustration.

When V_{IN} (or R_L) stabilizes at its new lower value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.

(b) When V_{IN} or R_L increases, V_{OUT} attempts to increase. The feedback voltage, V_{FB}, also attempts to increase, and as a result, V_B, applied to the base of the control transistor, attempts to decrease, thus compensating for the attempted increase in V_{OUT} by decreasing the Q_1 emitter voltage.

When V_{IN} (or R_L) stabilizes at its new higher value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.

▲ FIGURE 17–6

Illustration of series regulator action that keeps V_{OUT} constant when V_{IN} or R_L changes.

Therefore, the regulated output voltage of the series regulator (neglecting the base-emitter voltage of Q_1) is

$$V_{OUT} \cong \left(1 + \frac{R_2}{R_3}\right)V_{REF}$$

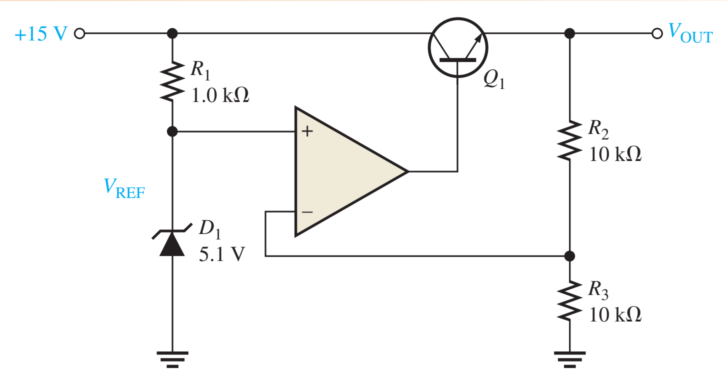
Equation 17–5

From this analysis, you can see that the output voltage is determined by the zener voltage and the resistors R_2 and R_3. It is relatively independent of the input voltage, and therefore, regulation is achieved (as long as the input voltage and load current are within specified limits).

EXAMPLE 17–3

Determine the output voltage for the regulator in Figure 17–7.

▶ FIGURE 17–7



Solution $V_{REF} = 5.1$ V, the zener voltage. The regulated output voltage is therefore

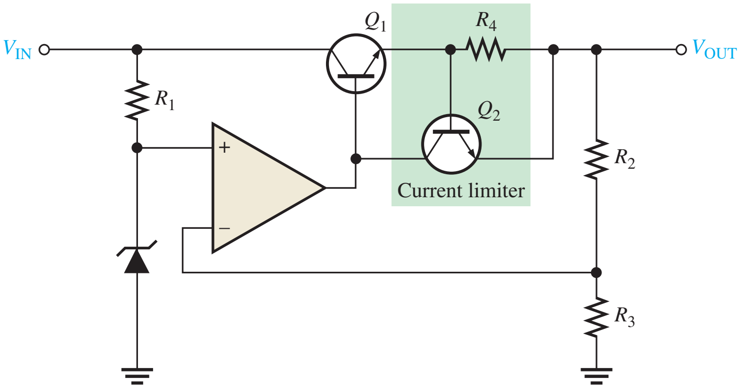
$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right)V_{REF} = \left(1 + \frac{10\text{ k}\Omega}{10\text{ k}\Omega}\right)5.1\text{ V} = (2)5.1\text{ V} = \mathbf{10.2\ V}$$

Related Problem The following changes are made in the circuit in Figure 17–7: A 3.3 V zener replaces the 5.1 V zener, $R_1 = 1.8\text{ k}\Omega$, $R_2 = 22\text{ k}\Omega$, and $R_3 = 18\text{ k}\Omega$. What is the output voltage?

Open the Multisim file E17-03 in the Examples folder on the companion website. Measure the output voltage with 15 V dc applied to the input. Compare to the calculated value.

Short-Circuit or Overload Protection

If an excessive amount of load current is drawn, the series-pass transistor can be quickly damaged or destroyed. Most regulators use some type of excess current protection in the form of a current-limiting mechanism. Figure 17–8 shows one method of current limiting to prevent overloads called *constant-current limiting.* The current-limiting circuit consists of transistor Q_2 and resistor R_4.



▲ FIGURE 17–8

Series regulator with constant-current limiting.

The load current through R_4 produces a voltage from base to emitter of Q_2. When I_L reaches a predetermined maximum value, the voltage drop across R_4 is sufficient to forward-bias the base-emitter junction of Q_2, thus causing it to conduct. Enough op-amp output current is diverted through Q_2 to reduce the Q_1 base current, so that I_L is limited to its maximum value, $I_{L(max)}$. Since the base-to-emitter voltage of Q_2 cannot exceed approximately 0.7 V, the voltage across R_4 is held to this value, and the load current is limited to

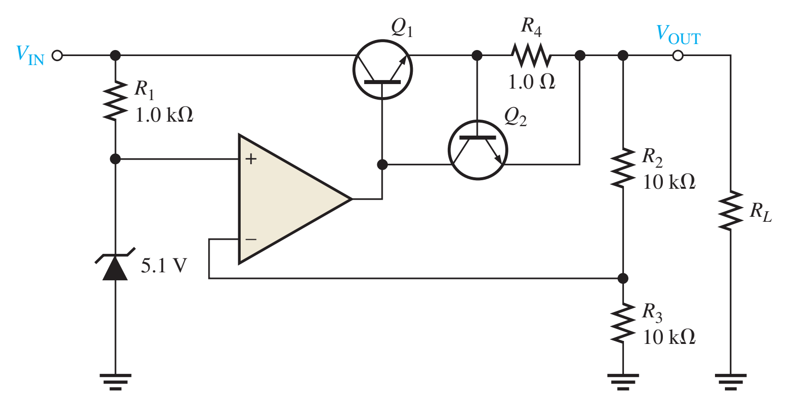
Equation 17–6

$$\mathbf{I_{L(max)} = \frac{0.7\ V}{R_4}}$$

EXAMPLE 17–4

Determine the maximum current that the regulator in Figure 17–9 can provide to a load.

▶ FIGURE 17–9



Solution

$$I_{L(max)} = \frac{0.7\text{ V}}{R_4} = \frac{0.7\text{ V}}{1.0\ \Omega} = \mathbf{0.7\ A}$$

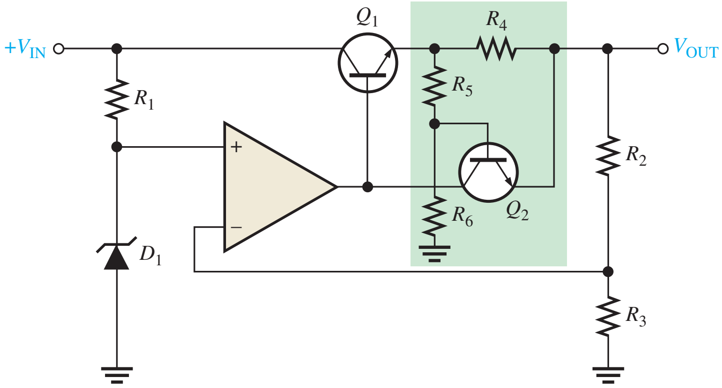
Related Problem If the output of the regulator in Figure 17–9 is shorted, what is the current?

Regulator with Fold-Back Current Limiting

In the previous current-limiting technique, the current is restricted to a maximum constant value. **Fold-back current limiting** is a method used particularly in high-current regulators whereby the output current under overload conditions drops to a value well below the peak load current capability to prevent excessive power dissipation.

The basic concept of fold-back current limiting is as follows, with reference to Figure 17–10. The circuit in the green-shaded area is similar to the constant current-limiting arrangement in Figure 17–8, with the exception of resistors R_5 and R_6. The voltage drop developed across R_4 by the load current must not only overcome the base-emitter voltage required to turn on Q_2, but it must also overcome the voltage across R_5. That is, the voltage across R_4 must be

$$V_{R4} = V_{R5} + V_{BE}$$



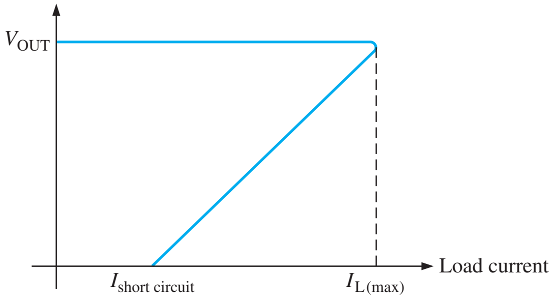
▲ FIGURE 17–10

Series regulator with fold-back current limiting.

In an overload or short-circuit condition, the load current increases to a value, $I_{L(max)}$, that is sufficient to cause Q_2 to conduct. At this point the current can increase no further. The decrease in output voltage results in a proportional decrease in the voltage across R_5; thus, less current through R_4 is required to maintain the forward-biased condition of Q_1. So, as V_{OUT} decreases, I_L decreases, as shown in the graph of Figure 17–11.

▶ **FIGURE 17–11**

Fold-back current limiting (output voltage versus load current).



The advantage of this technique is that the regulator is allowed to operate with peak load current up to $I_{L(max)}$; but when the output becomes shorted, the current drops to a lower value to prevent overheating of the device.

SECTION 17–2 CHECKUP

1. What are the basic components in a series regulator?
2. A certain series regulator has an output voltage of 8 V. If the op-amp's closed loop gain is 4, what is the value of the reference voltage?

17–3 BASIC LINEAR SHUNT REGULATORS

The second basic type of linear voltage regulator is the shunt regulator. As you have learned, the control element in the series regulator is the series-pass transistor. In the shunt regulator, the control element is a transistor in parallel (shunt) with the load.

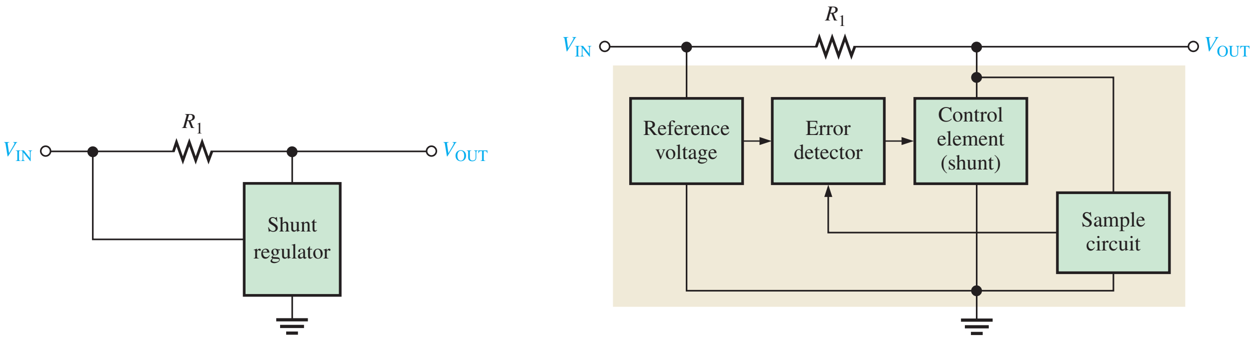
After completing this section, you should be able to

- **Describe and analyze the operation of linear shunt regulators**
  - Determine the maximum load current
  - Compare series and shunt regulators

A simple representation of a shunt type of linear regulator is shown in Figure 17–12(a), and the basic components are shown in the block diagram in part (b).

In the basic shunt regulator, the control element is a transistor, Q_1, in parallel with the load, as shown in Figure 17–13. A resistor, R_1, is in series with the load. The operation of the circuit is similar to that of the series regulator, except that regulation is achieved by controlling the current through the parallel transistor Q_1.

When the output voltage tries to decrease due to a change in input voltage or load current caused by a change in load resistance, as shown in Figure 17–14(a), the attempted decrease is sensed by R_3 and R_4 and applied to the op-amp's noninverting input. The

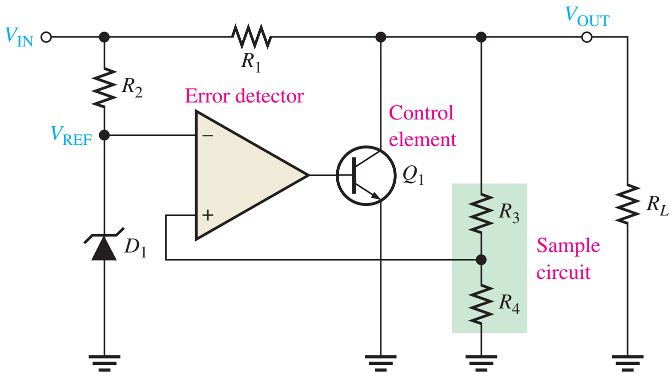


R_1
V_{IN}
V_{OUT}
Shunt regulator
R_1
V_{IN}
V_{OUT}
Reference voltage
Error detector
Control element (shunt)
Sample circuit

(a) (b)

▲ FIGURE 17–12

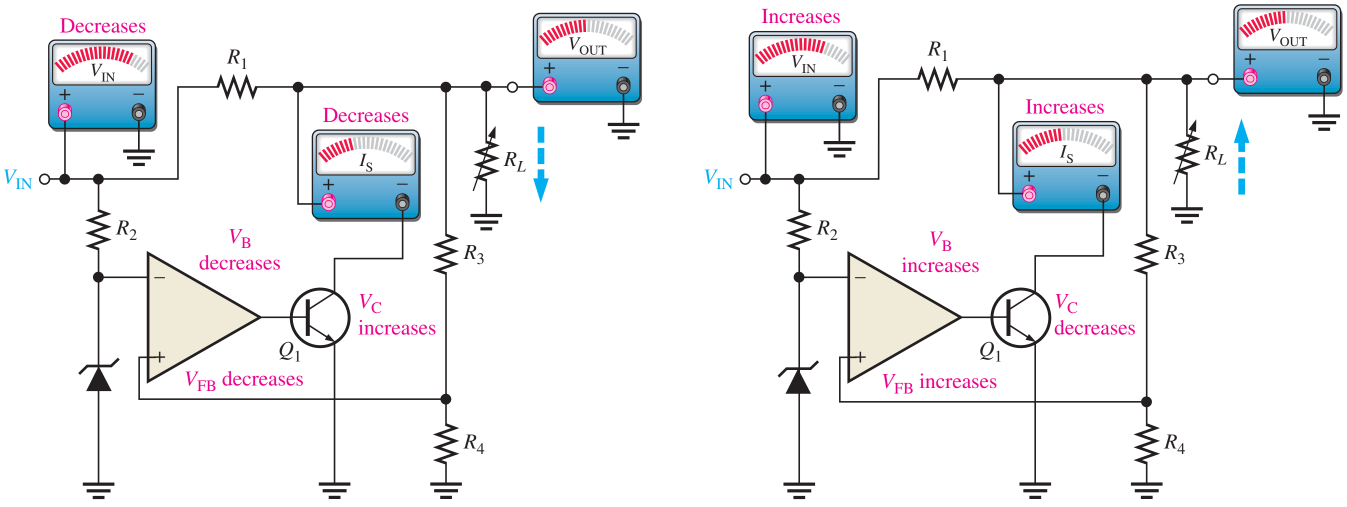
Simple shunt regulator and block diagram.



V_{OUT}
V_{IN}
R_1
R_2
Error detector
Control element
V_{REF}
Q_1
R_3
R_L
D_1
Sample circuit
R_4

▲ FIGURE 17–13

Basic op-amp shunt regulator with load resistor.



Decreases
V_{IN}
R_1
V_{OUT}
Decreases
I_S
R_L
V_{IN}
R_2
V_B decreases
R_3
V_C increases
Q_1
V_{FB} decreases
R_4
Increases
V_{IN}
R_1
V_{OUT}
Increases
I_S
R_L
V_{IN}
R_2
V_B increases
R_3
V_C decreases
Q_1
V_{FB} increases
R_4

(a) Response to a decrease in V_{IN} or R_L

(b) Response to an increase in V_{IN} or R_L

▲ FIGURE 17–14

Sequence of responses when V_{OUT} tries to decrease as a result of a decrease in R_L or V_{IN} (opposite responses for an attempted increase).

resulting difference voltage reduces the op-amp's output (V_B), driving Q_1 less, thus reducing its collector current (shunt current) and increasing the collector voltage. Thus, the original decrease in voltage is compensated for by this increase, keeping the output nearly constant.

The opposite action occurs when the output tries to increase, as indicated in Figure 17–14(b). With I_L and V_{OUT} constant, a change in the input voltage produces a change in shunt current (I_S) as follows (Δ means "a change in"):

$$\Delta I_S = \frac{\Delta V_{IN}}{R_1}$$

With a constant V_{IN} and V_{OUT}, a change in load current causes an opposite change in shunt current. If I_L increases, I_S decreases, and vice versa.

$$\Delta I_S = -\Delta I_L$$

The shunt regulator is less efficient than the series type but offers inherent short-circuit protection. If the output is shorted ($V_{OUT} = 0$), the load current is limited by the series resistor R_1 to a maximum value as follows ($I_S = 0$).

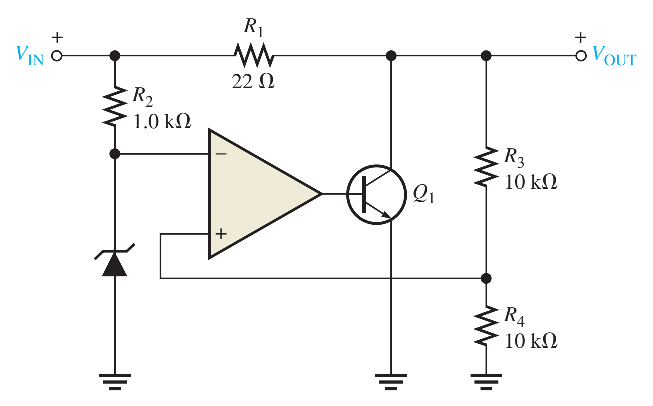
Equation 17–7

$$\boldsymbol{I_{L(max)} = \frac{V_{IN}}{R_1}}$$

EXAMPLE 17–5

In Figure 17–15, what power rating must R_1 have if the maximum input voltage is 12.5 V?

FIGURE 17–15



Solution The worst-case power dissipation in R_1 occurs when the output is short-circuited and $V_{OUT} = 0$. When $V_{IN} = 12.5$ V, the voltage dropped across R_1 is

$$V_{R1} = V_{IN} - V_{OUT} = 12.5\text{ V}$$

The power dissipation in R_1 is

$$P_{R1} = \frac{V_{R1}^2}{R_1} = \frac{(12.5\text{ V})^2}{22\ \Omega} = \mathbf{7.10\ W}$$

Therefore, a resistor with a rating of at least 10 W should be used. This illustrates that a major disadvantage of this type of regulator is the power wasted in R_1, which makes the regulator inefficient.

Related Problem In Figure 17–15, R_1 is changed to 33 Ω. What must be the power rating of R_1 if the maximum input voltage is 24 V?

Open the Multisim file E17-05 in the Examples folder on the companion website. Measure the output voltage with 15 V applied to the input.

SECTION 17–3 CHECKUP

1. How does the control element in a shunt regulator differ from that in a series regulator?
2. What is one advantage of a shunt regulator over a series type? What is a disadvantage?

17–4 BASIC SWITCHING REGULATORS

The two types of linear regulators, series and shunt, have control elements (transistors) that are conducting all the time, with the amount of conduction varied as demanded by changes in the output voltage or current. The switching regulator is different because the control element operates as a switch.

After completing this section, you should be able to

- **Discuss the principles of switching regulators**
- Describe the step-down configuration of a switching regulator
    - Determine the output voltage of the step-down configuration
- Describe the step-up configuration of a switching regulator
- Describe the voltage-inverter configuration

A much greater efficiency can be realized with a switching type of voltage regulator than with the linear types because the transistor switches on and off and dissipates power only when it is on. In a linear regulator, the transistor is always on and constantly dissipates power because the transistor looks like a variable resistor. This causes heat to be generated and wastes power. In a **switching regulator**, the transistor operates only on the ends of the load line except during the very short switching time. As a result, efficiencies can be greater than 90%. Switching regulators are particularly useful where efficiency is important, such as for computers. An efficient converter avoids excessive heat, which can destroy electronic components.

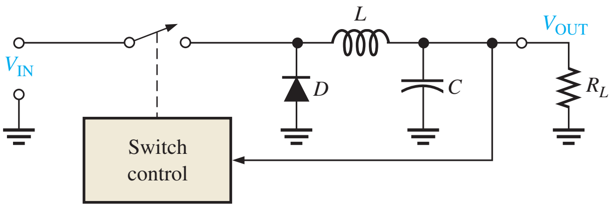
Switching regulators are designed for various power levels. They range in power levels from less than one watt for some battery-operated portable equipment to hundreds and thousands of watts in major applications. The requirements for the application determine the particular design, but all switching regulators require feedback to control the on-off time for the switch. Three basic configurations of switching regulators are step-down, step-up, and inverting. In some cases, such as a laptop computer, all three types may be employed for various parts of the system; for example, the display typically will use an inverting type, the microprocessor would use a step-down type, and the disk drive may use a step-up type.

Step-Down Configuration

In the step-down configuration (also called a *buck converter*), the output voltage is always less than the input voltage. The basic idea for a step-down type is shown in the simplified circuit shown in Figure 17–16. The basic control element is a high-speed switch, which

▶ FIGURE 17–16

Simplified step-down regulator.

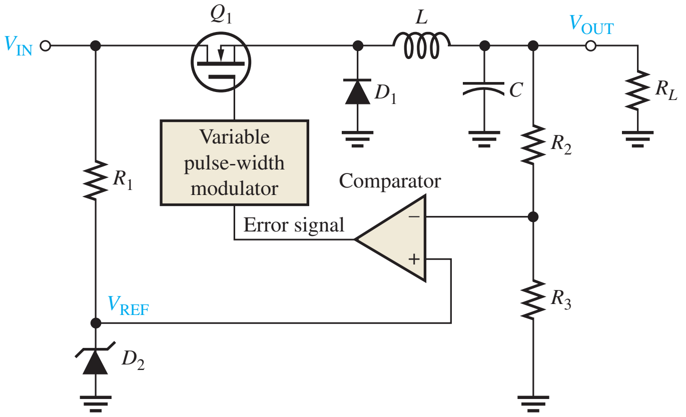


opens and closes rapidly from a control circuit that senses the output, and it adjusts the on-time and the off-time to keep the desired output. When the switch is closed, the diode is *off* and the magnetic field of the inductor builds, storing energy. When the switch opens, the magnetic field collapses, keeping nearly constant current in the load. A path for the load current is provided through the forward-biased diode (as long as the load resistance is not too large). The capacitor smoothes the dc to a nearly constant level.

Let's look at the circuit, including the switching device, in more detail. The switch turns on and off the input voltage at a rapid rate and with a duty cycle that is based on the regulator's load requirement. Figure 17–17 shows a basic step-down switching regulator using a D-MOSFET switching transistor. MOSFET transistors can switch faster than BJTs and have been improved in recent years, so they have become the preferred type of switching device, provided that the off-state voltage is not too high. As in most electronic devices, there are trade-offs for designers in choosing a switching device. Differences in break-down voltage, on-state resistance, and switching time must all be considered for a given design. In addition to transistor switches, you may see thyristors used occasionally.

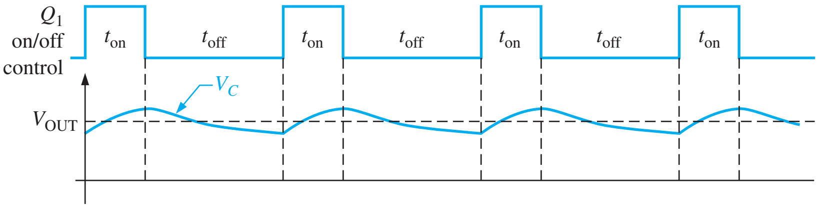
▶ FIGURE 17–17

A basic step-down switching regulator.

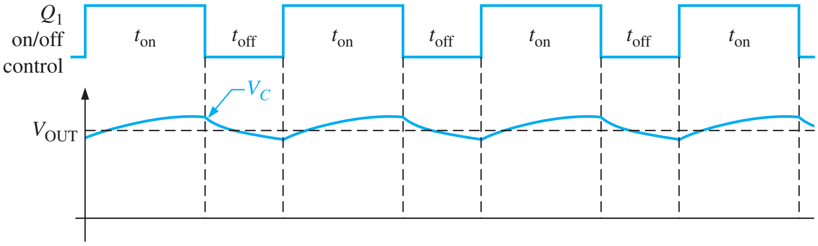


The pulsed current from the transistor switch is smoothed by an *LC* filter. The inductor tries to keep current constant, and the capacitor tends to keep voltage constant. Ideally, these components do not dissipate power, but in practice some loss is encountered due to various factors. To avoid requiring large (and expensive) inductors and capacitors, the switching frequency is selected to be much higher than the utility frequency; 20 kHz is common. The drawback to higher frequencies is electrical noise. Switching power supplies can radiate harmonic frequency noise to nearby circuits, so they need to be well shielded and frequently require EMI (electromagnetic interference) filters. Since the switching device spends most of its time either in cutoff or saturation, the power lost in the control element is usually relatively small (although instantaneous power dissipated in the switching device can be large).

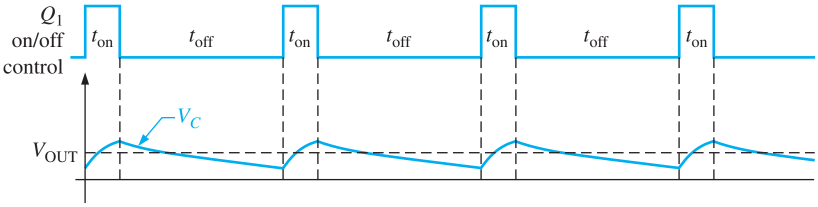
The *on* and *off* intervals of Q_1 are shown in the waveform of Figure 17–18(a). For an *n*-channel D-MOSFET, the control voltage swings between a negative value (*off*) to a positive value (*on*). The capacitor charges during the on-time (t_{on}) and discharges during the off-time (t_{off}). When the on-time is increased relative to the off-time, the capacitor charges



(a) V_{OUT} depends on the duty cycle.



(b) Increase the duty cycle and V_{OUT} increases.



(c) Decrease the duty cycle and V_{OUT} decreases.

▲ **FIGURE 17–18**

Switching regulator waveforms. The V_C waveform is shown for no inductive filtering to illustrate the charge and discharge action (ripple). L and C smooth V_C to a nearly constant level, as indicated by the dashed line for V_{OUT}.

more, thus increasing the output voltage, as indicated in Figure 17–18(b). When the on-time is decreased relative to the off-time, the capacitor discharges more, thus decreasing the output voltage, as in Figure 17–18(c). The inductor further smoothes the fluctuations of the output voltage caused by the charging and discharging action.

Ideally, the output voltage is expressed as

$$\mathbf{V_{OUT} = \left(\frac{t_{on}}{T}\right)V_{IN}}$$

Equation 17–8

T is the period of the on-off cycle of Q_1 and is related to the frequency by $T = 1/f$. The period is the sum of the on-time and the off-time.

$$T = t_{\text{on}} + t_{\text{off}}$$

As you know, the ratio t_{on}/T is called the *duty cycle.*

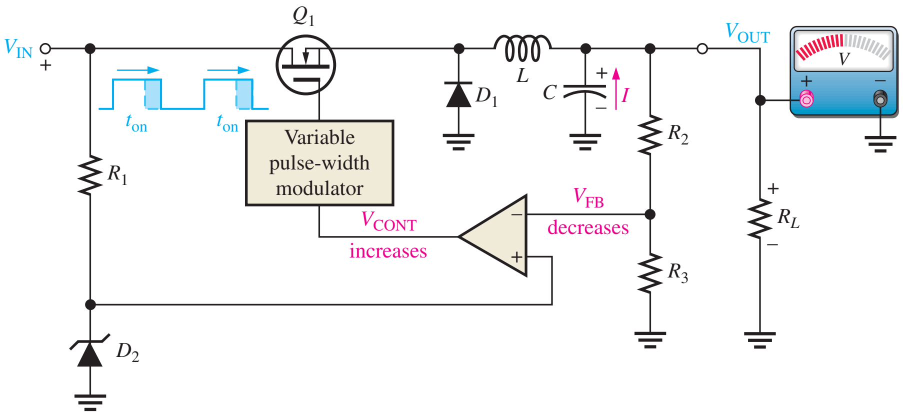
The regulating action is as follows and is illustrated in Figure 17–19. When V_{OUT} tries to decrease, the on-time of Q_1 is increased, causing an additional charge on C to offset the attempted decrease. When V_{OUT} tries to increase, the on-time of Q_1 is decreased, causing the capacitor to discharge enough to offset the attempted increase.

Step-Up Configuration

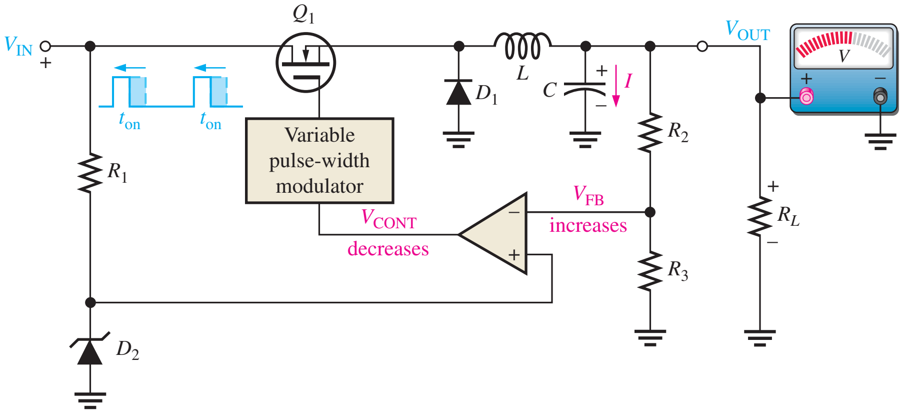
A basic step-up type of switching regulator (sometimes called a *boost converter*) is shown in Figure 17–20, where transistor Q_1 operates as a switch to ground.

FIGURE 17–19

Basic regulating action of a step-down switching regulator.


Q_1
V_{IN}
+
t_{on}
t_{on}
Variable pulse-width modulator
D_1
L
C
+
−
I
V_{OUT}
V
+
−
R_1
R_2
R_3
R_L
V_{FB} decreases
V_{CONT} increases
D_2

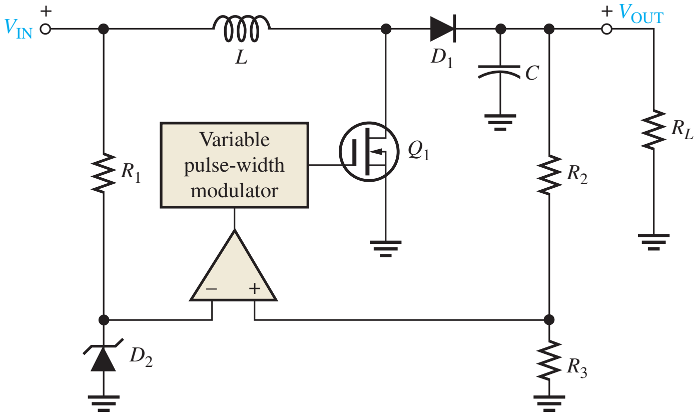
(a) When V_{OUT} attempts to decrease, the on-time of Q_1 increases.


Q_1
V_{IN}
+
t_{on}
t_{on}
Variable pulse-width modulator
D_1
L
C
+
−
I
V_{OUT}
V
+
−
R_1
R_2
R_3
R_L
V_{FB} increases
V_{CONT} decreases
D_2

(b) When V_{OUT} attempts to increase, the on-time of Q_1 decreases.

FIGURE 17–20

Basic step-up switching regulator.


+
V_{IN}
L
D_1
C
+ V_{OUT}
R_L
Variable pulse-width modulator
Q_1
R_1
R_2
R_3
−
+
D_2

The switching action is illustrated in Figures 17–21 and 17–22. When Q_1 turns on, a voltage equal to approximately V_{IN} is induced across the inductor with a polarity as indicated in Figure 17–21. During the on-time (t_{on}) of Q_1, the inductor voltage, V_L, decreases from its initial maximum and diode D_1 is reverse-biased. The longer Q_1 is on, the smaller V_L becomes. During the on-time, the capacitor only discharges an extremely small amount through the load.

When Q_1 turns off, as indicated in Figure 17–22, the inductor voltage suddenly reverses polarity and adds to V_{IN}, forward-biasing diode D_1 and allowing the capacitor to charge.

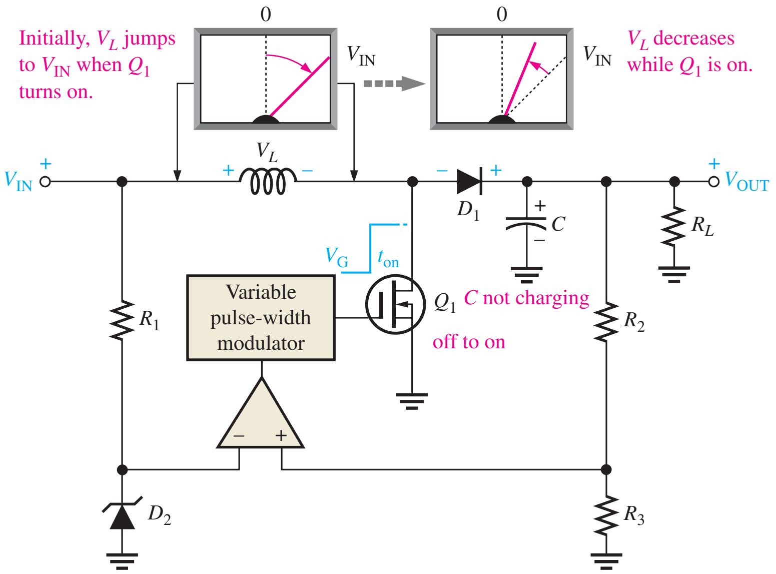

0
0
Initially, V_L jumps to V_{IN} when Q_1 turns on.
V_{IN}
V_{IN}
V_L decreases while Q_1 is on.
V_{IN}
V_L
D_1
C
V_{OUT}
R_L
V_G
t_{on}
Variable pulse-width modulator
Q_1
C not charging
off to on
R_1
R_2
D_2
R_3

FIGURE 17–21

Basic action of a step-up regulator when Q_1 is on.

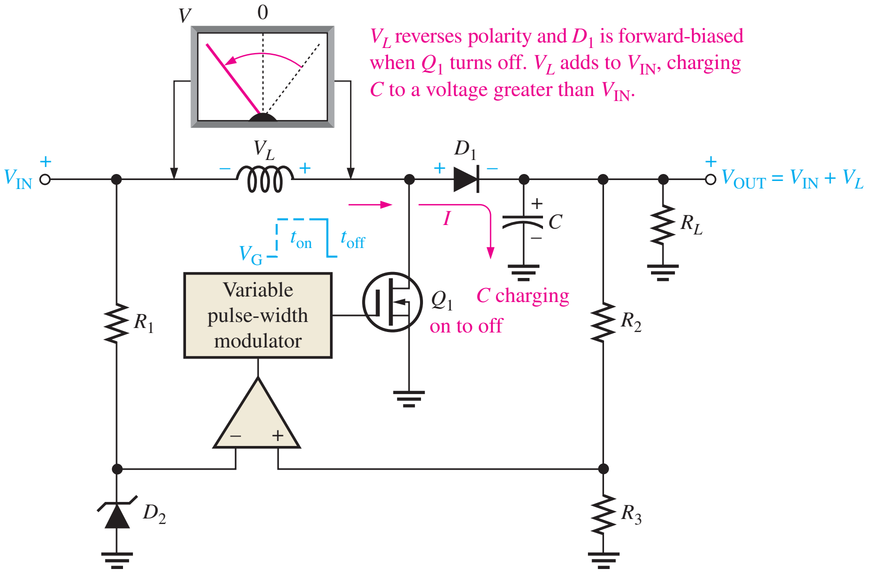

V
0
V_L reverses polarity and D_1 is forward-biased when Q_1 turns off. V_L adds to V_{IN}, charging C to a voltage greater than V_{IN}.
V_{IN}
V_L
D_1
$V_{OUT} = V_{IN} + V_L$
I
C
R_L
t_{on}
t_{off}
V_G
Variable pulse-width modulator
Q_1
C charging
on to off
R_1
R_2
D_2
R_3

FIGURE 17–22

Basic switching action of a step-up regulator when Q_1 turns off.

The output voltage is equal to the capacitor voltage and can be larger than V_{IN} because the capacitor is charged to V_{IN} plus the voltage induced across the inductor during the off-time of Q_1. The output voltage is dependent on both the inductor's magnetic field action (determined by t_{on}) and the charging of the capacitor (determined by t_{off}).

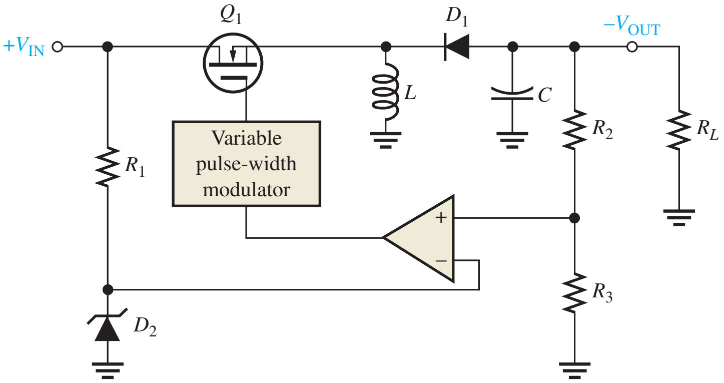
Voltage regulation is achieved by the variation of the on-time of Q_1 (within certain limits) as related to changes in V_{OUT} due to changing load or input voltage. If V_{OUT} tries to increase, the on-time of Q_1 will decrease, resulting in a decrease in the amount that C will charge. If V_{OUT} tries to decrease, the on-time of Q_1 will increase, resulting in an increase in the amount that C will charge. This regulating action maintains V_{OUT} at an essentially constant level.

Voltage-Inverter Configuration

A third type of switching regulator produces an output voltage that is opposite in polarity to the input. A basic diagram is shown in Figure 17–23. This is sometimes called a *buck-boost converter*.

FIGURE 17–23

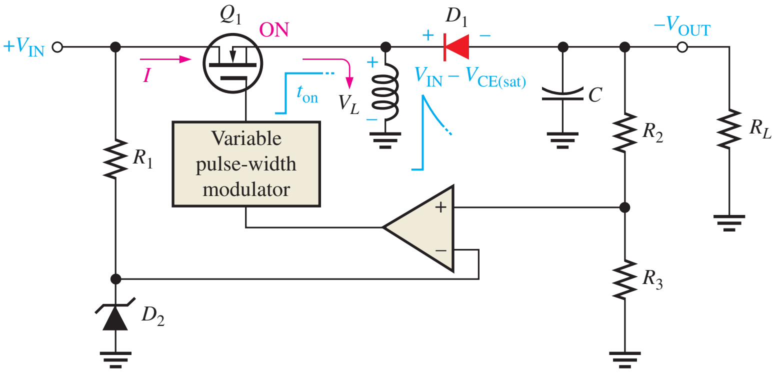
Basic inverting switching regulator.


Q_1
D_1
$-V_{OUT}$
$+V_{IN}$
L
C
R_2
R_L
R_1
Variable pulse-width modulator
R_3
D_2

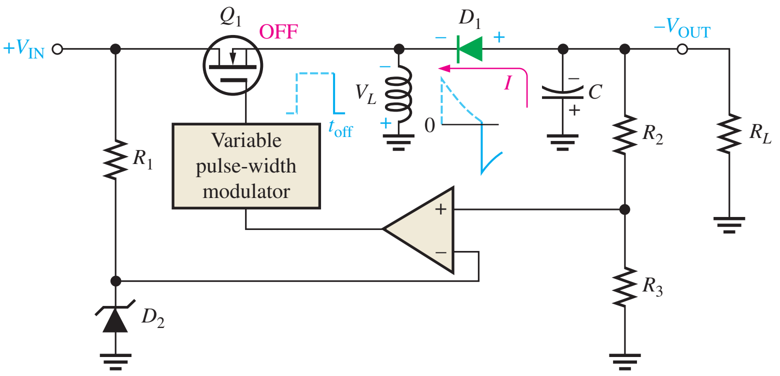
When Q_1 turns on, the inductor voltage jumps to approximately $V_{IN} - V_{CE(sat)}$ and the magnetic field rapidly expands, as shown in Figure 17–24(a). While Q_1 is on, the diode is reverse-biased and the inductor voltage decreases from its initial maximum. When Q_1 turns off, the magnetic field collapses and the inductor's polarity reverses, as shown in Figure 17–24(b). This forward-biases the diode, charges C, and produces a negative output voltage, as indicated. The repetitive on-off action of Q_1 produces a repetitive charging and discharging that is smoothed by the LC filter action.

FIGURE 17–24

Basic inverting action of an inverting switching regulator.


Q_1
ON
D_1
$-V_{OUT}$
$+V_{IN}$
I
t_{on}
V_L
$V_{IN} - V_{CE(sat)}$
C
R_2
R_L
R_1
Variable pulse-width modulator
R_3
D_2

(a) When Q_1 is on, D_1 is reverse-biased.

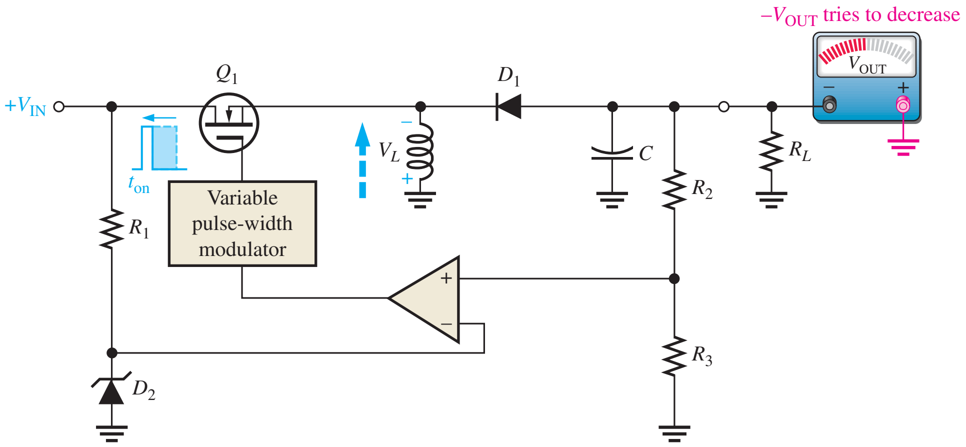

Q_1
OFF
D_1
$-V_{OUT}$
$+V_{IN}$
V_L
I
C
t_{off}
0
R_2
R_L
R_1
Variable pulse-width modulator
R_3
D_2

(b) When Q_1 turns off, D_1 forward biases.

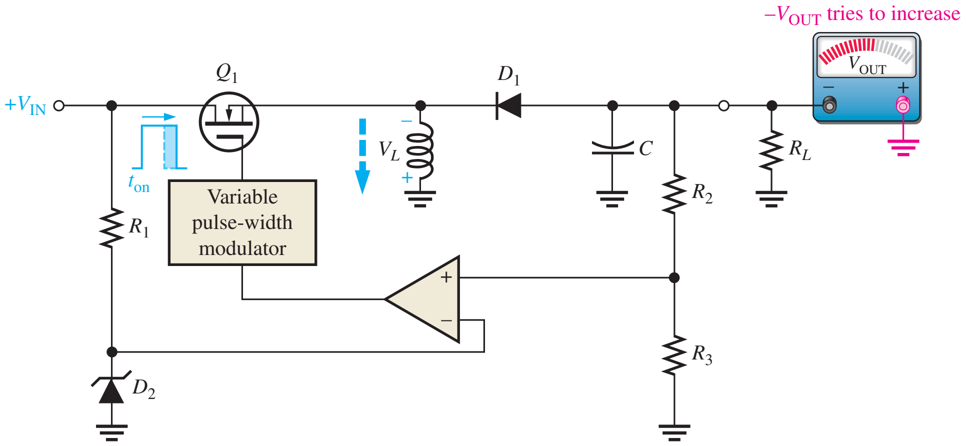
As with the step-up regulator, the less time Q_1 is on, the greater the output voltage is, and vice versa. This regulating action is illustrated in Figure 17–25.

FIGURE 17–25

Basic regulating action of an inverting switching regulator.


$-V_{OUT}$ tries to decrease
Q_1
D_1
V_{OUT}
−
+
$+V_{IN}$
t_{on}
V_L
−
+
C
R_L
R_2
R_1
Variable pulse-width modulator
+
−
R_3
D_2

(a) When $-V_{OUT}$ tries to decrease, t_{on} decreases, causing V_L to increase. This compensates for the attempted decrease in $-V_{OUT}$.


$-V_{OUT}$ tries to increase
Q_1
D_1
V_{OUT}
−
+
$+V_{IN}$
t_{on}
V_L
−
+
C
R_L
R_2
R_1
Variable pulse-width modulator
+
−
R_3
D_2

(b) When $-V_{OUT}$ tries to increase, t_{on} increases, causing V_L to decrease. This compensates for the attempted increase in $-V_{OUT}$.

SECTION 17–4 CHECKUP

1. What are three types of switching regulators?
2. What is the primary advantage of switching regulators over linear regulators?
3. How are changes in output voltage compensated for in the switching regulator?

17–5 INTEGRATED CIRCUIT VOLTAGE REGULATORS

In the previous sections, the basic voltage regulator configurations were presented. Several types of both linear and switching regulators are available in integrated circuit (IC) form. Generally, the linear regulators are three-terminal devices that provide either positive or negative output voltages that can be either fixed or adjustable. In this section, typical linear and switching IC regulators are introduced.

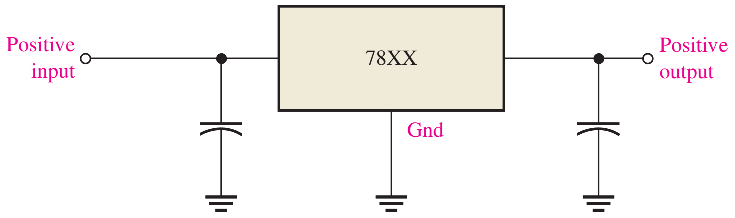
After completing this section, you should be able to

- **Discuss integrated circuit voltage regulators**
- Discuss fixed positive linear voltage regulators
  - Describe the 78XX regulators
  - Explain thermal overload

- Discuss fixed negative linear voltage regulators
    - Describe the 79XX regulators
- Discuss adjustable positive linear voltage regulators
    - Describe the LM317 regulator
    - Determine the output voltage
- Discuss adjustable negative linear voltage regulators
    - Describe the LM337 regulator
- Discuss switching voltage regulators
    - Describe the 78S40 regulator

Fixed Positive Linear Voltage Regulators

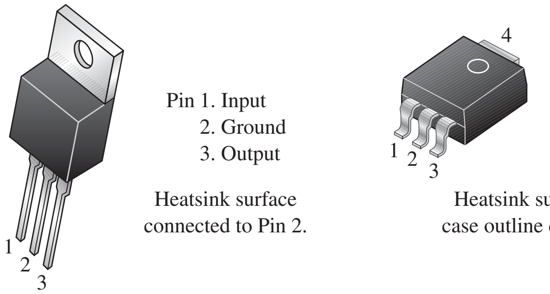
Although many types of IC regulators are available, the 78XX series of IC regulators is representative of three-terminal devices that provide a fixed positive output voltage. The three terminals are input, output, and ground as indicated in the standard fixed voltage configuration in Figure 17–26(a). The last two digits in the part number designate the output voltage. For example, the 7805 is a +5.0 V regulator. For any given regulator, the output voltage can be as much as ±4% of the nominal output. Thus, a 7805 may have an output from 4.8 V to 5.2 V but will remain constant in that range. Other available output voltages are given in Figure 17–26(b) and common packages are shown in part (c).



(a) Standard configuration

Type number	Output voltage
7805	+5.0 V
7806	+6.0 V
7808	+8.0 V
7809	+9.0 V
7812	+12.0 V
7815	+15.0 V
7818	+18.0 V
7824	+24.0 V

(b) The 78XX series



Pin 1. Input
2. Ground
3. Output

Heatsink surface
connected to Pin 2.

Heatsink surface (shown as terminal 4 in
case outline drawing) is connected to Pin 2.

(c) Typical packages

▲ FIGURE 17–26

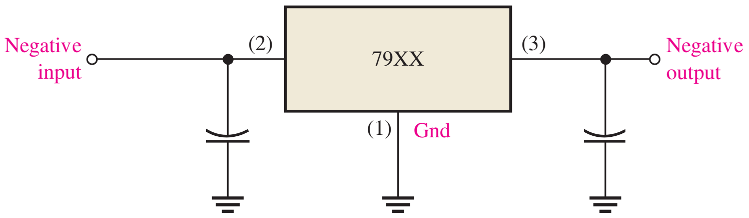
The 78XX series three-terminal fixed positive voltage regulators.

Capacitors, although not always necessary, are sometimes used on the input and output as indicated in Figure 17–26(a). The output capacitor acts basically as a line filter to improve transient response. The input capacitor filters the input and prevents unwanted oscillations when the regulator is some distance from the power supply filter such that the line has a significant inductance.

The 78XX series can produce output currents up to in excess of 1 A when used with an adequate heat sink. The input voltage must be approximately 2.5 V above the output voltage in order to maintain regulation. The circuits have internal thermal overload protection and short-circuit current-limiting features. **Thermal overload** occurs when the internal power dissipation becomes excessive and the temperature of the device exceeds a certain value. Almost all applications of regulators require that the device be secured to a heat sink to prevent thermal overload.

Fixed Negative Linear Voltage Regulators

The 79XX series is typical of three-terminal IC regulators that provide a fixed negative output voltage. This series is the negative-voltage counterpart of the 78XX series and shares most of the same features and characteristics except the pin numbers are different than the positive regulators. Figure 17–27 indicates the standard configuration and part numbers with corresponding output voltages that are available.



(a) Standard configuration

Type number	Output voltage
7905	–5.0 V
7905.2	–5.2 V
7906	–6.0 V
7908	–8.0 V
7912	–12.0 V
7915	–15.0 V
7918	–18.0 V
7924	–24.0 V

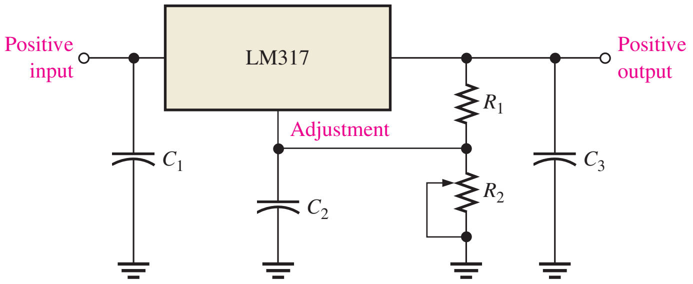
(b) The 79XX series

▲ FIGURE 17–27

The 79XX series three-terminal fixed negative voltage regulators.

Adjustable Positive Linear Voltage Regulators

The LM317 is an example of a three-terminal positive regulator with an adjustable output voltage. The standard configuration is shown in Figure 17–28. The capacitors are for decoupling and do not affect the dc operation. Notice that there is an input, an output, and an adjustment terminal. The external fixed resistor R_1 and the external variable resistor R_2 provide the output voltage adjustment. V_{OUT} can be varied from 1.2 V to 37 V depending on the resistor values. The LM317 can provide over 1.5 A of output current to a load.



◀ FIGURE 17–28

The LM317 three-terminal adjustable positive voltage regulator.

The LM317 is operated as a "floating" regulator because the adjustment terminal is not connected to ground, but floats to whatever voltage is across R_2. This allows the output voltage to be much higher than that of a fixed-voltage regulator.

Basic Operation As indicated in Figure 17–29, a constant 1.25 V reference voltage (V_{REF}) is maintained by the regulator between the output terminal and the adjustment terminal. This constant reference voltage produces a constant current (I_{REF}) through R_1, regardless of the value of R_2. I_{REF} is also through R_2.

$$I_{REF} = \frac{V_{REF}}{R_1} = \frac{1.25\text{ V}}{R_1}$$

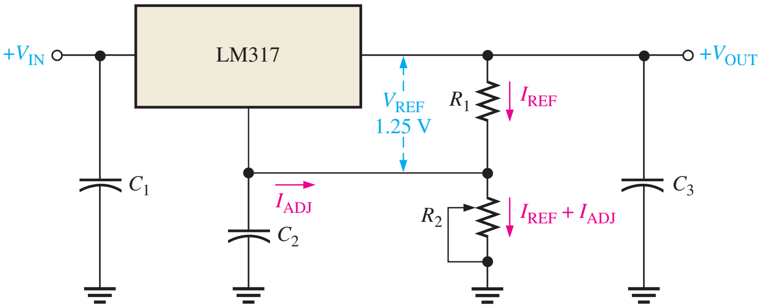


FIGURE 17–29

Operation of the LM317 adjustable positive voltage regulator.

There is a very small constant current at the adjustment terminal of approximately 50 μA called I_{ADJ}, which is through R_2. A formula for the output voltage is developed as follows.

$$V_{OUT} = V_{R1} + V_{R2} = I_{REF}R_1 + I_{REF}R_2 + I_{ADJ}R_2$$

$$= I_{REF}(R_1 + R_2) + I_{ADJ}R_2 = \frac{V_{REF}}{R_1}(R_1 + R_2) + I_{ADJ}R_2$$

Equation 17–9

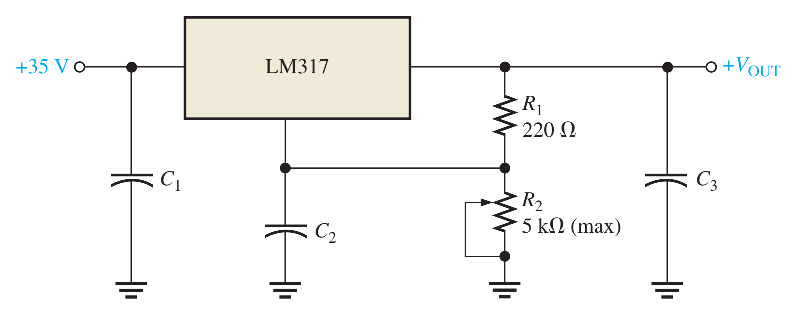
$$\boldsymbol{V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2}$$

As you can see, the output voltage is a function of both R_1 and R_2. Once the value of R_1 is set, the output voltage is adjusted by varying R_2.

EXAMPLE 17–6

Determine the minimum and maximum output voltages for the voltage regulator in Figure 17–30. Assume $I_{ADJ} = 50\ \mu$A.

FIGURE 17–30



Solution

$$V_{R1} = V_{REF} = 1.25\text{ V}$$

When R_2 is set at its minimum of 0 Ω,

$$V_{OUT(min)} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 = 1.25\text{ V}(1) = \mathbf{1.25\ V}$$

When R_2 is set at its maximum of 5 kΩ,

$$V_{OUT(max)} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 = 1.25\text{ V}\left(1 + \frac{5\text{ k}\Omega}{220\ \Omega}\right) + (50\ \mu\text{A})\,5\text{ k}\Omega$$

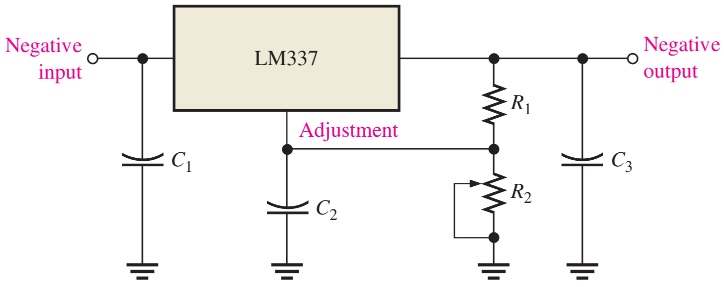
$$= 29.66\text{ V} + 0.25\text{ V} = \mathbf{29.9\ V}$$

Related Problem

What is the output voltage of the regulator if R_2 is set at 2 kΩ?

Adjustable Negative Linear Voltage Regulators

The LM337 is the negative output counterpart of the LM317 and is a good example of this type of IC regulator. Like the LM317, the LM337 requires two external resistors for output voltage adjustment as shown in Figure 17–31. The output voltage can be adjusted from −1.2 V to −37 V, depending on the external resistor values. The capacitors are for decoupling and do not affect the dc operation.



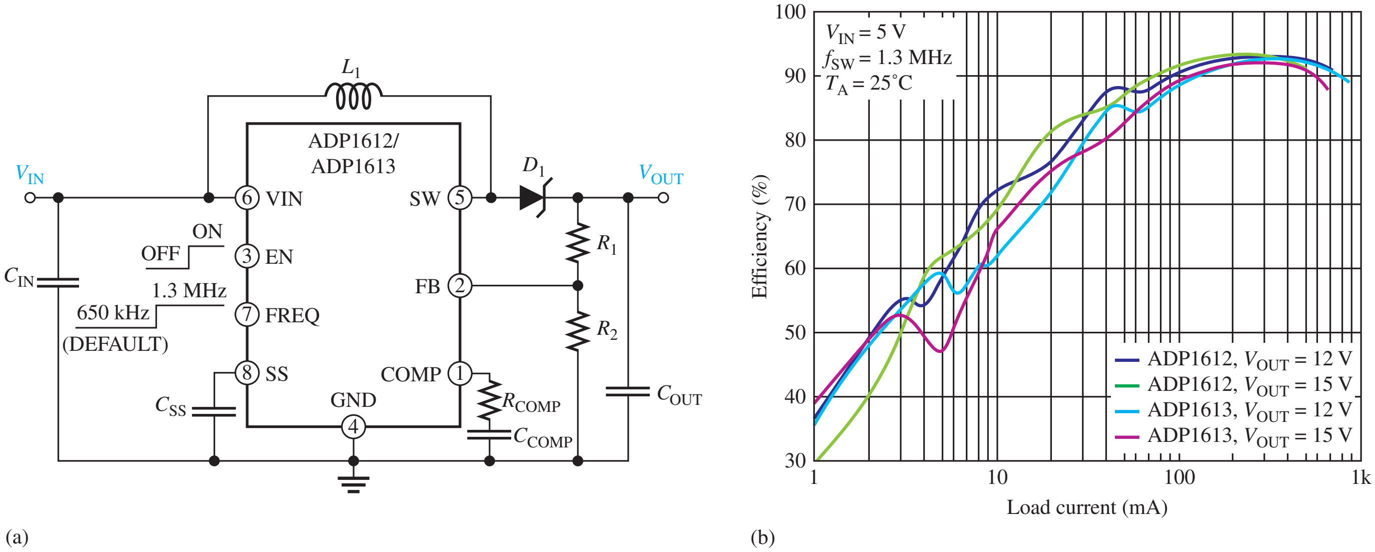
◀ FIGURE 17–31

The LM337 three-terminal adjustable negative voltage regulator.

Switching Voltage Regulators

There are many integrated circuit switching regulators available. The two used as typical examples are the ADP1612/ADP1613 step-up (boost) regulator and the ADP2300/ADP2301 step-down (buck) regulator. The basic operation was explained earlier in the chapter.

The Step-Up Switching Regulator The step-up regulator configuration using an ADP1612/ADP1613 is shown in Figure 17–32(a). The ADP1612 and the ADP1613 are essentially the same except for their switching frequency, which is used in the pulse-width modulation (PWM) operation.



(a)

(b)

▲ FIGURE 17–32

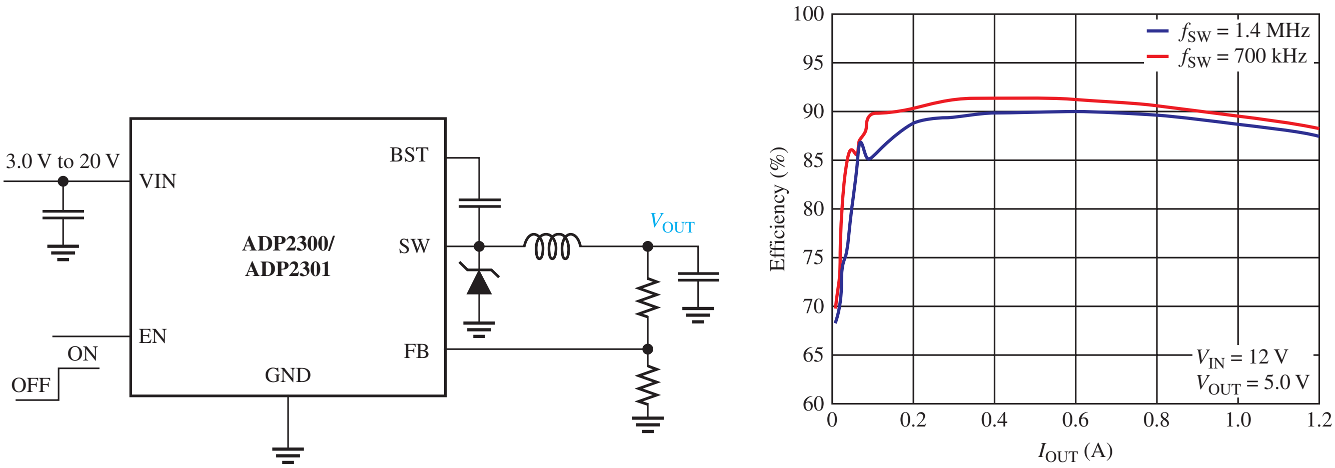
Step-up configuration and efficiency vs. current graph.

This regulator operates with PWM and exhibits an efficiency of up to 94% at the higher switch frequency, depending on the output current and voltage, as shown by the graphs in Figure 17–32(b). Notice that as the load current increases, the efficiency increases. The output voltage has a much smaller effect. The operating frequency of the PWM is pin-selectable for 650 kHz or 1.3 MHz. The lower frequency results in better efficiency, and the higher frequency allows the use of smaller external components. For the 650 kHz operation, pin 7 (FREQ) is connected to ground or left open (floating for default). For the 1.3 MHz operation, pin 7 is connected to VIN (pin 6). The input voltage range is 1.8 V to 5.5 V and the output voltage can be as high as 20 V.

This device has thermal shutdown (TSD) protection in case the temperature exceeds 150°C and turns back on when the temperature drops to 130°C. Also, the under-voltage lock-out (UVLO) feature prevents erratic output voltages if the input voltage falls below a minimum value.

The capacitor connected to pin 8 (soft start) prevents a large inrush of current when the device is first turned on. The EN input (pin 3) turns the regulator on or off. The COMP input (pin 1) requires a series *RC* circuit for compensation. The FB input (pin 2) is connected to a voltage divider to provide feedback for output voltage control. An inductor is connected from the input to SW (switching output, pin 5), and a rectifier diode is connected from SW to the output voltage. Notice the diode in this case is a Schottky diode for faster switching.

The Step-Down Switching Regulator The step-down regulator configuration using an ADP2300/ADP2301 is shown in Figure 17–33(a). The ADP2300 and the ADP2301 are essentially the same except for their switching frequency. Unlike the ADP1612/ADP1613, this device does not have pin-selectable frequencies. Instead, each has a fixed internal oscillator with a frequency of 700 kHz for the ADP2300 and 1.4 MHz for the ADP2301.



(a) (b)

▲ FIGURE 17–33

Step-down configuration and efficiency vs. current graph.

This device has thermal shutdown (TSP) protection in case temperature exceeds 140°C and turns back on when the temperature drops to 150°C. Also, it has an under-voltage lock-out (UVLO) feature and short-circuit protection.

This regulator operates with PWM and exhibits an efficiency of up to 91%, depending on the output current, as shown by the graphs in Figure 17–33(b) for each frequency. Notice that as the load current increases above about 0.2 A, the efficiency remains relatively constant (between about 91% and about 88%) and drops off a little as the output current increases. In this case, the output voltage is constant at 5 V. The input voltage range is 3 V to 20 V, and the output voltage can be as high as 20 V. The output voltage is from $0.8 \times V_{IN}$ to $0.85 \times V_{IN}$.

The only input that is not on the step-up device is the BST (boot-strap). A capacitor must be connected from BST (pin 1) to SW (pin 6). The regulator generates a voltage for a MOSFET gate drive circuit by sensing a regulating voltage difference between the BST and SW pins.

SECTION 17–5 CHECKUP

1. What are the three terminals of a fixed-voltage regulator?
2. What is the output voltage of a 7809? Of a 7915?
3. What are the three terminals of an adjustable-voltage regulator?
4. What external components are required for a basic LM317 configuration?

17–6 INTEGRATED CIRCUIT VOLTAGE REGULATOR CONFIGURATIONS

In the last section, you saw several devices that are representative of the general types of IC voltage regulators. Now, several different ways these devices can be modified with external circuitry to improve or alter their performance are examined.

After completing this section, you should be able to

- **Describe applications of IC voltage regulators**
- Explain the purpose of an external pass transistor
  - Calculate the value of the external resistor required
- Explain how current limiting can be implemented
- Describe how to use a three-terminal regulator as a current regulator
- Describe switching regulator configurations using the 78S40
  - Describe the step-down configuration
  - Describe the step-up configuration

The External Pass Transistor

As you know, an IC voltage regulator is capable of delivering only a certain amount of output current to a load. For example, the 78XX series regulators can handle a peak output current of 1.3 A (more under certain conditions). If the load current exceeds the maximum allowable value, there will be thermal overload and the regulator will shut down. A thermal overload condition means that there is excessive power dissipation inside the device.

If an application requires more than the maximum current that the regulator can deliver, an external pass transistor Q_{ext}, can be used. Figure 17–34 illustrates a three-terminal regulator with an external pass transistor for handling currents in excess of the output current capability of the basic regulator.

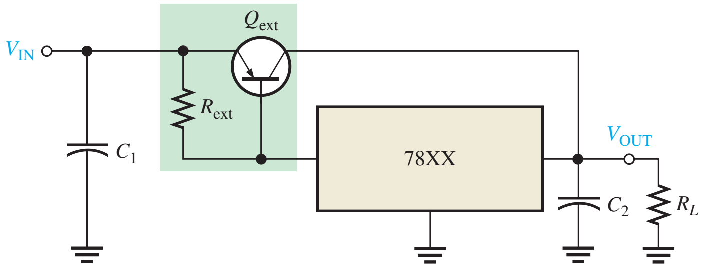


FIGURE 17–34

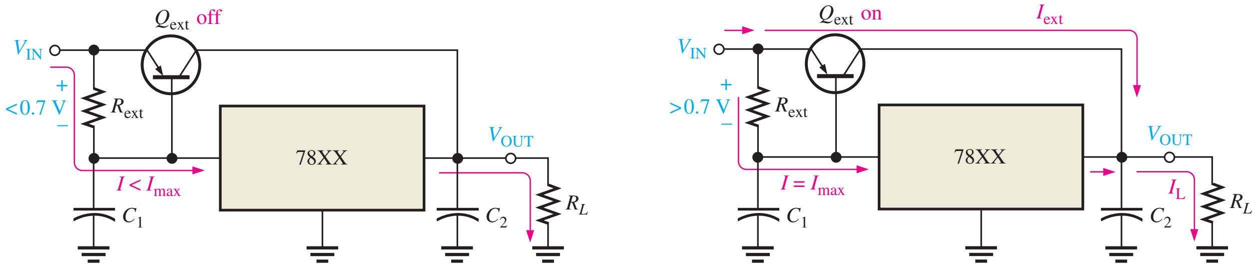
A 78XX-series three-terminal regulator with an external pass transistor to increase power dissipation.

The value of the external current-sensing resistor, R_{ext}, determines the value of current at which Q_{ext} begins to conduct because it sets the base-to-emitter voltage of the transistor. As long as the current is less than the value set by R_{ext}, the transistor Q_{ext} is off, and the regulator operates normally as shown in Figure 17–35(a). This is because the voltage drop across R_{ext} is less than the 0.7 V base-to-emitter voltage required to turn Q_{ext} on. R_{ext} is determined by the following formula, where I_{max} is the highest current that the voltage regulator is to handle internally.

Equation 17–10

$$\mathbf{R_{ext} = \frac{0.7\ V}{I_{max}}}$$

When the current is sufficient to produce at least a 0.7 V drop across R_{ext}, the external pass transistor Q_{ext} turns on and conducts any current in excess of I_{max}, as indicated in Figure 17–35(b). Q_{ext} will conduct more or less, depending on the load requirements. For example, if the total load current is 3 A and I_{max} was selected to be 1 A, the external pass transistor will conduct 2 A, which is the excess over the internal voltage regulator current I_{max}.



(a) When the regulator current is less than I_{max}, the external pass transistor is off and the regulator is handling all of the current.

(b) When the load current exceeds I_{max}, the drop across R_{ext} turns Q_{ext} on and it conducts the excess current.

▲ FIGURE 17–35

Operation of the regulator with an external pass transistor.

EXAMPLE 17–7

What value is R_{ext} if the maximum current to be handled internally by the voltage regulator in Figure 17–34 is set at 700 mA?

Solution

$$R_{ext} = \frac{0.7\ V}{I_{max}} = \frac{0.7\ V}{0.7\ A} = \mathbf{1\ \Omega}$$

Related Problem If R_{ext} is changed to 1.5 Ω, at what current value will Q_{ext} turn on?

The external pass transistor is typically a power transistor with a heat sink that must be capable of handling a maximum power of

$$P_{ext} = I_{ext}(V_{IN} - V_{OUT})$$

EXAMPLE 17–8

What must be the minimum power rating for the external pass transistor used with a 7824 regulator in a circuit such as that shown in Figure 17–34? The input voltage is 30 V and the load resistance is 10 Ω. The maximum internal current is to be 700 mA. Assume that there is no heat sink for this calculation. Keep in mind that the use of a heat sink increases the effective power rating of the transistor and you can use a lower rated transistor.

Solution The load current is

$$I_L = \frac{V_{OUT}}{R_L} = \frac{24\text{ V}}{10\ \Omega} = 2.4\text{ A}$$

The current through Q_{ext} is

$$I_{ext} = I_L - I_{max} = 2.4\text{ A} - 0.7\text{ A} = 1.7\text{ A}$$

The power dissipated by Q_{ext} is

$$P_{ext(min)} = I_{ext}(V_{IN} - V_{OUT}) = (1.7\text{ A})(30\text{ V} - 24\text{ V}) = (1.7\text{ A})(6\text{ V}) = \mathbf{10.2\ W}$$

For a safety margin, choose a power transistor with a rating greater than 10.2 W, say at least 15 W.

Related Problem Rework this example using a 7815 regulator.

Current Limiting

A drawback of the circuit in Figure 17–34 is that the external transistor is not protected from excessive current, such as would result from a shorted output. An additional current-limiting circuit (Q_{lim} and R_{lim}) can be added as shown in Figure 17–36 to protect Q_{ext} from excessive current and possible burn out.

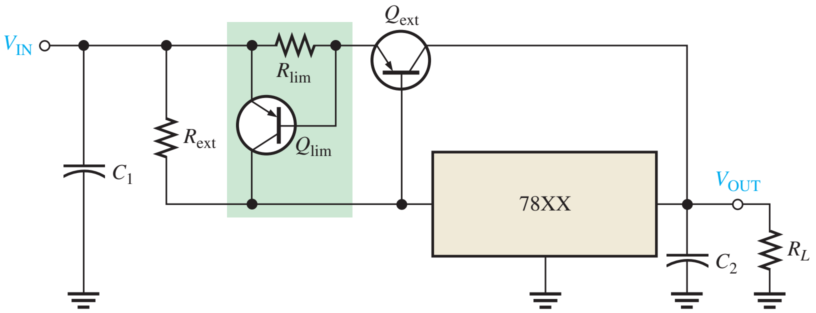
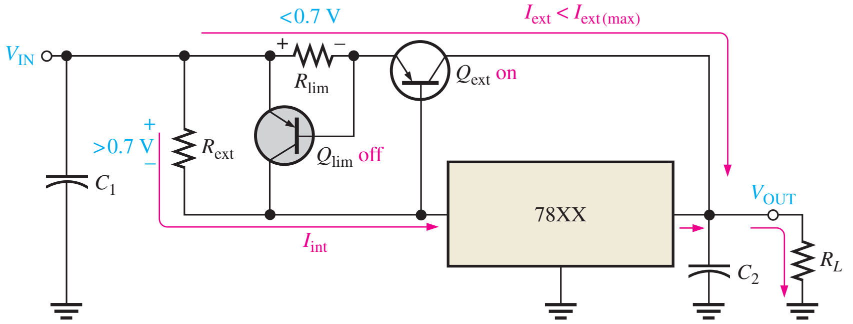


FIGURE 17–36

Regulator with current limiting.

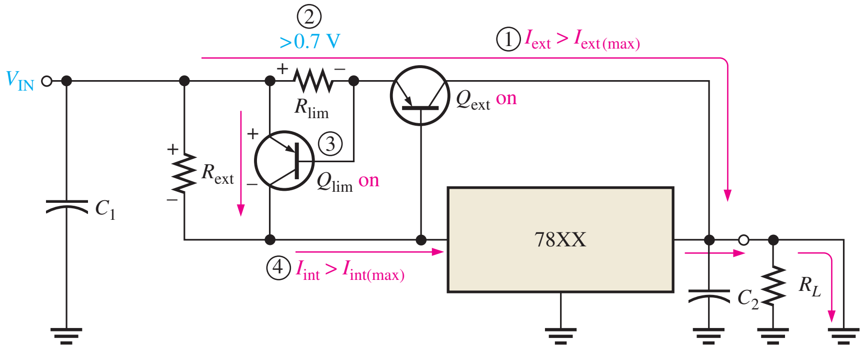
The following describes the way the current-limiting circuit works. The current-sensing resistor R_{lim} sets the V_{BE} of transistor Q_{lim}. The base-to-emitter voltage of Q_{ext} is now determined by $V_{R_{ext}} - V_{R_{lim}}$ because they have opposite polarities. So, for normal operation, the drop across R_{ext} must be sufficient to overcome the opposing drop across R_{lim}. If the current through Q_{ext} exceeds a certain maximum ($I_{ext(max)}$) because of a shorted output or a faulty load, the voltage across R_{lim} reaches 0.7 V and turns Q_{lim} on. Q_{lim} now conducts current through the regulator and away from Q_{ext}, forcing a thermal overload to occur and shut down the regulator. Remember, the IC regulator is internally protected from thermal overload as part of its design.

This action is illustrated in Figure 17–37. In part (a), the circuit is operating normally with Q_{ext} conducting less than the maximum current that it can handle with Q_{lim} off. Part (b) shows what happens when there is a short across the load. The current through Q_{ext} suddenly increases and causes the voltage drop across R_{lim} to increase, which turns Q_{lim} on. The current is now diverted through the regulator, which causes it to shut down due to thermal overload.



<0.7 V
$I_{ext} < I_{ext(max)}$
V_{IN}
+
−
R_{lim}
Q_{ext} on
+
>0.7 V
−
R_{ext}
Q_{lim} off
C_1
78XX
V_{OUT}
I_{int}
C_2
R_L

(a) During normal operation, when the load current is not excessive, Q_{lim} is off.



②
>0.7 V
① $I_{ext} > I_{ext(max)}$
V_{IN}
+
−
R_{lim}
Q_{ext} on
+
③
R_{ext}
−
Q_{lim} on
C_1
78XX
④ $I_{int} > I_{int(max)}$
C_2
R_L

(b) When short occurs ①, the external current becomes excessive and the voltage across R_{lim} increases ② and turns on Q_{lim} ③, which then routes current through the regulator and conducts it away from Q_{ext}, causing the internal regulator current to become excessive ④ which forces the regulator into thermal shut down.

▲ **FIGURE 17–37**

The current-limiting action of the regulator circuit.

A Current Regulator

The three-terminal regulator can be used as a current source when an application requires that a constant current be supplied to a variable load. The basic circuit is shown in Figure 17–38 where R_1 is the current-setting resistor. The regulator provides a fixed constant voltage, V_{OUT}, between the ground terminal (not connected to ground in this case) and the output terminal. This determines the constant current supplied to the load.

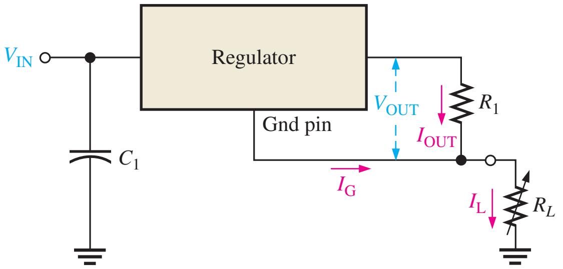
Equation 17–11

$$I_L = \frac{V_{OUT}}{R_1} + I_G$$

The current, I_G, from the ground pin is very small compared to the output current and can often be neglected.

▶ **FIGURE 17–38**

The three-terminal regulator as a current source.



V_{IN}
Regulator
Gnd pin
C_1
V_{OUT}
R_1
I_{OUT}
I_G
I_L
R_L

EXAMPLE 17–9

What value of R_1 is necessary in a 7805 regulator to provide a constant current of 0.5 A to a variable load that can be adjusted from 1 Ω to 10 Ω?

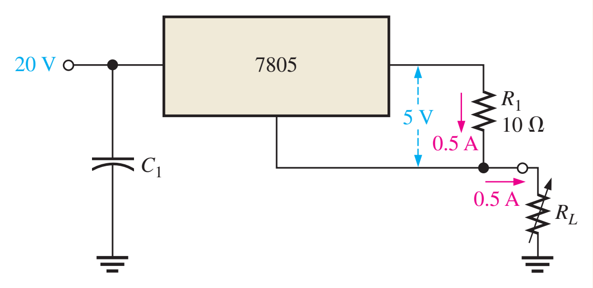
Solution The 7805 produces 5 V between its ground terminal and its output terminal. Therefore, if you want 0.5 A of current, the current-setting resistor must be (neglecting I_G)

$$R_1 = \frac{V_{OUT}}{I_L} = \frac{5\text{ V}}{0.5\text{ A}} = \mathbf{10\ \Omega}$$

The circuit is shown in Figure 17–39.

▶ **FIGURE 17–39**

A constant-current source of 0.5 A.



Related Problem If a 7808 regulator is used instead of the 7805, to what value would you change R_1 to maintain a constant current of 0.5 A?

SECTION 17–6 CHECKUP

1. What is the purpose of using an external pass transistor with an IC voltage regulator?
2. What is the advantage of current limiting in a voltage regulator?
3. What does *thermal overload* mean?

Application Activity: *Variable DC Power Supply*

A regulated power supply with a fixed output voltage of +12 V was developed in Chapter 3. The company that manufactures this power supply plans to offer a new line of variable power supplies for which a specified voltage can be preset at the factory or can be adjusted by the user. In this application, the power supply with a variable regulator is developed to provide an output voltage from +9 V to +30 V and a maximum load current of 250 mA.

The Circuit

Recall that in the original power supply, a 7812 provided a +12 V regulated output. In this new power supply, a 7809 is used to produce that variable output voltage. As in the earlier design, it is recommended by the manufacturer that a 0.33 μF capacitor be connected from the input terminal to ground and a 0.1 μF capacitor be connected from the output terminal to ground, as shown in Figure 17–40, to prevent high frequency oscillations and improve the performance. The reason for a small-value capacitor in parallel with a large one is that the large filter capacitor has an internal equivalent series resistance, which affects the high frequency response of the system. The effect is cancelled with the small capacitor.

The Transformer The transformer must convert the 120 V rms line voltage to an ac voltage that will result in a rectified voltage that will produce 34 V ± 10% when filtered.

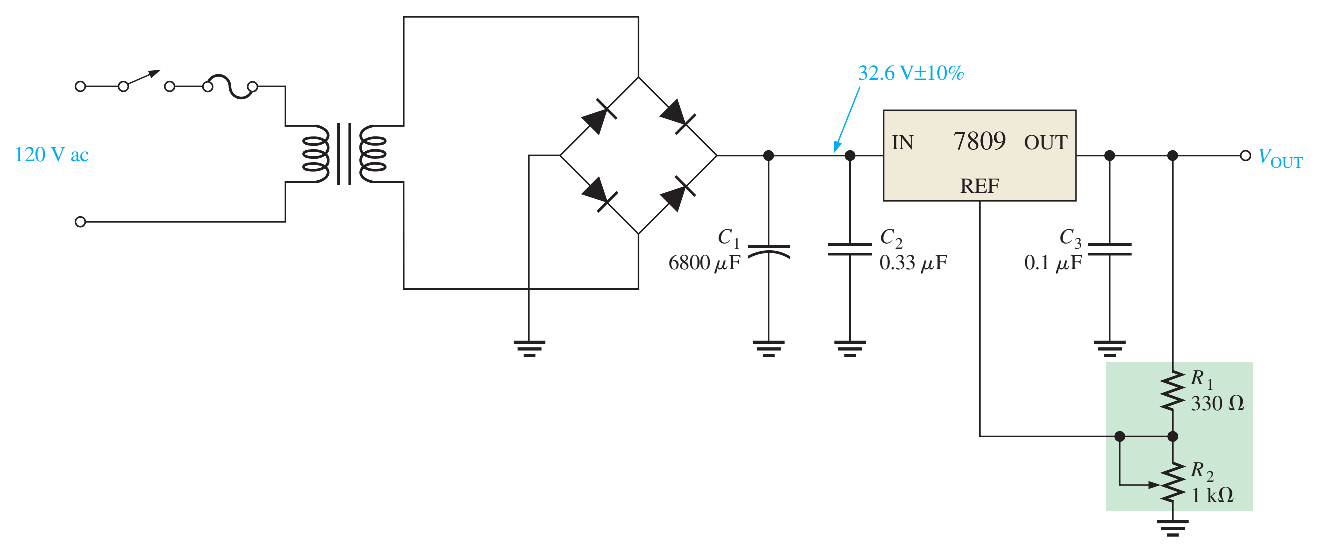


FIGURE 17–40

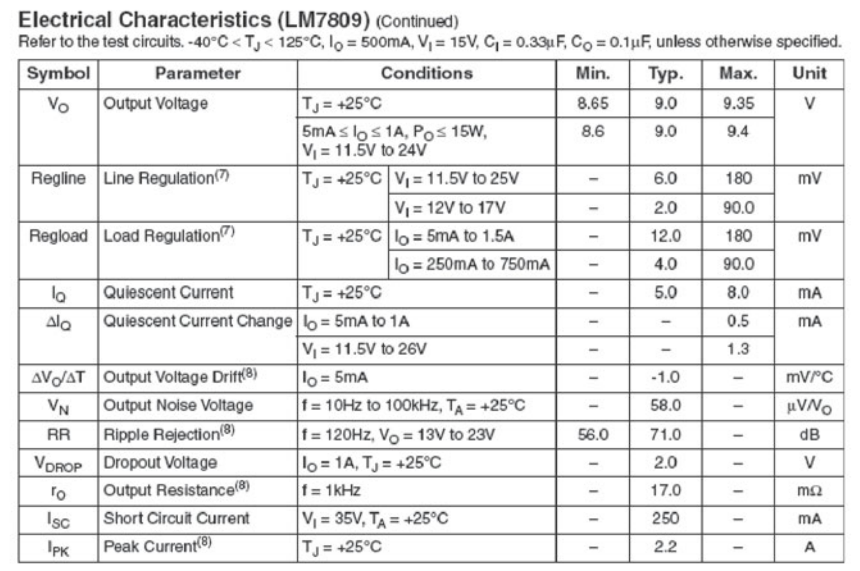
Variable output power supply.

The Voltage Regulator A partial datasheet for a 7809 is shown in Figure 17–41. Notice that there is a range of nominal output voltages, but it is typically 9.0 V. The line and load regulations specify how much the output can vary about the nominal output value. For example, the typical 9.0 V output will change no more than 12 mV (typical) as the load current changes from 5 mA to 1.5 A. The output voltage of the regulator is the voltage between the output (OUT) terminal and the reference (REF) terminal. The voltage divider formed by R_1 and R_2 provides a reference voltage other than ground and increases the output voltage with respect to ground above the 9 V nominal regulator output by an amount equal to the voltage across R_2.

1. What are the minimum and maximum nominal output voltages specified on the datasheet when I_O is 500 mA.
2. From the datasheet, determine the maximum change in the output voltage when the load current changes from 5 mA to 1.5 A.

FIGURE 17–41

Partial datasheet for a 7809 regulator. Copyright Fairchild Semiconductor Corporation. Used by permission.



Electrical Characteristics (LM7809) (Continued)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 15V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		8.65	9.0	9.35	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 11.5V to 24V		8.6	9.0	9.4	
Regline	Line Regulation[7]	T_J = +25°C	V_I = 11.5V to 25V	–	6.0	180	mV
			V_I = 12V to 17V	–	2.0	90.0	
Regload	Load Regulation[7]	T_J = +25°C	I_O = 5mA to 1.5A	–	12.0	180	mV
			I_O = 250mA to 750mA	–	4.0	90.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 11.5V to 26V		–	–	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[8]	I_O = 5mA		–	-1.0	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	58.0	–	μV/V_O
RR	Ripple Rejection[8]	f = 120Hz, V_O = 13V to 23V		56.0	71.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[8]	f = 1kHz		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	250	–	mA
I_{PK}	Peak Current[8]	T_J = +25°C		–	2.2	–	A

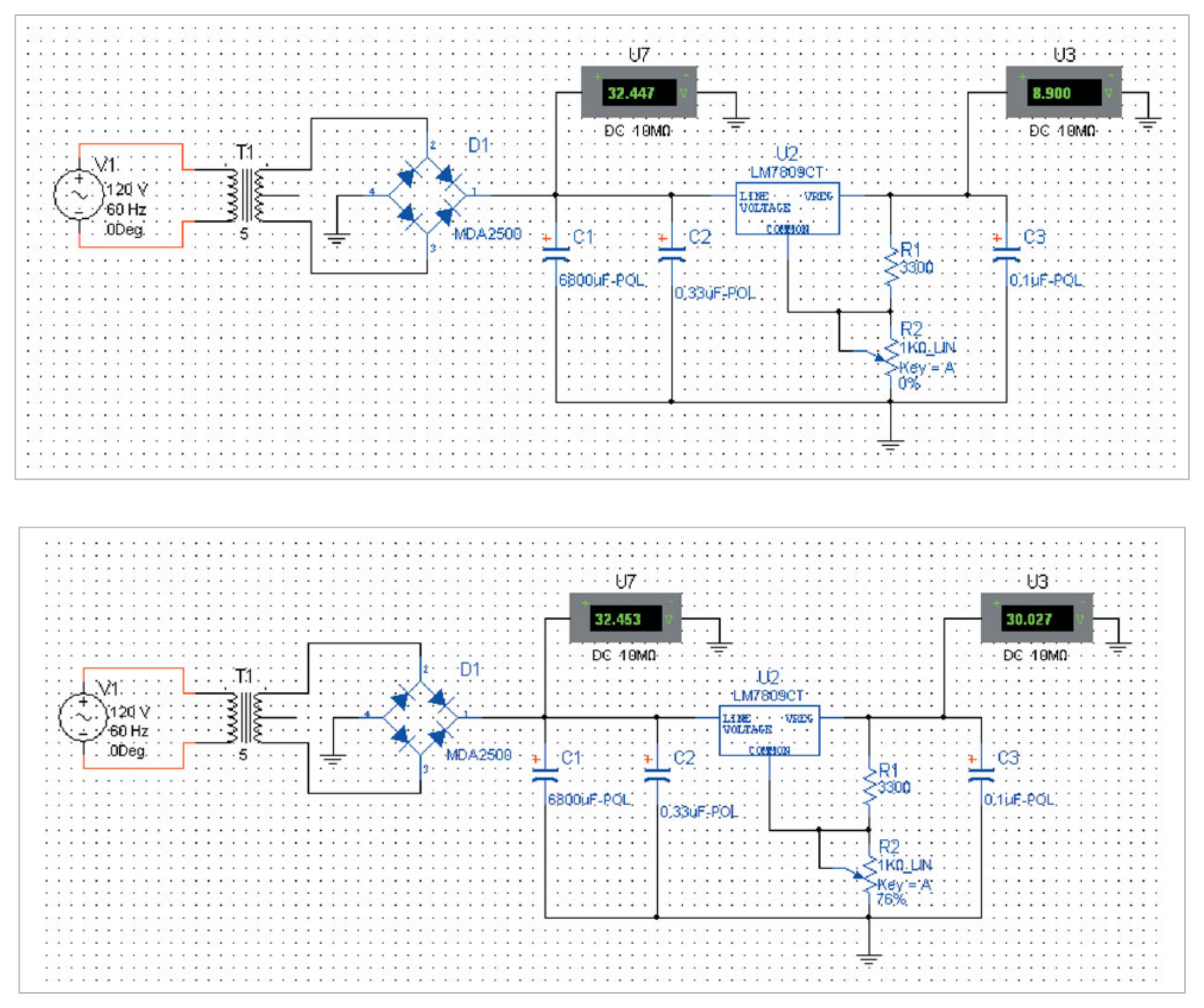
3. Calculate the maximum power dissipation in R_1.
4. Calculate the maximum power dissipation in R_2.

The Fuse The fuse will be in series with the primary winding of the transformer, as shown in Figure 17–40. The fuse should be calculated based on the maximum allowable primary current. Recall from your dc/ac circuits course that if the voltage is stepped down, the current is stepped up. From the specifications for the unregulated power supply, the maximum load current is 100 mA.

5. Calculate the primary current and use this value to select a fuse rating for the circuit in Figure 17–40.

Simulation

Multisim is used to simulate this power supply circuit. Figure 17–42 shows the simulated regulated power supply circuit adjusted to show that it meets or exceeds the specified minimum and maximum output voltages.


U7
32.447
DC 10MΩ
U3
8.900
DC 10MΩ
V1
120 V
60 Hz
0Deg
T1
5
D1
MDA2500
U2
LM7809CT
LINE VOLTAGE
VREG
COMMON
C1
6800µF-POL
C2
0.33µF-POL
R1
330Ω
R2
1KΩ_LIN
Key = A
0%
C3
0.1µF-POL
U7
32.453
DC 10MΩ
U3
30.027
DC 10MΩ
V1
120 V
60 Hz
0Deg
T1
5
D1
MDA2500
U2
LM7809CT
LINE VOLTAGE
VREG
COMMON
C1
6800µF-POL
C2
0.33µF-POL
R1
330Ω
R2
1KΩ_LIN
Key = A
76%
C3
0.1µF-POL

▲ FIGURE 17–42

Simulation of the regulated variable power supply circuit at the minimum and maximum specified output voltages.

Build and simulate the circuit using your Multisim software. Verify the operation.

Prototyping and Testing

Now that all the components have been selected and the circuit has been simulated, the circuit is breadboarded and tested.

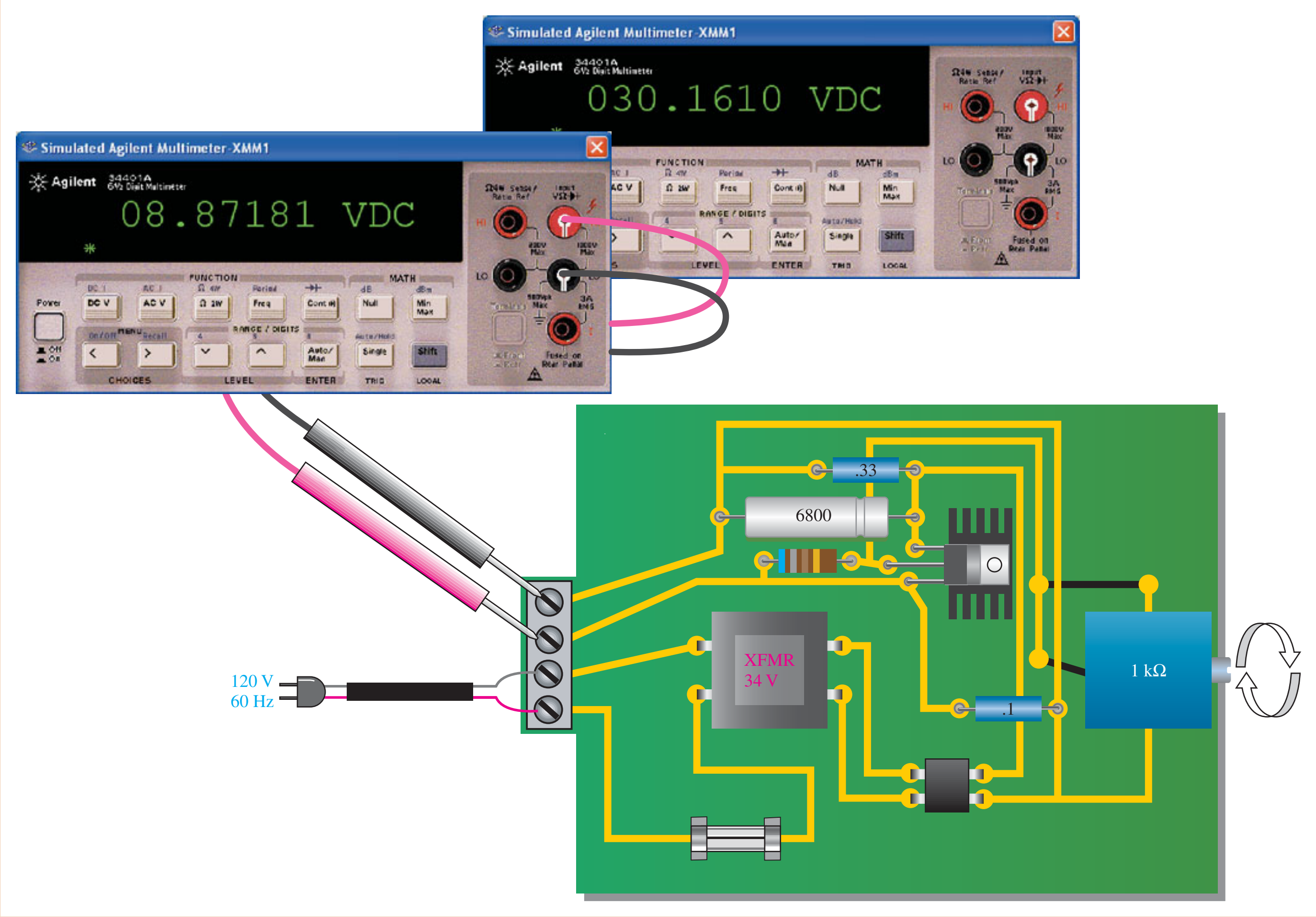
Lab Experiment

To build and test a similar circuit, go to Experiment 17 in your lab manual (*Laboratory Exercises for Electronic Devices* by David Buchla and Steven Wetterling).

Printed Circuit Board

The variable regulated power supply prototype has been built and tested. It is now committed to a printed circuit layout, as shown in Figure 17–43. Notice that a heat sink is used with the regulator IC to increase its ability to dissipate power. The output voltage is measured at the potentiometer.

6. Compare the printed circuit board to the schematic in Figure 17–40.
7. Calculate the power dissipated by the regulator for an output of 9 V and $I_L = 100$ mA.
8. Calculate the power dissipated by the regulator for an output of 30 V and $I_L = 100$ mA.


Simulated Agilent Multimeter-XMM1
Agilent 34401A 6½ Digit Multimeter
030.1610 VDC
Simulated Agilent Multimeter-XMM1
Agilent 34401A 6½ Digit Multimeter
08.87181 VDC
DC V
AC V
Ω 2W
Freq
Cont
Null
Min Max
Single
Shift
FUNCTION
MATH
RANGE / DIGITS
LEVEL
ENTER
CHOICES
Power
.33
6800
XFMR
34 V
.1
1 kΩ
120 V
60 Hz

▲ FIGURE 17–43

Regulated power supply PC board adjusted for output voltages that meet the minimum and maximum specifications.

SUMMARY

Section 17–1

- Voltage regulators keep a constant dc output voltage when the input or load varies within limits.
- Line regulation is the percentage change in the output voltage for a given change in the input voltage of a regulator.
- Load regulation is the percentage change in output voltage for a given change in load current.

Section 17–2

- A basic voltage regulator consists of a reference voltage source, an error detector, a sampling element, and a control device. Protection circuitry is also found in most regulators.
- Two basic categories of voltage regulators are linear and switching.
- Two basic types of linear regulators are series and shunt.
- In a linear series regulator, the control element is a transistor in series with the load.

Section 17–3

- In a linear shunt regulator, the control element is a transistor in parallel with the load.

Section 17–4

- Three configurations for switching regulators are step-down, step-up, and inverting.
- Switching regulators are more efficient than linear regulators and are particularly useful in low-voltage, high-current applications.

Section 17–5

- Three-terminal linear IC regulators are available for either fixed output or variable output voltages of positive or negative polarities.
- The 78XX series are three-terminal IC regulators with fixed positive output voltage.
- The 79XX series are three-terminal IC regulators with fixed negative output voltage.
- The LM317 is a three-terminal IC regulator with a positive variable output voltage.
- The LM337 is a three-terminal IC regulator with a negative variable output voltage.

Section 17–6

- An external pass transistor increases the current capability of a regulator.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Linear regulator A voltage regulator in which the control element operates in the linear region.

Line regulation The percentage change in output voltage for a given change in input (line) voltage.

Load regulation The percentage change in output voltage for a given change in load current from no load to full load.

Regulator An electronic circuit that maintains an essentially constant output voltage with a changing input voltage or load current.

Switching regulator A voltage regulator in which the control element operates as a switch.

Thermal overload A condition in a rectifier where the internal power dissipation of the circuit exceeds a certain maximum due to excessive current.

KEY FORMULAS

Voltage Regulation

17–1	$\textbf{Line regulation} = \left(\dfrac{\Delta V_{OUT}}{\Delta V_{IN}}\right)100\%$	Line regulation as a percentage
17–2	$\textbf{Line regulation} = \dfrac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}}$	Line regulation in %/V
17–3	$\textbf{Load regulation} = \left(\dfrac{V_{NL} - V_{FL}}{V_{FL}}\right)100\%$	Percent load regulation
17–4	$\textbf{Load regulation} = \left(\dfrac{R_{OUT}}{R_{FL}}\right)100\%$	Load regulation in terms of output resistance and full-load resistance

Basic Series Regulator

17–5 $V_{OUT} > \left(1 + \frac{R_2}{R_3}\right)V_{REF}$ Regulator output

17–6 $I_{L(max)} = \frac{0.7\text{ V}}{R_4}$ For constant-current limiting (silicon)

Basic Shunt Regulator

17–7 $I_{L(max)} = \frac{V_{IN}}{R_1}$ Maximum load current

Basic Switching Regulators

17–8 $V_{OUT} = \left(\frac{t_{on}}{T}\right)V_{IN}$ For step-down switching regulator

Integrated Circuit Voltage Regulators

17–9 $V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$ IC regulator

17–10 $R_{ext} = \frac{0.7\text{ V}}{I_{max}}$ For external pass circuit

17–11 $I_L = \frac{V_{OUT}}{R_1} + I_G$ Regulator as a current source

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. Line regulation is a measure of how constant the output voltage is for a given change in the input voltage.
2. Load regulation depends on the amount of power dissipated in the load.
3. Linear and switching are two main categories of voltage regulators.
4. Two types of linear regulator are series and bypass.
5. Three types of switching regulator are step-down, step-up, and inverting.
6. The three terminals of a 78XX series regulator are input, output, and control.
7. An external bypass transistor is sometimes used to increase the current capability of a regulator.
8. Current limiting is used to protect the external bypass transistor.
9. The purpose of a heat sink is to help the regulator dissipate excessive heat.
10. A variable pulse-width modulator is part of a linear voltage regulator.

CIRCUIT-ACTION QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. If the input voltage in Figure 17–7 is increased by 1 V, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

2. If the zener diode in Figure 17–7 is changed to one with a zener voltage of 6.8 V, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

3. If R_3 in Figure 17–7 is increased in value, the output voltage will

   (a) increase **(b)** decrease **(c)** not change

4. If R_4 in Figure 17–9 is reduced, the amount of current that the regulator can supply to the load will

   (a) increase **(b)** decrease **(c)** not change

5. If R_2 in Figure 17–15 is increased, the power dissipation in R_1 will

(a) increase **(b)** decrease **(c)** not change

6. If the duty cycle of the variable pulse-width modulator in Figure 17–17 is increased, the output voltage will

(a) increase **(b)** decrease **(c)** not change

7. If R_2 in Figure 17–30 is adjusted to a lower value, the output voltage will

(a) increase **(b)** decrease **(c)** not change

8. To increase the maximum current that the regulator in Figure 17–35 can supply, the value of R_{ext} must

(a) increase **(b)** decrease **(c)** not change

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 17–1

1. In the case of line regulation,

(a) when the temperature varies, the output voltage stays constant
(b) when the output voltage changes, the load current stays constant
(c) when the input voltage changes, the output voltage stays constant
(d) when the load changes, the output voltage stays constant

2. In the case of load regulation,

(a) when the temperature varies, the output voltage stays constant
(b) when the input voltage changes, the load current stays constant
(c) when the load changes, the load current stays constant
(d) when the load changes, the output voltage stays constant

3. All of the following are parts of a basic voltage regulator *except*

(a) control element **(b)** sampling circuit
(c) voltage-follower **(d)** error detector **(e)** reference voltage

Section 17–2

4. The basic difference between a series regulator and a shunt regulator is

(a) the amount of current that can be handled **(b)** the position of the control element
(c) the type of sample circuit **(d)** the type of error detector

5. In a basic series regulator, V_{OUT} is determined by

(a) the control element **(b)** the sample circuit
(c) the reference voltage **(d)** answers (b) and (c)

6. The main purpose of current limiting in a regulator is

(a) protection of the regulator from excessive current
(b) protection of the load from excessive current
(c) to keep the power supply transformer from burning up
(d) to maintain a constant output voltage

7. In a linear regulator, the control transistor is conducting

(a) a small part of the time **(b)** half the time
(c) all of the time **(d)** only when the load current is excessive

Section 17–3

8. In a basic shunt regulator, V_{OUT} is determined by

(a) the control element **(b)** the sample circuit
(c) the reference voltage **(d)** answers (b) and (c)

Section 17–4

9. In a switching regulator, the control transistor is conducting

(a) part of the time **(b)** all of the time
(c) only when the input voltage exceeds a set limit **(d)** only when there is an overload

Section 17–5

10. The LM317 is an example of an IC
- **(a)** three-terminal negative voltage regulator
- **(b)** fixed positive voltage regulator
- **(c)** switching regulator
- **(d)** linear regulator
- **(e)** variable positive voltage regulator
- **(f)** answers (b) and (d) only
- **(g)** answers (d) and (e) only

Section 17–6

11. An external pass transistor is used for
- **(a)** increasing the output voltage
- **(b)** improving the regulation
- **(c)** increasing the current that the regulator can handle
- **(d)** short-circuit protection

PROBLEMS

Answers to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

Section 17–1

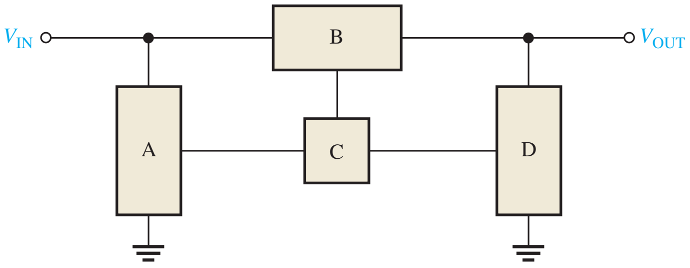
Voltage Regulation

1. The nominal output voltage of a certain regulator is 8 V. The output changes 2 mV when the input voltage goes from 12 V to 18 V. Determine the line regulation and express it as a percentage change over the entire range of V_{IN}.
2. Express the line regulation found in Problem 1 in units of %/V.
3. A certain regulator has a no-load output voltage of 10 V and a full-load output voltage of 9.90 V. What is the percent load regulation?
4. In Problem 3, if the full-load current is 250 mA, express the load regulation in %/mA.

Section 17–2

Basic Linear Series Regulators

5. Label the functional blocks for the voltage regulator in Figure 17–44.

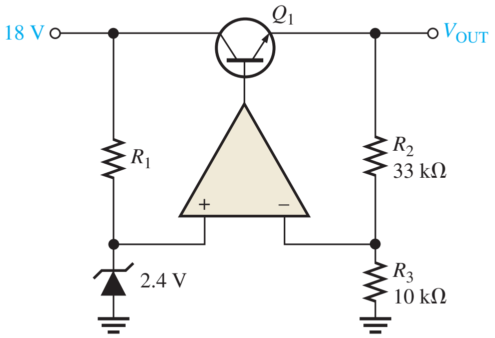


▶ FIGURE 17–44

6. Determine the output voltage for the regulator in Figure 17–45.

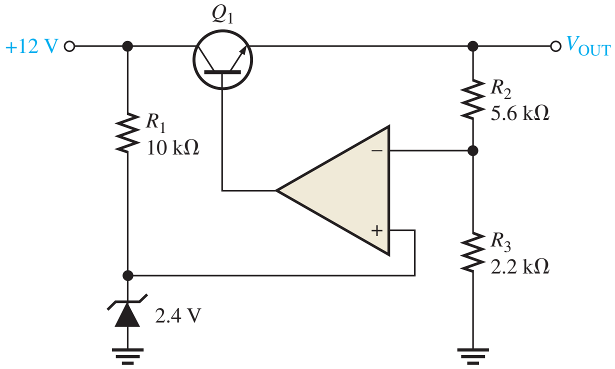
▶ FIGURE 17–45

Multisim file circuits are identified with a logo and are in the Problems folder on the companion website. Filenames correspond to figure numbers (e.g., F17–45).



7. Determine the output voltage for the series regulator in Figure 17–46.

FIGURE 17–46


Q_1
+12 V
V_{OUT}
R_2
5.6 kΩ
R_1
10 kΩ
–
+
R_3
2.2 kΩ
2.4 V

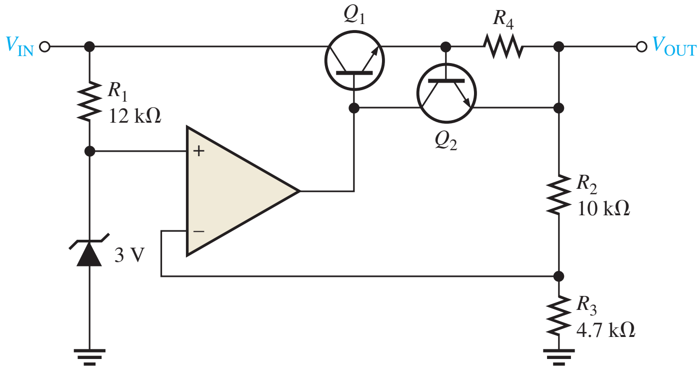
8. If R_3 in Figure 17–46 is increased to 4.7 kΩ, what happens to the output voltage?

9. If the zener voltage is 2.7 V instead of 2.4 V in Figure 17–46, what is the output voltage?

10. A series voltage regulator with constant-current limiting is shown in Figure 17–47. Determine the value of R_4 if the load current is to be limited to a maximum value of 250 mA. What power rating must R_4 have?

11. If the R_4 determined in Problem 10 is halved, what is the maximum load current?

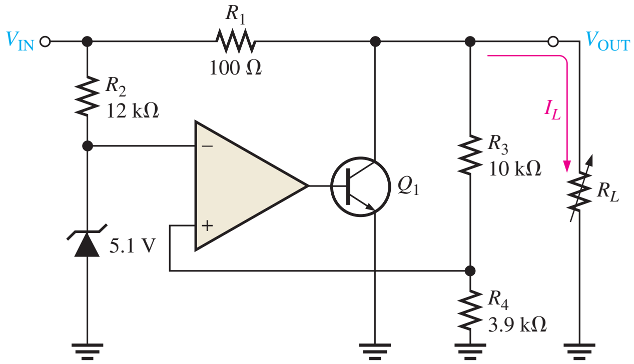
FIGURE 17–47


Q_1
R_4
V_{IN}
V_{OUT}
R_1
12 kΩ
Q_2
+
R_2
10 kΩ
–
3 V
R_3
4.7 kΩ

Section 17–3 Basic Linear Shunt Regulators

12. In the shunt regulator of Figure 17–48, when the load current increases, does Q_1 conduct more or less? Why?

FIGURE 17–48


R_1
V_{IN}
100 Ω
V_{OUT}
R_2
12 kΩ
I_L
–
R_3
10 kΩ
Q_1
R_L
+
5.1 V
R_4
3.9 kΩ

13. Assume I_L remains constant and V_{IN} changes by 1 V in Figure 17–48. What is the change in the collector current of Q_1?

14. With a constant input voltage of 17 V, the load resistance in Figure 17–48 is varied from 1 kΩ to 1.2 kΩ. Neglecting any change in output voltage, how much does the shunt current through Q_1 change?

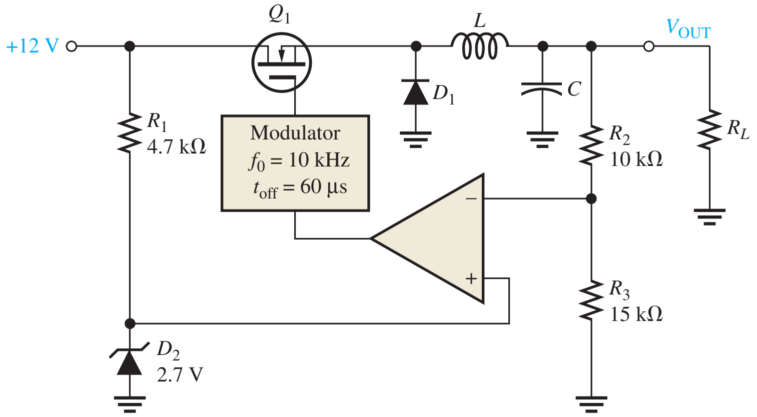
15. If the maximum allowable input voltage in Figure 17–48 is 25 V, what is the maximum possible output current when the output is short-circuited? What power rating should R_1 have?

Section 17–4

Basic Switching Regulators

16. A basic switching regulator is shown in Figure 17–49. If the switching frequency of the transistor is 10 kHz with an off-time of 60 μs, what is the output voltage?

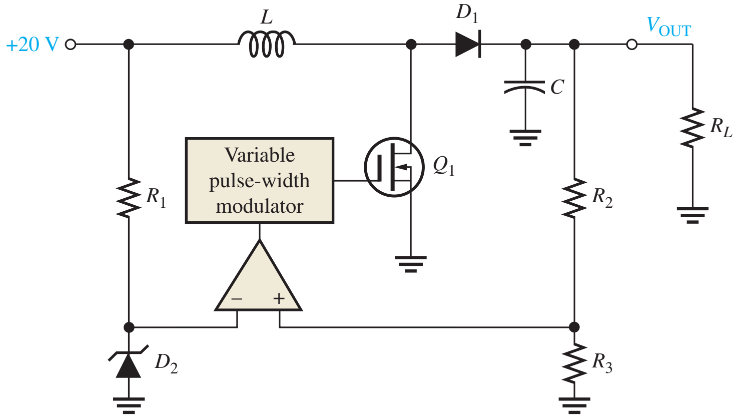
▶ FIGURE 17–49


+12 V
Q_1
L
V_{OUT}
D_1
C
R_1
4.7 kΩ
Modulator
f_0 = 10 kHz
t_{off} = 60 µs
R_2
10 kΩ
R_L
−
+
R_3
15 kΩ
D_2
2.7 V

17. What is the duty cycle of the transistor in Problem 16?

18. When does the diode D_1 in Figure 17–50 become forward-biased?

▶ FIGURE 17–50


+20 V
L
D_1
V_{OUT}
C
R_L
Variable
pulse-width
modulator
Q_1
R_1
R_2
−
+
D_2
R_3

19. If the on-time of Q_1 in Figure 17–50 is decreased, does the output voltage increase or decrease?

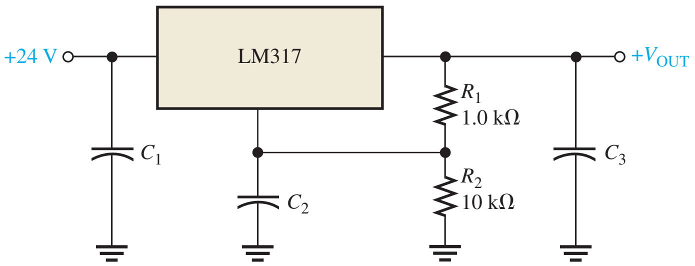
Section 17–5

Integrated Circuit Voltage Regulators

20. What is the output voltage of each of the following IC regulators?
    (a) 7806 **(b)** 7905.2 **(c)** 7818 **(d)** 7924

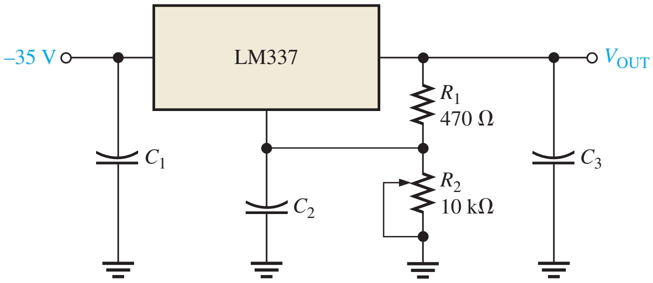
21. Determine the output voltage of the regulator in Figure 17–51. $I_{ADJ} = 50\ \mu A$.

FIGURE 17–51



22. Determine the minimum and maximum output voltages for the circuit in Figure 17–52. $I_{ADJ} = 50\ \mu A$.

FIGURE 17–52



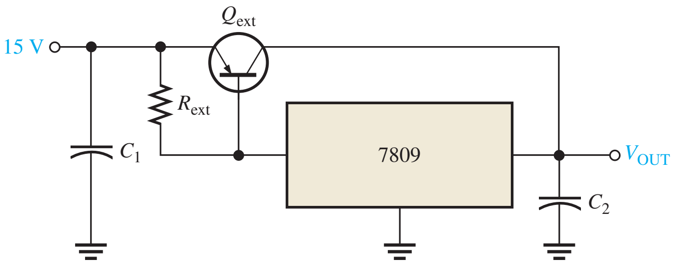
23. With no load connected, how much current is there through the regulator in Figure 17–51? Neglect the adjustment terminal current.

24. Select the values for the external resistors to be used in an LM317 circuit that is required to produce an output voltage of 12 V with an input of 18 V. The maximum regulator current with no load is to be 2 mA. There is no external pass transistor.

Section 17–6 Integrated Circuit Voltage Regulator Configurations

25. In the regulator circuit of Figure 17–53, determine R_{ext} if the maximum internal regulator current is to be 250 mA.

FIGURE 17–53



26. Using a 7812 voltage regulator and a 10 Ω load in Figure 17–53, how much power will the external pass transistor have to dissipate? The maximum internal regulator current is set at 500 mA by R_{ext}.

27. Show how to include current limiting in the circuit of Figure 17–53. What should the value of the limiting resistor be if the external current is to be limited to 2 A?

28. Using an LM317, design a circuit that will provide a constant current of 500 mA to a load.

29. Repeat Problem 28 using a 7908.

30. How do you set up the ADP1612/1613 switching regulator for a switching frequency of 1.3 MHz?

MULTISIM TROUBLESHOOTING PROBLEMS

These file circuits are in the Troubleshooting Problems folder on the companion website.

31. Open file TSP17-31 and determine the fault.

32. Open file TSP17-32 and determine the fault.

33. Open file TSP17-33 and determine the fault.

34. Open file TSP17-34 and determine the fault.

18 BASIC PROGRAMMING CONCEPTS FOR AUTOMATED TESTING

CHAPTER OUTLINE

18–1 Programming Basics
18–2 Automated Testing Basics
18–3 The Simple Sequential Program
18–4 Conditional Execution
18–5 Program Loops
18–6 Branching and Subroutines

CHAPTER OBJECTIVES

- Discuss fundamental concepts of programming
- Discuss fundamental concepts of automated testing
- Describe and discuss a simple sequential program
- Discuss and apply the concept of conditional execution
- Discuss and apply the concept of programming loops
- Discuss and apply the concepts of branching and subroutines

KEY TERMS

- Program
- Programming language
- Instruction set
- Flowchart
- Pseudocode
- Automated test system
- Test controller
- Test fixture
- Unit under test (UUT)
- Sequential program
- Conditional execution
- Nesting
- Program loop
- Branching
- Subroutine

VISIT THE COMPANION WEBSITE

Study aids for this chapter are available at
http://www.pearsonhighered.com/electronics

LABVIEW

An overview of National Instrument's LabVIEW is available on the companion website as an optional feature. LabVIEW software is a **visual programming** environment that allows you to create and use virtual instruments (VIs) in applications that can generate, acquire, process, analyze, display, and store signal data. These LabVIEW applications can interface with National Instruments' TestStand software for automated test applications.

INTRODUCTION

For many years there was little common ground between electronics and programming. Now programmable handheld calculators and personal computers are standard tools for designing and simulating circuits. Computer technology is deeply integrated with manufacturing, validating, and troubleshooting hardware. Some common computer-controlled and automated processes include device characterization, parts placement, in-circuit testing, and board level functional testing.

Computers cannot operate until they are told what to do. The list of instructions that tell the computer what to do is called a **program**, and writing these instructions is called **programming**. Although the subject of programming is too broad to cover completely, this chapter will discuss basic programming concepts, using basic automated testing examples to illustrate these concepts.

18–1 PROGRAMMING BASICS

All programming consists of specifying the instructions for a processor to accomplish some specific task. The set of programming language instructions can be divided into basic instruction types. Programmers use tools, such as flowcharts and pseudocode, to define the tasks and structure of the final program.

After completing this section, you should be able to

- ❑ **Discuss fundamental concepts of programming**
- ❑ Discuss programming languages and instructions
  - ◆ Define *programming language* and *instruction set*
  - ◆ Describe the basic difference between machine language and high-level languages like Visual Basic and C++
  - ◆ Identify and describe the five basic instruction types
- ❑ Describe a flowchart and discuss its advantages and disadvantages
- ❑ Describe pseudocode and discuss its advantages and disadvantages

Programming Languages and Instructions

The instructions that a computer can process make up a **programming language**. Microprocessors use a device-specific **instruction set**, which consists of all the binary machine language instructions that the microprocessor hardware can directly decode and execute. **Assembly language** uses English-like mnemonics, like MOV and JMP, to replace the groups of 0s and 1s that make up **machine language** instructions. Mnemonics are easier for humans to use than machine language, but they still work directly with the processor hardware. Programs, called *assemblers*, convert assembly language into machine language. Assemblers also allow programmers to use programming features that simplify programming. Programmers typically use assembly or machine language only when the program requires extremely compact, efficient code.

Most programming uses high-level general-purpose programming languages, which are easier for people to understand and use than machine or assembly language. Each high-level language instruction can represent many machine language instructions. There are many general-purpose programming languages, such as C++, that programmers can use to develop applications for many different **platforms** (types of computers and operating systems). There are also many proprietary programming languages that manufacturers develop for their own products. An advantage of proprietary languages is that they simplify accessing the features for a product. A disadvantage is that programmers must learn a new language whenever they use a new manufacturer's product.

Despite the variety of programming languages, all programming languages consist of specific types of instructions. There are five basic instruction types.

1. ***Simple instructions.*** These instructions perform a basic task, such as adding two numbers, and then sequence to the next instruction in the program.
2. ***Conditional instructions.*** These instructions evaluate specific conditions, such as whether a number is zero, to determine how program execution should proceed.
3. ***Looping instructions.*** These instructions allow a set of instructions in the program to execute more than once.
4. ***Branching instructions.*** These instructions change the sequence of program execution.

5. ***Exception instructions.*** These instructions execute when unexpected circumstances, or exceptions, arise during program execution. Exceptions can arise due to hardware or software. Exception instructions are rarely used in application programming and will not be discussed.

Some programming languages contain instructions that merge basic instruction types that often occur together, such as conditional and other instruction types.

Programs organize instructions so that the computer can achieve a specific objective. The first step to writing a program is to clearly define the tasks the computer must perform and the sequence in which the computer must perform them. Two common ways of doing this are the flowchart and pseudocode.

Flowcharts

A **flowchart** uses distinctively shaped blocks, or symbols, to graphically represent each task, the nature of each task, and how each task relates to other tasks in the program. Figure 18–1 shows some common flowchart symbols.

▶ FIGURE 18–1

Common flowchart symbols.

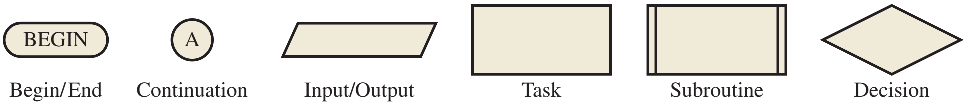
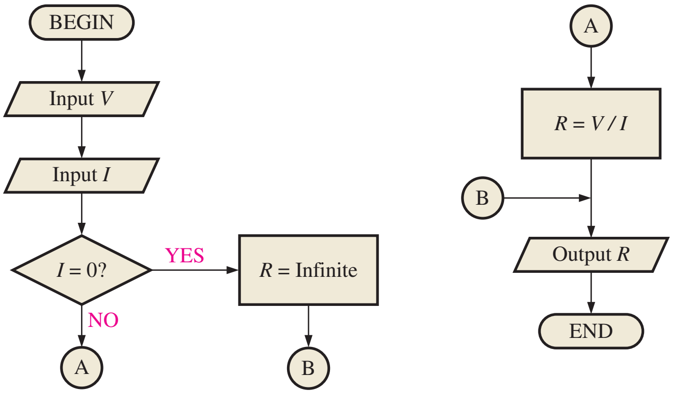


Figure 18–2 shows an example flowchart for determining the resistance, R, from the voltage, V, and current, I. As the flowchart shows, the program begins and inputs the voltage value, V, and the current value, I. It next determines whether I is zero. If $I = 0$, it assigns an infinite value to R, outputs R, and ends. If $I \neq 0$, the program calculates the value of R from Ohm's law, outputs R, and ends.

▶ FIGURE 18–2

Sample flowchart.



For smaller programs, the flowcharts are relatively easy to follow because they graphically represent the flow of the process. Although flowcharts for large programs can be quite large, these large flowcharts can use a **hierarchical structure**. This sort of structure first represents the program with a small number of very general tasks. These tasks are then broken down into smaller units that represent a small number of still-general but more specific tasks. This process continues until it breaks down the program into very specific, manageable tasks that the programmer can then use to write the code.

A potential disadvantage of flowcharting is that the **process flow** is not always the best way to represent some programs. In some cases, how parts of a program interact is more important. This is usually the case with **object-oriented programming**, in which programming entities called **objects** interact with each other to accomplish some objective.

Pseudocode

Pseudocode is similar to actual programming except that pseudocode uses generic descriptions rather than specific instructions. The pseudocode for the flowchart in Figure 18–2 might read as follows:

```
procedure CalculateResistance
   begin
      input voltage value
      input current value
      if (current value is 0) then
         begin if
            resistance value is infinite
         end if
      else
         begin else
            resistance value is voltage value divided by current value
         end else
      output resistance value
   end CalculateResistance
```

Pseudocode can also have a hierarchical structure. The pseudocode for a large program can consist of a relatively small number of very general procedures, each of which can consist of a relatively small number of still-general but more specific procedures. This process continues until the pseudocode is specific enough for the programmer to write the code to implement the procedure.

An advantage of pseudocode is that it provides a high level of structure, which provides an excellent view of the final program structure. This helps reviewers to identify and correct potential errors before the program is actually written, potentially reducing the time to deliver the program. Because pseudocode is textual, it can usually be written and modified quicker than a flowchart can be drawn and modified. Pseudocode can also be incorporated in the headers for the final program **source code**.

A disadvantage of pseudocode is that following the overall process flow of a program is more difficult than with a flowchart. Another disadvantage is that changes to the final code often require changes to the pseudocode that more closely describe the code. This often creates inconsistencies between the pseudocode, which represents the program code, and the actual program code, which contains the specific instructions that the computer is to execute.

SECTION 18–1 CHECKUP

Answers can be found at www.pearsonhighered.com/floyd.

1. What are the five basic instruction types?
2. What are two methods of defining the tasks and sequence of tasks that a computer must perform?
3. How could you modify the flowchart of Figure 18–2 to calculate the current from voltage and resistance rather than the resistance from voltage and current?
4. What is an advantage of using pseudocode compared to using a flowchart?

18–2 AUTOMATED TESTING BASICS

Automated testing includes both a software component that coordinates and executes the testing operations and a hardware component that executes the test code and interfaces with the unit under test. This section looks at the components of a basic automated test system and some practical aspects of automated testing and test systems.

After completing this section, you should be able to

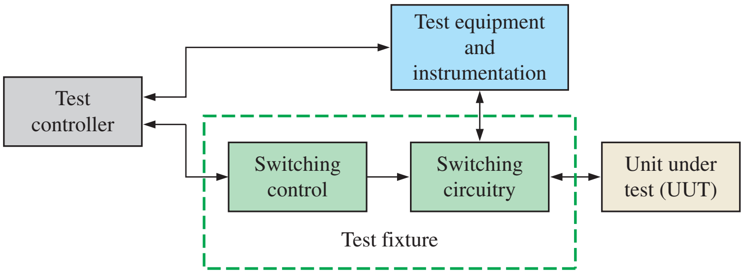
- ❑ **Discuss fundamental concepts of automated testing**
- ❑ Describe a basic automated test system
  - ◆ Identify the system components
  - ◆ Describe the purpose of each component
- ❑ Discuss the test fixture
  - ◆ Describe how current is measured
- ❑ Discuss a sample automated test system
  - ◆ Describe testing a diode with the system
- ❑ Discuss practical considerations of automated testing

A Basic Automated Test System

Figure 18–3 shows the components that make up a basic **automated test system**.

▶ **FIGURE 18–3**

A basic automated test system.



The **test controller** executes the test code that operates the test system. The test controller can be a PC running proprietary company code, a workstation running commercial test software, or a dedicated component of a commercial automated test system. The test controller communicates with the **test equipment**, **test instrumentation**, and test fixture over system buses. These buses can be proprietary or adhere to an industry standard. The test equipment, test instrumentation, and test fixture can use the same or different buses to communicate with the test controller.

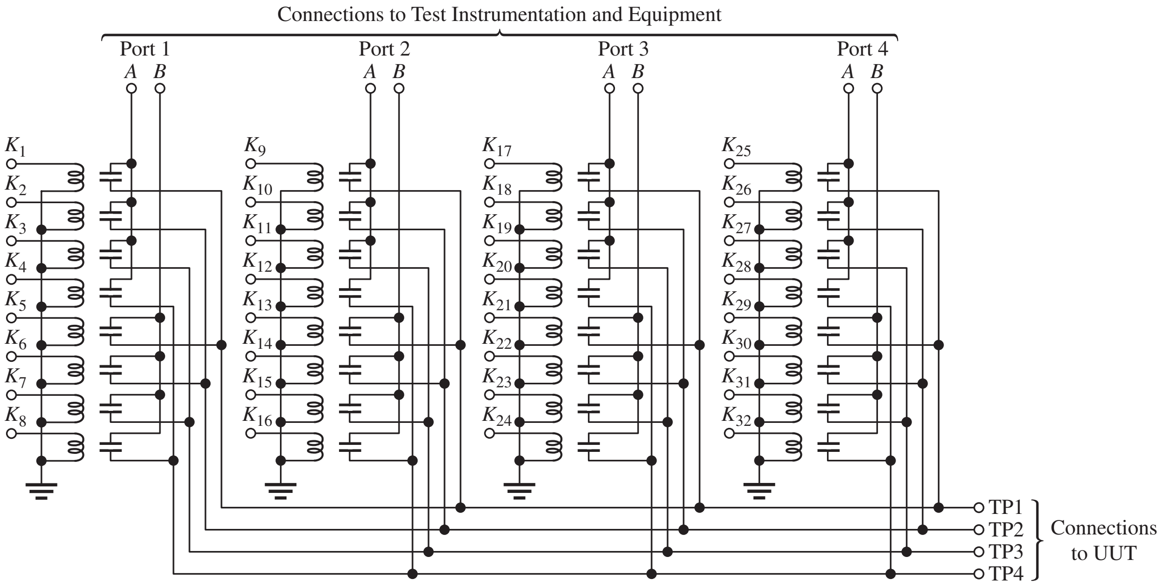
The test equipment and test instrumentation provide power and test signals to the unit under test and measure the operating characteristics of the unit under test.

The **test fixture** connects the automated test system to the **unit under test (UUT)**. The test controller interfaces with the switching control, which in turn controls the switching circuit. The switching circuit connects the test equipment and test instrumentation to specific locations, called *test points*, on the unit under test.

The UUT can be a single component, a circuit board, or a complete electronics assembly. Companies often standardize the interface between the text fixture and UUT. Designers must ensure that their finished product designs adhere to these standards. As circuits have become more complex, organizations such as the Joint Test Association Group (JTAG) have developed and established industry standards so that manufacturers can develop and use standardized test tools and procedures.

The Test Fixture

As Figure 18–3 shows, the test controller connects to the switching control. The switching control interprets instructions from the test controller to configure the switching circuitry, which connects the test equipment and test instrumentation to specific test points on the UUT. Figure 18–4 shows an example of a switching circuit that uses relays.


Connections to Test Instrumentation and Equipment
Port 1
A B
Port 2
A B
Port 3
A B
Port 4
A B
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
K16
K17
K18
K19
K20
K21
K22
K23
K24
K25
K26
K27
K28
K29
K30
K31
K32
TP1
TP2
TP3
TP4
Connections to UUT

▲ **FIGURE 18–4**

Example test fixture switching circuit.

The switching circuit in Figure 18–4 uses 32 relays to connect four two-terminal ports to four test point (TP) terminals. The switching controller applies a voltage to the coil terminal of one of the relays to close the contacts for that relay. This connects a test instrument or equipment lead through a port terminal to one of the test points on the unit under test through a test terminal.

EXAMPLE 18–1

For Figure 18–4, what coil terminals must the switching control energize to connect terminal *A* of Port 3 to the TP2 terminal and terminal *B* of Port 3 to the TP3 terminal?

Solution

Terminal *A* of Port 3 connects to the TP2 terminal through the contacts of relay K_{18}, and terminal *B* of Port 3 connects to the TP3 terminal through the contacts of relay K_{23}. The switching control must energize the coils of relays K_{18} and K_{23}.

*Related Problem**

When you connect an ohmmeter between the port and test point terminals in Figure 18–4, you find a short between terminal *B* of Port 1 and the terminal for TP4. Assuming there is no fault, which relay is energized?

***Answers can be found at www.pearsonhighered.com/floyd.**

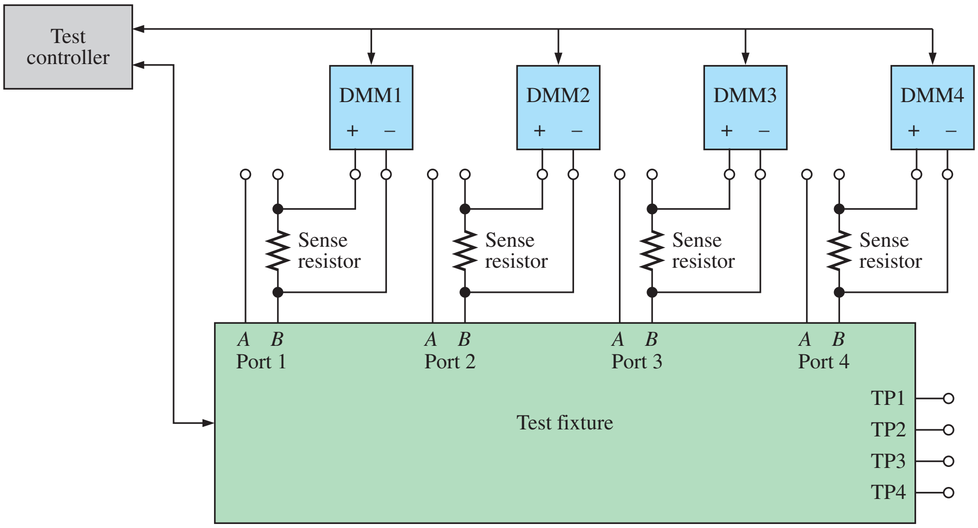
The switching circuit in Figure 18–4 requires 32 relays to connect any of the eight port terminals to any test point terminal. Some test systems have hundreds of test points and can require a large number of relays. Connecting specific port terminals to specific test point terminals reduces the cost and complexity of the test system, but it also reduces its flexibility.

Although the switching circuit in Figure 18–4 uses electromechanical relays, some fixtures use other devices, such as silicon-controlled switches or solid-state relays. Electromechanical relays offer good electrical isolation and can handle high currents and voltages, but there are potential issues that can affect their operation and reliability.

Measuring Current

The fixture in Figure 18–4 connects instruments and equipment on the two-terminal ports in parallel with circuitry connected across sets of test points. This works well for voltage and resistance measurements, but not for current measurements. There are several ways for the test system to measure current.

- Use power supplies that can measure the supply current. This works well if the measurement is accurate enough for the test application.
- Measure the voltage across a resistor in series with the component of interest and use Ohm's law to calculate the current. A drawback is that the designer must add a sense resistor just for testing if the circuit does not already have one.
- Add additional switching circuitry to support current measurements on the port and test point terminals. This increases the complexity of the test system.
- Add an external sense resistor and dedicated voltmeter to one terminal of each two-terminal port, as shown in Figure 18–5. This increases the expense of the test system. Restricting current measurements to one port can minimize this, but it will reduce the flexibility of the system. Another disadvantage is that the test system must compensate for the voltage drop across the resistor to apply the correct voltage to the unit under test.



▲ FIGURE 18–5

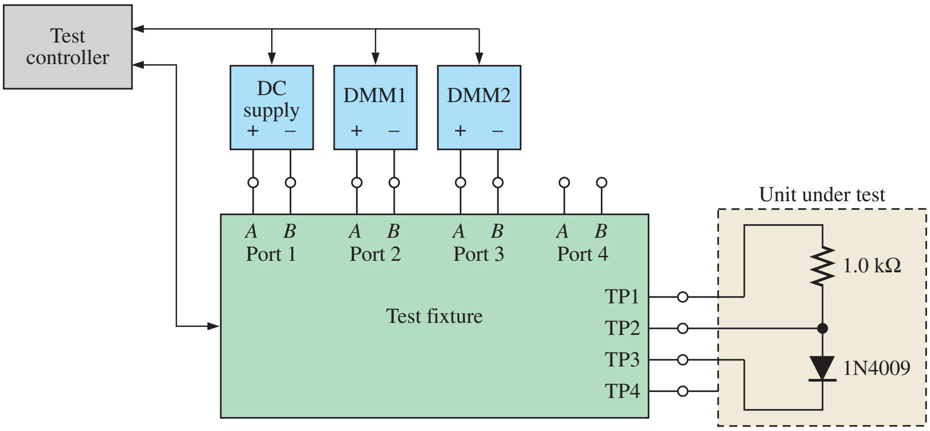
Current measurements with an external sense resistor.

A Sample Automated Test System

Figure 18–6 shows one example of an automated test system based on the switching circuit in Figure 18–4. As you can see, the system connects a dc power supply to the terminals of Port 1 and digital multimeters (DMMs) to the terminals of Ports 2 and 3. The UUT consists of a 1.0 kΩ resistor and a 1N4009 diode in series.

The automated test system verifies that the diode is functioning correctly by forward-biasing the diode and measuring the diode voltage and current. To do so, the test controller in the automated test system performs the following operations:

1. Sets the dc supply to +5 V_{DC}
2. Sets DMM1 and DMM2 for dc voltmeter function
3. Connects the positive and negative terminals of the dc supply to test point terminals TP1 and TP3, respectively



◀ **FIGURE 18–6**

A sample automated test system.

4. Connects the positive and negative terminals of DMM1 to test point terminals TP1 and TP2, respectively
5. Connects the positive and negative terminals of DMM2 to test point terminals TP2 and TP3, respectively
6. Activates the dc supply outputs
7. Measures the resistor voltage on DMM1
8. Measures the diode voltage on DMM2
9. Calculates the diode current from the resistor voltage and resistor value

EXAMPLE 18–2

For the test system in Figure 18–6, which relays must be energized to connect the dc voltage supply and DMMs to the diode test circuit? Assume that the test fixture uses the switching circuitry in Figure 18–4.

Solution The positive and negative terminals of the dc supply connect to terminals *A* and *B* of Port 1, respectively. To connect the dc supply as described in the test procedure, the test controller must energize the coils of relays K_1 and K_7.

The positive and negative terminals of DMM1 connect to terminals *A* and *B* of Port 2, respectively. To connect DMM1 as described in the test procedure, the test controller must energize the coils of relays K_9 and K_{14}.

The positive and negative terminals of DMM2 connect to terminals *A* and *B* of Port 3, respectively. To connect DMM2 as described in the test procedure, the test controller must energize the coils of relays K_{18} and K_{23}.

Related Problem How could the relay configuration in Example 18–2 be modified to reverse-bias the diode?

EXAMPLE 18–3

Suppose the value of the resistor in Figure 18–6 is not known. How could the test controller determine the value of the resistor?

Solution The test controller in the automated test system can use DMM1 to measure the resistance of resistor. To do so, it performs the following operations:

1. Sets DMM1 for ohmmeter function
2. Connects the positive and negative terminals of DMM1 to test point terminals TP1 and TP2, respectively
3. Measures the resistance value on DMM1

Related Problem What are two advantages of measuring the actual resistor value, rather than assuming a value of 1.0 kΩ to calculate the diode current?

Some Practical Considerations

The discussion of the sample automated test system assumes an ideal system. Practical test systems must compensate for limitations and conditions that exist in the systems.

One practical consideration is that the test system must always begin in a known state that will not accidentally damage the test system or UUT. The test controller should deactivate voltage and signal sources until it can properly configure the system for the UUT. The test controller should also disconnect all sources while adjusting their settings. Voltage supplies should have current-limited outputs, and the test controller should adjust the supply limits to suitable levels for the test.

A general limitation is that all circuits contain some amount of inductance and capacitance so that practical systems do not react instantaneously. Equipment and instruments have some settling time, and each circuit requires some time to reaches its final, or steady-state, condition. Test controllers must introduce delays to ensure that the test system and UUT are stable. It is not always possible to predict these delays, so appropriate delays may require trial and error.

Another limitation is that test systems are as subject to failures as the units they test. Diagnostics and self-tests can ensure that the test system is functioning properly. Tests can use known good and bad boards to ensure that the system will not indicate a fault when none exists (false negative) or indicate that there is no fault when a fault exists (false positive).

SECTION 18–2 CHECKUP

1. What four components make up a basic automated test system?
2. What is the purpose of the test controller in an automated test system?
3. Which component in an automated test system connects the test equipment and instrumentation to the unit under test?
4. What is the purpose of introducing delays in an automated test system?

18–3 THE SIMPLE SEQUENTIAL PROGRAM

The simple **sequential program** begins, executes a series of instructions in sequence, and then terminates. Many consumer products, such as microwave ovens, video recorders, and sprinkler systems support this sort of programming. The user specifies the sequence of tasks the product is to perform, and the product performs the specified tasks.

After completing this section, you should be able to

- **Describe and discuss a simple sequential program**
- Draw a flowchart showing the structure for a simple sequential program
- Describe the characteristics of a basic program
- Write pseudocode showing the sequence of instructions for a basic program

Simple Sequential Program Structure

Figure 18–7 shows the sequence of instruction execution, or process flow, for this type of program. Note that the instructions can be any instructions that do not alter the sequence of program execution.

The simple sequential program shown has limited applications, but the linear structure of its process flow is common to many sections of code in complex programs. Large programs often use **subroutines** to perform this type of task. (You will learn more about subroutines later in this chapter.) The following two examples show some simple sequential programs.

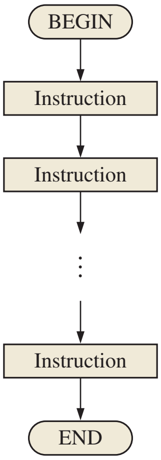


FIGURE 18–7

Flowchart for a simple sequential program.

EXAMPLE 18–4 Write the pseudocode description for a program to calculate the value of power dissipated by a load resistor from the measured voltage and current values.

Solution One possible pseudocode description is

```
program CalculatePower
   begin
      input voltage value
      input current value
      power value is voltage value times current value
      output power value
   end CalculatePower
```

Related Problem Modify the pseudocode for Example 18–4 to calculate the values of power dissipated by the load resistor from the measured current and resistance values.

EXAMPLE 18–5 Write the pseudocode description for a program to calculate the minimum value for a resistor from its nominal value and tolerance.

Solution One possible pseudocode description is

```
program CalculateMinimumValue
   begin
      input resistance value
      input tolerance value
      deviation value is resistance value times tolerance value
      minimum value is resistance value minus deviation value
      output minimum value
   end CalculateMinimumValue
```

Related Problem Modify the pseudocode for Example 18–5 to calculate the maximum value for a resistor from its nominal value and tolerance.

SECTION 18–3 CHECKUP

1. What are some applications of simple sequential programs?
2. What instructions can a simple sequential program contain?
3. What is a subroutine?

18–4 CONDITIONAL EXECUTION

The simple sequential program is limited because it assumes that the conditions for the program will never change and cannot deviate from its specified process flow. Conditional execution greatly increases the power and usefulness of programs. **Conditional execution** allows the program to test for specific conditions and determine which instructions, if any, to execute.

After completing this section, you should be able to

- ❑ **Discuss and apply the concept of conditional execution**
- ❑ Describe the IF-THEN-ELSE instruction
  ◆ Draw a flowchart for the IF-THEN-ELSE instruction ◆ Write pseudocode using IF-THEN-ELSE and IF-THEN instructions ◆ Define *nesting*
- ❑ Describe the CASE instruction
  ◆ Draw a flowchart for the CASE instruction ◆ Write pseudocode using the CASE instruction

Flowcharts that represent conditional execution use the decision block. The decision block indicates the test condition and the series of instructions the program is to follow based on the test result. Program decisions ultimately always have two possible outcomes, so programs must use tests and decisions that will always generate a "TRUE/FALSE" or "YES/NO" answer. For example, a program cannot directly implement the test "What is the temperature?". The program must instead measure the temperature and then test the measured value against specific values (i.e., "Is the temperature greater than 0° C?").

Programs use two basic types of conditional execution: the IF-THEN-ELSE instruction and the CASE instruction.

The IF-THEN-ELSE Instruction

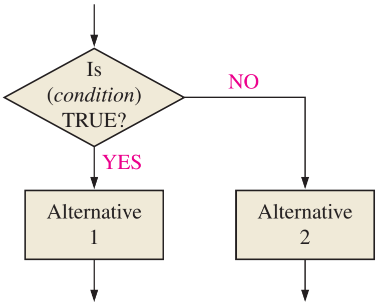
The IF-THEN-ELSE instruction implements the most basic form of conditional execution. If the result of the test is TRUE, then the program will execute one set of instructions. If the result is FALSE, the program will execute an alternate set of instructions. The basic pseudocode for the IF-THEN-ELSE instruction is

```
if (condition) then
   begin if
      alternative 1
   end if
else
   begin else
      alternative 2
   end else
```

Figure 18–8 shows the flowchart for the IF-THEN-ELSE instruction.

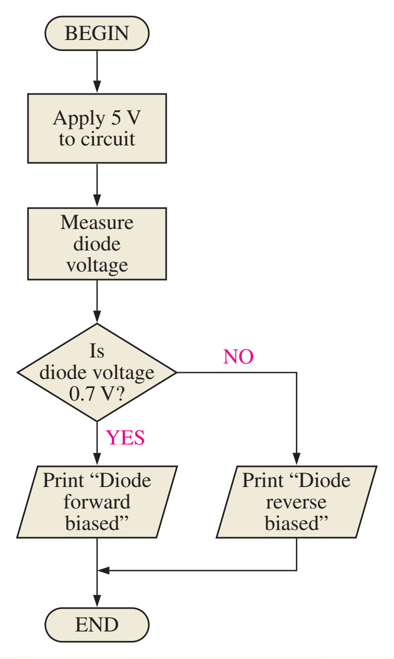
▶ FIGURE 18–8

IF-THEN-ELSE flowchart.



EXAMPLE 18–6 Draw the flowchart for a program that applies 5 V_{DC} to a diode circuit, measures the voltage drop across a diode, and prints "Diode forward biased" if the voltage is 0.7 V and "Diode reverse biased" otherwise.

Solution Figure 18–9 shows the flowchart for the program.


BEGIN
Apply 5 V to circuit
Measure diode voltage
Is diode voltage 0.7 V?
NO
YES
Print "Diode forward biased"
Print "Diode reverse biased"
END

▲ FIGURE 18–9

Flowchart for IF-THEN program.

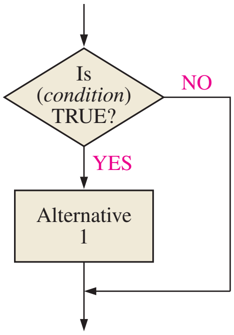
Related Problem Write the pseudocode description that corresponds to the flowchart in Figure 18–9.

A special form of the IF-THEN-ELSE instruction is the IF-THEN instruction, for which the ELSE portion of the instruction does nothing. The basic pseudocode for the IF-THEN instruction is

```
if (condition) then
    begin if
        alternative 1
    end if
else
    begin else
        NULL
    end else
```

This can also be reduced to

```
if (condition) then
    begin if
        alternative 1
    end if
```


Is (condition) TRUE?
NO
YES
Alternative 1

▲ FIGURE 18–10

IF-THEN flowchart.

Figure 18–10 shows the flowchart for the IF-THEN instruction.

Although the IF-THEN-ELSE instruction appears to be limited because it offers only two alternatives, either or both of those alternatives can be IF-THEN-ELSE instructions.

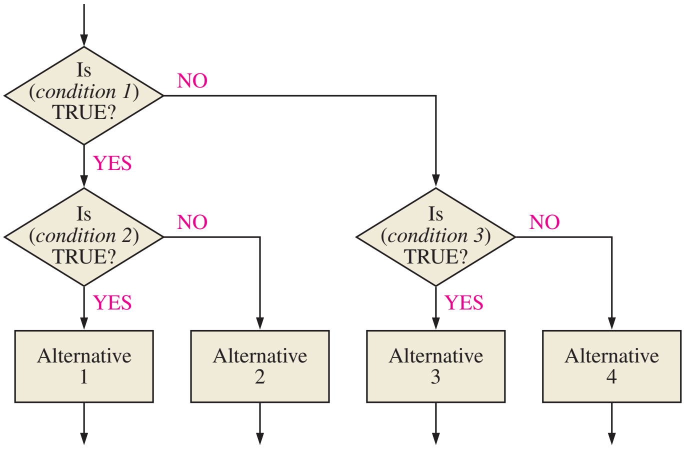
Using the same type of instruction for the subparts of an instruction is called **nesting**. The pseudocode for a typical nested IF-THEN-ELSE instruction is

```
if (condition 1) then
   begin if
      if (condition 2) then
         begin if
            alternative 1
         end if
      else
         begin else
            alternative 2
         end else
   end if
else
   begin else
      if (condition 3) then
         begin if
            alternative 3
         end if
      else
         begin else
            alternative 4
         end else
end else
```

Figure 18–11 shows the flowchart for the nested IF-THEN_ELSE instruction. By nesting IF-THEN-ELSE statements, you can write a program that will execute any number of alternatives.

FIGURE 18–11

Nested IF-THEN-ELSE flowchart.


Is (condition 1) TRUE?
NO
YES
Is (condition 2) TRUE?
NO
YES
Is (condition 3) TRUE?
NO
YES
Alternative 1
Alternative 2
Alternative 3
Alternative 4

EXAMPLE 18–7

Write the pseudocode description for a program that applies 5 V to a diode circuit, measures the diode voltage, and prints “Diode forward biased” if the measured voltage is less than 1 V, “Diode reverse biased” if the measured voltage is greater than 4.5 V, and “Diode bad” for any other measured voltage.

Solution One possible pseudocode description for the program is

```
program NewDiodeCheck
   begin
      apply 5 V to circuit
      measure diode voltage
```

```
          if (diode voltage is less than 1 V) then
             begin if
                print "Diode forward biased"
             end if
          else
             begin else
                if (diode voltage is greater than 4.5 V) then
                   begin if
                      print "Diode reverse biased"
                   end if
                else
                   begin else
                      print "Diode bad"
                   end else
             end else
       end NewDiodeCheck
```

Related Problem How could you use nesting so that the program prints "Diode shorted" if the measured voltage is 0 V and "Diode open" if the measured voltage is 5.0 V?

The CASE Instruction

The CASE instruction is a special type of nested IF-THEN-ELSE instruction that compares a program value against a set of specific values to select a course of action. The flowchart in Figure 18–12 shows the operation of the CASE instruction. Note that the instructions for any case, or even the default action, can be to do nothing.

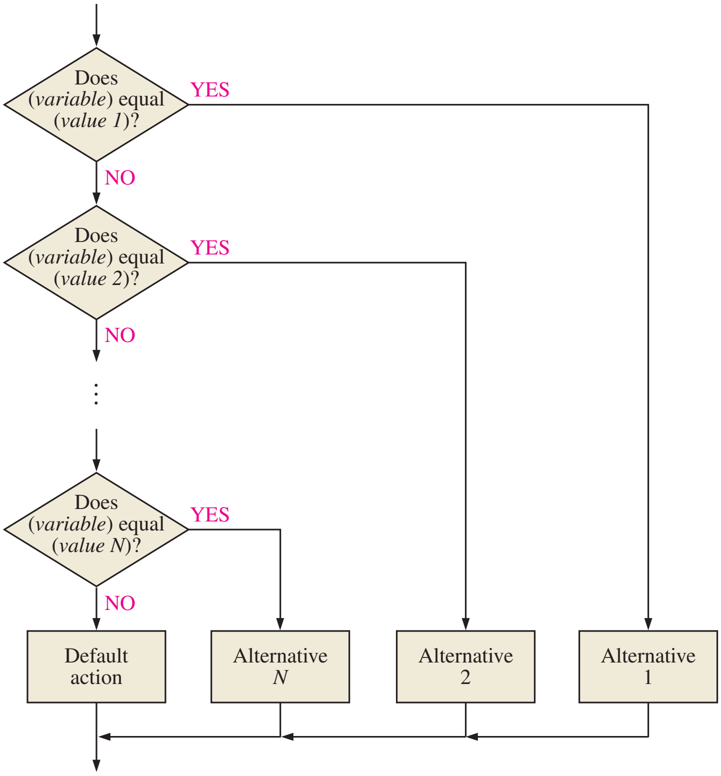

Does (*variable*) equal (*value 1*)?
YES
NO
Does (*variable*) equal (*value 2*)?
YES
NO
Does (*variable*) equal (*value N*)?
YES
NO
Default action
Alternative *N*
Alternative 2
Alternative 1

FIGURE 18–12

CASE instruction operation.

EXAMPLE 18–8

Use the CASE instruction to write the pseudocode description for a program that applies 5 V to a diode circuit, measures the diode voltage, and prints “Diode forward biased” if the measured voltage is 0.7 V, “Diode reverse biased” if the measured voltage is 4.5 V, and “Diode bad” for any other measured voltage.

Solution One possible pseudocode description for the program is

```
program CaseDiodeCheck
   begin
      apply 5 V to circuit
      measure diode voltage
      case (diode voltage)
         begin case
               0.7 V:    print "Diode forward biased"
                         break
               4.5 V:    print "Diode reverse biased"
                         break
               default:  print "Diode bad"
                         break
         end case
   end CaseDiodeCheck
```

Note the break statement at the end of the instructions for each case. The break statement causes the program to exit the CASE instruction.

Related Problem Modify the pseudocode for Example 18–8 so that if the diode voltage equals 0 V the program prints “Diode shorted” and if the diode voltage equals 5 V the program prints “Diode open”. What will the program print if the measured diode voltage is 2.5 V?

The CASE instruction determines whether or not a variable equals specific values, rather than whether a condition is TRUE or FALSE as in an IF-THEN-ELSE statement. IF-THEN-ELSE instructions can test “greater than” and “less than” as well as “equal to” or “not equal to” conditions. You can use IF-THEN-ELSE instructions to overcome this limitation with the CASE instruction.

EXAMPLE 18–9

Use IF-THEN-ELSE and CASE instructions to write the pseudocode description for a program that applies 5 V to a diode circuit, measures the diode voltage, and prints “Diode forward biased” if the measured voltage is less than 1.0 V, “Diode reverse biased” if the measured voltage is between 1.0 V and 4.5 V, and “Diode bad” for any other measured voltage.

Solution One possible pseudocode description for the program is

```
program MixedDiodeCheck
   begin
      apply 5 V to circuit
      measure diode voltage
      if (diode voltage is less than 1.0 V)
         begin if
            set diode condition to 1
         end if
      else
         begin else
      if (diode voltage is greater than 4.5 V) then
        begin if
          set diode condition to 2
        end if
      else
        begin else
          set diode condition to 3
        end else
    end else
  case (diode condition)
    begin case
      1: print "Diode forward biased"
        break
      2: print "Diode reverse biased"
        break
      3: print "Diode bad"
        break
    end case
end MixedDiodeCheck
```

Related Problem Modify the pseudocode for Example 18–9 so that if the diode voltage equals 0 V the program prints “Diode shorted” and if the diode voltage equals 5 V the program prints “Diode open”.

SECTION 18–4 CHECKUP

1. What flowchart block is associated with conditional execution?
2. What two instructions are used in conditional execution?
3. What is the basic difference between the IF-THEN and IF-THEN-ELSE instructions?
4. What is the major difference between the IF-THEN-ELSE and CASE instructions?

18–5 PROGRAM LOOPS

Very few programs perform tasks only once. For example, a word processing program allows you to enter more than one letter into a document, and the operating system on your computer allows you to run more than one application before shutting down. Program loops allow computers to execute the same set of instructions multiple times.

After completing this section, you should be able to

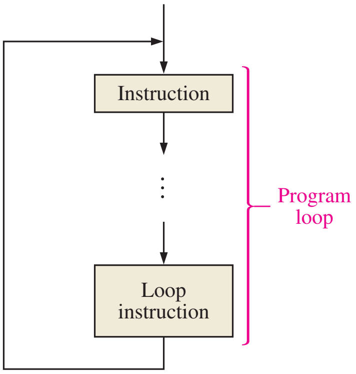
- **Discuss and apply the concept of programming loops**
- Describe a basic program loop
- Discuss the FOR-TO-STEP loop
  - Draw the flowchart and write the pseudocode
  - Describe the automated testing of a zener diode
- Discuss the WHILE-DO loop
  - Draw the flowchart and write the pseudocode
  - Describe the automated testing of a JFET
- Discuss the REPEAT-UNTIL loop
  - Draw the flowchart and write the pseudocode
  - Describe the automated testing of an SCR
- Discuss nested loops and their application in program loops
  - Describe the automated testing of a BJT

The Basic Program Loop

A **program loop** is a sequence of execution in which the program returns to a previous point of execution, forming a closed path or "loop". Figure 18–13 shows the flowchart for a basic program loop.

▶ FIGURE 18–13

Flowchart for a basic program loop.



As the flowchart shows, execution proceeds through the instructions inside the program loop and the last instruction, called the *loop instruction*, redirects execution back to the first instruction in the loop. This circular path gives the program loop its name. Loop instructions and the program loops they create may be conditional or unconditional.

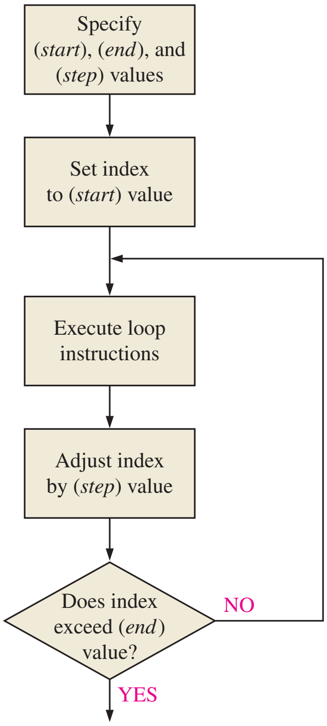
A conditional loop will execute only if some condition is satisfied. Most program loops are conditional loops. The three major types of conditional loops are the FOR-TO-STEP loop, the WHILE-DO loop, and the REPEAT-UNTIL loop.

An unconditional loop will cause the program loop to execute indefinitely. A loop that executes indefinitely is called an **infinite loop**. Infinite loops can result from programming or system errors, but they are intentionally used in applications that must operate indefinitely. Operating systems, embedded applications in consumer products, and automated systems are infinite loops.

The FOR-TO-STEP Loop

The FOR-TO-STEP loop is a program loop that uses a counter or index value to determine whether it should repeat or exit the loop. The programmer sets the initial, end, and step values for the loop index, which is the counter that keeps track of how many times the loop has executed. Figure 18–14 shows the flowchart for the FOR-TO-STEP loop.

As the flowchart shows, the FOR-TO-STEP loop specifies the start, end, and step values and initializes the loop index to the start value. The program loop then executes the loop instructions and adjusts the loop index by the step value. If the loop index does not exceed the end value, the loop repeats; otherwise, the program exits the loop.


Specify (start), (end), and (step) values
Set index to (start) value
Execute loop instructions
Adjust index by (step) value
Does index exceed (end) value?
NO
YES

▲ FIGURE 18–14

Flowchart for the FOR-TO-STEP loop.

EXAMPLE 18–10

Write the pseudocode description for a procedure to multiply two nonzero positive integers using repeated addition with a FOR-TO-STEP loop.

Solution One possible pseudocode description is

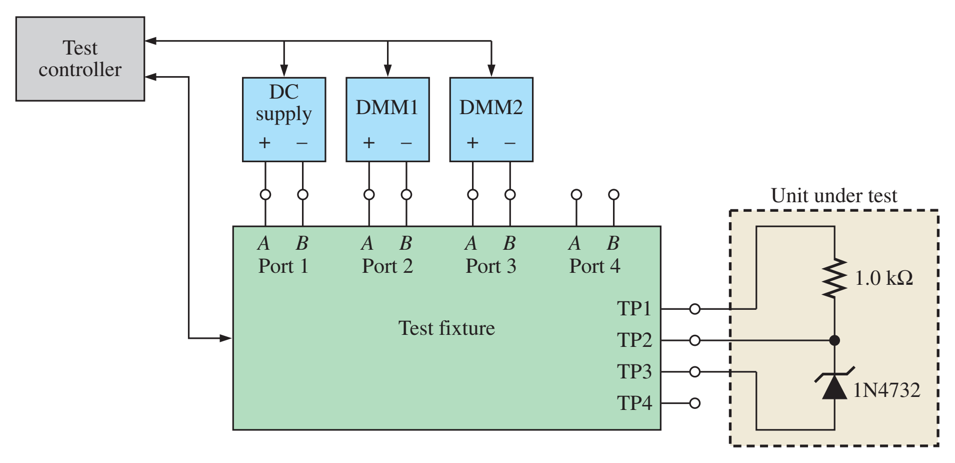
```
procedure Multiply
    begin
        input multiplicand value and multiplier value
        set product value to 0
        for (index = 0) to (index equals multiplier value) step (1)
```

```
            begin for-to-step
                product value is product value plus multiplicand value
            end for-to-step
        output product value
    end Multiply
```

Related Problem Verify the pseudocode in Example 18–10 for multiplying 4 (the multiplicand) by 5 (the multiplier).

Note that if the step value for a loop is negative, the loop index will decrease with each loop. Many programs use a negative step value and end value of 0 because processors can easily check for a value of 0.

EXAMPLE 18–11 Figure 18–15 shows a test system to determine the *V-I* characteristics of a 1N4732 4.7 V zener diode. Write the pseudocode description that uses a FOR-TO-STEP loop to decrease the voltage across TP1 and TP3 from 6 V to 0 V in 0.1 V increments and to plot the zener current vs. zener voltage for each voltage setting.



▲ FIGURE 18–15

1N4732 test system.

Solution One possible pseudocode description is

```
program Plot1N4732ReverseBias
    begin
        set DMM1 function to dc voltmeter mode
        connect Port 2A to TP2 and Port 2B to TP1
        set DMM2 function to dc voltmeter mode
        connect Port 3A to TP2 and Port 3B to TP3
        set dc supply to 0 V
        connect Port 1A to TP1 and Port 1B to TP3
        for (index = 6) to (index equals 0) step (-0.1)
            begin for-to-step
                set dc supply value to index value
                read resistor voltage value on DMM1
                IZ value is resistor voltage value divided by 1.0 kilohms
```

```
                              read VZ value on DMM2
                              plot IZ value vs. VZ value
                          end for-to-step
                  end Plot1N4732ReverseBias
```

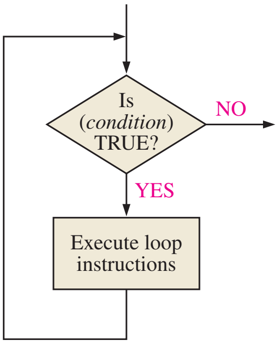
Related Problem Modify the pseudocode in Example 18–11 to decrease the voltage across TP1 and TP3 from 0 V to −1 V in 0.1 V increments and to plot the zener current vs. zener voltage for each voltage setting.

The WHILE-DO Loop

The FOR-TO-STEP loop is useful for applications in which the range of loop condition values is already known or well-defined. Unfortunately, the range for some electrical characteristics is not known. The $V_{GS(off)}$ and I_{DSS} values for FETs, for example, can vary widely for each part number. A FOR-TO-STEP loop may run too many times and exceed the maximum rating for the UUT, or it may run too few times and not apply the signals needed to properly test the UUT.

The WHILE-DO loop solves these problems. Rather than running the loop a predetermined of times, the WHILE-DO loop checks some condition to determine whether or not to continue. In this way, the loop runs only as many times as necessary. Figure 18–16 shows the flowchart for the WHILE-DO loop.

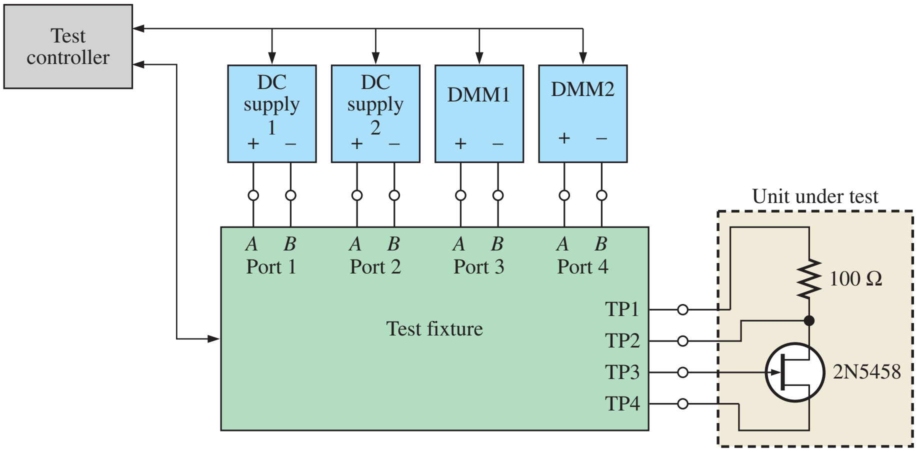
Note that the WHILE-DO loop does not automatically modify the condition that eventually terminates the loop. The loop instructions must evaluate information obtained during the loop and alter the terminating condition at the proper time. Note also that the loop will not execute at all if the condition is initially FALSE.



▲ FIGURE 18–16

Flowchart for the WHILE-DO loop.

EXAMPLE 18–12 Figure 18–17 shows a test system to determine the characteristics for a 2N5458 *n*-channel JFET. Write the pseudocode description that uses a WHILE-DO loop to determine and print the value of I_{DSS} and $V_{GS(off)}$.



▲ FIGURE 18–17

2N5458 test system.

Solution One possible pseudocode description is

```
program Find2N5458JFETValues
    begin
        set DMM1 function to dc voltmeter mode
        connect Port 3A to TP1 and Port 2B to TP2
        set DMM2 function to dc voltmeter mode
        connect Port 4A to TP3 and Port 4B to TP4
        set dc supply 1 to 10 V
        set dc supply 2 to 0 V
        connect Port 1A to TP1 and Port 1B to TP4
        connect Port 2A to TP4 and Port 2B to TP3
        read voltage value on DMM1
        IDSS value is DMM1 voltage value divided by 100 ohms
        print IDSS value
        while (DMM1 voltage value is not 0)
            begin while-do
                increase dc supply 2 by 0.1 V
                read voltage value on DMM1
            end while-do
        read voltage value on DMM2
        VGS(off) value is DMM2 voltage value
        print VGS(off) value
    end Find2N5458JFETValues
```

Related Problem What is a possible problem with the WHILE-DO loop for the pseudocode description in Example 18–12?

The REPEAT-UNTIL Loop

The REPEAT-UNTIL loop differs from the WHILE-DO loop in two ways.

- The REPEAT-UNTIL loop checks the specified condition at the end of the loop.
- The REPEAT-UNTIL loop remains in the loop while the specified condition is FALSE and exits when the condition becomes TRUE.

Because the REPEAT-UNTIL loop checks the specified condition at the end of the loop, a REPEAT-UNTIL loop will always execute at least once. Figure 18–18 shows the flowchart for the REPEAT-UNTIL loop.

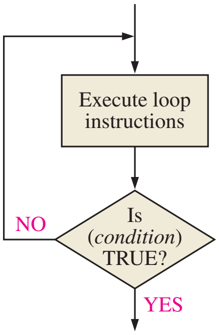


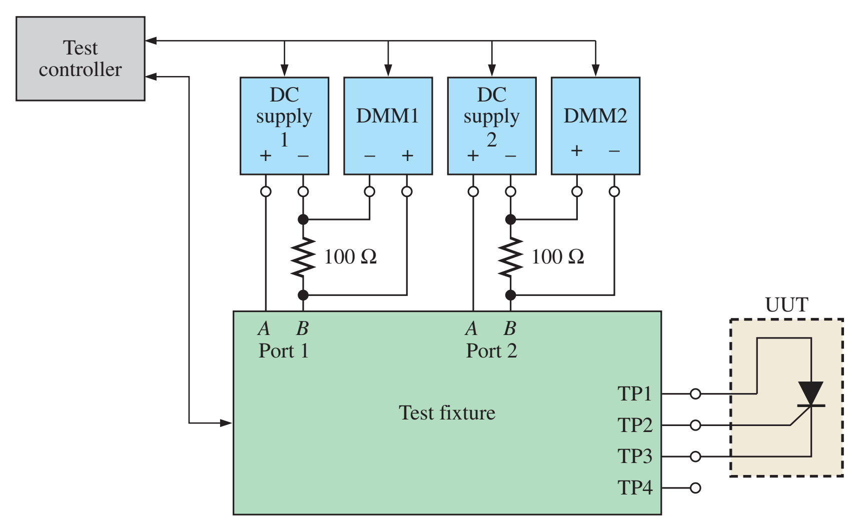
FIGURE 18–18

Flowchart for the REPEAT-UNTIL loop.

EXAMPLE 18–13 Figure 18–19 shows the test system to determine the holding current for an SCR. Write a pseudocode description that uses REPEAT-UNTIL loops to determine and print the value of the gate current that will fire the SCR into conduction for $V_{AK} = 5$ V and the value of the holding current that will keep the SCR in conduction for this value of gate current.

▶ **FIGURE 18–19**

Test system for an SCR.



Solution One possible pseudocode description is

```
program FindSCRValues
    begin
        set DMM1 function to dc voltmeter mode
        set DMM2 function to dc voltmeter mode
        set dc supply 1 to 0 V
        set dc supply 2 to 5 V
        connect Port 1A to TP2 and Port 1B to TP3
        connect Port 2A to TP1 and Port 2B to TP3
        read voltage value on DMM2
        IAK is DMM2 voltage value divided by 100
        repeat until (IAK is greater than 45 mA)
            begin repeat-until
                increase dc supply 1 by 0.01 V
                read voltage value on DMM2
                IAK is DMM2 voltage value divided by 100
            end repeat-until
        read voltage value on DMM1
        IG(5) value is DMM1 voltage value divided by 100
        print IG(5) value
        repeat until (IAK is less than 10 μA)
            begin repeat-until
                decrease dc supply 2 by 0.1 V
                read voltage value on DMM2
                IAK is DMM2 voltage value divided by 100
            end repeat-until
        IH value is IAK value
        print IH value
    end FindSCRValues
```

Related Problem Write a pseudocode description that uses a REPEAT-UNTIL loop to determine and print the value of breakover voltage will fire the SCR into conduction for $I_G = 0$.

Nested Loops

You can place loops within loops to create nested loops. Nested loops are used when a program must execute a task multiple times when the task itself must execute multiple times.

An example of this is the program used by an auto-insertion machine in an electronics assembly line. The auto-insertion machine places multiple parts on blank circuit boards. The outer loop processes the multiple circuit boards and contains inner loops that place multiple parts on each board. In theory, there is no limit to the number of levels in a nested loop, but most programs use only two or three levels of nesting. Figure 18–20 shows the flowchart for a two-level nested loop. Nested loops can consist of any combination of FOR-TO-STEP, WHILE-DO, and REPEAT-UNTIL loops.

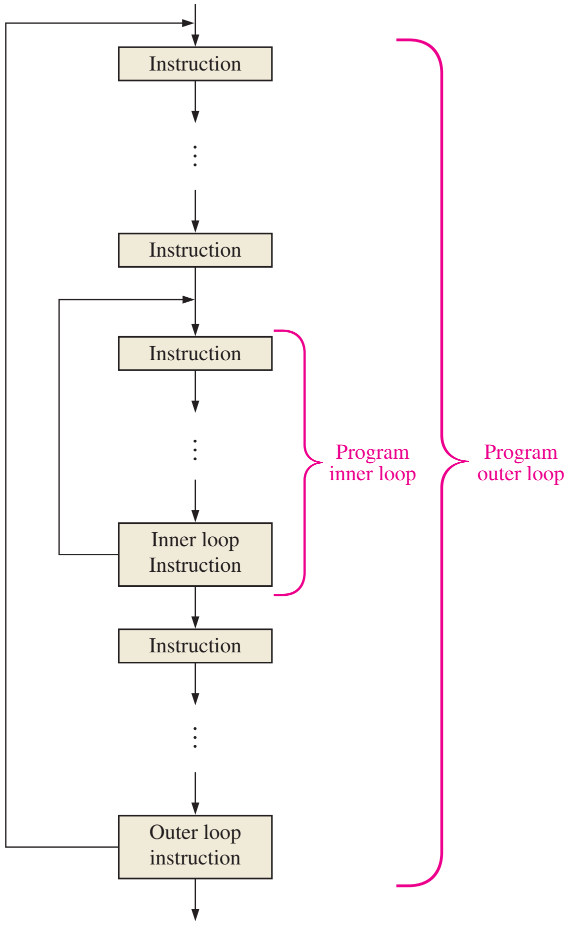


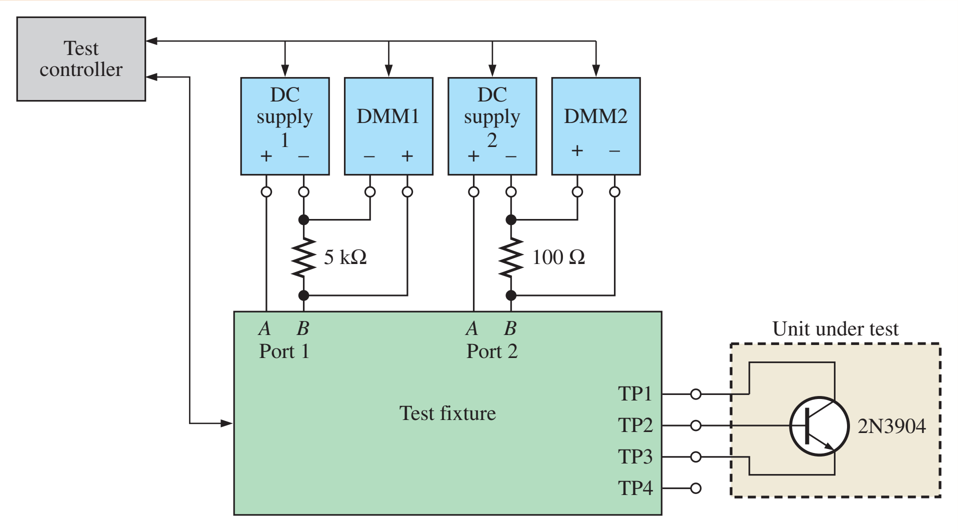
FIGURE 18–20

Flowchart for a two-level nested loop.

Nested loops are useful when programs must work with multiple parameters at the same time. One example is the effect of the SCR gate current on the SCR *V-I* curve. A specific value of gate current produces a specific *V-I* characteristic curve, and a range of gate values produces a family of *V-I* curves. A single loop that varies the value of V_{AK} can generate a single characteristic curve like that shown in Figure 11–10(a). Nesting this loop inside a loop that varies the value of I_G can generate the family of characteristic curves shown in Figure 11–10(b).

EXAMPLE 18–14

Figure 18–21 shows the test system for a 2N3904 *npn* BJT. Write a pseudocode description that uses nested FOR-TO-STEP loops to determine and plot the family of characteristic V_{CE} vs. I_C curves for base supply voltages ranging from 0.7 to 1 V in 0.05 V increments and collector supply voltages ranging from 0 V to 10 V in 1 V increments.



▲ FIGURE 18–21

Test system for a 2N3904 BJT.

Solution One possible pseudocode description is

```
program Plot2N3904Curves
    begin
        set DMM1 function to dc voltmeter mode
        set DMM2 function to dc voltmeter mode
        set dc supply 1 to 0 V
        set dc supply 2 to 0 V
        connect Port 1A to TP2 and Port 1B to TP3
        connect Port 2A to TP1 and Port 2B to TP3
        for (index1 = 0.7) to (index1 equals 1.0) step (0.05)
            begin for-to-step
                set dc supply 1 to index1 value
                IB value is dc supply voltage value divided by 5 kilohms
                plot label "IB = " and IB value
                for (index2 = 0) to (index2 equals 10) step (1)
                    begin for-to-step
                        set dc supply 2 to index2 value
                        read voltage on DMM2
                        IC value is DMM2 voltage value divided by 100 ohms
                        VCE value is index 2 value minus DMM2 voltage value
                        plot IC value vs. VCE value
                    end for-to-step
            end for-to-step
    end Plot2N3904Curves
```

Related Problem What changes would the pseudocode description in Example 18–14 require to test a 2N3906 *pnp* BJT?

SECTION 18–5 CHECKUP

1. What is a basic program loop?
2. Explain the reason for using the term *program loop*.
3. What are the three major types of program loops?
4. In what two ways does a WHILE-DO loop differ from a REPEAT-UNTIL loop?
5. Explain what is meant by the term *nested loop*.

18–6 BRANCHING AND SUBROUTINES

As previous sections have shown, the process flow for most programs is rarely linear. Programs typically contain instructions that redirect execution to some part of the program other than what immediately follows in memory. This program redirection is called **branching**. Programs use branching instructions (such as JUMP instructions) to transfer control to specific sections of code. The conditional and looping instructions from previous sections are special cases of branching. The IF-THEN-ELSE instruction, for example, redirects execution to either the IF or ELSE section of the instruction, but nowhere else. The more general branching instructions can redirect execution anywhere in (or even outside) the program. This makes branching instructions very powerful, as well as potentially very problematic.

After completing this section, you should be able to

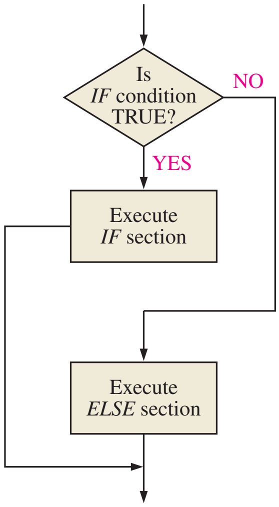
- ❑ **Discuss and apply the concepts of branching and subroutines**
- ❑ Describe branching in programs
    - ◆ Discuss basic branching guidelines ◆ Define *coupling* and *cohesion*
    - ◆ Describe automated testing of an inverting amplifier
- ❑ Describe subroutines in programs
    - ◆ Describe automated testing of a summing amplifier ◆ Discuss the subroutine call

Branching in Programs

Branching achieves one of two objectives.

1. It avoids executing code that immediately follows the branching instruction.
2. It accesses code that does not immediately follow the branching instruction.

In either case, the branching instruction must be able to specify the location of the code that the processor should execute. Some instructions (such as conditional and loop instructions) automatically determine the process flow. The flowchart in Figure 18–22 illustrates this for an IF-THEN-ELSE instruction.



▲ **FIGURE 18–22**

IF-THEN-ELSE branching example.

The branches in Figure 18–22 illustrate two points. The first point is that the objective of the branch from the IF section is to avoid the ELSE section (the first objective of branching) and that the objective of the branch to the ELSE section is to access the ELSE section (the second objective of branching). The second point is that the branch to the ELSE section is conditional and proceeds to *either* the IF or ELSE section, while the branch around the ELSE section from the IF section is unconditional and *must* proceed to whatever follows the ELSE section.

General branching instructions require the programmer to explicitly specify the next instruction to execute. In low-level programs, the programmer specifies the memory location of the instruction. One way to do so is to provide the physical memory address of the instruction, as in the following assembly program listing for a multiplication program:

```
;   ADDRESS    INSTRUCTION    ; COMMENTS
;
    0000       MVI A,00       ; Clear accumulator
    0002       MVI B,02       ; Load multiplicand into B register
    0004       MVI C,03       ; Load multiplier into C register
    0006       ADD B          ; Increase product value by multiplicand
    0007       DCR C          ; Decrement multiplier by 1
    0008       JNZ 0006       ; Repeat loop until multiplier is 0
    000B       HLT            ; Halt when done
```

The program uses the repeated addition method of Example 18–10 to multiply two numbers. The main thing to note about this program is the loop formed by the conditional JNZ (Jump if Not Zero) branching instruction. If the instruction that decrements the multiplier in the C register by 1 does not result in 0, the JNZ instruction "jumps" to address 0006 to add the multiplicand to the running product total. As soon as the multiplier is zero, the JNZ instruction sequences to the HLT instruction, halting the program.

Labels Another way to specify the target of a branching instruction is to use a label that identifies the address. A **label** is a symbolic reference, or name, that an assembler associates with a memory address. The following is a sample listing for the same assembly program using labels:

```
;   LABEL     INSTRUCTION   ; COMMENTS
;
    START:    MVI A,00      ; Clear accumulator
              MVI B,02      ; Load multiplicand into B register
              MVI C,03      ; Load multiplier into C register
    LOOP:     ADD B         ; Increase product value by multiplicand
              DCR C         ; Decrement multiplier by 1
              JNZ LOOP      ; Repeat loop until multiplier is 0
    DONE:     HLT           ; Halt when done
```

This program listing does not specify addresses for each instruction. Instead, it uses the labels START, LOOP, and DONE to indicate the addresses of specific instructions in the program. Labels allow programmers to clearly identify program sections and make both pseudocode and source code easier to understand. They also allow programmers to specify the location to which an instruction should branch.

Some advantages of using labels rather than actual addresses are that errors are easier for programmers to avoid, detect, and correct. Labels allow assemblers to change address references if the program is modified, and they also allow code to be relocatable so that the program can be placed anywhere in memory.

Branching Guidelines Branching is a convenient tool for modifying the sequence in which instructions execute. This convenience can cause problems. When programmers manually loaded instructions directly into memory, they could use branching to modify or correct code without having to reload all memory locations that the change would affect. Suppose, for example, that a programmer accidentally forgot to include Instruction 5 in a program containing a hundred instructions. Without branching, the programmer would have to correct the program by entering Instruction 5 in the correct memory location and then laboriously reenter Instructions 6 through 100. This task could be even more difficult if Instructions 6 through 100 contained any branches because the programmer would have to find and update the target address for each branch. With branching, the programmer could branch to the missing instruction and then branch back to the next instruction. Programmers could also use this method to add code to an existing program.

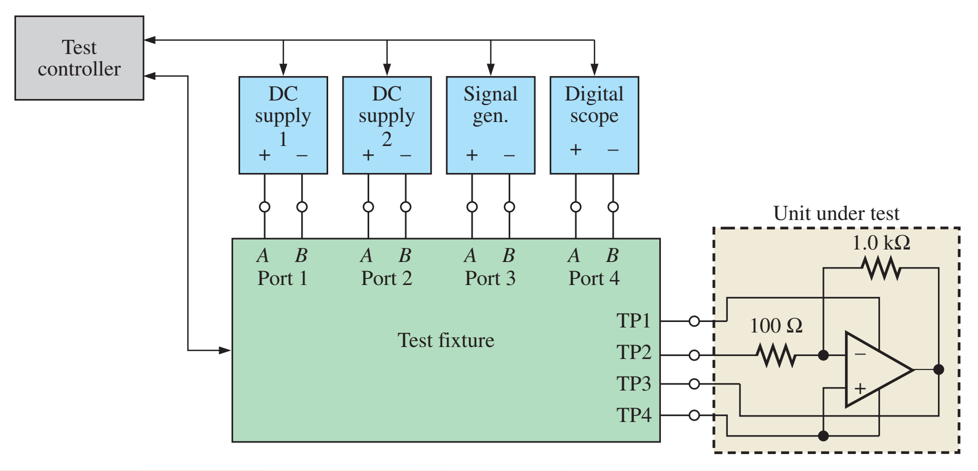
Programmers rarely load instructions into memory by hand anymore; modern programming software allows them to freely modify source code, so this sort of branching is seldom required or justified. Even so, programmers are often tempted to use branches as a shortcut when modifying code. There are three general rules for using branches in programs.

Rule 1 Programs, especially high-level programs, should avoid unconditional branching. One reason for this rule is that the structure of a program should be the result of deliberate design rather than afterthought. A second reason is that unrestricted unconditional branching often results in poorly organized "spaghetti code" that is difficult to understand and maintain. A third reason is that an unconditional branch always results in the same sequence of instructions, so the program instructions could be written that way without using a branch at all.

Example 18–15 illustrates a program modified by several unconditional branches. Note the impact of these branches on understanding the process flow of the program.

EXAMPLE 18–15

Figure 18–23 shows the test system for an inverting amplifier.


Test controller
DC supply 1
DC supply 2
Signal gen.
Digital scope
+
−
A
B
Port 1
Port 2
Port 3
Port 4
Test fixture
TP1
TP2
TP3
TP4
Unit under test
1.0 kΩ
100 Ω

▲ FIGURE 18–23

Test system for an inverting op-amp circuit.

The following pseudocode represents a program that used branches to progressively add features to the test. What is the sequence of test messages that the modified pseudocode will generate?

```
        program TestInvertingAmplifier
            begin
                initialize test fixture
                print "Test fixture initialized"
                branch to NewTestInit
ResumeTest3:
                branch to DCTest
ResumeTest4:
                set signal generator offset to 0 Vdc
                set signal generator ac output to 100 mVpp
                apply input test signal
                measure and record peak-to-peak output signal
                print "100 mV ac test completed"
                branch to CalculateNominalGain
ResumeTest1:
                branch to TestMinimumSignal
ResumeTest2:
                branch to TestMaximumSignal
AllTestsRun:
                print "AC test completed"
                branch to TestsComplete
CalculateNominalGain:
                nominal gain value is output signal divided by 100 mV
                print "Gain calculated for nominal input"
                branch to ResumeTest1
TestMinimumSignal:
                set signal generator ac output to 10 mVpp
                measure and record peak-to-peak output signal
                print "10 mV ac test completed"
                minimum gain value is output test divided by 10 mV
                print "Gain calculated for minimum input"
                branch to ResumeTest2
```

```
TestMaximumSignal:
            set signal generator ac output to 1 Vpp
            measure and record peak-to-peak output signal
            print "1 V ac test completed"
            maximum gain value is output signal
            print "Gain calculated for maximum input"
            branch to AllTestsRun
NewTestInit:
            set signal generator offset to 500 mVdc
            set signal generator ac output to 0 Vpp
            print "System intialized for dc test"
            branch to ResumeTest3
DCTest:
            measure and record dc output signal
            print "500 mV dc test completed"
            dc gain value is output signal divided by 500 mV
            print "Gain calculated for dc input"
            branch to ResumeTest4
TestsComplete:
            print "Inverting amplifier testing complete"
        end TestInvertingAmplifier
```

Solution The pseudocode will first generate the test message

```
Test fixture initialized
```

The program branches to NewTestInit, which generates the message

```
System intialized for dc test
```

and then branches back to ResumeTest3 in the main program body. This is followed by an immediate branch to DCTest, which generates the messages

```
500 mV dc test completed
```

and

```
Gain calculated for dc input
```

and then branches back to ResumeTest4 in the main program body. The main program body generates the message

```
100 mV ac test completed
```

and then branches to CalculateNominalGain. CalculateNominalGain generates the message

```
Gain calculated for nominal input
```

and branches back to ResumeTest1 in the main program body. This is followed by an immediate branch to TestMinimumSignal, which generates the messages

```
10 mV ac test completed
```

and

```
Gain calculated for minimum input
```

and then branches back to ResumeTest2 in the main program body. This is followed by an immediate branch to TestMaximumSignal, which generates the messages

```
1 V ac test completed
```

and

```
Gain calculated for maximum input
```

and then branches back to AllTestsRun in the main program body. The main program body generates the message

```
AC test completed
```

and branches around the added code to TestsComplete. The program then generates the final message

```
Inverting amplifier testing complete
```

and ends.

Related Problem Rewrite the pseudocode in Example 18–15 to eliminate all the unconditional branch instructions.

Rule 2 Programs should avoid nested branches. A branch should not lead to more branches. There are several good reasons for this rule.

- Nested branches complicate and disguise the structure of a program. This makes it more difficult to maintain and modify the program.
- Nested branches can increase the coupling between parts of a program. **Coupling** reflects the extent to which one part of a program interacts with or potentially affects another part of the program. High coupling can result in unintended and unwanted effects, due either to program execution or modification to some part of the code. If you have ever tried to remove one empty clothes hanger from a closet and wound up removing several, you can understand the concept and the undesirable effects of coupling.
- Nested branches can reduce the cohesion of a program. **Cohesion** refers to how well a program or procedure keeps together all the code that is associated with a specific task. Just as keeping tools and materials for some job organized and together greatly simplifies working on that job, high program cohesion greatly simplifies working with programs.
- Nested branches increase the potential for programming errors. In programs without branches, it is easy to trace the process flow because each instruction immediately follows the previous instruction. In programs with a single branch, this path is still fairly obvious. As the number of nesting levels increases, the process flow becomes less and less clear. This complicates knowing how the program arrived at some point in its execution, the current state of the program, and the impact of adding further branches.

Rule 3 Any branch (as any instruction) should always be a conscious design decision to simplify the program. It should not be a convenient shortcut that simplifies the programmer's life. Used properly, branches can simplify a program by eliminating duplicated code, avoiding very complicated conditional instructions, or simplifying the structure or organization of a program.

Subroutines

As the previous discussions showed, general branches affect both program structure and the sequence of program execution. Branching can needlessly complicate the structure of a program and create "spaghetti code" that can lead in turn to programming errors. The branches that modified and added new tests to the pseudocode in Example 18–15 complicated the process flow, especially as the additional tests were not added in the same order in which they executed. **Subroutines**, which are sequences of instructions that perform specific tasks in a program, can help organize programs and simplify the process flow.

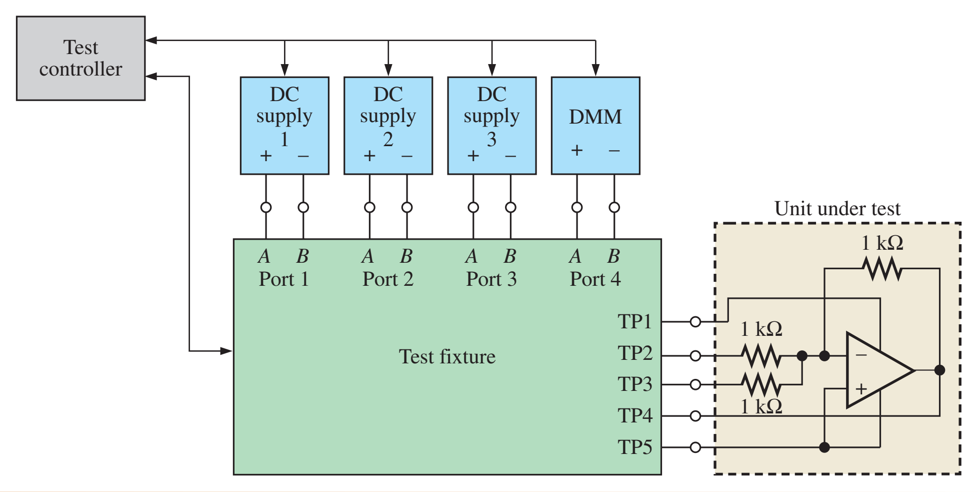
Programs access subroutines using subroutine calls. A **subroutine call** instruction is a special type of branching instruction that can avoid the problems that can arise from general branching instructions. Specifically, a subroutine call is a controlled branch that redirects execution to a subroutine, executes the subroutine instructions, and allows the program to resume execution at the instruction that immediately follows the subroutine call instruction.

Subroutine calls can return to the point from which they were called because the processor uses a special section of memory, called the **stack**, to store the memory address of the instruction that follows the call instruction. When the subroutine ends, the processor retrieves the return address from the stack and resumes program execution at this location.

Subroutines (also called functions or procedures in **high-level programming** languages) help simplify the structure of a program by eliminating duplicated code and improve program cohesion by collecting the code associated with a specific task in one place. Another benefit of subroutines is that they more easily allow programmers to use the same code in more than one program, reducing the amount of time needed to develop and write new programs.

EXAMPLE 18–16

Figure 18–24 shows a test system used to test a summing amplifier.



▲ FIGURE 18–24

Test system for a summing amplifier.

Rewrite the following pseudocode description to replace the instructions that initialize the test system with a subroutine call to InitializeTestFixture and shut down the text fixture with a call to ShutdownTestFixture.

```
     program TestSummingAmplifier
        begin
            open all relays
            set dc supply 1 to 5.0 V
            set dc supply 2 to 0.0 V
            set dc supply 3 to 0.0 V
Test00:
            measure summing amplifier output
            open all relays
            set dc supply 1 to 5.0 V
            set dc supply 2 to 0.0 V
            set dc supply 3 to 0.0 V
```

```
Test01:
             set dc supply 2 to 5.0 V
             close all relays
             measure summing amplifier output
             open all relays
             set dc supply 1 to 5.0 V
             set dc supply 2 to 0.0 V
             set dc supply 3 to 0.0 V
Test10:
             set dc supply 3 to 5.0 V
             close all relays
             measure summing amplifier output
             open all relays
             set dc supply 1 to 5.0 V
             set dc supply 2 to 0.0 V
             set dc supply 3 to 0.0 V
Test11:
             set dc supply 2 to 5.0 V
             set dc supply 3 to 5.0 V
             close all relays
             measure summing amplifier output
             call ShutdownTestFixture
         end TestSummingAmplifier
```

Solution One possible pseudocode description is

```
     program NewTestSummingAmplifier
         begin
             call InitializeTestFixture
Test00:
             measure summing amplifier output
             call InitializeTestFixture
Test01:
             set dc supply 2 to 5.0 V
             measure summing amplifier output
             call InitializeTestFixture
Test10:
             set dc supply 3 to 5.0 V
             measure summing amplifier output
             call InitializeTestFixture
Test11:
             set dc supply 2 to 5.0 V
             set dc supply 3 to 5.0 V
             close all relays
             measure summing amplifier output
             call ShutdownTestFixture
         end NewTestSummingAmplifier

     procedure InitializeTestFixture
         begin
             open all relays
             set dc supply 1 to 5.0 V
             set dc supply 2 to 0.0 V
             set dc supply 3 to 0.0 V
         end InitializeTestFixture

     procedure ShutdownTestFixture
         begin
             open all relays
```

```
            set dc supply 1 to 0.0 V
            set dc supply 2 to 0.0 V
            set dc supply 3 to 0.0 V
        end ShutdownTestFixture
```

Related Problem Would there be any benefit to replacing the multiple instances of "measure summing amplifier output" in the pseudocode for Example 18–16 with calls to a subroutine MeasureSummingAmplfiierOutput? Why or why not?

High-level languages, like C++ and Visual Basic, can also use the stack to pass information between subroutines and the calling program in a parameter list. This increases the value of using subroutines because programs can use a single subroutine to perform multiple tasks when the tasks differ from each other only in the values they use.

EXAMPLE 18–17 Modify the pseudocode description for CalculateAmplifierGains to replace the subroutine calls InitializeTestFixture and ShutdownTestFixture with a single subroutine ConfigureTestFixture.

```
program CalculateAmplifierGains
    begin
        call InitializeTestFixture
        print "Test fixture initialized"
NewTestInit:
        set signal generator offset to 500 mVdc
        set signal generator ac output to 0 Vpp
        print "System intialized for dc test"
NominalACTest:
        call MeasureNominalGain
MinimumACTest:
        call MeasureMinimumGain
MaximumACTest:
        call MeasureMaximumGain
AllGainsMeasured:
        print "AC test completed"
        print "Inverting amplifier testing complete"
        call ShutdownTestFixture
    end CalculateAmplifierGains

procedure InitializeTestFixture
    begin
        open all relays
        set dc supply 1 to 5.0 V
        set dc supply 2 to 0.0 V
        set dc supply 3 to 0.0 V
    end InitializeTestFixture

procedure ShutdownTestFixture
    begin
        open all relays
        set dc supply 1 to 0.0 V
        set dc supply 2 to 0.0 V
        set dc supply 3 to 0.0 V
    end ShutdownTestFixture
```

```
procedure MeasureNominalGain
    begin
        set signal generator offset to 0 Vdc
        set signal generator ac output to 500 mVpp
        apply input test signal
        measure and record peak-to-peak output signal
        nominal gain value is output signal divided by 500 mV
        print "0.5 V ac test completed"
    end MeasureNominalGain

procedure MeasureMinimumGain
    begin
        set signal generator offset to 0 Vdc
        set signal generator ac output to 50 mVpp
        apply input test signal
        measure and record peak-to-peak output signal
        minimum gain value is output test divided by 50 mV
        print "0.05 V ac test completed"
    end MeasureMinimumGain

procedure MeasureMaximumGain
    begin
        set signal generator ac output to 5.0 Vpp
        apply input test signal
        measure and record peak-to-peak output signal
        maximum gain value is output signal
        print "5.0 V ac test completed"
    end MeasureMaximumGain
```

Solution The subroutines InitializeTestFixture and ShutdownTestFixture differ only in the value to which dc supply 1 is set. One possible pseudocode description is

```
program CalculateAmplifierGains
    begin
        call ConfigureTestFixture (5.0)
        print "Test fixture initialized"
NewTestInit:
        set signal generator offset to 500 mVdc
        set signal generator ac output to 0 Vpp
        print "System intialized for dc test"
NominalACTest:
        call MeasureNominalGain
MinimumACTest:
        call MeasureMinimumGain
MaximumACTest:
        call MeasureMaximumGain
AllGainsMeasured:
        print "AC test completed"
        print "Inverting amplifier testing complete"
        call ConfigureTestFixture (0.0)
    end CalculateAmplifierGains

procedure ConfigureTestFixture(DCSupp1y1Value)
    begin
        open all relays
        set dc supply 1 to DCSupply1Value
        set dc supply 2 to 0.0
        set dc supply 3 to 0.0
    end ConfigureTestFixture
```

```
procedure MeasureNominalGain
   begin
      set signal generator offset to 0 Vdc
      set signal generator ac output to 500 mVpp
      apply input test signal
      measure and record peak-to-peak output signal
      nominal gain value is output signal divided by 500 mV
      print "0.5 V ac test completed"
   end MeasureNominalGain

procedure MeasureMinimumGain
   begin
      set signal generator offset to 0 Vdc
      set signal generator ac output to 50 mVpp
      apply input test signal
      measure and record peak-to-peak output signal
      minimum gain value is output test divided by 50 mV
      print "0.05 V ac test completed"
   end MeasureMinimumGain

procedure MeasureMaximumGain
   begin
      set signal generator ac output to 5.0 Vpp
      apply input test signal
      measure and record peak-to-peak output signal
      maximum gain value is output signal
      print "5.0 V ac test completed"
   end MeasureMaximumGain
```

When the program calls the subroutine ConfigureTestFixture, the value specified inside the parentheses is passed to the subroutine as DCSupply1Value. When the subroutine runs, this value is used to set the value of dc supply 1. The first subroutine call sets dc supply 1 to 5.0 V, and the second subroutine call sets dc supply 1 to 0.0 V.

Related Problem Rewrite the pseudocode description for Example 18–17 to replace the procedures MeasureNominalGain, MeasureMinimumGain, and MeasureMaximumGain with the single subroutine MeasureGain.

SECTION 18–6 CHECKUP

1. What is a branching instruction?
2. What two objectives does branching accomplish?
3. What are coupling and cohesion in programming?
4. What are three basic guidelines for using general branches in programs?
5. How does a subroutine call differ from a general branching instruction?

SUMMARY

Section 18–1

- Programming languages are made up of instructions that a computer can process.
- An instruction set consists of the machine language instructions that a processor can decode and execute.
- Machine and assembly languages are low-level languages that operate directly on the level of the processor hardware.

- Most programming uses high-level languages like C++ and Visual Basic that are easier for people to use.
- Programming languages consist of five basic instruction types: simple instructions, conditional instructions, looping instructions, branching instructions, and exception handling instructions.
- Flowcharts use distinctively-shaped interconnected blocks to graphically represent the structure and process flow of programs.
- Pseudocode uses generic descriptions of program operations to textually represent the structure and process flow of programs.

Section 18–2

- Automated test systems consist of a test controller, a test fixture, test equipment and instrumentation, and the unit under test.
- The test controller executes the text code that defines the test tasks, configures the rest of the test system, and coordinates the test system activities.
- The test fixture selectively connects the test equipment and instrumentation to the unit under test.
- Test programs must take into account limitations that exist in practical test systems.

Section 18–3

- Simple sequential programs are the simplest programs that contain no branches or loops and have limited applications.
- Simple sequential programs can use any instructions that do not alter the sequence of program execution.

Section 18–4

- Conditional execution tests whether specific conditions exist to determine which sequence of instructions, if any, to execute.
- The two basic conditional execution instructions are the IF-THEN-ELSE and CASE instructions.
- Programs can nest conditional execution instructions to increase the number of alternative execution sequences.

Section 18–5

- Program loops are program sequences that return the program to a previous point of execution.
- The three basic types of program loop instructions are the FOR-TO-STEP, WHILE-DO, and REPEAT-UNTIL instructions.
- The FOR-TO-STEP instruction is used to loop a specific number of times. The WHILE-DO and REPEAT-UNTIL instructions are used when the exact number of loops required for a task cannot be determined ahead of time.
- The WHILE-DO instruction tests whether the loop condition is TRUE before entering the loop and need not execute the loop instruction. The REPEAT-UNTIL instruction tests whether the loop condition is FALSE after entering the loop and must execute the loop instructions at least once.
- Programs can nest loops so that a loop contains the same or another type of loop.

Section 18–6

- Branching modifies the sequence in which instructions execute.
- The intent of branching is either to avoid executing code that immediately follows the branching instruction or to execute code that does not immediately follow that branching instruction.
- Programs should limit and carefully control branching in programs. Unconditional branches in programs in particular can create problems and should be avoided if possible.
- Subroutines can help simplify and organize programs, increase cohesion, and reduce coupling.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

Automated test system A system that operates under the control of an automated controller to conduct tests on a component, circuit, or system.

Branching Redirection of program execution to some program location other than what immediately follows in memory.

Conditional execution The selective processing of program instructions based upon the validity of some condition.

Flowchart A graphical means of representing the organization and process flow of a program using distinctively-shaped interconnected blocks.

Instruction set The set of binary patterns that the hardware of a microprocessor can decode and execute.

Nesting The use of an instruction type within another instruction of the same type.

Program A series of instructions that has a computer perform some specific task or achieve some specific objective.

Program loop A sequence of execution in which a program returns to a previous point of execution.

Programming language A set of instructions and rules for their use that allow programmers to provide a processor with the necessary information to accomplish some specific task.

Pseudocode A textual means of representing the organization and process flow of a program using generic descriptions of program operations.

Sequential programming Programming in which instructions execute in the order in which they appear in the program.

Subroutine A sequence of instructions, usually written separately from the main program, that accomplishes a specific task in a program.

Test controller The component in an automated test system that executes the test code that defines the test tasks, configures the other components in the test system, and coordinates the activities of the test system components.

Test fixture The component in an automated test system that selectively connects the test equipment and instrumentation to the unit under test.

Unit under test (UUT) The component, circuit, or system to be tested in a test system. The UUT is sometimes referred to as the device under test (DUT).

TRUE/FALSE QUIZ

Answers can be found at www.pearsonhighered.com/floyd.

1. All programming consists of specifying instructions required for a processor to accomplish some specific task.
2. The instructions of a low-level language interacts directly with the processor hardware.
3. Each instruction of a high-level language typically represents multiple machine language instructions.
4. Unconditional loops are never intentionally used in programs.
5. An advantage of subroutines over general branching instructions is that subroutines increase coupling and minimize cohesion.
6. The purpose of the test fixture in an automated test system is to selectively connect the test equipment and instruments to the test controller.
7. A graphical means of representing the organization and process flow in a program is a flowchart.
8. Unconditional branches should be used whenever possible to simplify programming.
9. Pseudocode uses generic descriptions of program operations to represent the structure and process flow of programs.
10. WHILE-DO and REPEAT-UNTIL instructions are different names for the same thing.
11. If you wish to repeat some task a specific number of times in a program, a FOR-TO-STEP instruction is probably your best choice.
12. Programs that convert assembly language programs into machine language are called assemblers.
13. A CASE instruction is an example of a nested loop instruction.

SELF-TEST

Answers can be found at www.pearsonhighered.com/floyd.

Section 18–1

1. All the instructions that the hardware of a processor can directly decode and execute is called
   (a) pseudocode (b) a flowchart
   (c) an assembly program (d) the instruction set
2. All of the following are instruction types except
   (a) conditional instructions (b) pseudocode instructions
   (c) loop instructions (d) branching instructions

3. One disadvantage of flowcharts is that
   - **(a)** the process flow of a program is difficult to follow in a flowchart
   - **(b)** it is not possible for flowcharts to represent large programs
   - **(c)** process flow is not always the best way to represent a program
   - **(d)** flowcharts cannot distinguish between WHILE-DO and REPEAT-UNTIL loops
4. An advantage of pseudocode is that it
   - **(a)** uses easily recognized and distinctively-shaped symbols
   - **(b)** shows the overall process flow of a program better than a flowchart
   - **(c)** provides a high level of structure for implementing the final program
   - **(d)** changes to the final program code do not affect the pseudocode

Section 18–2

5. A basic automated test system consists of all the following components except
   - **(a)** a connection to access the Internet
   - **(b)** a test fixture
   - **(c)** the unit under test
   - **(d)** a test controller
6. The component that physically connects the UUT to the rest of the automated test system is the
   - **(a)** test controller
   - **(b)** test instrumentation
   - **(c)** test equipment
   - **(d)** test fixture
7. The test fixture consists of
   - **(a)** the test controller and unit under test
   - **(b)** the test equipment and test instrumentation
   - **(c)** electromechanical relays and silicon controlled switches
   - **(d)** the switching control and switching circuitry

Section 18–3

8. Simple sequential programs can include any instructions except
   - **(a)** I/O instructions
   - **(b)** arithmetic instructions
   - **(c)** branching instructions
   - **(d)** assembly language instructions
9. Simple sequential programs
   - **(a)** have limited applications
   - **(b)** have nonlinear structures
   - **(c)** cannot be represented with flowcharts
   - **(d)** cannot be represented with pseudocode

Section 18–4

10. Conditional execution
    - **(a)** limits the power and usefulness of programs
    - **(b)** uses the decision block in flowcharts
    - **(c)** is always limited to two alternatives
    - **(d)** always sequences through the same instructions
11. The IF-THEN-ELSE instruction
    - **(a)** is a special form of the more general IF-THEN instruction
    - **(b)** provides three alternative sequences of instructions
    - **(c)** implements the most basic form of conditional execution
    - **(d)** is a theoretical construct with no practical application in programming
12. The CASE instruction
    - **(a)** must determine whether a program value is equal to or not equal to specific values
    - **(b)** implements the most basic form of conditional execution
    - **(c)** is limited to two alternative sequences of instructions
    - **(d)** is another name for an IF-THEN instruction

Section 18–5

13. An infinite loop
    - **(a)** has no practical value and is never used
    - **(b)** is used in operating systems and other specialized applications
    - **(c)** is another name for an unconditional loop
    - **(d)** occurs only when intended

14. The difference between a WHILE-DO instruction and REPEAT-UNTIL instruction is
  (a) the WHILE-DO instruction loops when a condition is False
  (b) the WHILE-DO loop always executes at least once
  (c) the REPEAT-UNTIL loop tests the loop condition at the end of the loop
  (d) the two are identical

15. A FOR-TO-STEP instruction with a STEP value of 0 will
  (a) probably result in an infinite loop
  (b) set the initial index value to 0
  (c) exit when the index value reaches 0
  (d) never execute

Section 18–6

16. The difference between general branch instructions and conditional or loop instructions is
  (a) general branch instructions can create infinite loops and conditional or loop instructions cannot
  (b) conditional and loop instructions execute faster than general branch instructions
  (c) general branch instructions are available only in low-level languages
  (d) a conditional or loop instruction implicitly specifies the next instruction to execute

17. Subroutine calls differ from general branch instructions in that
  (a) subroutine calls to programs use labels and general branch instructions do not
  (b) subroutine calls allow the program to resume execution at the instruction immediately following the call to the subroutine
  (c) general branch instructions use a special section of memory called the stack
  (d) subroutine calls can be nested and general branch instructions cannot

18. Another name for a subroutine is
  (a) a procedure
  (b) a stack
  (c) a flowchart
  (d) a process flow

PROBLEMS

Answers to all odd-number problems are at the end of the book.

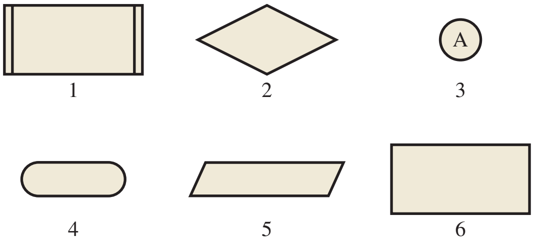
Section 18–1

Programming Basics

1. What are the five basic instruction types?
2. Identify each of the flowchart symbols in Figure 18–25.
3. Write the pseudocode for a program that inputs and prints the average for three numbers.

FIGURE 18–25

Flowchart symbols for Problem 2.



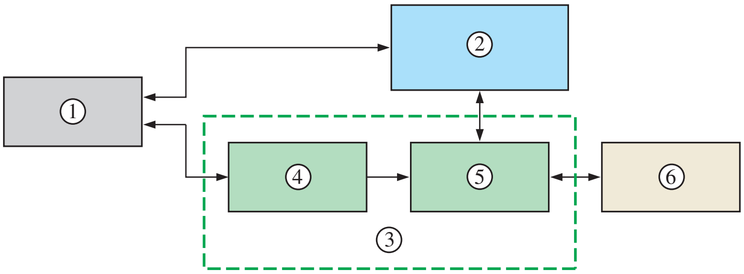
Section 18–2

Automated Testing Basics

4. Identify each of indicated components in the automated test system in Figure 18–26.

FIGURE 18–26

Automated test system block diagram for Problem 4.



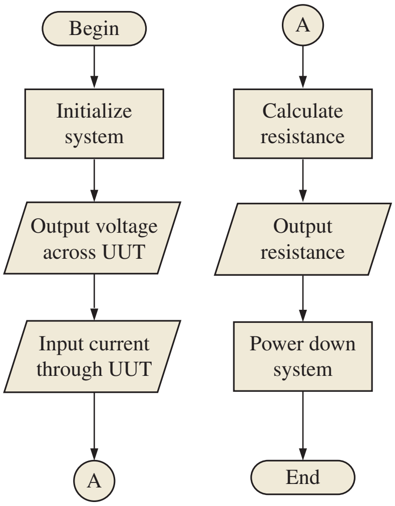
5. What are advantages of using electromechanical relays to connect the UUT to the test equipment and instrumentation in an automated test system?

Section 18–3 The Simple Sequential Program

6. What is the process flow for a simple sequential program?
7. Does the flowchart shown in Figure 18–27 represent a simple sequential program? Justify your answer.

FIGURE 18–27

Program flowchart for Problem 7.


Begin
Initialize system
Output voltage across UUT
Input current through UUT
A
A
Calculate resistance
Output resistance
Power down system
End

Section 18–4 Conditional Execution

8. What output value will the pseudocode below print if the start value is 7?

```
program Confused
    begin
        input start value
        output value is 1
        if (start value is less than 5) then
            begin if
                output value is start value plus 2
                if (start value is less than 2) then
                    begin if
                        output value is output value times 3
                    end if
                else
                    begin else
                        output value is output value times 2
                    end else
            end if
        else
            begin else
                output value is start value minus 2
                if (start value is more than 7) then
                    begin if
                        if (start value is more than 9)
                            begin if
                                output value is output value divided by 3
                            end if
                        else
                            begin else
                                output value is output value divided by 2
                            end else
                end if
            else
         begin else
            if (start value is more then 6) then
                begin if
                   output value is output value divided by 3
                end if
            else
                begin else
                   output value is output value divided by 2
                end else
            end else
        end else
    print output value
end Confused
```

9. Rewrite the following pseudocode to replace the nested IF-THEN-ELSE statements with a CASE statement.

```
program IdentifyKeyValue
    begin
        input key value
        if (key value equals "1") then
            begin if
                print "Key value equals 1"
            end if
        else
            begin else
                if (key value equals "2") then
                    begin if
                        print "Key value equals 2"
                    end if
                else
                    begin else
                        if (key value equals "3") then
                            begin if
                                print "Key value equals 3"
                            end if
                        else
                            begin else
                                print "Key value is more than 3"
                            end else
                    end else
            end else
    end IdentifyKeyValue
```

Section 18–5 Program Loops

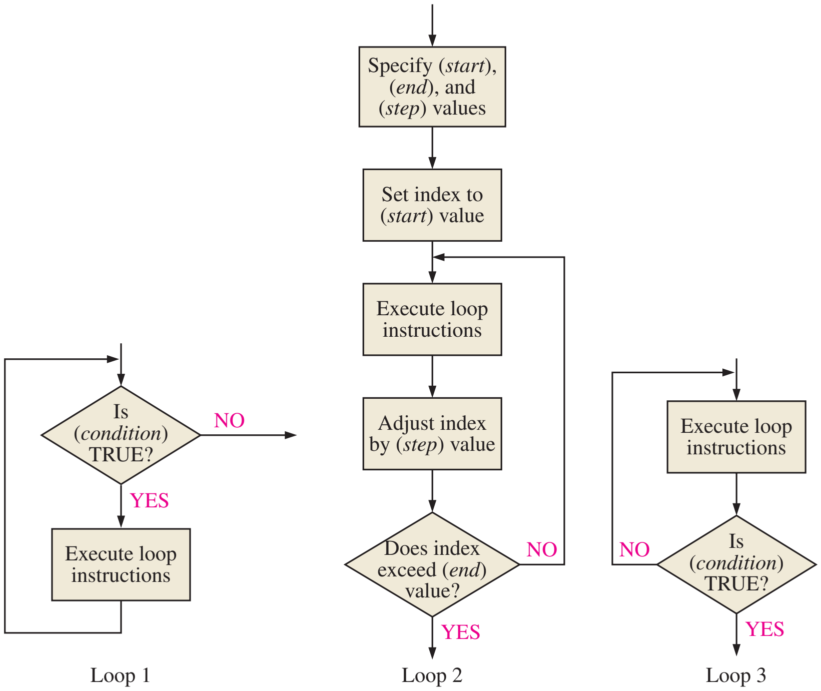
10. Which of the flowcharts in Figure 18–28 correspond to the FOR-TO-STEP, the WHILE-DO, and the REPEAT-UNTIL instructions?

11. What output value will the following pseudocode print?

```
program LoopAdder
    begin
        sum is 0
        for (index = 1) to (index equals 10) step (2)
            begin for-to-step
                sum is sum plus index plus 1
            end for-to-step
        print sum
    end LoopAdder
```

FIGURE 18–28

Program loop flowcharts for Problem 10.


Specify (start), (end), and (step) values
Set index to (start) value
Execute loop instructions
Adjust index by (step) value
Does index exceed (end) value?
NO
YES
Loop 2
Is (condition) TRUE?
NO
YES
Execute loop instructions
Loop 1
Execute loop instructions
Is (condition) TRUE?
NO
YES
Loop 3

12. What output value will the following nested loop pseudocode print?

```
program NestedLoopAdder
   begin
      sum = 0
      for (index1 = 1) to (index2 equals 3) step (1)
         begin for-to-step
            for (index2 = 1) to (index2 = index1) step (1)
               begin for-to-step
                  sum = sum + 1
               end for-to-step
         end for-to-step
      print sum
   end NestedLoopAdder
```

Section 18–6 Branches and Subroutines

13. What are three reasons why programs should avoid using unconditional branch instructions such as JUMP and GOTO?

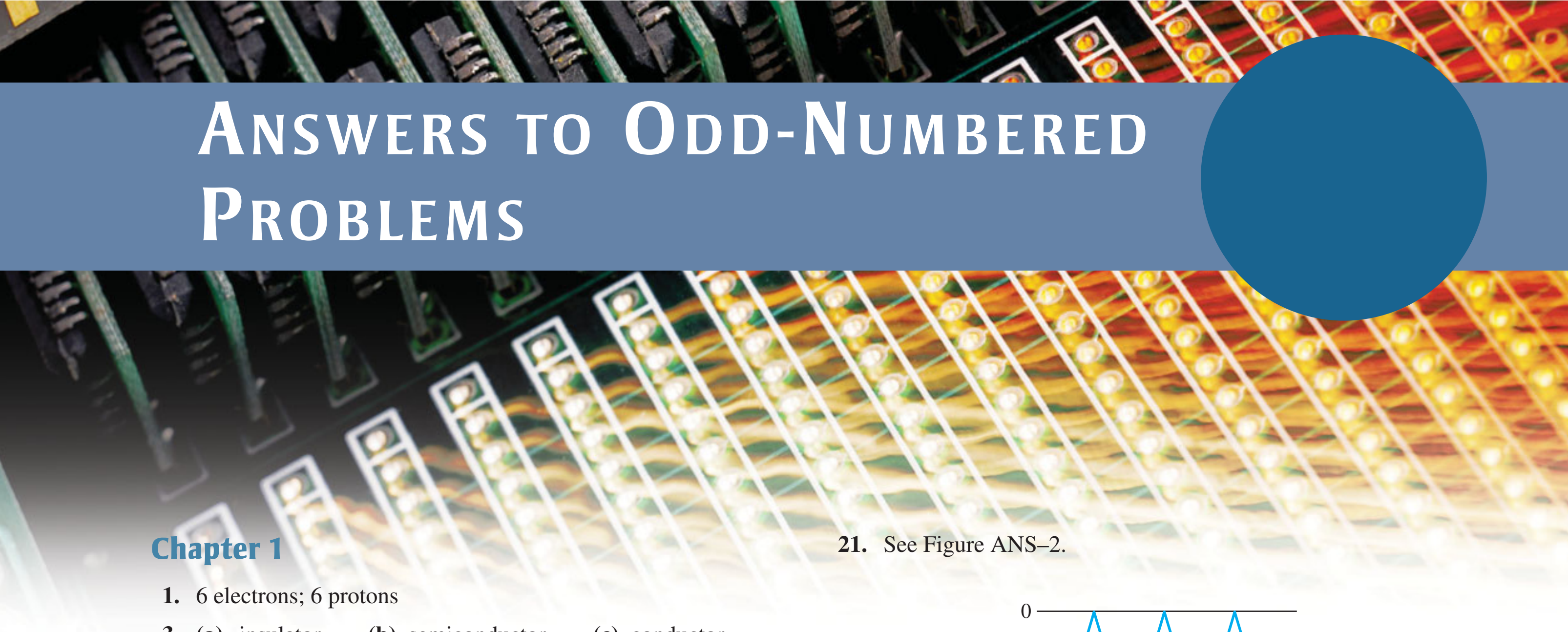
14. Write the pseudocode description for a subroutine called CompareValues that will allow you to rewrite the following pseudocode description:

```
program NoSubroutineCall
   begin
      input Resistor1 value
      input Resistor2 value
      print "First resistor value is " and Resistor1 value
      print "Second resistor value is " and Resistor2 value
      if (Resistor1 value is greater than Resistor2 value) then
         begin if
            print "First resistor value is greater than second
                  resistor value"
         end if
      else
         begin else
```

```
            print "Second resistor value is greater than first
                    resistor value"
         end else
      input Resistor3 value
      input Resistor4 value
      print "First resistor value is " and Resistor3 value
      print "Second resistor value is " and Resistor4 value
      if (Resistor3 value is greater than Resistor4 value) then
         begin if
            print "First resistor value is greater than second
                    resistor value"
         end if
      else
         begin else
            print "Second resistor value is greater than first
                    resistor value"
         end else
   end NoSubroutineCall
```

as

```
program UseSubroutineCall
   begin
      call CompareValues(Resistor1, Resistor2)
      call CompareValues(Resistor3, Resistor4)
   end UseSubroutineCall
```



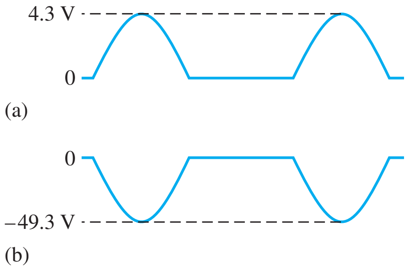
ANSWERS TO ODD-NUMBERED PROBLEMS

Chapter 1

1. 6 electrons; 6 protons
3. **(a)** insulator **(b)** semiconductor **(c)** conductor
5. Four
7. Conduction band and valence band
9. Antimony is a pentavalent material. Boron is a trivalent material. Both are used for doping.
11. No. The barrier potential is a voltage drop.

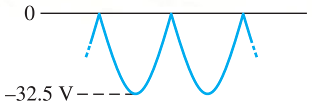
Chapter 2

1. *p* region
3. To generate the forward bias portion of the characteristic curve, connect a voltage source across the diode for forward bias and place an ammeter in series with the diode and a voltmeter across the diode. Slowly increase the voltage from zero and plot the forward voltage versus the current.
5. **(a)** reversed-biased **(b)** forward-biased
   (c) forward-biased **(d)** forward-biased
7. **(a)** −3 V **(b)** 0 V **(c)** 0 V **(d)** 0 V
9. See Figure ANS–1.



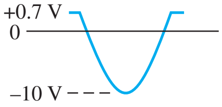
▲ FIGURE ANS–1

11. 63.7 V
13. 24 V rms
15. **(a)** 1.59 V **(b)** 63.7 V **(c)** 16.4 V **(d)** 10.5 V
17. 186 V
19. 78.5 V
21. See Figure ANS–2.



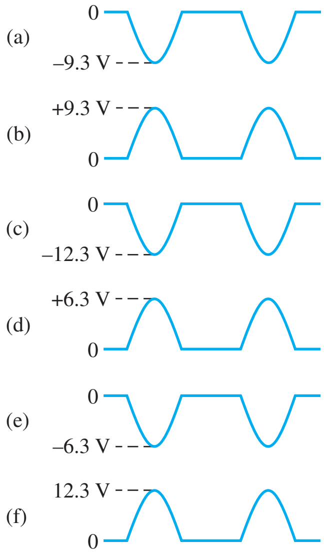
▲ FIGURE ANS–2

23. $V_r = 8.33$ V; $V_{DC} = 25.8$ V
25. 556 μF
27. $V_{r(pp)} = 1.25$ V; $V_{DC} = 48.9$ V
29. 4%
31. See Figure ANS–3.



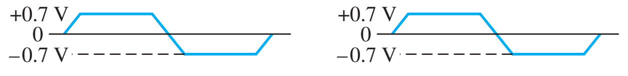
▲ FIGURE ANS–3

33. See Figure ANS–4.



▲ FIGURE ANS–4

35. See Figure ANS–5.



(a) (b)

▲ **FIGURE ANS–5**

37. **(a)** 7.86 mA **(b)** 8.5 mA
(c) 18.8 mA **(d)** 19.4 mA

39. **(a)** A sine wave with a positive peak at +0.7 V, a negative peak at −7.3 V, and a dc value of −3.3 V.

(b) A sine wave with a positive peak at +29.3 V, a negative peak at −0.7 V, and a dc value of +14.3 V.

(c) A square wave varying from +0.7 V down to −15.3 V, with a dc value of −7.3 V.

(d) A square wave varying from +1.3 V down to −0.7 V, with a dc value of +0.3 V.

41. 56.6 V

43. 100 V

45. 50 Ω

47. $V_A = +25$ V; $V_B = +24.3$ V; $V_C = +8.7$ V; $V_D = +8.0$ V

49. R_{surge} is open. Capacitor is shorted.

51. The circuit should not fail because the diode ratings exceed the actual PIV and maximum current.

53. The rectifier must be connected backwards.

55. 177 μF

57. 651 mΩ (nearest standard 0.68 Ω)

59. See Figure ANS–6.

61. $V_{C1} = 170$ V; $V_{C2} = 338$ V

63. Diode open

65. Diode shorted

67. Diode shorted

69. Diode open

71. Diode shorted

73. Diode open

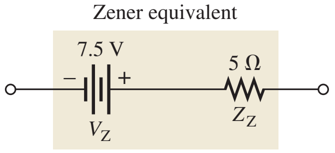
75. Reduced transformer turns ratio

77. Diode leaky

79. Load resistor open

Chapter 3

1. See Figure ANS–7.



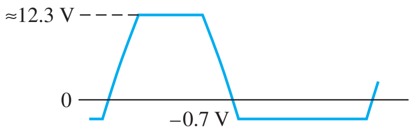
▲ **FIGURE ANS–7**

3. 5 Ω

5. 6.92 V

7. 14.3 V

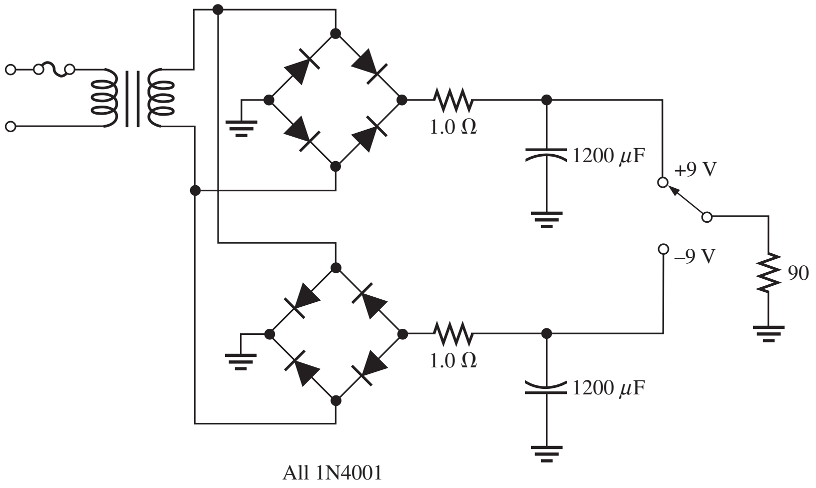
9. See Figure ANS–8.



▲ **FIGURE ANS–8**

11. 10.3%

13. 3.13%



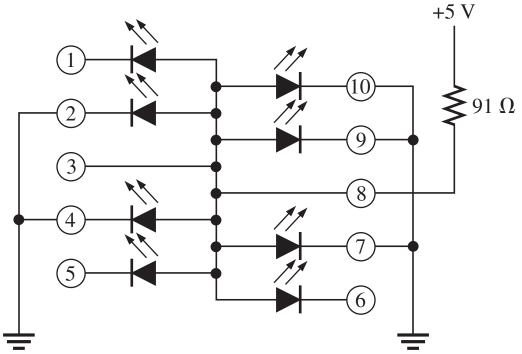
▲ **FIGURE ANS–6**

15. 5.88%

17. 3 V

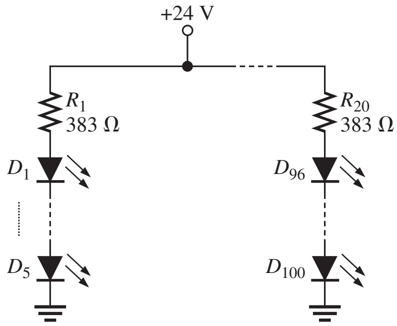
19. $V_R \cong 3$ V

21. See Figure ANS–9.


+5 V
91 Ω
1
2
3
4
5
10
9
8
7
6

▲ FIGURE ANS–9

23. See Figure ANS–10.


+24 V
R_1
383 Ω
R_{20}
383 Ω
D_1
D_5
D_{96}
D_{100}

▲ FIGURE ANS–10

25. **(a)** 30 kΩ **(b)** 8.57 kΩ **(c)** 5.88 kΩ

27. −750 Ω

29. The reflective ends cause the light to bounce back and forth, thus increasing the intensity of the light. The partially reflective end allows a portion of the reflected light to be emitted.

31. **(a)** ≈30 V dc

(b) 0 V

(c) Excessive 120 Hz ripple limited to 12 V by zener

(d) Full-wave rectified waveform limited at 12 V by zener

(e) 60 Hz ripple limited to 12 V

(f) 60 Hz ripple limited to 12 V

(g) 0 V

(h) 0 V

33. Incorrect transformer secondary voltage

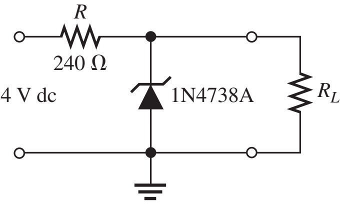
35. 48 mW

37. **(a)** 200 mA **(b)** 11 pF **(c)** 100 pF to 15.4 pF

39. **(a)** 1 μV **(b)** 940 nm **(c)** 830 nm

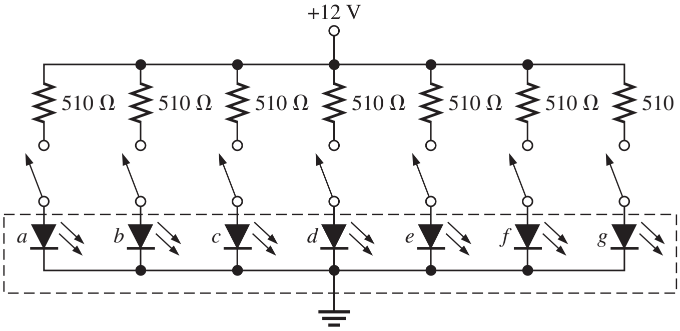
41. $V_{OUT(1)} = 6.8$ V; $V_{OUT(2)} = 24$ V

43. See Figure ANS–11.


R
240 Ω
24 V dc
1N4738A
R_L

▲ FIGURE ANS–11

45. See Figure ANS–12.


+12 V
510 Ω
510 Ω
510 Ω
510 Ω
510 Ω
510 Ω
510
a
b
c
d
e
f
g

▲ FIGURE ANS–12

47. Zener diode open

49. Zener diode shorted

Chapter 4

1. Holes

3. The base is narrow and lightly doped so that a small recombination (base) current is generated compared to the collector current.

5. Negative, positive

7. 0.947

9. 101.5

11. 8.98 mA

13. 0.99

15. 5.3 V increase

17. **(a)** $V_{BE} = 0.7$ V, $V_{CE} = 5.10$ V, $V_{CB} = 4.40$ V

(b) $V_{BE} = -0.7$ V, $V_{CE} = -3.83$ V, $V_{CB} = -3.13$ V

19. $I_B = 30$ μA, $I_E = 1.3$ mA, $I_C = 1.27$ mA

21. 3 μA

23. 425 mW

25. 33.3

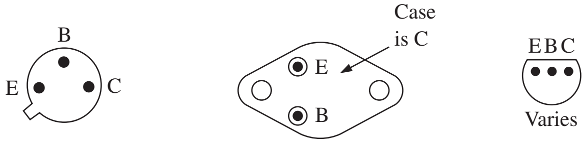
27. 1.1 kΩ

29. 500 μA, 3.33 μA, 4.03 V

31. 20 mA

33. 30 mA

35. See Figure ANS–13.



▲ FIGURE ANS–13

37. Open, low resistance

39. **(a)** 27.8 **(b)** 109

41. 60 Ω

43. **(a)** 40 V **(b)** 200 mA dc **(c)** 625 mW
(d) 500 mW **(e)** 70

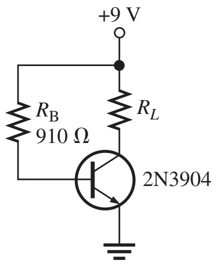
45. 840 mW

47. **(a)** Saturated **(b)** Not saturated

49. **(a)** No parameters are exceeded.
(b) No parameters are exceeded.

51. Yes, marginally; $V_{CE} = 1.5$ V; $I_C = 75$ mA

53. See Figure ANS–14.



▲ FIGURE ANS–14

55. R_B shorted

57. Collector-emitter shorted

59. R_E leaky

61. R_B open

Chapter 5

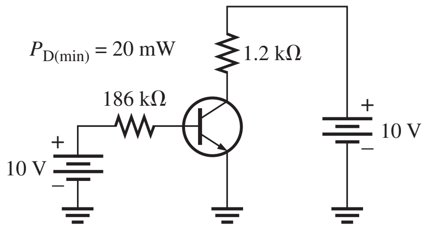
1. Saturation

3. 18 mA

5. $V_{CE} = 20$ V; $I_{C(sat)} = 2$ mA

7. See Figure ANS–15.

9. **(a)** $I_{C(sat)} = 50$ mA
(b) $V_{CE(CUTOFF)} = 10$ V
(c) $I_B = 250\ \mu$A; $I_C = 25$ mA; $V_{CE} = 5$ V

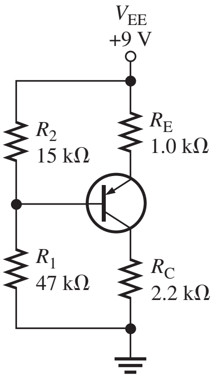


▲ FIGURE ANS–15

11. 63.2

13. $I_C \cong 809\ \mu$A; $V_{CE} = 13.2$ V

15. See Figure ANS–16.



▲ FIGURE ANS–16

17. **(a)** −1.63 mA, −8.16 V **(b)** 13.3 mW

19. $V_B = -186$ mV; $V_E = -0.886$ V; $V_C = 3.14$ V

21. 0.09 mA

23. $I_C = 16.3$ mA; $V_{CE} = -6.95$ V

25. 2.53 kΩ

27. 7.87 mA; 2.56 V

29. $I_{CQ} = 92.5$ mA; $V_{CEQ} = 2.75$ V

31. 27.7 mA to 69.2 mA; 6.23 V to 2.08 V; Yes

33. $V_1 = 0$ V, $V_2 = 0$ V, $V_3 = 8$ V

35. **(a)** Open collector **(b)** No problems
(c) Transistor shorted collector-to-emitter **(d)** Open emitter

37. **(a)** 1: 10 V, 2: float, 3: −3.59 V, 4: 10 V
(b) 1: 10 V, 2: 4.05 V, 3: 4.75 V, 4: 4.05 V
(c) 1: 10 V, 2: 0 V, 3: 0 V, 4: 10 V
(d) 1: 10 V, 2: 570 mV, 3: 1.27 V, 4: float
(e) 1: 10 V, 2: 0 V, 3: 0.7 V, 4: 0 V
(f) 1: 10 V, 2: 0 V, 3: 3.59 V, 4: 10 V

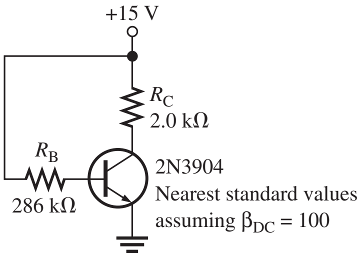
39. R_1 open, R_2 shorted, BE junction open

41. $V_C = V_{CC} = 9.1$ V, V_B normal, $V_E = 0$ V

43. None are exceeded.

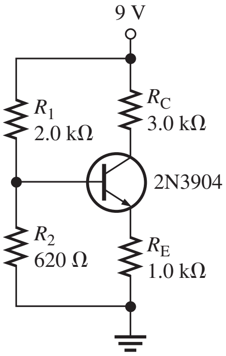
45. 457 mW

47. See Figure ANS–17.


+15 V
R_C
2.0 kΩ
R_B
286 kΩ
2N3904
Nearest standard values
assuming β_{DC} = 100

▲ FIGURE ANS–17

49. See Figure ANS–18.


9 V
R_1
2.0 kΩ
R_C
3.0 kΩ
2N3904
R_2
620 Ω
R_E
1.0 kΩ

▲ FIGURE ANS–18

51. Yes

53. V_{CEQ} will be less, causing the transistor to saturate at a slightly higher temperature, thus limiting the low temperature response.

55. R_C open

57. R_2 open

59. R_C shorted

Chapter 6

1. Slightly greater than 1 mA min.

3. 8.33 Ω

5. $r'_e \cong 19\ \Omega$

7. See Figure ANS–19.

9. 37.5 mW

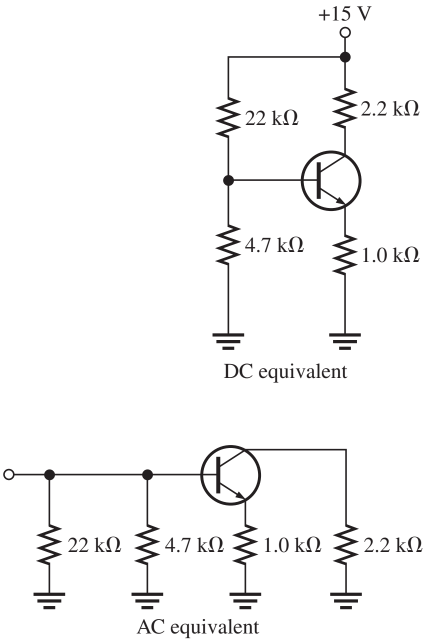
11. **(a)** 1.29 kΩ **(b)** 968 Ω **(c)** 171

13. **(a)** $I_E = 2.63$ mA **(b)** $V_E = 2.63$ V

(c) $V_B = 3.76$ V **(d)** $I_C \cong 2.63$ mA

(e) $V_C = 9.32$ V **(f)** $V_{CE} = 6.69$ V

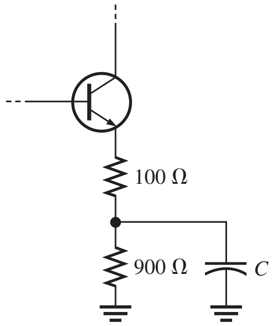
15. $A'_v = 131; \theta = 180°$


+15 V
22 kΩ
2.2 kΩ
4.7 kΩ
1.0 kΩ
DC equivalent
22 kΩ
4.7 kΩ
1.0 kΩ
2.2 kΩ
AC equivalent

▲ FIGURE ANS–19

17. $A_{v(max)} = 74.7, A_{v(min)} = 2.07$

19. A_v is reduced to 30.1. See Figure ANS–20.



▲ FIGURE ANS–20

21. $R_{in(tot)} = 3.1\ \text{k}\Omega; V_{OUT} = 1.06$ V

23. 270 Ω

25. 8.8

27. $R_{in(emitter)} = 2.28\ \Omega; A_v = 526; A_i \cong 1; A_p = 526$

29. 400

31. **(a)** $A_{v1} = 93.6, A_{v2} = 303$

(b) $A'_v = 28{,}361$

(c) $A_{v1(\text{dB})} = 39.4$ dB, $A_{v2(\text{dB})} = 49.6$ dB, $A'_{v(\text{dB})} = 89.1$ dB

33. $V_{B1} = 2.16$ V, $V_{E1} = 1.46$ V, $V_{C1} \cong 5.16$ V, $V_{B2} = 5.16$ V, $V_{E2} = 4.46$ V, $V_{C2} \cong 7.54$ V, $A_{v1} = 66, A_{v2} = 179$, $A'_v = 11{,}814$

35. **(a)** 1.41 **(b)** 2.00 **(c)** 3.16

(d) 10.0 **(e)** 100

37. V_1: differential output voltage
V_2: noninverting input voltage
V_3: single-ended output voltage
V_4: differential input voltage
I_1: bias current

39. **(a)** Single-ended differential input; differential output
(b) Single-ended differential input; single-ended output
(c) Double-ended differential input; single-ended output
(d) Double-ended differential input; differential output

41. Cutoff, 10 V

43.

TEST POINT	DC VOLTS	AC VOLTS (RMS)
Input	0 V	25 μV
Q_1 base	2.99 V	20.8 μV
Q_1 emitter	2.29 V	0 V
Q_1 collector	7.44 V	1.95 mV
Q_2 base	2.99 V	1.95 mV
Q_2 emitter	2.29 V	0 V
Q_2 collector	7.44 V	589 mV
Output	0 V	589 mV

45. **(a)** No output signal
(b) Reduced output signal
(c) No output signal
(d) Reduced output signal
(e) No output signal
(f) Increased output signal (perhaps with distortion)

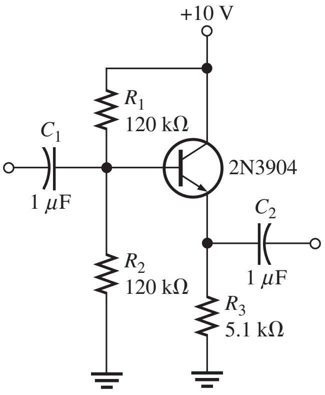
47. **(a)** Q_1 is in cutoff **(b)** V_{EE} **(c)** Unchanged

49. **(a)** 700 **(b)** 40 Ω **(c)** 20 kΩ

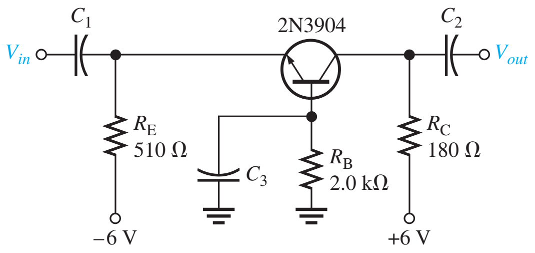
51. A leaky coupling capacitor affects the bias voltages and attenuates the ac voltage.

53. Make $R_9 = 69.1\ \Omega$.

55. See Figure ANS–21.


+10 V
R_1
120 kΩ
C_1
1 μF
2N3904
C_2
1 μF
R_2
120 kΩ
R_3
5.1 kΩ

▲ FIGURE ANS–21


C_1
2N3904
C_2
V_{in}
V_{out}
R_E
510 Ω
C_3
R_B
2.0 kΩ
R_C
180 Ω
−6 V
+6 V

▲ FIGURE ANS–22

57. See Figure ANS–22.

59. $A_v = R_C/r'_e$
$A_v \cong (V_{R_C}/I_C)/(0.025\text{ V}/I_C) = V_{R_C}/0.025 = 40V_{R_C}$

61. C_2 shorted

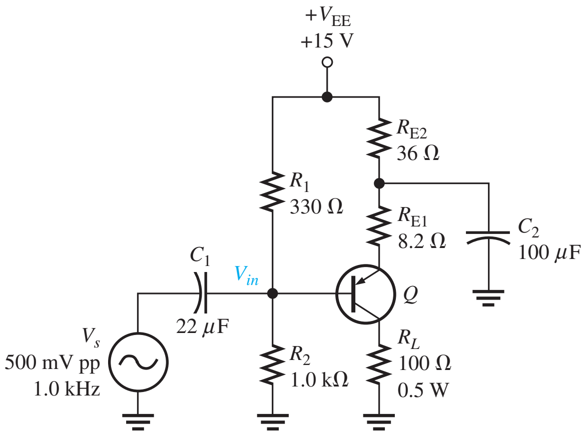
63. C_1 open

65. C_3 open

Chapter 7

1. **(a)** $I_{\text{CQ}} = 68.4$ mA; $V_{\text{CEQ}} = 5.14$ V
(b) $A_v = 11.7$; $A_p = 263$

3. The changes are shown on Figure ANS–23. The advantage of this arrangement is that the load resistor is referenced to ground.


$+V_{\text{EE}}$
+15 V
R_{E2}
36 Ω
R_1
330 Ω
R_{E1}
8.2 Ω
C_2
100 μF
C_1
V_{in}
Q
22 μF
V_s
500 mV pp
1.0 kHz
R_2
1.0 kΩ
R_L
100 Ω
0.5 W

▲ FIGURE ANS–23

5. **(a)** $I_{\text{C}} = 54$ mA; $V_{\text{CE}} = 2.3$ V
(b) $I_{\text{C}} = 15.7$ mA; $V_{\text{CE}} = 2.39$ V

7. For Figure 7–43(a): 46 mA, 2.3 V; For Figure 7–43(b): 10.2 mA, 2.39 V

9. 169 mW

11. **(a)** $V_{\text{B}(Q1)} = 0.7$ V; $V_{\text{B}(Q2)} = -0.7$ V; $V_{\text{E}} = 0$ V;
$V_{\text{CEQ}(Q1)} = 9$ V; $V_{\text{CEQ}(Q2)} = -9$ V; $I_{\text{CQ}} = 8.3$ mA
(b) $P_L = 0.5$ W

13. 457 Ω

15. **(a)** $V_{B(Q1)} = 8.2$ V; $V_{B(Q2)} = 6.8$ V;
$V_E = 7.5$ V;
$I_{CQ} = 6.8$ mA; $V_{CEQ(Q1)} = 7.5$ V;
$V_{CEQ(Q2)} = -7.5$ V
(b) $P_L = 167$ mW

17. **(a)** C_2 open or Q_2 open
(b) Power supply off, open R_1, Q_1 base shorted to ground
(c) Q_1 has collector-to-emitter short
(d) One or both diodes shorted

19. 450 μW

21. 24 V

23. Negative half of input cycle

25. **(a)** No dc supply voltage or R_1 open
(b) D_2 open
(c) No fault
(d) Q_1 shorted C-to-E

27. −15 V dc, output signal same as input signal

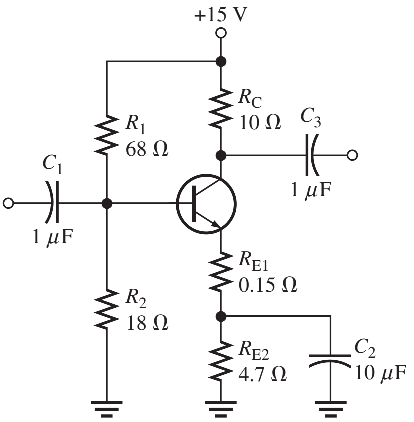
29. The vertically oriented diode is connected backwards.

31. 10 W

33. Gain increases, then decreases at a certain value of I_C.

35. T_C is much closer to the actual junction temperature than T_A. In a given operating environment, T_A is always less than T_C.

37. See Figure ANS–24.



▲ FIGURE ANS–24

39. C_{in} open

41. Q_1 collector-emitter open

43. Q_2 drain-source open

Chapter 8

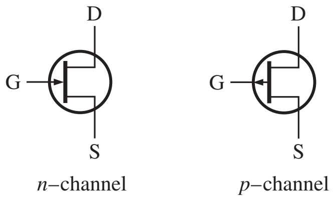
1. **(a)** Narrows **(b)** Increases

3. See Figure ANS–25.

5. 5 V

7. 10 mA

9. 4 V



▲ FIGURE ANS–25

11. −2.63 V

13. $g_m = 1429\ \mu$S, $g_{fs} = 1429\ \mu$S

15. $V_{GS} = 0$ V, $I_D = 8$ mA
$V_{GS} = -1$ V, $I_D = 5.12$ mA
$V_{GS} = -2$ V, $I_D = 2.88$ mA
$V_{GS} = -3$ V, $I_D = 1.28$ mA
$V_{GS} = -4$ V, $I_D = 0.320$ mA
$V_{GS} = -5$ V, $I_D = 0$ mA

17. 800 Ω

19. **(a)** 20 mA **(b)** 0 A **(c)** Increases

21. 211 Ω

23. 9.80 MΩ

25. $I_D \cong 5.3$ mA, $V_{GS} \cong 2.1$ V

27. $I_D \cong 1.9$ mA, $V_{GS} \cong -1.5$ V

29. From 1.33 kΩ to 2.67 kΩ

31. 935 Ω

33. The enhancement mode

35. The gate is insulated from the channel.

37. 4.69 mA

39. **(a)** Depletion **(b)** Enhancement
(c) Zero bias **(d)** Depletion

41. **(a)** 4 V **(b)** 5.4 V **(c)** −4.52 V

43. **(a)** 5 V, 3.18 mA **(b)** 3.2 V, 1.02 mA

45. The input resistance of an IGBT is very high because of the insulated gate structure.

47. R_D or R_S open, JFET open D-to-S, $V_{DD} = 0$ V, or ground connection open.

49. Essentially no change

51. The 1.0 MΩ bias resistor is open.

53. $V_{G2S} = 6$ V, $I_D \cong 10$ mA; $V_{G2S} = 1$ V, $I_D \cong 5$ mA

55. 3.04 V

57. **(a)** −0.5 V **(b)** 25 V **(c)** 310 mW **(d)** −25 V

59. 2000 μS

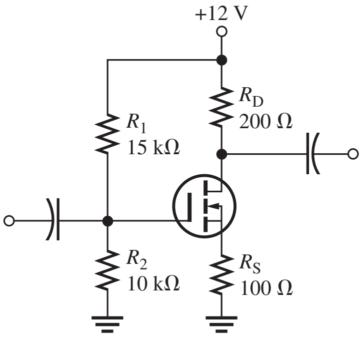
61. $I_D \cong 1.4$ mA

63. $I_D \cong 13$ mA when $V_{GS} = +3$ V, $I_D \cong 0.4$ mA when $V_{GS} = -2$ V.

65. −3.0 V

67. $I_D = 3.58$ mA; $V_{GS} = -4.21$ V

69. 6.01 V



▲ FIGURE ANS–26

71. See Figure ANS–26.

73. R_D shorted

75. R_1 open

77. R_D open

79. Drain-source shorted

Chapter 9

1. **(a)** 60 μA **(b)** 900 μA **(c)** 3.6 mA **(d)** 6 mA

3. 14.2

5. **(a)** *n*-channel D-MOSFET with zero-bias; $V_{GS} = 0$

(b) *p*-channel JFET with self-bias; $V_{GS} = -0.99$ V

(c) *n*-channel E-MOSFET with voltage-divider bias; $V_{GS} = 3.84$ V

7. **(a)** *n*-channel D-MOSFET

(b) *n*-channel JFET

(c) *p*-channel E-MOSFET

9. Figure 9–16(b): approximately 4 mA
Figure 9–16(c): approximately 3.2 mA

11. 920 mV

13. **(a)** 4.32 **(b)** 9.92

15. 7.5 mA

17. 2.54

19. 33.6 mV rms

21. 9.84 MΩ

23. $V_{GS} = 9$ V; $I_D = 3.13$ mA; $V_{DS} = 13.3$ V; $V_{ds} = 675$ mV

25. $R_{in} \cong 10$ MΩ; $A_v = 0.620$

27. **(a)** 0.906 **(b)** 0.299

29. 250 Ω

31. $A_v = 2640$; $R_{in} = 14.6$ MΩ

33. 0.95

35. 30 kHz

37. 40 kΩ

39. **(a)** 3.3 V **(b)** 3.3 V **(c)** 3.3 V **(d)** 0 V

41. The MOSFET has lower on-state resistance and can turn off faster.

43. **(a)** $V_{out} = 0$ V if C_1 is open

(b) $A_{v1} = 7.5$, $A_{v2} = 2.24$, $A_v = 16.8$, $V_{out} = 168$ mV

(c) $V_{GS} = 0$ V for Q_2. $I_D = I_{DSS}$. Output is clipped.

(d) No V_{out} because no signal at Q_2 gate.

45. **(a)** −3.0 V **(b)** 20 V dc

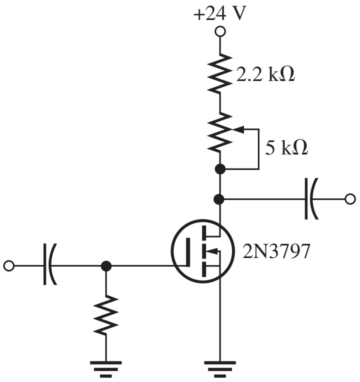
(c) 200 mW **(d)** ±10 V dc

47. 900 μS

49. 1.5 mA

51. 2.0; 6.82

53. See Figure ANS–27.



▲ FIGURE ANS–27

55. C_2 open

57. R_S shorted

59. R_1 open

61. R_2 open

Chapter 10

1. If $C_1 = C_2$, the critical frequencies are equal, and they will both cause the gain to drop at 40 dB/decade below f_c.

3. BJT: C_{be}, C_{bc}, C_{ce}; FET: C_{gs}, C_{gd}, C_{ds}

5. 812 pF

7. $C_{in(miller)} = 6.95$ pF; $C_{out(miller)} \cong 5.28$ pF

9. 24 mV rms; 34 dB

11. **(a)** 3.01 dBm **(b)** 0 dBm

(c) 6.02 dBm **(d)** −6.02 dBm

13. **(a)** 318 Hz

(b) 1.59 kHz

15. At 0.1f_c: $A_v = 18.8$ dB

At f_c: $A_v = 35.8$ dB

At 10f_c: $A_v = 38.8$ dB

17. Input *RC* circuit: $f_c = 3.34$ Hz

Output *RC* circuit: $f_c = 3.01$ kHz

Output f_c is dominant.

19. Input circuit: $f_c = 4.32$ MHz
Output circuit: $f_c = 94.9$ MHz
Input f_c is dominant.

21. Input circuit: $f_c = 12.9$ MHz
Output circuit: $f_c = 54.5$ MHz
Input f_c is dominant.

23. $f_{cl} = 136$ Hz, $f_{cu} = 8$ kHz

25. $BW = 5.26$ MHz, $f_{cu} \cong 5.26$ MHz

27. 230 Hz; 1.2 MHz

29. 514 kHz

31. ≈2.5 MHz

33. Increase the frequency until the output voltage drops to 3.54 V rms. This is f_{cu}.

35. 15.9 Hz

37. No effect

39. 112 pF

41. $C_{gd} = 1.3$ pF; $C_{gs} = 3.7$ pF; $C_{ds} = 3.7$ pF

43. ≈10.9 MHz

45. R_C open

47. R_2 open

Chapter 11

1. $I_A = 24.1$ mA

3. See "Turning the SCR On" in Section 11–2.

5. When the switch is closed, the battery V_2 causes illumination of the lamp. The light energy causes the LASCR to conduct and thus energize the relay. When the relay is energized, the contacts close and 115 V ac are applied to the motor.

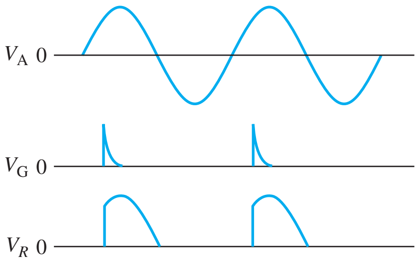
7. Add a transistor to provide inversion of negative half-cycle in order to obtain a positive gate trigger.

9. See Figure ANS–28.

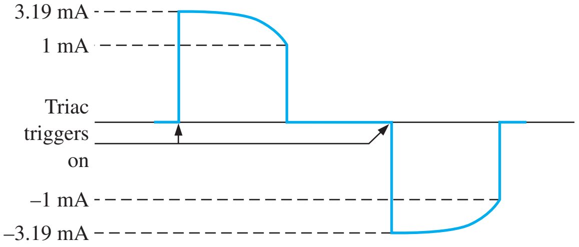
11. See Figure ANS–29.

13. Anode, cathode, anode gate, cathode gate

15. 6.48 V



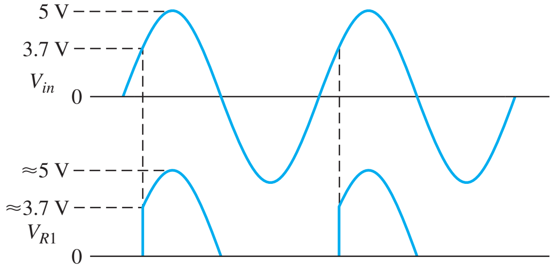
▲ FIGURE ANS–28



▲ FIGURE ANS–29

17. **(a)** 9.79 V **(b)** 5.2 V

19. See Figure ANS–30.

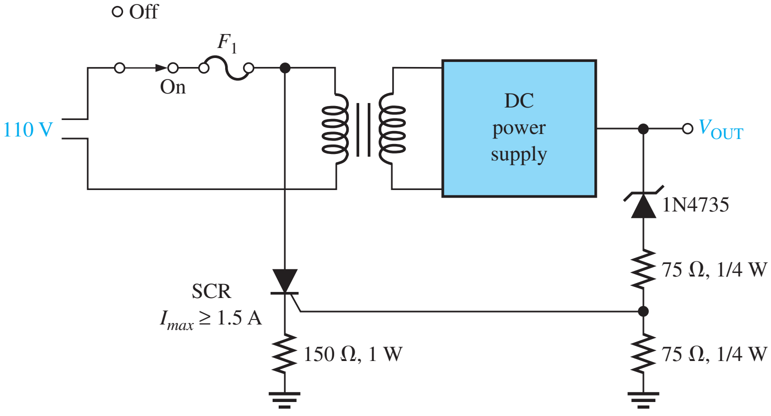


▲ FIGURE ANS–30

21. 0 V

23. As the PUT gate voltage increases, the PUT triggers on later to the ac cycle causing the SCR to fire later in the cycle, conduct for a shorter time, and decrease power to the motor.

25. See Figure ANS–31.



▲ FIGURE ANS–31

27. Cathode-anode shorted

29. R_1 shorted

Chapter 12

1. *Practical op-amp:* High open-loop gain, high input impedance, low output impedance, high CMRR.
Ideal op-amp: Infinite open-loop gain, infinite input impedance, zero output impedance, infinite CMRR.

3. **(a)** Single-ended differential input

(b) Double-ended differential input

(c) Common-mode input

5. 120 dB

7. 8.1 μA

9. 1.6 V/μs

11. **(a)** Voltage-follower **(b)** Noninverting **(c)** Inverting

13. **(a)** $A_{cl(NI)} = 374$ **(b)** $V_{out} = 3.74$ V rms

(c) $V_f = 9.99$ mV rms

15. **(a)** 49 kΩ **(b)** 3 MΩ **(c)** 84 kΩ **(d)** 165 kΩ

17. **(a)** 10 mV, in phase

(b) −10 mV, 180° out of phase

(c) 223 mV, in phase

(d) −100 mV, 180° out of phase

19. **(a)** $Z_{in(NI)} = 8.41\ \text{G}\Omega$; $Z_{out(NI)} = 89.2\ \text{m}\Omega$

(b) $Z_{in(NI)} = 6.20\ \text{G}\Omega$; $Z_{out(NI)} = 4.04\ \text{m}\Omega$

(c) $Z_{in(NI)} = 5.30\ \text{G}\Omega$; $Z_{out(NI)} = 19.0\ \text{m}\Omega$

21. **(a)** $Z_{in(I)} = 10\ \text{k}\Omega$; $Z_{out(I)} = 5.12\ \text{m}\Omega$

(b) $Z_{in(I)} = 100\ \text{k}\Omega$; $Z_{out(I)} = 7.32\ \text{m}\Omega$

(c) $Z_{in(I)} = 470\ \Omega$; $Z_{out(I)} = 6.22\ \text{m}\Omega$

23. **(a)** 2.69 kΩ **(b)** 1.45 kΩ **(c)** 53 kΩ

R_c is placed between V_{in} and the + input

25. 175 nV

27. $A_v = 125{,}892$; $BW_{ol} = 200$ Hz

29. **(a)** 0.997 **(b)** 0.923 **(c)** 0.707

(d) 0.515 **(e)** 0.119

31. **(a)** −51.5° **(b)** −7.17° **(c)** −85.5°

33. **(a)** 90 dB **(b)** −281°

35. **(a)** 29.8 dB **(b)** 23.9 dB **(c)** 0 dB

All are closed-loop gains.

37. 71.7 dB

39. **(a)** $A_{cl(VF)} = 1$; $BW = 2.8$ MHz

(b) $A_{cl(I)} = -45.5$; $BW = 61.6$ kHz

(c) $A_{cl(NI)} = 13$; $BW = 215$ kHz

(d) $A_{cl(I)} = -179$; $BW = 15.7$ kHz

41. **(a)** Faulty op-amp or R_1 open

(b) R_2 open, forcing open-loop operation

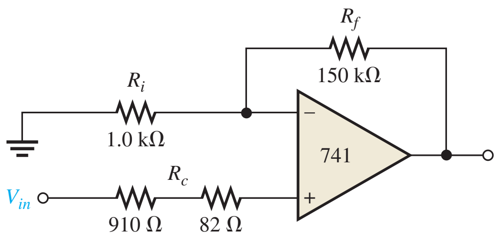
43. The gain becomes a fixed −100, with no effect as the gain potentiometer is adjusted.

45. Op-amp gain will be reduced by 100.

47. $Z_{in(NI)} = 3.96\ \text{G}\Omega$

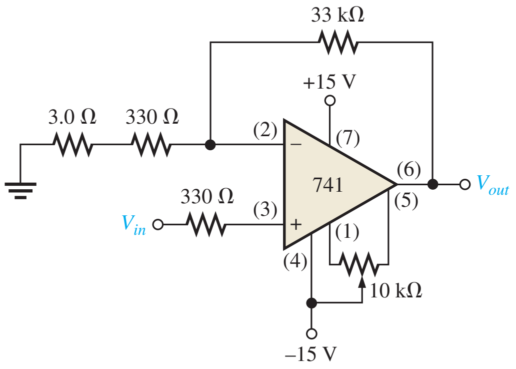
49. 50,000

51. See Figure ANS–32.



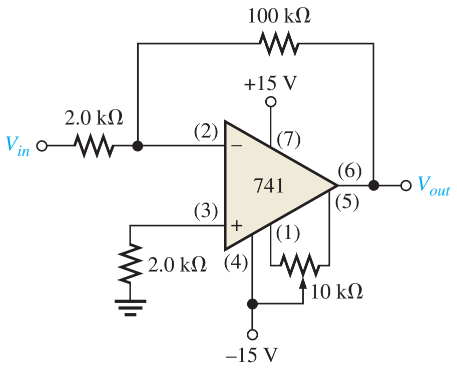
▲ **FIGURE ANS–32**

53. See Figure ANS–33.



▲ **FIGURE ANS–33**

55. See Figure ANS–34.



▲ **FIGURE ANS–34**

57. R_f open

59. R_f leaky

61. R_f shorted

63. R_f leaky

65. R_i shorted

67. R_f open

69. R_f open

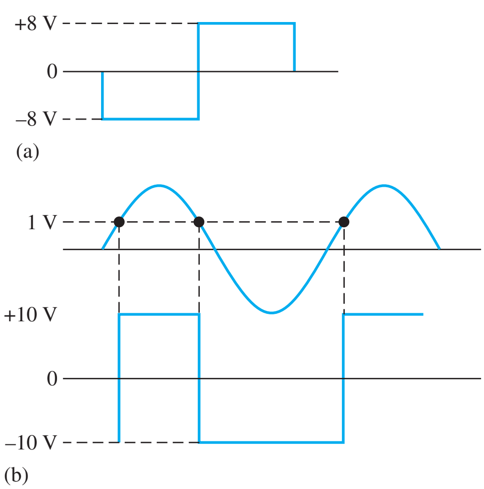
71. R_i open

Chapter 13

1. 24 V, with distortion

3. $V_{\text{UTP}} = 2.77\text{ V}, V_{\text{LTP}} = -2.77\text{ V}$

5. See Figure ANS–35.



▲ FIGURE ANS–35

7. 8.57 V and −0.968 V

9. **(a)** −2.5 V

(b) −3.52 V

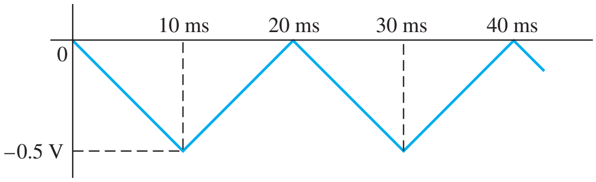
11. 110 kΩ

13. $V_{\text{OUT}} = -3.57\text{ V}, I_f = 357\ \mu\text{A}$

15. −4.06 mV/μs

17. 1 mA

19. See Figure ANS–36.



▲ FIGURE ANS–36

21. Output not correct; R_2 is open.

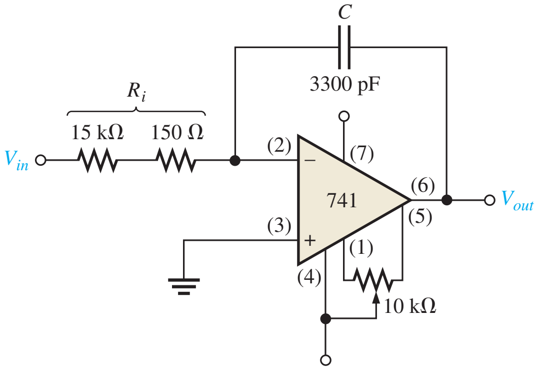
23. 50 kΩ resistor open

25. An increase in susceptibility to power line noise.

27. min. duty cycle = 6.39%

max. duty cycle = 93.6%

29. $f_{in} = 100$ kHz. See Figure ANS–37.



▲ FIGURE ANS–37

31. Op-amp inputs shorted together

33. D_1 shorted

35. Middle 10 kΩ resistor shorted

37. R_f open

39. C open

Chapter 14

1. $A_{v(1)} = A_{v(2)} = 101$

3. 1.005 V

5. 51.5

7. Change R_G to 2.2 kΩ.

9. 300

11. Change the 18 kΩ resistor to 68 kΩ.

13. Connect pin 6 directly to pin 10, and connect pin 14 directly to pin 15 to make $R_f = 0$.

15. 500 μA, 5 V

17. $A_v \cong 11.6$

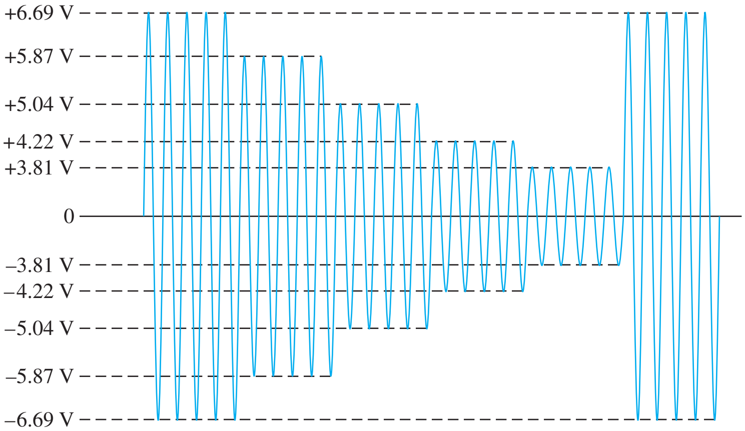
19. See Figure ANS–38.

21. See Figure ANS–39.

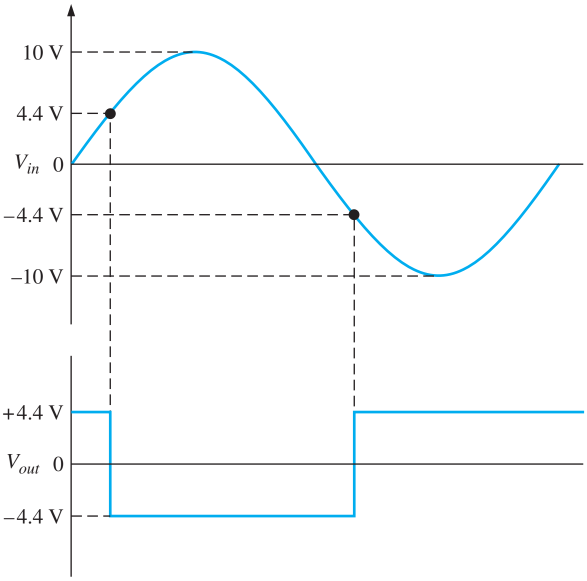
23. **(a)** −0.301 **(b)** 0.301 **(c)** 1.70 **(d)** 2.11

25. The output of a log amplifier is limited to 0.7 V because of the transistor's *pn* junction.

27. −157 mV



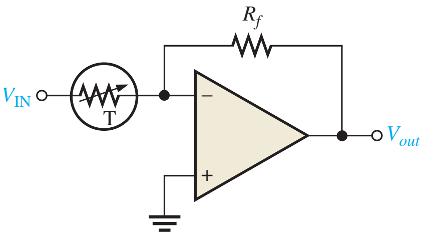
▲ FIGURE ANS–38



▲ FIGURE ANS–39

29. $V_{out(max)} = -147$ mV, $V_{out(min)} = -89.2$ mV; the 1 V input peak is reduced 85% whereas the 100 mV input peak is reduced only 10%.

31. See Figure ANS–40.



▲ FIGURE ANS–40

33. *R* open

35. Zener diode open

Chapter 15

1. **(a)** Band-pass **(b)** High-pass
(c) Low-pass **(d)** Band-stop

3. 48.2 kHz, No

5. 700 Hz, 5.04

7. **(a)** 1, not Butterworth
(b) 1.44, approximate Butterworth
(c) 1st stage: 1.67; 2nd stage: 1.67; Not Butterworth

9. **(a)** Chebyshev **(b)** Butterworth
(c) Bessel **(d)** Butterworth

11. 190 Hz

13. Add another identical stage and change the ratio of the feedback resistors to 0.068 for first stage, 0.586 for second stage, and 1.482 for third stage.

15. Exchange positions of resistors and capacitors.

17. **(a)** Decrease R_1 and R_2 or C_1 and C_2.
(b) Increase R_3 or decrease R_4.

19. **(a)** $f_0 = 4.95$ kHz, $BW = 3.84$ kHz
(b) $f_0 = 449$ Hz, $BW = 96.4$ Hz
(c) $f_0 = 15.9$ kHz, $BW = 838$ Hz

21. Sum the low-pass and high-pass outputs with a two-input adder.

23. R_4 shorted

25. C_3 shorted

27. R_1 open

29. R_1 open

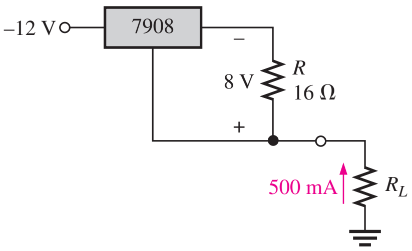
31. R_7 open

Chapter 16

1. An oscillator requires no input (other than dc power).
3. $\frac{1}{75} = 0.0133$
5. 733 mV
7. 50 kΩ
9. 2.34 kΩ
11. 136 kΩ, 628 Hz
13. 10
15. Change R_1 to 3.54 kΩ
17. $R_4 = 65.8\text{ k}\Omega, R_5 = 47\text{ k}\Omega$
19. 3.33 V, 6.67 V
21. 0.0076 μF
23. Drain-to-source shorted
25. Collector-to-emitter shorted
27. R_2 open

Chapter 17

1. 0.0333%
3. 1.01%
5. A: Reference voltage, B: Control element, C: Error detector, D: Sampling circuit
7. 8.51 V
9. 9.57 V
11. 500 mA
13. 10 mA
15. $I_{L(max)} = 250\text{ mA}, P_{R1} = 6.25\text{ W}$
17. 40%
19. V_{OUT} decreases
21. 14.3 V
23. 1.3 mA
25. 2.8 Ω
27. $R_{limit} = 0.35\ \Omega$
29. See Figure ANS–41.



▲ FIGURE ANS–41

31. R_2 leaky
33. Q_2 collector-to-emitter open

Chapter 18

1. Simple instructions, conditional instructions, loop instructions, branching instructions, and exception instructions
3. One possible pseudocode description is

```
program PrintAverage
   begin
      input first number
      input second number
      input third number
      sum is first number plus second
         number plus third number
      average is sum divided by 3
      print average
   end PrintAverage
```

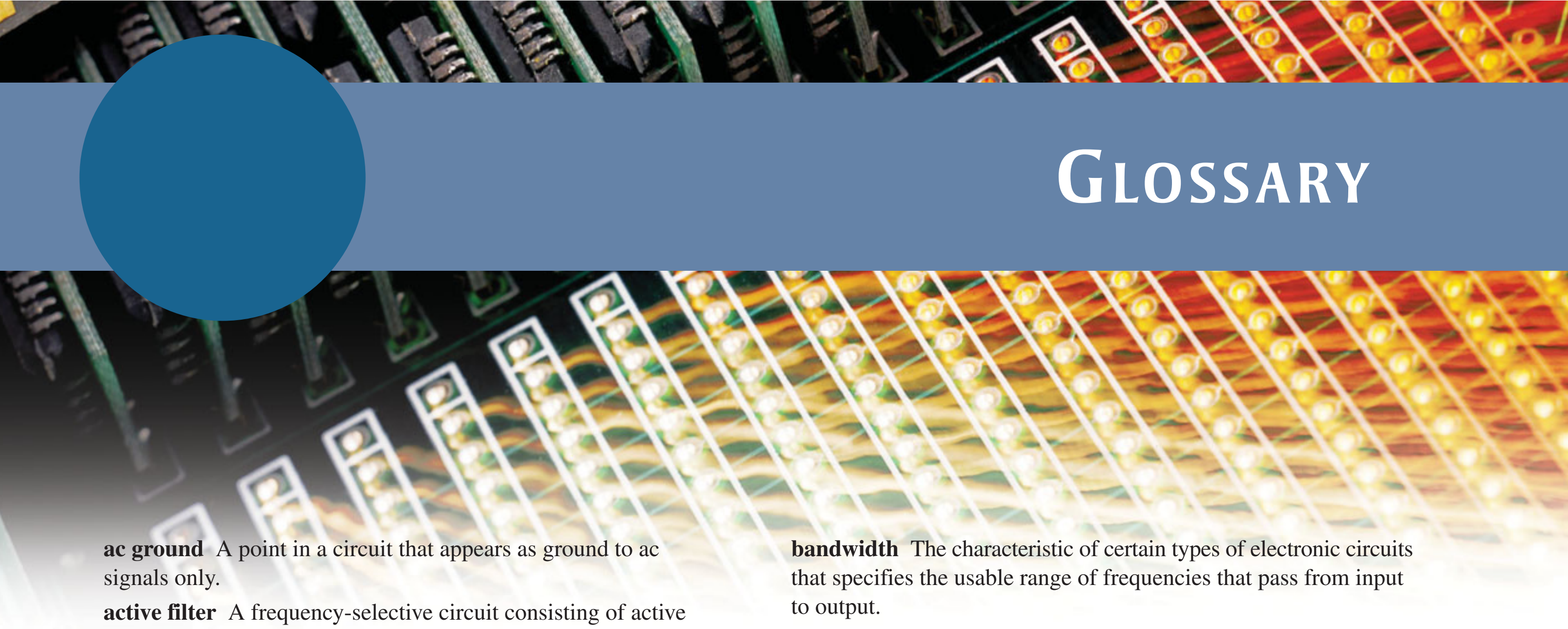
5. Advantages of electromechanical relays are good electrical isolation and high current and voltage handling ability.
7. The flowchart represents a simple sequential program, as none of the program operations alters the sequence of program execution from its linear process flow.
9. One possible pseucode description is

```
NewIdentifyKeyValue
   begin
      input key value
      case (key value)
         begin case
            "1":     print "Key value equals 1"
                     break
            "2":     print "Key value equals 2"
                     break
            "3":     print "Key value equals 3"
                     break
            default: print "Key value is more than 3"
                     break
         end case
   end NewIdentifyKeyValue
```

11. The FOR-TO-STEP loop will execute once each for index values of 1 through 10, and exit on an index value of 11. The sum begins at 0 and each loop will add the index value plus 1, so

$$\begin{aligned}\text{sum} &= (1{+}1) + (2{+}1) + (3{+}1) + (4{+}1) + (5{+}1) + (6{+}1) \\ &\quad + (7{+}1) + (8{+}1) + (9{+}1) + (10{+}1) \\ &= 2 + 3 + 4 + 5 + 6 + 7 + 8 + 9 + 10 + 11 \\ &= 65\end{aligned}$$

13. **(a)** Unconditional branches too often encourage poor programming practices by compensating for poorly designed code.
    (b) Unrestricted unconditional branching typically results in “spaghetti code” that is difficult to modify and maintain.
    (c) Replacing the branch instruction with the desired target instruction(s) produces the same result as the unconditional branch, so that unconditional branches are often unnecessary.



GLOSSARY

ac ground A point in a circuit that appears as ground to ac signals only.

active filter A frequency-selective circuit consisting of active devices such as transistors or op-amps coupled with reactive components.

A/D conversion A process whereby information in analog form is converted into digital form.

alpha (α) The ratio of dc collector current to dc emitter current in a bipolar junction transistor.

amplification The process of increasing the power, voltage, or current by electronic means.

amplifier An electronic circuit having the capability to amplify power, voltage, or current.

analog Characterized by a linear process in which a variable takes on a continuous set of values.

analog switch A device that switches an analog signal on and off.

anode The *p* region of a diode.

antilogarithm The result obtained when the base of a number is raised to a power equal to the logarithm of that number.

assembly language A low-level programming language that represents each machine language instruction with an English-like instruction that is easier to remember than groups of 0s and 1s.

astable Characterized by having no stable states.

atom The smallest particle of an element that possesses the unique characteristics of that element.

atomic number The number of protons in an atom.

attenuation The reduction in the level of power, current, or voltage.

automated test system A system that operates under the control of an automated controller to conduct tests on a component, circuit, or system.

avalanche breakdown The higher voltage breakdown in a zener diode.

avalanche effect The rapid buildup of conduction electrons due to excessive reverse-bias voltage.

band gap The difference in energy between energy levels in an atom.

band-pass filter A type of filter that passes a range of frequencies lying between a certain lower frequency and a certain higher frequency.

band-stop filter A type of filter that blocks or rejects a range of frequencies lying between a certain lower frequency and a certain higher frequency.

bandwidth The characteristic of certain types of electronic circuits that specifies the usable range of frequencies that pass from input to output.

barrier potential The amount of energy required to produce full conduction across the *pn* junction in forward bias.

base One of the semiconductor regions in a BJT. The base is very thin and lightly doped compared to the other regions.

Bessel A type of filter response having a linear phase characteristic and less than −20 dB/decade/pole rolloff.

beta (β) The ratio of dc collector current to dc base current in a BJT; current gain from base to collector.

bias The application of a dc voltage to a diode, transistor, or other device to produce a desired mode of operation.

bipolar Characterized by both free electrons and holes as current carriers.

BJT Bipolar junction transistor; a transistor constructed with three doped semiconductor regions separated by two *pn* junctions.

Bode plot An idealized graph of the gain in dB versus frequency used to graphically illustrate the response of an amplifier or filter.

bounding The process of limiting the output range of an amplifier or other circuit.

branching Redirection of program execution to some program location other than what immediately follows in memory.

breakdown The phenomenon of a sudden and drastic increase when a certain voltage is reached across a device.

bridge rectifier A type of full-wave rectifier consisting of diodes arranged in a four-cornered configuration.

Butterworth A type of filter response characterized by flatness in the passband and a −20 dB/decade/pole roll-off.

bypass capacitor A capacitor placed across the emitter resistor of an amplifier.

CAM Configurable analog module; a predesigned analog circuit used in an FPAA or dpASP for which some of its parameters can be selectively programmed.

capacitance ratio The ratio of varactor capacitances at minimum and at maximum reverse voltages.

cascade An arrangement of circuits in which the output of one circuit becomes the input to the next.

cascode A FET amplifier configuration in which a common-source amplifier and a common-gate amplifier are connected in a series arrangement.

cathode The *n* region of a diode.

center-tapped rectifier A type of full-wave rectifier consisting of a center-tapped transformer and two diodes.

channel The conductive path between the drain and source in a FET.

Chebyshev A type of filter response characterized by ripples in the passband and a greater than -20 dB/decade/pole roll-off.

clamper A circuit that adds a dc level to an ac voltage using a diode and a capacitor.

class A A type of amplifier that operates entirely in its linear (active) region.

class AB A type of amplifier that is biased into slight conduction.

class B A type of amplifier that operates in the linear region for 180° of the input cycle because it is biased at cutoff.

class C A type of amplifier that operates only for a small portion of the input cycle.

class D A nonlinear amplifier in which the transistors are operated as switches.

clipper See Limiter.

closed-loop An op-amp configuration in which the output is connected back to the input through a feedback circuit.

closed-loop voltage gain (A_{cl}) The voltage gain of an op-amp with external feedback.

CMOS Complementary MOS.

CMRR Common-mode rejection ratio; the ratio of open-loop gain to common-mode gain; a measure of an op-amp's ability to reject common-mode signals.

coherent light Light having only one wavelength.

cohesion An indication of how well a procedure or program keeps together the code associated with a specific task.

collector The largest of the three semiconductor regions of a BJT.

common-base (CB) A BJT amplifier configuration in which the base is the common terminal to an ac signal or ground.

common-collector (CC) A BJT amplifier configuration in which the collector is the common terminal to an ac signal or ground.

common-drain (CD) A FET amplifier configuration in which the drain is the grounded terminal.

common-emitter (CE) A BJT amplifier configuration in which the emitter is the common terminal to an ac signal or ground.

common-gate (CG) A FET amplifier configuration in which the gate is the grounded terminal.

common mode A condition where two signals applied to differential inputs are of the same phase, frequency, and amplitude.

common-source (CS) A FET amplifier configuration in which the source is the grounded terminal.

comparator A circuit which compares two input voltages and produces an output in either of two states indicating the greater or less than relationship of the inputs.

complementary symmetry transistors Two transistors, one *npn,* and one *pnp,* having matched characteristics.

conditional execution The selective processing of program instructions based upon the validity of some condition.

conduction electron A free electron.

conductor A material that conducts electrical current very well.

core The central part of an atom, includes the nucleus and all but the valence electrons.

coupling An indication of how much one part of a program interacts with or potentially affects another part of the program.

covalent Related to the bonding of two or more atoms by the interaction of their valence electrons.

critical frequency The frequency at which the response of an amplifier or filter is 3 dB less than at midrange.

crossover distortion Distortion in the output of a class B push-pull amplifier at the point where each transistor changes from the cutoff state to the *on* state.

crystal A solid material in which the atoms are arranged in a symmetrical pattern.

CTR Current transfer ratio. An indication of how efficiently a signal is coupled from input to output.

current The rate of flow of electrical charge.

current mirror A circuit that uses matching diode junctions to form a current source. The current in a diode junction is reflected as a matching current in the other junction (which is typically the base-emitter junction of a transistor). Current mirrors are commonly used to bias a push-pull amplifier.

cutoff The nonconducting state of a transistor.

cutoff frequency Another term for critical frequency.

cutoff voltage The value of the gate-to-source voltage that makes the drain current approximately zero.

D/A conversion The process of converting a sequence of digital codes to an analog form.

damping factor A filter characteristic that determines the type of response.

dark current The amount of thermally generated reverse current in a photodiode in the absence of light.

Darlington pair A configuration of two transistors in which the collectors are connected and the emitter of the first drives the base of the second to achieve beta multiplication.

dBm A unit for measuring power levels referenced to 1 mW.

dc load line A straight line plot of I_C and V_{CE} for a transistor circuit.

dc power supply The dc power of an amplifier with no input signal.

decade A ten-times increase or decrease in the value of a quantity such as frequency.

decibel (dB) A logarithmic measure of the ratio of one power to another or one voltage to another.

depletion In a MOSFET, the process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.

depletion region The area near a *pn* junction on both sides that has no majority carriers.

diac A two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction when properly activated.

differential amplifier (diff-amp) An amplifier in which the output is a function of the difference between two input voltages, used as the input stage of an op-amp.

differential mode A mode of op-amp operation in which two opposite polarity signal voltages are applied to two inputs (double-ended) or in which a signal is applied to one input and ground to the other (single-ended).

differentiator A circuit that produces an output which approximates the instantaneous rate of change of the input function.

digital Characterized by a process in which a variable takes on either of two values.

diode A semiconductor device with a single *pn* junction that conducts current in only one direction.

diode drop The voltage across the diode when it is forward-biased; approximately the same as the barrier potential and typically 0.7 V for silicon.

doping The process of imparting impurities to an intrinsic semiconductive material in order to control its conduction characteristics.

downloading The process of implementing the software description of a circuit in an FPAA.

drain One of the three terminals of a FET analogous to the collector of a BJT.

dynamic reconfiguration The process of downloading a design modification or new design in an FPAA while it is operating in a system without the need to power down or reset the system; also known as "on-the-fly" reprogramming.

dynamic resistance The nonlinear internal resistance of a semiconductive material.

efficiency The ratio of the signal power delivered to a load to the power from the power supply of an amplifier.

electroluminescence The process of releasing light energy by the recombination of electrons in a semiconductor.

electron cloud In the quantum model, the area around an atom's nucleus where an electron can probably be found.

electrostatic discharge (ESD) The discharge of a high voltage through an insulating path that can destroy an electronic device.

electron The basic particle of negative electrical charge.

electron-hole pair The conduction electron and the hole created when the electron leaves the valence band.

emitter The most heavily doped of the three semiconductor regions of a BJT.

emitter-follower A popular term for a common-collector amplifier.

enhancement In a MOSFET, the process of creating a channel or increasing the conductivity of the channel by the addition of charge carriers.

feedback The process of returning a portion of a circuit's output back to the input in such a way as to oppose or aid a change in the output.

feedback oscillator An electronic circuit that operates with positive feedback and produces a time-varying output signal without an external input signal.

FET Field-effect transistor; a type of unipolar, voltage-controlled transistor that uses an induced electric field to control current.

filter In a power supply, a capacitor used to reduce the variation of the output voltage from a rectifier; a type of circuit that passes or blocks certain frequencies to the exclusion of all others.

floating point A point in the circuit that is not electrically connected to ground or a "solid" voltage.

flowchart A graphical means of representing the organization and process flow of a program using distinctively-shaped interconnected blocks.

fold-back current limiting A method of current limiting in voltage regulators.

forced commutation A method of turning off an SCR.

forward bias The condition in which a diode conducts current.

forward-breakover voltage ($V_{BR(F)}$) The voltage at which a device enters the forward-blocking region.

4-layer diode The type of two-terminal thyristor that conducts current when the anode-to-cathode voltage reaches a specified "breakover" value.

FPAA Field-programmable analog array; an integrated circuit that can be programmed for implementation of an analog circuit design.

free electron An electron that has acquired enough energy to break away from the valance band of the parent atom; also called a conduction electron.

frequency response The change in gain or phase shift over a specified range of input signal frequencies.

full-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with two output pulses occurring for each input cycle.

fuse A protective device that burns open when the current exceeds a rated limit.

gain The amount by which an electrical signal is increased or amplified.

gain-bandwidth product A constant parameter which is always equal to the frequency at which the op-amp's open-loop gain is unity (1).

gate One of the three terminals of a FET analogous to the base of a BJT.

germanium A semiconductive material.

half-wave rectifier A circuit that converts an ac sinusoidal input voltage into a pulsating dc voltage with one output pulse occurring for each input cycle.

hierarchical structure A means of using multiple levels of detail to represent information, with subparts of higher levels shown in greater detail in lower levels.

high-level languages Programming languages in which each instruction represents multiple machine language instructions and do not interact directly with the computer hardware.

high-level programming Programming in which instructions represent multiple machine language instructions and do not interact directly with the processor hardware.

high-pass filter A type of filter that passes frequencies above a certain frequency while rejecting lower frequencies.

holding current **(I_H)** The value of the anode current below which a device switches from the forward-conduction region to the forward-blocking region.

hole The absence of an electron in the valence band of an atom.

hysteresis Characteristic of a circuit in which two different trigger levels create an offset or lag in the switching action.

IGBT Insulated-gate bipolar transistor; a device that combines features of the MOSFET and the BJT and used mainly for high-voltage switching applications.

infinite loop A program loop that executes indefinitely because either (1) a condition for exiting the loop is never specified or (2) the loop execution never satisfies a specified condition for exiting the loop.

infrared (IR) Light that has a range of wavelengths greater than visible light.

input resistance The resistance looking in at the transistor base.

instruction set The set of binary patterns that the hardware of a microprocessor can decode and execute.

instrumentation amplifier An amplifier used for amplifying small signals riding on large common-mode voltages.

insulator A material that does not conduct current.

integrated circuit (IC) A type of circuit in which all the components are constructed on a single tiny chip of silicon.

integrator A circuit that produces an output which approximates the area under the curve of the input function.

intrinsic The pure or natural state of a material.

inverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the inverting input.

ionization The removal or addition of an electron from or to a neutral atom so that the resulting atom (called an ion) has a net positive or negative charge.

irradiance (E) The power per unit area at a specified distance for the LED; the light intensity.

isolation amplifier An amplifier with electrically isolated internal stages.

JFET Junction field-effect transistor; one of two major types of field-effect transistors.

label A symbolic reference to a specific location in a program that permits instructions in other locations to refer to it.

large-signal A signal that operates an amplifier over a significant portion of its load line.

LASCR Light-activated silicon-controlled rectifier; a four-layer semiconductor device (thyristor) that conducts current in one direction when activated by a sufficient amount of light and continues to conduct until the current falls below a specified value.

laser *L*ight *a*mplification by *s*timulated *e*mission of *r*adiation.

light-emitting diode (LED) A type of diode that emits light when there is forward current.

limiter A diode circuit that clips off or removes part of a waveform above and/or below a specified level.

linear Characterized by a straight-line relationship.

linear region The region of operation along the load line between saturation and cutoff.

linear regulator A voltage regulator in which the control element operates in the linear region.

line regulation The change in output voltage for a given change in input (line) voltage, normally expressed as a percentage.

load The amount of current drawn from the output of a circuit through a load resistance.

load regulation The change in output voltage for a given change in load current, normally expressed as a percentage.

logarithm An exponent; the logarithm of a quantity is the exponent or power to which a given number called the base must be raised in order to equal the quantity.

loop gain An op-amp's open-loop gain times the attenuation.

low-pass filter A type of filter that passes frequencies below a certain frequency while rejecting higher frequencies.

machine language A low-level binary programming language that consists of instructions that can interact directly with the processor hardware.

majority carrier The most numerous charge carrier in a doped semiconductive material (either free electrons or holes).

midrange gain The gain that occurs for the range of frequencies between the lower and upper critical frequencies.

minority carrier The least numerous charge carrier in a doped semiconductive material (either free electrons or holes).

modulation The process in which a signal containing information is used to modify a characteristic of another signal such as amplitude, frequency, or pulse width so that the information on the first is also contained on the second.

monochromatic Related to light of a single frequency; one color.

MOSFET Metal oxide semiconductor field-effect transistor; one of two major types of FETs; sometimes called IGFET for insulated-gate FET.

multistage Characterized by having more than one stage; a cascaded arrangement of two or more amplifiers.

natural logarithm The exponent to which the base e ($e = 2.71828$) must be raised in order to equal a given quantity.

negative feedback The process of returning a portion of the output signal to the input of an amplifier such that it is out of phase with the input signal.

nesting The use of an instruction type within another instruction of the same type.

neutron An uncharged particle found in the nucleus of an atom.

noise An unwanted signal that affects the quality of a desired signal.

noninverting amplifier An op-amp closed-loop configuration in which the input signal is applied to the noninverting input.

nucleus The central part of an atom containing protons and neutrons.

object A programming entity that contains data and functions that characterize it and exhibits the characteristics of encapsulation, inheritance, and polymorphism.

object-oriented programming Program that focuses on the behavior and interaction of programming objects.

octave A two-times increase or decrease in the value of a quantity such as frequency.

ohmic region The portion of the FET characteristic curve lying below pinch-off in which Ohm's law applies.

OLED Organic light-emitting diode; a device that consists of two or three layers of materials composed of organic molecules or polymers that emit light with an application of voltage.

open-loop voltage gain (A_{ol}) The voltage gain of an op-amp without external feedback.

operational amplifier (op-amp) A type of amplifier that has a very high voltage gain, very high input impedance, very low output impedance, and good rejection of common-mode signals.

operational transconductance amplifier (OTA) A voltage-to-current amplifier.

optocoupler A device in which an LED is used to couple a photodiode or a phototransistor in a single package.

orbit The path an electron takes as it circles around the nucleus of an atom.

orbital Subshell in the quantum model of an atom.

order The number of poles in a filter.

oscillator A circuit that produces a periodic waveform on its output with only the dc supply voltage as its input.

output resistance The resistance looking in at the transistor collector.

passband The range of frequencies that are allowed to pass through a filter with minimum attenuation.

peak inverse voltage (PIV) The maximum value of reverse voltage across a diode that occurs at the peak of the input cycle when the diode is reversed-biased.

pentavalent Describes an atom with five valence electrons.

phase inversion A 180° change in the phase of a signal.

phase shift The relative angular displacement of a time-varying function relative to a reference.

phase-shift oscillator A type of feedback oscillator that is characterized by three RC circuits in the positive feedback loop that produces a phase shift of 180°.

photodiode A diode in which the reverse current varies directly with the amount of light.

photon A particle of light energy.

phototransistor A transistor in which base current is produced when light strikes the photosensitive semiconductor base region.

photovoltaic effect The process where by light energy is converted directly into electrical energy.

piezoelectric effect The property of a crystal whereby a changing mechanical stress produces a voltage across the crystal.

pinch-off voltage The value of the drain-to-source voltage of a FET at which the drain current becomes constant when the gate-to-source voltage is zero.

pixel In an LED display screen, the basic unit for producing colored light and consisting of red, green, and blue LEDs.

platform A specific combination of a computer and operating system.

***pn* junction** The boundary between two different types of semiconductive materials.

pole A circuit containing one resistor and one capacitor that contributes -20 dB/decade to a filter's roll-off.

positive feedback The return of a portion of the output signal to the input such that it reinforces and sustains the output. This output signal is in phase with the input signal.

power gain The ratio of output power to input power of an amplifier.

power supply A circuit that converts ac line voltage to dc voltage and supplies constant power to operate a circuit or system.

process flow The sequence of execution of instructions in a program.

program A series of instructions that has a computer perform some specific task or achieve some specific objective.

program loop A sequence of execution in which a program returns to a previous point of execution.

programming Specifying the sequence of instructions required for a computer to accomplish some specific task or to achieve some specific objective.

programming language A set of instructions and rules for their use that allow programmers to provide a processor with the necessary information to accomplish some specific task.

proton The basic particle of positive charge.

pseudocode A textual means of representing the organization and process flow of a program using generic descriptions of program operations.

pulse width modulation A process in which a signal is converted to a series of pulses with widths that vary proportionally to the signal amplitude.

push-pull A type of class B amplifier with two transistors in which one transistor conducts for one half-cycle and the other conducts for the other half-cycle.

PUT Programmable unijunction transistor; a type of three-terminal thyristor (more like an SCR than a UJT) that is triggered into conduction when the voltage at the anode exceeds the voltage at the gate.

Q-point The dc operating (bias) point of an amplifier specified by voltage and current values.

quality factor (Q) For a reactive component, a figure of merit which is the ratio of energy stored and returned by the component to the energy dissipated; for a band-pass filter, the ratio of the center frequency to its bandwidth.

quantum dots A form of nanocrystals made from semiconductor material such as silicon, germanium, cadmium sulfide, cadmium selenid and indium phosphide.

radiant intensity (I_θ) The output power of an LED per steradian in units of mW/sr.

radiation The process of emitting electromagnetic or light energy.

recombination The process of a free (conduction band) electron falling into a hole in the valence band of an atom.

rectifier An electronic circuit that converts ac into pulsating dc; one part of a power supply.

regulator An electronic device or circuit that maintains an essentially constant output voltage for a range of input voltage or load values; one part of a power supply.

relaxation oscillator An electronic circuit that uses an *RC* timing circuit to generate a nonsinusoidal waveform without an external input signal.

reverse bias The condition in which a diode prevents current.

ripple factor A measure of effectiveness of a power supply filter in reducing the ripple voltage; ratio of the ripple voltage to the dc output voltage.

ripple voltage The small variation in the dc output voltage of a filtered rectifier caused by the charging and discharging of the filter capacitor.

***r* parameter** One of a set of BJT characteristic parameters that include α_{DC}, β_{DC}, r'_e, r'_b, and r'_c.

roll-off The rate of decrease in the gain above or below the critical frequencies of a filter.

saturation The state of a BJT in which the collector current has reached a maximum and is independent of the base current.

schematic A symbolized diagram representing an electrical or electronic circuit.

Schmitt trigger A comparator with built-in hysteresis.

SCR Silicon-controlled rectifier; a type of three-terminal thyristor that conducts current when triggered on by a voltage at the single gate terminal and remains on until the anode current falls below a specified value.

SCS Silicon-controlled switch; a type of four-terminal thyristor that has two gate terminals that are used to trigger the device on and off.

semiconductor A material that lies between conductors and insulators in its conductive properties.

sequential programming Programming in which instructions execute in the order in which they appear in the program.

shell An energy band in which electrons orbit the nucleus of an atom.

signal compression The process of scaling down the amplitude of a signal voltage.

silicon A semiconductive material.

slew rate The rate of change of the output voltage of an op-amp in response to a step input.

source One of the three terminals of a FET analogous to the emitter of a BJT.

source code The instructions written by a programmer to create a program. Special programs called assemblers and compilers convert the program source code into the executable machine code that a processor can execute.

source-follower The common-drain amplifier.

spectral Pertaining to a range of frequencies.

stability A measure of how well an amplifier maintains its design values (Q-point, gain, etc.) over changes in beta and temperature.

stack A region of memory, primarily under automatic control of the processor, that temporarily stores program information during program execution.

stage One of the amplifier circuits in a multistage configuration.

standoff ratio The characteristic of a UJT that determines its turn-on point.

stiff voltage divider A voltage divider for which loading effects can be neglected.

subroutine A sequence of instructions, usually written separately from the main program, that accomplishes a specific task in a program.

subroutine call A controlled branch in a program that redirects execution to a subroutine, executes the subroutine instructions, and resumes execution at the instruction that immediately follows the subroutine call instruction.

summing amplifier An op-amp configuration with two or more inputs that produces an output voltage that is proportional to the negative of the algebraic sum of its input voltages.

switched-capacitor circuit A combination of a capacitor and transistor switches used in programmable analog devices to emulate resistors.

switching current (I_S) The value of anode current at the point where the device switches from the forward-blocking region to the forward-conduction region.

switching regulator A voltage regulator in which the control element operates as a switch.

Sziklai pair A complementary Darlington arrangement.

test controller The component in an automated test system that executes the test code that defines the test tasks, configures the other components in the test system, and coordinates the activities of the test system components.

test equipment The components in an automated test system that provide the voltages, signals, and currents for the unit under test.

test fixture The component in an automated test system that selectively connects the test equipment and instrumentation to the unit under test.

test instrumentation The components in an automated test system that measure and record the response of the unit under test to the test equipment.

thermal overload A condition in a rectifier where the internal power dissipation of the circuit exceeds a certain maximum due to excessive current.

thermistor A temperature-sensitive resistor with a negative temperature coefficient.

thyristor A class of four-layer (*pnpn*) semiconductor devices.

transconductance (g_m) The ratio of a change in drain current to a change in gate-to-source voltage in a FET; in general, the ratio of the output current to the input voltage.

transformer An electrical device constructed of two or more coils (windings) that are electromagnetically coupled to each other to provide a transfer of power from one coil to another.

transistor A semiconductive device used for amplification and switching applications.

triac A three-terminal thyristor that can conduct current in either direction when properly activated.

trigger The activating input of some electronic devices and circuits.

trivalent Describes an atom with three valence electrons.

troubleshooting A systematic process of isolating, identifying, and correcting a fault in a circuit or system.

turns ratio The number of turns in the secondary of a transformer divided by the number of turns in the primary.

UJT Unijunction transistor; a three-terminal single *pn* junction device that exhibits a negative resistance characteristic.

unit under test (UUT) The component, circuit, or system to be tested in a test system. The UUT is sometimes referred to as a device under test (DUT).

valence Related to the outer shell of an atom.

varactor A variable capacitance diode.

***V-I* characteristic** A curve showing the relationship of diode voltage and current.

visual programming Programming that uses graphical objects rather than textual instructions to create the final program.

voltage-controlled oscillator (VCO) A type of relaxation oscillator whose frequency can be varied by a dc control voltage; an oscillator for which the output frequency is dependent on a controlling input voltage.

voltage-follower A closed-loop, noninverting op-amp with a voltage gain of 1.

voltage multiplier A circuit using diodes and capacitors that increases the input voltage by two, three, or four times.

wavelength The distance in space occupied by one cycle of an electromagnetic or light wave.

Wien bridge oscillator A type of feedback oscillator that is characterized by an *RC* lead-lag circuit in the positive feedback loop.

zener breakdown The lower voltage breakdown in a zener diode.

zener diode A diode designed for limiting the voltage across its terminals in reverse bias.

INDEX

Abrupt junction device, 150
AC analysis, 280
Acceptor atom, 15
AC collector resistance, 272, 275, 278, 281, 285
AC emitter resistance, 272, 275, 276, 278, 282, 284, 286
AC ground, 280, 324, 453
AC quantities, 272
AC resistance, 28, 190, 275
Active antenna, 485
Active filter, 763–799
Active region, 182, 184, 387, 388
AC-to-DC converter, 268
A/D conversion, 476, 676
Alpha, 178
Aluminum, 8
Amplification, 191, 213
Amplifier, 175, 190–192, 229, 272–324
  antilogarithmic, 740–741
  audio, 314, 368, 549, 638
  averaging, 681
  BJT, 190–192
  capacitively-coupled, 302, 311
  cascaded, 301
  cascode, 468–469, 492
  class A, 340–346, 365, 374, 604
  class AB, 353–357, 368, 374
  class B, 347–353, 374, 604
  class C, 357–365, 374
  class D, 470–474, 494
  common-base, 298–300, 321, 324
  common-collector, 291–298, 320, 324, 343
  common-drain, 464–466, 492, 494
  common-emitter, 278–291, 319, 324, 343, 358, 513
  common-gate, 467–469, 492, 494
  common-source, 452–464, 491, 494
  complementary transistors, 472
  Darlington class AB, 356
  Darlington/Complementary Darlington class AB, 357
  differential, 304–310, 322, 324, 604, 652
  direct-coupled, 304
  D-MOSFET, 460
  emitter-follower, 291, 292, 320, 324
  E-MOSFET, 413, 461
  FET, 385–427, 452–479
  instrumentation, 719–724
  inverting, 617–619, 626, 637, 650, 652
  isolation, 725–729
  large-signal, 340
  linear, 273
  logarithmic, 737–742
  multistage, 301–304, 543–546
  noninverting, 605, 625, 650, 652
  operational, 602–653, 667–708, 719, 725, 738, 739, 740, 742–744
  operational transconductance (OTA), 730–736, 755
  power, 339–374, 638–639
  push-pull, 348–353, 374, 604
  radio-frequency (RF), 201, 357
  small signal, 340
  source-follower, 464, 494
  summing, 679–687, 696, 707, 708
  transformer-coupled, 348, 350
  transistor, 190–192
  voltage-follower, 617, 622, 625, 637, 650, 652, 724
Amplifier response, 505–555
Amplitude modulation (AM), 725, 726, 733
Analog multiplexer, 477, 493
Analog signal processor, 477
Analog switch, 475, 493, 494
Analog-to-digital converter (ADC), 476, 676
Anode, 31, 40, 565
Anode current interruption, 572
Antenna, 485
Antilogarithm, 736, 740
Antimony, 8
Armstrong oscillator, 823
Arsenic, 8
ASK (amplitude shift keying), 790
ASK test generator, 836
Assemblers, 891
Assembly language, 891
Astable, 831, 844
Astatine, 8
Atom, 2–7, 8, 20
Atomic bond, 10
Atomic core, 8
Atomic nucleus, 2
Atomic number, 2
Attenuation, 283, 324, 509, 807, 809
Audio amplifier, 314, 368, 549, 638
Automated testing, 893–898
Automated test system, 896, 923
Automatic gain control (AGC), 813
Avalanche breakdown, 114
Avalanche effect, 35, 113, 148
Average value, 46, 51
Averaging amplifier, 681
Azimuth, 224

Back-to-back configuration, varactor, 130
Backup battery, 576
Band-gap, 8
Bandwidth, 541–543, 555, 628, 629, 634, 764, 767, 768
Barrier potential, 18, 20, 32, 34, 37, 41, 42, 47, 358
Base, 174, 213, 235, 280
Base-collector junction, 174, 178
Base current, 176
Base-emitter junction, 174, 178, 179, 358, 737
Battery, 31, 108
Bessel filter, 770
Beta (β), 178, 185, 188, 213, 241, 245, 277, 281, 356
Betz law, 269
Bias, 32, 34, 36, 38, 40, 93, 175, 349
  base, 179, 244, 249
  BJT, 202, 213. 229–256
  clamper, 363
  collector-feedback, 247, 255
  current-source, 407
  diode, 32–35
  D-MOSFET, 422
  drain-feedback, 421
  emitter, 241, 255
  emitter-feedback, 246, 243
  E-MOSFET, 421
  forward, 32–34, 36, 40, 46, 47, 133, 175, 178
  forward-reverse, 175
  JFET, 397–409
  LED, 134

Bias, (*continued*)
  midpoint, 400
  reverse, 34–35, 38, 40, 113, 128, 144, 175, 178, 386
  self, 397–403, 425
  voltage-divider, 67, 235–241, 249, 255, 404–407, 421
  zero, 422, 423
Bias current, 730, 734
Bias current compensation, 625
Biased limiter, 66
Bias resistance, 280
Bias stability, 238, 245, 247
Bias voltage, 32, 34, 36, 38, 40, 178, 229–255, 386, 388
BIFET, 626
Binary-weighted resistor DAC, 683
Bipolar, 174
Bipolar junction transistor (BJT), 174–214, 229–255, 272–324, 344–373, 424, 507, 513, 530, 737, 739
Bismuth, 15
Bode plot, 516, 540, 541, 542, 555, 628
Bohr model of the atom, 2, 4
Boltzmann's constant, 737
Bonding diagram, 11, 12
Boron, 8
Bounded comparator, 674
Bounding, 673, 708
Branching, 913, 923
Breakdown, 388
  avalanche, 112, 114
  reverse, 35, 38, 113, 114, 182
  zener, 113, 114, 160
Breakdown region, 182
Breakdown voltage, 38, 113
Break point, 516, 541
Bridge rectifier, 55–57, 62, 85, 92
Buffer, 295
Butterworth filter, 769
Bypass capacitor, 283, 284, 324

Calculator, TI89, 456
CAM (configurable analog module), 645
Capacitance
  diode, 75
  input, 396, 507, 537
  Miller, 507, 508, 537, 538
  output, 507, 537, 538
  reverse transfer, 536
  stray, 531, 723
  transistor junction, 507, 536
  varactor, 128–132
Capacitance ratio, 130
Capacitance tolerance range, 129
Capacitive coupling, 273, 278, 279, 302, 312, 725
Capacitively-coupled amplifier, 302–203
Capacitor, 58
  bypass, 283, 284, 324, 506, 519, 541
  coupling, 273, 280, 302, 313, 506, 541
  variable, 128, 130
Capacitor charge, 69, 688, 744, 808
Capacitor-input filter, 58–62, 82
Carbon, 8
Carrier, charge
  majority, 15, 19
  minority, 15, 19
Cascade, 301, 774, 778
Cascode amplifier, 468–469, 492
CASE Instruction, 903
Cathode, 31, 40, 565
CD player, 148
Center frequency, 767, 779, 780
Center-tap, 52, 348
Center-tapped rectifier, 52, 91
Channel (FET), 385, 413
Charge, 2, 3, 13, 17
Charge carrier, 15, 19
Charge controller, 30, 109
Chebyshev filter, 769
Chemical stability, 10
Chlorine, 5
Clamper, 69–70, 93
Clamper bias, 363
Clapp oscillator, 821
Class A amplifier, 340–346, 365, 374, 604
Class AB amplifier, 353–357, 368, 374
Class B amplifier, 347–353, 374, 604
Class C amplifier, 357–365, 374
Class D amplifier, 470–474, 494
Clipper, 64
Closed loop, 615
Closed-loop frequency response, 633–636
Closed-loop voltage gain, 615, 617, 618, 652, 809, 812, 813, 815, 856
CMOS, 479, 493
CMRR, 309, 324, 607, 652, 721
Coaxial cable, 723
Coherent light, 148
Cohesion, 917
Collector, 174, 213
Collector characteristic curve, 181–185, 230
Collector current, 176, 178, 181, 273, 277, 290, 350
Collector feedback bias, 247, 255
Collector leakage current, 182
Collector resistance, 274, 275, 278, 285
Colpitts oscillator, 818, 837
Common, 279, 280
Common anode, 138
Common-base amplifier, 298–300, 321, 324
Common cathode, 138
Common-collector amplifier, 291–298, 320, 324, 343
Common-drain amplifier, 464–466, 492, 494
Common-emitter amplifier, 278–291, 319, 324, 343, 358, 513
Common-gate amplifier, 467–469, 492, 494
Common mode, 308, 324, 606, 607, 652, 721
Common-mode input impedance, 608
Common-mode rejection, 309, 607, 730
Common-mode rejection ratio (CMRR), 309, 324, 607, 652, 721
Common-source amplifier, 452–464, 491, 494
Comparator, 668–688, 694, 707, 708, 735, 752
Compensation
  bias current, 625
  input offset voltage, 626
Complementary Darlington, 298
Complementary pair, 472
Complementary symmetry, 348
Compound semiconductor, 8
Compound transistor, 298
Conditional execution, 900, 923
Conduction angle, 581
Conduction band, 8, 9, 12, 13
Conduction electron, 12, 13, 15, 16, 175
Conductor, 8, 20
Configurable analog module (CAM), 645
Constant-current diode, 152
Constant-current limiting, 858
Constant-current region, 388
Constant-current source, 742
Control element, 855, 856
Conventional current, 176
Converter, 743
Copper, 9
Core, 8
Corner frequency, 510, 514
Coulomb's law, 18
Coupling, 917
Covalent bond, 10
Critical frequency, 510, 516, 521, 523, 534, 544, 555, 764, 765, 766, 771
Crossover distortion, 349
Crowbar circuit, 577
Crystal, 10, 13, 20, 823
Crystal-controlled oscillator, 823
Current, 8, 13
  base, 176, 273, 277, 290
  bias, 730, 734
  collector, 176, 178, 181, 273, 277, 290, 350
  constant, 152
  conventional, 176
  dark, 144
  electron, 13, 15
  emitter, 176, 178, 293, 295
  forward, 36, 75, 134, 572, 737
  holding, 566, 571, 595
  hole, 13, 15, 20
  input-bias, 609, 624
  input-offset, 609
  leakage, 119, 196, 207

  load, 45, 63, 123
  majority, 15, 19
  minority, 15, 19
  reverse, 35, 38, 40, 114
  saturation, 183, 188, 366
  shunt, 860
  surge, 62, 75
  switching, 566
  transistor, 176
  zener test, 114, 119
Current-controlled variable resistance, 149
Current gain, 178, 186, 290, 293, 299
Current limiting, 32, 34, 40, 152, 877
Current mirror, 349
Current regulator, 878
Current regulator diode, 152
Current source
  dependent, 179, 275
  independent, 179
Current-source bias, 407–408
Current-to-voltage converter, 743
Current transfer ratio, 198
Curve tracer, 207
Cutoff, 172, 173, 193, 213, 230, 347, 358
Cutoff frequency, 510, 764
Cutoff voltage, 391, 392
Czochralski method, 26

D/A conversion, 673
Damping factor, 767, 770, 798
Dark current, 144
Darlington pair, 295
Darlington class AB amplifier, 356
Darlington/Complementary Darlington class AB amplifier, 357
Darrieus turbine, 335
Datasheet
  BJT, 188–189
  diode, 74–78, 118, 129, 137, 146
  instrumentation amplifier, 747
  JFET, 394, 466, 487
  LED, 136–137
  MOSFET, 412–423
  operational amplifier, 640
  photodiode, 145–147
  PUT, 591
  SCR, 591
  varactor, 129–132
  voltage regulator, 157
  zener, 117–120
dB, 301, 509
dBm, 511
DC analysis, 279
DC load line, 184, 230, 256
DC operating point, 229–235
DC power supply, 45, 57, 78, 93, 153–155, 156–159, 852, 879
DC restorer, 69
DC value, 46, 51
Decade, 516, 555
Decibel (dB), 301, 324, 509–512, 555, 607
Delay angle, 581
Depletion, 17, 414, 436
Depletion region, 17–19, 33, 128, 386, 388, 390
Derating, 75, 117, 187
Diac, 578, 595
Dielectric, 128
Differential amplifier, 304–310, 322, 324, 604, 652
Differential gain, 309
Differential input, 306, 307
Differential input impedance, 608
Differential mode, 306, 307, 605, 652
Differentiator, 691–693, 708
Diffusion, 17
Digital switching, 479–482
Digital-to-analog converter (DAC), 683
Diode, 31–94, 113–161, 349, 737, 738
  complete model, 42
  constant-current, 152
  current-regulator, 152
  four-layer, 565–568
  high-intensity LED, 136, 138–142
  hot-carrier, 149
  ideal model, 40
  IR-emitting, 133
  laser, 148
  light-emitting, 133–143, 148, 160
  optical, 133–147
  photo, 144–147, 160
  pin, 149–150
  practical model, 41
  rectifier, 45, 46, 51, 55, 73, 81
  Schottky, 149
  Shockley, 565–568
  step-recovery, 150
  symbol, 31
  tunnel, 150–151
  varactor, 128–132, 160
  zener, 113–127,160, 856
Diode bias, 32–35, 36–39
Diode breakdown, 35
Diode capacitance, 75, 128, 130
Diode characteristic curve, 36–39, 75, 113
Diode clamper, 69–70, 93
Diode clipper, 64–68
Diode datasheet, 73–76
  1N4001–1N4007, 74–76
  1N4728A–1N4764A, 117–120
  TEMD1000, 145–146
  TSMF1000, 136–137
  Zetex 830, 129–130
Diode drop, 53
Diode limiter, 64–68, 93
Diode model, 39–44
  complete, 42
  ideal, 40
  practical, 41
Diode packages, 31
Diode pin configuration, 31
Diode rectifier, 44–57
Diode symbol summary, 159
Diode testing, 77–78
Diode test position (DMM), 204
Direct-coupled amplifier, 304
Discrete point measurement, 787
Distortion, 229, 349
DMM, 77, 202, 896
D-MOSFET, 414, 434, 460
Dominant critical frequency, 541, 544
Donor atom, 15
Doping, 14, 20, 113, 128, 174
Double ended, 307, 606
Download, 648
Drain, 385, 387, 436
Drain characteristic curve, 387, 388
Drain-to-source resistance, 396, 452, 814
Dual-axis solar tracking, 224
Dual-gate MOSFET, 417
Duty cycle, 832, 833, 864
Dynamically programmable analog signal processor (dpASP), 644
Dynamic range, 741
Dynamic resistance, 34, 38, 42

Efficiency, 345, 354, 362, 374, 470, 472
Electric field, 18, 114
Electroluminescence, 133, 160
Electron, 2, 20
  conduction, 5, 8, 12, 13, 15
  free, 5, 8, 12, 13, 15, 20, 175
  valence, 5, 8, 10, 11, 12, 13, 19
Electron cloud, 6
Electron current, 13
Electron-hole pair, 12, 16, 27, 144
Electron orbit, 3
Electron shell, 3, 4
Electrons per shell, 4
Electrostatic discharge (ESD), 420
Electrophosphorescence, 142
Element, 2, 4
Elevation, 224
Emitter, 174, 213
Emitter current, 176, 178
Emitter bias, 241, 255
Emitter-feedback bias, 246, 255
Emitter-follower, 291, 292, 324, 355
E-MOSFET, 413, 421, 434, 461
Emulation of a resistor, 478
Energy, 3, 5, 8, 12, 18
Energy diagram, 9, 12, 18
Energy gap, 8, 19
Energy gradient, 18
Energy hill, 18
Energy level, 3, 18
Enhancement, 413, 415, 436
Equivalent circuit, 114, 457, 513, 569, 578, 579, 584

Error detector, 855, 856
External pass transistor, 875

Fault analysis, 81–84, 312
Feedback, 256, 739
  negative, 246, 508, 613–614, 634, 652, 770, 856
  positive, 808, 812, 844
FET, 384–437, 451–494, 522, 536, 908
FET model, 452
Fetal heartbeat monitoring, 729
Field-effect transistor (FET), 384–437, 451–494, 507, 522, 536
Field-programmable analog array (FPAA), 644
Filter, 45, 58–62, 93, 794, 798
  active, 763–799
  band-elimination, 768
  band-pass, 131, 767, 779–784, 798
  band-reject, 768
  band-stop, 768, 785–788, 798
  Bessel, 770
  biquad, 784
  Butterworth, 769, 794
  capacitor-input, 58–62
  cascaded, 774, 778
  Chebyshev, 769
  high-pass, 766, 776–779, 798
  LC, 864
  low-pass, 473, 764–765, 772–776, 798
  multiple-feedback, 780, 785
  notch, 768
  power supply, 57–63
  RC, 764
  rectifier, 45, 58
  Sallen-Key, 773, 777
  single-pole, 773, 776
  state-variable, 782, 785
  three-pole, 774
  two-pole, 774
Flash ADC, 676
Flip-flop, 830
Floating point measurement, 202
Flow chart, 892, 923
Fluorescent phosphor, 134
Fold-back current limiting, 859
Forced commutation, 571
FOR-TO-STEP loop, 906
Forward bias, 32–34, 36, 40, 46, 47, 93, 133, 178, 183
Forward-blocking region, 566, 572
Forward-breakover voltage, 566, 571, 595
Forward characteristic curve, 37
Forward-conduction region, 555, 572
Forward current, 36, 73, 134, 572, 737
Forward-current gain, 277
Forward-resistance characteristic, 150
Forward-reverse bias, 175
Forward transconductance, 395
Forward voltage, 36, 74, 133, 151, 737
Four-layer diode, 565–568, 595
Free electron, 5, 8, 12, 13, 15, 20, 175
Frequency
  break, 514, 516
  center, 767, 779, 780
  corner, 510, 514
  critical, 510, 516, 521, 523, 534, 544, 555, 764, 765, 767, 771
  cutoff, 510, 764
  fundamental, 360, 824
  half-power, 541
  midrange, 516
  Nyquist, 476
  radio, 201, 357, 468
  rectifier, 46, 51
  resonant, 131, 811
  3 dB, 767
  unity gain, 542, 629
Frequency measurement, 546–549
Frequency multiplier, 360
Frequency response, 505–555, 611, 632
Frequency spectra, 472
Full-wave average value, 51
Full-wave rectifier, 50–57, 58, 80, 81, 82, 93
Function generator, 826
Fuse, 62, 156

Gain, 178, 207, 214, 627, 681, 720, 730
  common-mode, 309
  current, 178, 191, 290, 293, 299
  differential, 309
  midrange, 510, 555
  power, 291, 293, 299, 342, 374, 510
  voltage, 191, 282, 283, 284, 285, 286, 292, 298, 301, 303, 458, 459, 464, 467, 509, 515, 607, 615, 617, 627, 721, 728, 809
Gain-bandwidth product, 542, 635, 652
Gain-setting resistor, 719
Gain stability, 286
Gallium, 15
Gallium aluminum arsenide phosphide, 133
Gallium arsenide, 8, 133
Gallium arsenide phosphide, 133
Gallium nitride, 8, 134, 141
Gallium phosphide, 8, 133
Gate, 385, 480
Gate trigger current, 572
Germanium, 8, 18
Giromill turbine, 336
Gold, 8
Graphical analysis, 229, 401, 388, 454
Grid-tie, 171
Ground, 280, 453, 617
Guarding, 723

Half-splitting, 79, 80, 311, 312
Half-wave average value, 46
Half-wave power control, 574
Half-wave rectifier, 44–50, 81, 93
Handling precautions, MOSFET, 420
Harmonic distortion, 130
Hartley oscillator, 822
Heartbeat monitor, 729
Heat dissipation, 340
Heat sink, 340
Helical wind turbine, 337
Helium, 3
Hierarchical structure, 892
High-frequency response, 530–540
High-intensity LED, 136, 138–142
High-level programming, 918
Holding current, 566, 571, 595
Hole, 12, 13, 15, 20, 175
Hole current, 13, 15, 20, 175
Hot-carrier diode, 149
h-parameters, 178, 277
Hydrogen, 2, 4
Hyper-abrupt, 130
Hysteresis, 671, 708, 752

IC package, 603
IF-THEN-ELSE instruction, 900
IGBT (insulated-gate bipolar transistor), 423–425, 435, 437
Impedance
  input, 277, 608, 619, 623, 719
  output, 609, 620, 621, 623
  zener, 114, 115
Impurity atom
  pentavalent, 15
  trivalent, 15
Incoherent light, 148
In-circuit test, 206
Indium, 15
Indium gallium aluminum phosphide, 133
Indium phosphide, 8
Infinite loop, 906
Infrared, 133, 138
Inner-shell electron, 8
Input bias current, 608, 624
Input capacitance, 396, 508
Input impedance, 277, 608, 619, 623, 719
Input line voltage, 63, 852
Input offset current, 609
Input offset nulling, 612
Input offset voltage, 608, 626
Input power, 354
Input regulation, 64, 114, 852
Input resistance, 237, 280, 281, 287, 293, 299, 324, 355, 396, 460, 465, 467, 468
Instrumentation amplifier, 719–724
Instruction set, 891, 923
Insulator, 8, 21
Integrated circuit (IC), 603
Integrated circuit regulator, 62–63, 314, 869–879
Integrator, 687–691, 708
Interbase resistance, 585

Internal resistance, 190, 272
Internal transistor capacitance, 507, 531
Intrinsic region, 149
Intrinsic semiconductor, 8, 12, 13
Intrinsic standoff ratio, 585, 595
Inversion, 279
Inverter, 31, 170, 479, 493
Inverting amplifier, 617–619, 622, 626, 637, 650, 652
Ion
  negative, 5
  positive, 5, 13
Ionization, 5, 21
Irradiance, 136
Isolation amplifier, 725–729
Isolation barrier, 725

JFET stabilized oscillator, 814
JTAG (Joint Test Association Group), 894
Junction field-effect transistor (JFET), 385–412, 434, 437, 453–460, 464–469, 507, 813
Junction temperature, 39, 116, 185

Kelvin, 11, 737
Kirchhoff's voltage law, 42, 71, 179, 238, 239, 242, 244, 246, 620
Knee, 38, 114

Ladder, *R*/2*R*, 683, 685
Large-signal amplifier, 340
Large-signal voltage gain, 607
LASCR (light-activated SCR), 572, 595
Laser, 148, 160
Laser diode, 148
Latch-up, 425
LDMOSFET, 415
Lead circuit, 506
Lead-lag circuit, 811, 812
Leakage current, 119, 196, 207
Leaky capacitor, 82
LED displays, 138, 141
Light emission, 134
Light-emitting diode (LED), 133–143, 156, 160, 198
Lighting system, 576
Light intensity, 134, 135, 138
Limiter, 64–68, 93, 126
  biased, 66
  negative, 64
  positive, 64
Limiting resistor, 32, 34
Linear region, 182, 214, 232, 256
Line regulation, 63, 93, 120, 852
Liquid-level control, 744
Load, 45, 52, 123, 237, 285, 302, 459, 623, 731, 819
Load line
  ac, 273, 274, 454
  dc, 184, 231, 233, 274, 402, 405, 475
Load regulation, 63, 93, 123, 155, 853
Logarithm, 509, 736
Loop gain, 807
Loop instruction, 906
Lower trigger point (LTP), 672, 673, 826
Low-frequency response, 512–530
Lumen, 135

Machine language, 891
Majority carrier, 15, 19, 149
Maximally flat response, 769
Maximum power dissipation curve, 186
Maximum power point tracking (MPPT), 28, 109, 110–111
Measurement, 80, 511, 546, 549, 896
Metallic crystal structure, 13
Mho, 395
Midpoint bias, 400
Midrange, 516
Midrange gain, 510, 555
Miller capacitance, 508, 531, 534, 537
Miller's theorem, 468, 508, 530, 534, 537
Minority carrier, 15, 19
-3 dB point, 514
Modulator, 470, 725, 734
Monochromatic light, 148
MOSFET, 412–423, 437, 470, 472, 474
MOSFET handling precautions, 420
Motor speed control, 590
Multiplier, 71–73
Multistage amplifier, 301–304, 543–546
Multistage gain, 301
Multivibrator, 831

NAND gate, 480, 493
Natural logarithm, 737, 755
Negative charge, 2, 3
Negative feedback, 246, 369, 613–624, 634, 652
Negative ion, 5
Negative resistance, 149, 150, 151, 585
Nested loops, 910
Nesting, 923
Neutron, 2
Nitrogen, 6
Noise, 671, 723
Noise specification, 611
No latchup, 612
Noninverting amplifier, 615–616, 626, 636, 650, 652
Nonzero level detection, 669
NOR gate, 480, 493
Normalize 510
NPN transistor, 174
N-type semiconductor, 15, 17
Nucleus, 2

Object-oriented programming, 892
Octave, 516
Offset nulling, 612
Offset voltage, 608
Ohmic region, 387, 408–412, 437, 474
Ohm's law, 41, 115, 180, 238, 242, 247, 350, 387
Ohms function of a DMM, 78, 204
Open capacitor, 82
Open diode, 81
Open-loop bandwidth, 629
Open-loop response, 627–633
Open-loop voltage gain, 607, 629, 652
Operational amplifier (op amp), 602–653, 667–708, 719, 725, 738, 739, 740, 742–744
Operational transconductance amplifier (OTA), 730–736, 755
Optical diode, 133–147
Optical lens, 140
Optocoupler, 198
Orbit, 3, 5
Orbital, 6, 21
Order, filter, 770
Organic LED (OLED), 142–143
Oscillation, 151, 809, 824
Oscillator, 807–844
  Armstrong, 823
  Clapp, 821
  Colpitts, 818, 837
  crystal-controlled, 823
  feedback, 807, 808–825, 844
  555 timer, 830–835
  Hartley, 822
  LC feedback, 817–825
  phase-shift, 815
  pulse, variable duty cycle, 841
  RC feedback, 810–817
  relaxation, 567, 586, 589, 808, 825–830, 844
  sawtooth, 827–829
  square-wave, 725, 829, 841
  triangular-wave, 825–827, 841
  twin-T, 816
  voltage-controlled (VCO), 827–829, 834–835, 844
  Wien-bridge, 810–815
Oscillator start-up, 809, 812, 818
Oscilloscope, 788
OTA, 730–736, 755
Out-of-range indication of a DMM, 78
Output admittance, 277
Output bounding, 673
Output capacitance, 507
Output impedance, 609, 620, 621, 622
Output power, 343, 353, 362
Output resistance, 281, 293, 299, 324, 522
Output voltage swing, 607, 623
Overload protection, 858
Overshoot, 769
Over-temperature sensing circuit, 676
Overtone, 825
Over-voltage protection, 577

Parabolic, 393, 418
Parallel resonant circuit, 131, 151, 360
Parasitic component, 424, 425
Passband, 764, 779
Pass transistor, 875
Peak detector, 743
Peak inverse voltage (PIV), 48–49, 53–54, 56, 71, 72, 93
Peak operating voltage (POV), 152
Peak point voltage, 585
Peak rectified voltage, 47, 55
Peak sun, 30
Peak-to-peak value, 60, 190, 272
Peak value, 47, 49, 55, 190, 272
Pentavalent impurity atom, 15
Percent regulation, 63
Periodic table of the elements, 4
Phase angle, 524, 535, 538
Phase control, 581
Phase inversion, 279, 459
Phase-locked loop (PLL), 835
Phase response, 517, 630, 631
Phase shift, 517, 519, 534, 537, 630, 652, 723, 807, 809, 812
Phase-shift oscillator, 815
Phosphorous, 15
Photodiode, 144–147, 160, 198
Photogeneration, 196
Photon, 5, 26, 133, 148
Photosensitive, 196
Phototransistor, 195–199, 214
Photovoltaic effect, 26
pH sensor, 427
Piezoelectric effect, 823
Pinch-off, 388
Pinch-off voltage, 388, 390, 437
PIN diode, 149–150
Pink noise, 611
PIV, 48–49, 53–54, 56, 71, 72, 93
Pixel, 141, 160
Platform, 891
PLL(phase-locked loop), 835
PN junction, 16–19, 21, 26, 32, 74, 113, 128, 133, 144, 148, 174
PNP transistor, 174
Point of measurement, 206
Pole, filter, 764, 769, 770, 799
Polonium, 8
Positive charge, 2, 3
Positive feedback, 808, 844
Positive ion, 5, 13
Potential difference, 18
POV, 152
Power amplifier, 340–374, 638
Power derating, 117, 187
Power dissipation
  diode, 74, 117
  transistor, 186, 343, 359
Power gain, 291, 293, 299, 342, 374, 510
Power measurement, 511
Power MOSFET, 415
Power supply, 45, 57, 78, 93, 153–155, 156–158, 852, 879
Power supply current, 345
Power supply filter, 45, 58–62
Power supply rectifier, 45–49, 50–57
Power supply transformer, 45, 49–50
Power switching, 481
Power transistor, 199, 415
Preamplifier, 314
Pressure sensor, 744
Printed circuit board, 89, 159, 206, 211, 254, 317, 372, 432, 484, 490, 552, 554, 593, 642, 703, 750, 793, 840, 882
Priority encoder, 677
Process flow, 892
Program, 924
Program labels, 914
Program loop, 905–912, 924
Programmable analog technology, 644–649, 704–706, 750–754, 794–797, 840–843
Programmable unijunction transistor (PUT), 588–589, 594, 827
Programming, 890–924
Programming language, 891, 924
Proton, 2, 21
Pseudocode, 893, 924
P-type semiconductor, 15, 17
Public address system, 314, 368
Pulse, 360
Pulse-width modulation (PWM), 109–110, 470, 494, 726
Push-pull amplifier, 346–357, 374, 604
PUT, 588–589, 595, 827
PV cell, 26

Q (quality factor), 767, 781, 783, 819
Q-point, 229, 256, 273, 279, 340–344, 347, 350, 399, 402, 405, 406, 410, 411, 453, 454
Q-point stability, 245, 247, 406
Quadratic, 456
Quantum dots, 143–144
Quantum model of the atom, 5, 6
Quartz, 823
Quiescent power, 343

Radian, 46
Radiant intensity, 136
Radiation pattern, 135
Radio frequency (RF), 201, 357, 468, 789
Ramp, 689, 825
RC circuit, 69, 513, 514–525, 577, 629, 764, 810, 815, 830
Recombination, 12
Rectification, 46
Rectifier, 44–50, 93
  bridge, 56–59, 81, 82, 92
  center-tapped, 52, 91
  full-wave, 50–57, 58, 80, 81, 82, 91, 92, 93
  half-wave, 44–50, 81, 91, 93
  silicon-controlled, 568–572
  transformer-coupled, 49, 91
  Rectifier diode, 45, 46, 51, 55, 73, 81
Regulation
  current, 152, 878
  line, 63, 93, 852, 883
  load, 63, 93, 853, 883
  voltage, 62, 153–155, 156, 852–855
  zener, 114, 120–126
Regulator, voltage, 45, 62–63, 93, 126, 156, 314, 851–883
  adjustable, 871
  linear, 855–863, 869–879, 883
  series, 855–860
  shunt, 860–863
  switching, 863–869, 873, 884
Regulator current, 152, 858
Relaxation oscillator, 567, 586, 589, 808, 825–830, 844
Relay, 197, 895
REPEAT-UNTIL loop, 909
Resonant frequency, 131, 811
Reverse bias, 34–35, 40, 49, 56, 74, 93, 128, 144, 149, 386
Reverse-blocking region, 572
Reverse breakdown, 35, 38, 113, 114
Reverse current, 35, 38, 74, 76, 737
Reverse diode characteristics, 38, 76
Reverse resistance, 42
Reverse voltage, 38, 42, 73
RFID system, 789–793, 796, 836
RGB, 141
Ripple factor, 60
Ripple rejection, 62
Ripple voltage, 58, 59–61, 93
Rise time, 548
RMS, 190, 272
Roll-off, 515, 532, 764, 771, 798
r_e' formula, 276, 277
r-parameter, 275, 324
r-parameter transistor model, 275

Sallen-Key filter, 773, 777
Sampling circuit, 476
Saturation, 182, 183, 193, 214, 229, 232
Savonius turbine, 336
Sawtooth waveform, 577
Scaling adder, 682
Schmitt trigger, 673, 708, 735, 808
Schottky diode, 149
SCR, 568–577, 595
SCS, 582–583
Security alarm system, 208
Selectivity, 767
Self-bias, 397–403, 425

Semiconductor, 8, 21, 133
  n-type, 14, 15
  p-type, 14, 15
Sensitivity, photodiode, 145
Sequential program, 898–899, 924
Series regulator, 856–860
Seven-segment display, 138
Shell, 3, 4, 11, 21
Shield guard, 723, 748
Shock hazard, 49, 78
Shockley diode, 565–568
Short circuit protection, 62, 612, 859
Shorted capacitor, 82
Schottky diode, 149
Shunt regulator, 860–863
Siemens, 395
Signal, 280, 457, 488
Signal compression, 741
Signal flow, 457
Signal generator, 698, 751
Signal tracing, 312
Silicon, 8, 9, 18, 21
Silicon carbide, 134
Silicon-controlled rectifier (SCR), 568–577, 595
Silicon-controlled switch (SCS), 582–583
Silver, 8
Simulation, 88, 132, 210, 253, 316, 370, 431, 486, 528, 545, 551, 592, 641, 700, 747, 791, 836, 881
Simultaneous ADC, 676
Single-axis solar tracking, 224
Single-ended, 306, 605
Single-pole filter, 773, 776
Single-supply push-pull amplifier, 352
Slew rate, 609, 610, 652
Small-signal amplifier, 340
Solar cell, 26
Solar panel, 29, 30
Solar tracking, 224–227
Source, 385, 437
Source code, 893
Source-follower, 464, 494
Source resistance, 280
Spaghetti code, 914
Spectral response, 134, 144, 197
SPICE, 528
Square law, 393, 419
Stability, 238, 245, 247, 286
Stack, 918
Stage, 201, 303, 771
Stand-off ratio, 585, 595
Start-up conditions, oscillator, 809, 812, 818
Static charge, 420
Step, 548
Step-down regulator, 863, 874
Step-recovery diode, 150
Step response, 548
Step-up regulator, 865, 873
Steradian, 136
Stiff voltage divider, 235, 256
Stopband, 764
Subroutine, 898, 917, 924
Subroutine call, 918
Summing amplifier, 679–687, 696, 707, 708
Summing point, 680
Surface-mount package, 31
Surge current, 62, 75
Swamping, 286, 287, 513
Swept frequency measurement, 787
Switch, transistor, 192–195, 472, 474–482
Switched-capacitor circuit, 477, 493
Switching current, 566
Switching regulator, 863–869, 873, 874, 883
Sziklai pair, 297, 357

Tank circuit, 151, 360, 818
Tellurium, 8
Temperature coefficient, 116
Temperature control system, 252
Temperature effect on a diode, 39
Temperature stability, 247
Temperature-to-voltage conversion, 252
Test controller, 894, 924
Test fixture, 894–896, 924
Test point, 79
Thermal overload, 870, 883
Thermal resistance, 74
Thermal runaway, 350
Thermal shutdown, 62
Thermistor, 253
Thevenin's theorem, 238, 521, 538, 854
3 dB frequency, 764
Three-terminal regulator, 62, 126, 868–873
Threshold voltage, 413, 418, 735
Thyristor, 564, 595
Tickler coil, 823
Time constant, 60, 69, 828
Time-division multiplexing, 477
Timer, 830–835
TMOSFET, 416
Traffic light, 139
Transconductance, 392, 395, 411, 437, 453, 730, 731, 732
Transfer characteristic, 392, 393, 418, 419
Transformer, 45, 82, 87, 879
  step-down, 49
  step-up, 49
Transformer coupling, 49, 348, 727
Transistor
  bipolar junction (BJT), 174–214, 229–255, 272–324, 340–374, 424, 407, 513, 530, 737, 739
  external pass, 875
  junction field-effect (JFET), 385–412
  metal-oxide-semiconductor field-effect (MOSFET), 412–423
  switching, 192–195
  unijunction, 583–588, 595
Transistor ac model, 275–278
Transistor amplification, 191, 213
Transistor capacitance, 507, 531
Transistor currents, 176, 212
Transistor datasheet
  BF998, 430
  2N3904, 188–189
  2N2222A, 209
  2N5457/2N5459, 394
  2N5460, 466
  2N5484, 487, 488
Transistor equivalent circuit, 275, 276, 280–282, 292, 424, 452
Transistor dc model, 179
Transistor packaging, 199–200
Transistor, power, 199
Transistor ratings, 186–188
Transistor, small-signal, 199
Transistor switch, 192–195
Transistor terminals, 200
Transistor tester, 205
Transition region, 764, 765
Triac, 579–582, 595
Triangular waveform, 825
Trigger, 569, 831
Trigger current, 569
Trigger point, 672, 735, 753
Trigger voltage, 588
Trivalent impurity atom, 15, 17
Troubleshooting, 76–84, 93, 153–155, 201–208, 248–252, 310–314, 365–367, 425–427, 482–485, 636–638, 694–698
Tuned circuit, 130, 360
Tuning capacitor, 824
Tuning ratio, 130
Tunnel diode, 150–151
Turns ratio, 49, 52

Unijunction transistor (UJT), 583–588, 595
Uncertainty principle, 6
Unit under test (UUT), 894, 924
Unity gain, 679, 719, 812
Unity-gain bandwidth, 629, 635
Unity-gain frequency, 542, 629
Universal transfer characteristic, JFET, 392, 393
Upper trigger point (UTP), 672

Valence band, 8, 9, 12, 114
Valence electron, 5, 8, 9, 10, 12, 13, 19
Valence shell, 5, 21
Valley point, 585
Varactor, 128–132, 160
Variable resistance, 409
VCO, 827–829, 834–835, 844
Vertical-axis wind turbine, 335
V-I characteristic of a diode, 28, 36–39, 41, 93, 113, 131

Virtual ground, 617, 623, 742
Visible light, 133
VMOSFET, 416
Voltage
  bias, 32, 36, 38, 40, 66, 67, 178, 179, 235, 386, 388
  breakdown, 35, 113
  cutoff, 183, 230, 388, 390, 392
  forward, 41–42, 74, 134, 179
  forward-breakover, 566, 571, 595
  input offset, 608, 626
  output, bridge rectifier, 55
  output, center-tapped full-wave rectifier, 53
  peak inverse, 48–49, 53–54, 56, 71, 72, 93
  peak point, 585
  peak rectified, 49, 55
  pinch-off, 388, 390
  primary, 49
  reference, 126
  reverse, 38, 41, 42, 76
  ripple, 58, 59–61, 93
  saturation, 184, 188
  secondary, 49, 54
  threshold, 413, 418, 735
  zener, 113, 119
Voltage-controlled BJT, 424
Voltage-controlled oscillator (VCO), 827–829, 834–835, 844
Voltage-controlled voltage source (VCVS), 773
Voltage-current characteristic, 36–39, 113
Voltage divider, 67, 235, 349, 403, 615, 669, 811, 812, 830
Voltage-divider bias, 67, 235–241, 249, 255, 349, 403–407, 421
Voltage doubler, 71–72
  half-wave, 71
  full-wave, 72
Voltage feedback ratio, 277
Voltage follower, 617, 622, 625, 637, 650, 652, 724
Voltage gain, 191, 282, 283, 284, 285, 286, 292, 298, 301, 303, 458, 459, 464, 467, 507, 515, 607, 614, 615, 721, 728, 809
Voltage gain stability, 286
Voltage-inverter regulator, 867
Voltage multiplier, 71–73
Voltage quadrupler, 72
Voltage reference, 669
Voltage regulator, 62–63, 120–126, 851–883
Voltage-to-current converter, 743
Voltage tripler, 72
Waste water neutralization system, 427
Waveform distortion, 232
Waveform generator, 699
Wavelength, 133, 148
Wave-particle duality, 5
Weight, 682
Wheatstone bridge, 676
WHILE-DO loop, 908
Wien-bridge oscillator, 810–815
Wind power, 269
Wind turbine, 267

Zener breakdown, 113, 160
Zener current, 114, 119
Zener diode, 113–127, 160, 577, 856
Zener equivalent circuit, 114–116
Zener impedance, 114, 115
Zener limiting, 126
Zener power derating, 117
Zener power dissipation, 117
Zener regulation, 114, 120–126, 153–155
Zener temperature coefficient, 116
Zener test current, 114
Zener voltage, 113, 153
Zero bias, 422, 423
Zero dB reference, 510
Zero-level detection, 668